High yield assembly and electron transport investigation of semiconducting-rich local-gated carbon nanotube field effect transistors

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HIGH YIELD ASSEMBLY AND ELECTRON TRANSPORT
INVESTIGATION OF SEMICONDUCTING-RICH LOCAL-GATED SINGLE-WALLED CARBON NANOTUBE FIELD EFFECT TRANSISTORS

by

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A thesis submitted in partial fulfillment of the requirements for the Honors in the Major Program in Physics in the College of Sciences and in The Burnett Honors College at the University of Central Florida Orlando, Florida

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ABSTRACT

Single-walled carbon nanotubes (SWNTs) are ideal for use in nanoelectronic devices because of their high current density, mobility and subthreshold swing. However, assembly methods must be developed to reproducibly align all-semiconducting SWNTs at specific locations with individually addressable gates for future integrated circuits. We show high yield assembly of local-gated semiconducting SWNTs assembled via AC-dielectrophoresis (DEP). Using individual local gates and scaling the gate oxide shows faster switching behavior and lower power consumption. The devices were assembled by DEP between prefabricated Pd source and drain electrodes with a thin Al/Al₂O₃ gate in the middle, and the electrical characteristics were measured before anneal and after anneal. Detailed electron transport investigations on the devices show that 99% display good FET behavior, with an average threshold voltage of 1V, subthreshold swing as low as 140 mV/dec, and on/off current ratio as high as 8x10^5. Assembly yield can also be increased to 85% by considering devices where 2-5 SWNT bridge the gap between source and drain electrode. To examine the characteristics of devices bridged by more than one SWNT, similar electron transport measurements were taken for 35 devices with electrodes bridged by 2-3 SWNT and 13 devices connected by 4-5 SWNT. This high yield directed assembly of local-gated SWNT-FETs via DEP may facilitate large scale fabrication of CMOS compatible nanoelectronic devices.
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CHAPTER 1: INTRODUCTION

1.1 Motivation

Most laptop owners have experienced the pain of an overheated computer coming into contact with bare skin. There is even a name for a medical condition where prolonged exposure to a laptop has causes discoloration and discomfort in a patient’s legs, called “toasted skin syndrome”. However, this example is just a symptom of a problem much larger than consumers’ discomfort. For decades, the number of transistors on an integrated circuit has consistently doubled every two years, following what is known as “Moore’s Law” [1].

Figure 1.1: Extending Moore’s Law. As we reach the threshold of nanoelectronics, current device structure is reaching its limits.

However, as devices reach the threshold of nanoelectronics, traditional silicon-based devices are facing a number of technological and fundamental challenges. Several problems arise due to scaling such as heating, high power consumption, increased leakage current, and the rising role of quantum effects [2]. New device structures and materials are therefore being
investigated to extend Moore’s Law well into the 21st Century. One potential solution to the problems facing traditional silicon-based electronics was discovered in 1993; single walled carbon nanotubes (SWNTs) are seamless tubes made by rolling up a single atomic layer of graphite [2, 3]. SWNTs have a small diameter (~1nm) and are simultaneously low weight and robust, with device properties rivaling that of silicon [4-7].

However, there are a number of significant challenges facing the large scale fabrication of SWNT-based electronics. For practical applications, it is important to fabricate devices with high yield. For CNT devices, high throughput assembly has been achieved in two ways: chemical vapor deposition (CVD) grown patterned catalytic technique, and AC dielectrophoresis (DEP) post-grown solution-processed technique. In the former case approximately one-third of the as-grown nanotubes are metallic; in the latter case, DEP prefers metallic nanotubes over semiconducting, resulting in a semiconducting yield of 50% or lower [8-12]. Since only semiconducting CNT can be used for field effect transistor (FET) applications (see figure 1.2), these techniques leave a large percentage of devices non-functioning. In addition, most FET use a global back-gate geometry; as a result, these devices demonstrate high subthreshold swing, increased off-current, and threshold voltage in excess of 15 V [11-16]. Moreover, a global back-gate cannot address devices individually, rendering logic circuits impossible [6-7, 16-19]. Therefore, it is of great importance to develop a technique to attain all-semiconducting assembly of individually addressable SWNT-FET with low sub-threshold swing and high on/off ratio.
Figure 1.2: Transfer characteristics for a metallic and semiconducting SWNT-FET. The semiconducting SWNT shows many orders of magnitude change in drain current as a function of gate voltage, while the metallic SWNT shows very limited if any gate dependence.

### 1.2 Organization of Thesis

First, I will provide a background on important aspects of CNT electronics. I will discuss the properties of CNTs, provide a summary of CNT-FET operation, and outline assembly techniques including an in-depth look at AC-dielectrophoresis (DEP).

Chapter 3 concerns the details of device fabrication. Detailed descriptions are of the fabrication process are provided in this chapter, including electron beam lithography (EBL) definition of electrodes, DEP assembly of SWNT, and an outline of the measurement setup.

Subsequently, in Chapter 4, the results of the high yield assembly of local-gated nanotube FETs and their corresponding electron transport measurements will be discussed. I will describe assembly yield and variation of parameters to optimize for individual SWNT devices. I will
show the enhancement of device performance after annealing in Ar/H2 and after top contact. The local-gated devices show low subthreshold swing and high on/off ratio, as well as far reduced hysteresis and threshold voltage as compared to back-gated behavior. Furthermore, I will report on devices based on multiple SWNT with increased assembly yield.

Finally, concluding this thesis, in Chapter 5 I will discuss the impact of these results and possible directions for future research.
CHAPTER 2: LITERATURE REVIEW

2.1 Properties of CNT

2.1.1 CNT Structure

To understand the atomic structure of a carbon nanotube, one must first understand the structure of “graphene” [20], a network of hexagonally arranged sp² bonded carbon atoms. Thus, a carbon nanotube is understood as seamless tube made by a rolling up graphene sheet. Due to the hexagonal shape of the carbon atoms, the CNT can be rolled at a number of different angles; the chiral vector \( \vec{C}_h = n\vec{a}_1 + m\vec{a}_2 \) (shown in figure 2.1a) is used to define the angle rolled, where \( \vec{a}_1 = (a\sqrt{3}/2, a/2) \) and \( \vec{a}_2 = (a\sqrt{3}/2, -a/2) \) are the basis vectors and \( a=2.49 \) angstroms is the lattice constant. The “chirality” is measured by its chiral angle \( \theta \), the angle between \( \vec{a}_i \) and \( \vec{C}_h \). The chiral index, which can simply be written as \( (n,m) \), determines the nanotube’s diameter and electrical properties. For example, figure 2.1b shows two SWNT with very similar diameter, but different chiral indices. The diameter of the nanotube is given by

\[
d = \frac{|\vec{C}_h|}{\pi} = \frac{\sqrt{(na_1^2 + ma_2^2)}}{\pi} = \frac{3a\sqrt{n^2 + nm + m^2}}{\pi}.
\]

Different chiral indices are classified as semiconducting or metallic (room temperature) in figure 2.1a. Metallic nanotubes are those with \( n = m \) (armchair nanotubes) and \( n - m = 3j \), (\( j=0,1,2,\ldots \)) (green). Semiconducting carbon nanotubes are designated in figure 2.1a for \( n - m = \ldots \)
3j + 1 (pink) and \( n - m = 3j + 2 \) (purple). Shown along the top row of the diagram, zigzag nanotubes \((m = 0)\) can be either metallic or semiconducting.

Figure 2.1: CNT as a seamless cylinder of graphene. (a) The chirality of an SWNT determines its band gap. Depending on the chiral index, SWNT can be metallic at room temperature (labelled green) or semiconducting (labelled pink or purple) (b) Two nanotubes with almost the same diameter but different chiral indices. Adapted from ref [45].

### 2.2 Electronic Properties of CNT

The relationship between chirality and band gap is explained by examining the properties of graphene. The band structure of graphene in the low energy regime is shown in figure 2.2a [22]. When a graphene sheet is rolled into an SWNT, this quantizes the wave functions of the electrons in the material; conceptually, this can be seen as cutting slices out of the cone shaped structure, as shown in figure 2.2a. If these slices pass through the meeting point of the two cones, the nanotube is metallic, otherwise, it is semiconducting. When examining the energy dispersion of the \( i_{th} \) subband, given by

\[
E_i(k) = \pm \sqrt{v_F k + \epsilon_g^2 / 2},
\]

(2.2)
where $E_g^i$ is the band-gap energy for the $i_{th}$ sub-band, we can predict the resulting band gap diagram for metallic and semiconducting tubes, shown in figures 2.2a and 2.2b, respectively. For a metallic tube, inserting $E_g=0$ into equation 2.2 allows the band structure to become linear $E(k) = \pm \hbar v_F k$, as in figure 2.2b. In contrast, figure 2.2c illustrates that for semiconducting nanotubes, the dispersion is hyperbolic with a non-zero $E_g$.

Figure 2.2: Band structure diagrams. (a) Band structure of graphene. After rolling a graphene sheet into a nanotube, the circumferential momentum becomes quantized, conceptually cutting slices from the band structure of graphene. Where the slice cuts through the band structure depends on the chirality. If it cuts through meeting point of the two cones, the nanotube is metallic. In all other cases, it is semiconducting. The corresponding energy dispersion is shown for a metallic nanotube with linear band structure (b) and a semiconducting nanotube with hyperbolic dispersion and finite band gap (c).
2.3 CNT-FET

2.3.1 Operation

Carbon nanotube field effect transistors have been extensively studied since their initial implementation in 1998 [24, 25]. The common back-gated geometry is shown in figure 2.3a. Two metal electrodes (source and drain) are connected to either end of a semiconducting nanotube. The nanotube is also capacitively coupled to a nearby gate electrode that can control the current in the channel.

Figure 2.3: CNT-FET traditional operation. (a) Schematic of typical SWNT device. Electrodes contact either end of the nanotube. The nearby gate electrode is separated from the channel by the gate dielectric and controls the current in the channel via capacitive coupling. (b), (c), and (d) (adapted from reference [26]) show the band diagrams for a p-type CNT-FET under a gate voltage of -5V, 0V, and +5V, respectively. The density of states of the electrons are increased under negative gate voltages. (e) Representative corresponding graph of current versus gate voltage. The position of the Fermi level at the contacts (determined by contact material’s work function) relative to the Fermi level in the channel (controlled by the gate electrode) determines the conductance of the device. This p-type device is conducting at large negative gate voltages.
The corresponding band diagram helps us to understand the behavior of CNT-FET devices. Figures 2.3b through 2.3d show the band diagram of the CNT-FET at gate voltages of -5V, 0V and +5V respectively. The work function difference between the nanotube and the electrode material determines the Fermi level at the contacts, while the Fermi level in the channel depends on the applied gate voltage. The position of the Fermi level at the contacts relative to the position of the Fermi level in the nanotube determines whether the device is conducting. Palladium, gold, and platinum are common materials used to contact CNT, and these typically cause p-type conduction. By using low work function contact material, it is possible to elicit n-type behavior in SNWTs [27-28]. The applied gate voltage determines the position of the Fermi level in the nanotube. The number of available states is increased under higher negative gate voltage (figure 2.3b) by lowering the Fermi level deeper into the valence band, resulting in an increase in conduction. The opposite effect is seen when applying high positive gate voltage (figure 2.3d). Figure 2.3e plots drain current as a function of gate voltage for a p-type (hole transport) device [26]. The conductance is high at highly negative gate voltages, and the device turns off as the gate voltage becomes more positive.

From the transfer characteristics ($I_{DS}$ vs $V_G$) one can characterize the performance of a device. The on-state conductance of the device can be found by calculating $I_{on}/V_{DS}$. The threshold voltage ($V_{th}$) is describes the voltage at which the semiconducting device shuts off/tuns on. Another important characterization for SWNT devices is the subthreshold swing, 

$$S = \frac{dV}{d(\log(I))}. \tag{2.3}$$
The subthreshold swing (mV/decade) describes the voltage needed to change the drain current by an order of magnitude. Devices with low threshold voltage and subthreshold swing are preferred for low power consumption and high speed operation [18, 33]. The theoretical room-temperature lower limit of subthreshold swing is 60 mV/dec [29]; this limit has been reached in experiments using local gates and high-k dielectrics [33].

2.3.2 Local-gated SWNT-FET

We can fabricate local-gated devices using DEP [19]. These devices show low subthreshold swing and threshold voltage as compared to back-gated behavior. This is because, when active, a global back-gate must first overcome the Schottky barriers at the contacts before modulating the current in the conducting channel, leading to slow switching behavior and high threshold voltage [34]. By contrast, the thin Al gate is located in center of the channel; this means that the mechanism of the local gate, far away from the contacts, is therefore channel-controlled. Thus, the switching is not affected by the presence of large Schottky barriers (common in CNT devices), and the entire applied gate voltage can be used for switching in the channel.
Figure 2.4: Contact-controlled vs. channel-controlled operation. (a) Typical back-gated device measurement setup. The oxide layer is around 250 nm. When a voltage is applied to the back gate, the applied voltage must overcome the Schottky barriers before modulating the conducting channel. This results in inefficient gate coupling and hence slower switching. (b) For this local-gated device, the oxide layer is much thinner (2-3 nm). Additionally, the local gate is located far away from the contacts, and therefore the entire applied gate voltage can be used directly for switching the current in the channel.

2.4 Nanotube Assembly

2.4.1 Patterned Growth

In recent years, several approaches to assemble CNT devices have been explored. Chemical vapor deposition (CVD) has been used to grow CNTs directly on a substrate by patterning catalytic islands followed by high temperature growth in a quartz tube furnace [8]. This process is the most widely used and has produced a number of remarkable SWNT devices. However, CVD growth still results in a mix semiconducting and metallic nanotubes. CVD further requires extremely high temperatures, around 900° C, which is too high for current CMOS fabrication technologies, and the mechanical transfer used is neither precise nor efficient enough for large-scale assembly. The assembly of semiconducting SWNTs, especially individual devices, at selected position of the circuit and large scale assembly with high yield is still challenge.
Figure 2.5: PECVD CNT growth method. (a) Schematic drawing of the PECVD reactor used for the synthesis of SWNTs. (b) AFM image of nanotubes grown from PECVD on a SiO2 substrate. (c) AFM image of a tube grown from an iron-film island. (d) TEM image of an as-grown SWNT diameter = 1.2 nm.

2.4.2 Solution Processing and DEP

Solution based assembly techniques such as chemical and biological patterning [36, 37] flow assisted alignment [38], Langmuir-Blodgett assembly [39], bubble blown films [40] and contact printing [41], spin coating assisted alignment [42], and evaporation driven self assembly [43] have been demonstrated for 1D nanostructures.
Notably, several methods have been developed to sort SWNTs by chirality in solution. These methods, such as selective growth [5], ultracentrifugation [44], covalent functionalization [45], chromatography and electrophoresis [46, 47] can be used to sort nanotubes by chirality prior to device fabrication. In particular, surfactant-based separation using density gradient ultracentrifugation (DGU) has allowed for the manufacture of up to 99% semiconducting SWNTs in aqueous solution [44, 48].

Figure 2.6: Density-gradient ultracentrifugation sorting of SWNT by electronic type. (a) Photograph of DGU-sorted SWNTs suspended in solution by surfactants. Predominantly semiconducting SWNTs are contained in the top band (orange). The band just below (green) is highly metallic-enriched. (b) Absorbance spectra plotted in red for semiconducting and blue for metallic. Adapted from ref [46].

2.5 DEP Assembly

For the solution processing methods mentioned above, most methods encounter trouble when transitioning to large scale assembly or assembling a set number of nanotubes at particular locations within a circuit. AC dielectrophoresis (DEP) is a very convenient and emerging
technique for CNT assembly. DEP allows the reliable, controlled, and parallel site-selective deposition of CNTs from solution onto lithographically prefabricated structures. The alternating electric field induces a dipole moment in the nanotube, which interacts with strong electric field formed between the electrodes, causing the nanotubes to move to the area of strongest field, aligning between the patterned electrodes. This solution processing approach to fabrication of CNT-FETs is advantageous because of its control over the exact placement of CNTs on the surface, as well as its low cost and compatibility with a large number of substrates [8-12].

Figure 2.7: DEP assembly of SWNT. (a) Illustration of a Dielectrophoresis (DEP) of CNT on microelectrodes. CNTs are suspended in solution and drop cast onto the electrode pair for which the AC potential is applied. (b) Resulting SEM image after the DEP assembly. Scale bar – 1 μm. (c) Graph of Re(Kf) vs. frequency values up to ~5 GHz (where the curves drop off). At all frequencies, metallic SWNT feel a greater DEP force than semiconducting SWNT.

For an elongated object, an AC voltage gives rise to a time-averaged DEP force given by:

\[ F_{DEP} \propto \varepsilon_m \Re K_f \sqrt{E_{RMS}^2}, \]

where

\[ \Re[K_f] = \frac{\omega^2 (\varepsilon_m \varepsilon_p - \varepsilon_m^2) + \sigma_m \sigma_p - \sigma_m^2}{\omega^2 \varepsilon_m^2 + \sigma_m^2}, \]

in which \( K_f \) is the Claussius-Mossotti factor, \( \varepsilon \) is permittivity, \( \sigma \) is conductivity, \( \omega = 2\pi f \) is the angular frequency, and \( p \) and \( m \) refer to the particle and the medium in which \( \varepsilon \) is permittivity, \( \sigma \) is conductivity, \( \omega = 2\pi f \)
is the angular frequency, and $p$ and $m$ refer to the particle and the medium [9]. Figure 1 shows $\text{Re}[K_r]$ for metallic (m-) and semiconducting (s-) SWNTs as a function of frequency. This shows that when using a mixed solution, DEP assembly of all semiconducting SWNTs is not possible due to the greater force m-SWNTs feel during assembly. This is why, in the past, DEP assembly with a mixed solution resulted in a very low percentage (30%) of semiconducting SWNT, leaving a large percentage of devices non-functioning. To solve this problem, we propose to combine DEP with a semiconducting-enriched high-quality solution, in order to achieve controlled high-yield fabrication of quality SWNT devices.
CHAPTER 3: DEVICE FABRICATION AND EXPERIMENTAL METHODS

3.1 Lithography

Our primary substrate for assembly is a highly doped (<0.005 Ω cm) 3 inch silicon wafer (~350 μm thickness from Silicon Quest International) with a 250 nm thick SiO₂ thermally grown oxide layer. We define the large electrode patterns (bonding pads, EBL alignment markers, and electrode leads with features larger than 1 μm) using photolithography in order to save on time and cost. We use a Zeiss Ultra55 SEM with the JC Nabity patterning system to write smaller electrode patterns. A working area of 500 μm defined by markers is typical for alignment with the JC Nabity system. EBL can be done on single layer PMMA or double layer MAA/PMMA resist.

Figure 3.1: EBL process. (a) Spin-coat and bake PMMA (b) Expose pattern with electron beam (c) Develop in MIBK (d) Evaporate metal (e) Lift-off. Steps are discussed in more detail in the following sections.
3.1.1 Resist for EBL

For the double-layer resist recipe, the first step involves spin-coating MAA (MicroChem, EL9). The sample is spun at 4000 rpm for 1 minute and then baked at 180°C for 15 minutes, ensuring development of a 300 nm layer. The next layer PMMA 950 K (C2, MircoChem) is then spin-coated onto the wafer at 4000 rpm for 1 minute. The sample is then baked on a hot plate for 15 minutes at 180°C, creating a 100-150 nm thick layer covering the SiO₂. For single-layer resist, the initial layer of MAA is not needed, and one can simply follow the instructions for the PMMA layer.

The exposure and developer parameters are the same for both resist recipes. The typical dose is ~350 μC/cm² at 28 kV using the Nabity system. After exposure, the sample is developed in 1 part Methyl isobutyl ketone (MIBK) and 3 parts IPA for ~75 seconds. After a final rinse in IPA for 5-10 seconds, the sample is then blown dry in a stream of nitrogen gas.
3.1.2 Metal Evaporation and Lift-off

An electron beam evaporator is used for evaporation of most metals. 3 nm Cr is used as a sticking layer (rate~ 0.1 A/s), followed by 35 nm Pd. A thermal evaporator is also used for evaporation of other metals, such as gold after photolithography. Typical device structure is shown in figure 3.2. The fabrication process is capable of creating sharp features at a variety of length scales.

![Figure 3.2: Typical micro-electrodes for device assembly. (a) Optical image of a chip with gold patterned electrodes (b) SEM micrographs of the device’s 28 electrode pairs (c) expanded view of a single pair of electrodes.](image)

In order to remove excess metal and resist, the liftoff procedure is as follows: samples are bathed in warm acetone at 60\(^0\) C for 10-20 minutes. After liftoff starts, one can facilitate the removal process by flushing the sample in acetone using a plastic pipette. If facing additional difficulty during liftoff, as is common when using single-layer resist, it is possible to facilitate liftoff by sonicating in acetone and then IPA. After placing the sample in clean acetone or IPA, it is also possible to wipe the sample gently with a clean room swab to loosen stubborn metal. After all the excess metal has been removed, the sample is rinsed using IPA and then thoroughly
in DI H$_2$O. The surface can then be dried using nitrogen gas. It is very important to not allow any liquid to dry on the surface, but rather to push the drop off of the surface.

### 3.1.3 Patterned Aluminum Local Gates

A second round of EBL was used to define 100-nm local Aluminum (Al) gates centered between source and drain electrodes, as shown in Figure 3.2a and 3.2b. This second round of lithography is possible due to previous patterning of additional markers during the defining of electrodes. Because the thin Al gate tends to encounter problems regarding clean lift-off, it is advisable to use a double-layer be used for the patterning of the local gate.

For these gates with thin widths (100 nm or less), it is necessary to deposit a 1 nm thick Cr sticking layer before evaporating the Al. Additional care must be taken when evaporating aluminum, as the metal tends to be very grainy when deposited on a room-temperature sample. Notably, if liquid nitrogen is used to cool the stage during the Al deposition then the layer tends to be much smoother. This strategy is often done for single molecule transistors [49, 50]

![Figure 3.3: Aluminum local gate fabrication. (a) 100 nm-wide aluminum local gates are patterned for each quarter of the chip, with a native 2-3 nm oxide layer. (b) Expanded view of electrode pair with Al gate in the center. (c) Height analysis of electrode pair. Local-gate is around 30 nm tall](image)
Finally, the completed devices are put through a 10 minute treatment in oxygen plasma. This helps to simultaneously eliminate organic residue and ensure growth of a uniform 2-3 nm Al₂O₃ layer.

3.2 Nanotube Assembly

3.2.1 Solution Details

Recently, surfactant-based separation via density gradient ultracentrifugation (DGU) has allowed for the manufacture of 99% semiconducting SWNT (s-SWNT) in aqueous solution [48]. Here we used such a semiconducting-enriched, high quality s-SWNT aqueous solution to fabricate field effect transistors with high yield in a local gated geometry. Semiconducting-enriched (99%) SWNT solution suspended in deionized (DI) water was purchased from NanoIntegris [48]. These SWNTs are dispersed in deionized water with the help of surfactants, and come in varying purities of semiconducting, metallic, or a mixture. The average diameter of the nanotubes contained in solution was 1.4 nm, and the length ranged from 0.5 to 4 μm with an average value of 1 μm as measured by AFM as shown in figure 3.3b. The concentration of nanotubes in solution was diluted with DI water from the original value of 10 μg/mL down to the final concentration.
Figure 3.4: Semiconducting-enriched SWNT Solution. (a) Semiconducting-enriched high-quality SWNT in aqueous solution from NanoIntegris. The color of the solution shows that it is semiconducting-enriched. (b) Length distribution of SWNT in solution (ref. [28])

3.2.2 DEP Assembly

One of the advantages of DEP assembly is its low cost and simplicity, as described in this section. The list of necessary equipment includes a function generator to apply the AC voltage, an oscilloscope to monitor output, and a probe station to contact the electrode pads. An example setup is shown in figure 3.5a. A signal of 1 MHz, 5V is applied to the left electrode though a switch. The oscilloscope monitors the output from the function generator on Channel 1 and the right electrode on Channel 2. Alternatively, for simultaneous assembly at multiple electrode pairs, Channel 2 can also be connected to the highly doped Si back gate, as described in section 4.2. To begin assembly, a few microliter drop of SWNT in solution is cast onto the chip, and the AC voltage is applied for a set amount of time. Figure 3.5b shows an example electric field simulation, demonstrating that the field is strongest between the tapered electrodes.
Figure 3.5: DEP assembly of SWNTs. (a) Schematic of the experimental setup for DEP of SWNTs. A signal of 1 MHz, 5V is applied to the left electrode though a switch. The oscilloscope monitors the output from the function generator on Channel 1 and the right electrode on Channel 2. (b) Electric field simulation shows that electric field is strongest between the points of the two electrodes.

DEP parameters can be varied to adjust device yield. A voltage of 5V_{p-p} was found to be ideal for strong alignment without breaking the SWNT. A frequency of 1 MHz helps to avoid trapping of amorphous carbon and other junk. The concentration of nanotubes in solution and time of applied voltage were the main parameters adjusted during optimization.

### 3.3 Measurement Steps

Figure 3.11 shows the three-terminal DC measurement setup of a SWNT device. We use LabView to interface a high resolution DAC card combined with a BNC-2090 from National Instruments and a DL instruments 1211 current preamplifier. We use one of the BNC-2090’s analog outputs (AO) to supply the source-drain voltage. An analog input (AI) in differential mode is also used. The gate voltage is supplied either though a second AO channel (± 10 V
maximum) or using a Keithly 2400 source-meter (± 220 V maximum). A protector resistor (1 MΩ) is used in series with the gate voltage, to avoid sudden large voltages to the device.

Figure 3.6: Electron transport measurement of CNT devices. A BNC 2090 is used to apply the source-drain voltage, while a Kiethley 2400 is used to apply the gate voltage.
CHAPTER 4: HIGH YIELD LOCAL-GATED SWNT-FETS

4.1 Introduction

Single-walled carbon nanotube field effect transistors (SWNT-FET) have been shown as a promising material for future nano-electronic device applications due to their excellent electrical properties surpassing the traditional silicon metal-oxide-semiconductor FET (MOSFET) without the problem of scaling down [4-7]. For practical applications, it is important to fabricate FET devices with high yield. High yield assembly has been achieved through either chemical vapor deposition (CVD) grown patterned catalytic technique or post grown solution processed technique using AC dielectrophoresis (DEP). In the former case approximately one-third of the as-grown nanotubes are metallic, while in the latter case DEP prefers metallic nanotubes over semiconducting, resulting in a semiconducting yield of 50% or lower [8-12]. Since only semiconducting SWNT can be used for FET application, these techniques leave a large percentage of devices non-functioning. In addition, most FET use global back-gate geometry; as a result, these devices demonstrate high subthreshold swing, increased off-current, and threshold voltage in excess of 15 V [11-16]. Moreover, a global back-gate cannot address devices individually, rendering logic circuits impossible [6-7, 16-19]. Therefore, it is of great importance to develop a technique to attain all-semiconducting assembly of individually addressable SWNT-FET with low sub-threshold swing and high on/off ratio.

Recently, solution-based sorting techniques, have been used to separate nanotubes by chirality post-growth (see Section 2). In particular, surfactant-based separation via density
gradient ultracentrifugation (DGU) has allowed for the manufacture of 99% semiconducting SWNT (s-SWNT) in aqueous solution [49]. Here we used such a semiconducting-enriched, high quality s-SWNT aqueous solution to fabricate field effect transistors with high yield in a local gated geometry. The devices were assembled by DEP between prefabricated Pd source and drain electrodes with a thin Al/Al₂O₃ gate in the middle, and the electrical characteristics were measured before anneal and after anneal. Out of the 70 devices assembled, 99% showed semiconducting behavior (on/off current ratio greater than 10). Detailed electron transport characterization showed a median on/off ratio of 5x10⁴ with a maximum of 8x10⁵, while the median subthreshold swing was 300 mV/dec with a best value of 140 mV/dec. The demonstration of high yield semiconducting local-gates SWNT-FET is an important step forward in the development of large-scale carbon nanotube electronics.

### 4.2 Device Fabrication

Devices were fabricated on highly doped silicon (Si) wafer with a 250 nm layer of thermally grown silicon dioxide (SiO₂). The source and drain electrodes with a channel length of 1 µm were defined with standard EBL, as described in section 3. Taper-shaped source and drain electrodes were chosen to maximize the electric field at the sharp edges and increase the chance of obtaining an individual SWNT connection during the DEP assembly [18]. The 28 pairs of electrodes per chip were patterned with a common drain to facilitate simultaneous trapping of SWNT between source and drain electrodes. A second round of EBL was used to define 100-nm local Al gates centered between source and drain electrodes, as described in section 3.
4.2.1 Assembly of local-gated devices

Semiconducting-enriched (99%) SWNT solution suspended in deionized (DI) water was purchased from NanoIntegris [49]. The schematic of DEP for nanotube assembly is shown in Figure 4.2a. A ~3µL drop of solution was deposited onto the electrode array, and an ac voltage of 5 V p-p at 1 MHz was then applied between the back gate and the common source electrode. DEP assembly with common source allows each drain electrode to capacitively couple with and obtain a similar potential to the back gate. As a result, the potential difference across each electrodes pair becomes the same, allowing nanotube alignment at each electrode pair simultaneously. After 3 min, the ac voltage was turned off and the chip was blown dry with a stream of nitrogen gas to remove the remaining solution drop from the surface, leaving behind only aligned s-SWNT.

![Schematic of SWNT assembly](image)

Figure 4.1: Individual SWNT Assembly. (a) Schematic of SWNT assembly. (b) and (c) Resulting SEM images of devices based on (a) an individual and SWNT and (b) two SWNT connecting source and drain. Gap = 1µm.
4.2.2 Assembly Yield

The results of the DEP assembly of the SWNT devices were examined with a high resolution scanning electron microscope (SEM). Figure 4.2b and 4.2c show representative SEM image of such an assembly. We optimized assembly conditions for individual device yield by varying solution concentration and time for DEP. For single SWNT assembly, low concentration and long assembly time are preferred. Out of the 308 electrode pairs used in this study, we found that on average 20% of these electrodes pairs were bridged by an individual SWNT. The maximum yield of individual SWNT assembled on one chip was 33%. This device yield is comparable to other studies using DEP assembly of mixed nanotubes [11-16].

4.3 Electron Transport Measurements

Following DEP assembly, the devices were annealed in Ar/H₂ at 200°C for 1 hour to eliminate residual surfactant at the nanotube/electrode contacts and restore device performance [49]. Room temperature electrical transport measurements of the assembled devices were performed as detailed in section 3.

4.3.1 Individual SWNT Transfer and Output Characteristics

The FET characteristics of a typical individual s-SWNT local-gated device are shown in Figure 4.3a and 4.3b. Figure 4.3a shows the transfer characteristics ($I_{DS}$ versus $V_{LG}$) at $V_{DS} = --0.5V$ for the typical device, respectively, before and after anneal in Ar/H₂. Due to the reduction of residual surfactant at the nanotube/electrode interface after annealing, the on-state resistance
decreased by an order of magnitude from 430 MΩ to 44 MΩ. The device shows p-type semiconducting behavior due to oxygen doping and Pd contact material, as described in section 2.2. The on/off current ratio \( I_{on}/I_{off} \) further increased from \( 2 \times 10^2 \) to \( 1 \times 10^4 \) after anneal. The gate leakage current is less than 1 pA for the gate voltage range used. Additionally, the subthreshold swing \( S \) was calculated using the formula \( S = (d\log I_D/dV_G)_{fl}^{-1} \); after anneal this value was and found to decrease from 440 mV/dec to 250 mV/dec. The corresponding output characteristics \( I_{DS} \) versus \( V_{DS} \) at different local gate voltages \( V_{LG} \) from -2 V to 2V in 0.5V increments) for this device are shown in Figure 4.3b. The linear behavior of the curve at low biases indicates that ohmic contact is formed between SWNT and electrode. In addition, the output curve shows very good field effect modulation at higher bias voltage.

Figure 4.3c shows the before- and after- anneal transfer characteristics for a second device. This device shows high on/off ratio = \( 3 \times 10^5 \) and low subthreshold swing = 135 mV/dec after anneal. Before anneal, on/off = \( 3 \times 10^3 \) and \( S=435 \) mV/dec. The on-state resistance for this device decreased from 18 MΩ to 2 MΩ after anneal. The subthreshold swing of our device is superior to reported values for other DEP-assembled s-SWNT-FET with back gated [11-15] and comparable to other Al₂O₃ local gated devices [16-19]. The corresponding output characteristics for this device are shown in Figure 2(d), this time a saturation current around 0.7 µA.
Figure 4.2: Representative room temperature electron transport measurement. (a) Drain current ($I_{DS}$) versus $V_{LG}$ at $V_{DS} = -500$ mV for a typical individual SWNT device before and after annealing. (b) Measured drain current ($I_{DS}$) out to the saturation regime at different local gate voltages ($V_{LG}$ from -2 V to 2V in 0.5V increments) for the same device. (c) and (d) Full characteristics for a device with high on/off current ratio and subthreshold swing of 140 mV/dec. 
4.3.2 Statistics on the FET Devices

![Histograms of on/off current ratio and subthreshold swing for individual devices before and after annealing.](image)

Figure 4.3: Individual SWNT device statistics. Histograms of (a) on/off current ratio and (b) subthreshold swing for the individual devices before and after annealing.

Similar characteristics were measured before and after anneal for a total of 70 individual SWNT devices. The histograms of the on/off current ratio and subthreshold swing for these devices can be seen in Figures 4.4a and 4.4b, respectively. Upon annealing, the median on-state resistance of the individual SWNT devices decreased from 45 MΩ to 9 MΩ. In addition, the average current on/off ratio and threshold voltage of the device before annealing were $4.8 \times 10^3$ and $\sim 500$ mV/dec, and after annealing these values improved to $4.9 \times 10^4$ and $\sim 300$ mV/dec, respectively. In our study, devices displaying on/off current ratios greater than one order of magnitude change in drain current as a function of gate voltage were categorized as semiconducting. Out of the 70 devices, only one device showed metallic behavior. 99% of the
devices showed semiconducting behavior. In the past, assembly of local-gated SWNT via DEP from a mixed solution of semiconducting and metallic nanotubes yielded a very low percentage (~30%) of semiconducting devices [19]. This is due to the fact that metallic SWNT feel a greater force than semiconducting SWNT during DEP assembly, as described in section 2. By utilizing a semiconducting-enriched solution, we show 99% local-gated SWNT with a higher device yield via DEP.

4.3.3 Back-gated comparison

In order to compare and contrast the local- vs. back- gated device performance, Device A was also measured by applying a back gate voltage to the heavily doped Si substrate. Figure 4.5 shows the transfer characteristics in both forward and reverse sweeps of the same device with back gate voltage ($V_{BG}$) from -10V to +10V and local gate voltage ($V_{LG}$) from -2V to +2V. The local gate displays reduced hysteresis of less than ~1V as compared to the back gated ~7V. This hysteresis may be caused by charge trapping between substrate and SWNT. Although beneficial in memory devices, the presence of hysteresis in a SWNT-FET causes undesired unpredictability of output, and should hence be reduced as much as possible [24].
A device with low subthreshold swing was also measured by applying a back gate voltage to the heavily doped Si substrate. Figure 3a shows the transfer characteristics in both forward and reverse sweeps of the same device with back gate voltage \( V_{BG} \) from -10V to +10V and local gate voltage \( V_{LG} \) from -2V to +2V. This indicates that the device shows much faster switching behavior by the local gate than the back gate. Furthermore, the back-gated device shows a subthreshold swing of 1000 mV/dec, while for the local gate \( S=140 \) mV/dec. This indicates that the device shows much faster switching behavior by the local gate than the back gate. When a gate voltage is applied to the back gate, part of this applied voltage is used to control the Schottky barriers while the rest is used to modulate the conducting channel [10]. This results in inefficient gate coupling and hence slower switching. On the other hand, the local gate is situated far away from the contacts. In this case, the local gate voltage is not used to modulate the contact but rather is completely dedicated to modulation the channel itself. As a result, the local gated device makes a stronger gate coupling and hence exhibits improved switching speed.
4.3.4 Multiple SWNT Devices

One concern with fabrication of individual SWNT devices by DEP is assembly yield. DEP yield of 100% individual SWNT would be ideal. By optimizing parameters such as assembly time and concentration, the maximum individual SWNT assembly yield I attained was 33%.

In order to increase assembly yield, I then optimized parameters for overall device yield rather than individual SWNT yield. In this case, an increasing percentage of electrode pairs are bridged by 2-5 SWNT. For these devices, I used the same concentration, voltage, and frequency for DEP, but decreased the assembly time from 3 minutes to 15 seconds, meaning that DEP assembly for the entire chip with 28 electrode pairs increased from 3 to 7 minutes. Additionally, I used point-to-point DEP between source and drain electrodes rather than between common source and back gate. This allowed each electrode pair to be addressed individually, and combined with the shortened time for DEP decreased the number of short SWNT trapped between source and local gate.

With this altered assembly, I was able to increase overall assembly yield such that 85% of the electrode pairs were bridged by 1-5 SWNT. It may be possible to attain 100% assembly yield, but one must be wary of assembling too many SWNT (details below.)

We find that devices based on 2-3 SWNT continue to show properties similar to individual SWNT devices. An image of a 2-connection SWNT device is shown in figure 4.5a. The corresponding transfer and output characteristics are shown in figure 4.5b and 4.5c. This device shows a higher on current than that of due to the higher number of nanotubes present. At
500mV, the subthreshold swing for Device B was found to be 245 mV/dec and the on/off current ratio was $8 \times 10^5$.

Figure 4.5: Source and drain electrode connected by 2-3 SWNT. (a) SEM image of a device connected by 2 SWNT. (b) Plot of drain current $I_{\text{DS}}$ versus $V_{\text{LG}}$ at $V_{\text{DS}} = 100, 500, \text{ and } 1000 \text{ mV}$ for the multiple SWNT device. The device shows increased on-current and good FET characteristics. (c) $I_{\text{DS}}$ out to the saturation regime at different local gate voltages ($V_{\text{LG}}$ from -2 V to 2V in 0.5V increments) for the same device.
As mentioned previously, an increased device yield generally elicits an increase in the number of nanotubes for gap. An image of a 5+ -connection SWNT device is shown in figure 4.6a. The corresponding transfer characteristics at $V_{DS} = -0.5V$ are shown in figure 4.6b. This device shows low resistance due to the higher number of nanotubes present. However, the gate modulation is significantly decreased. This device shows on/off ratio around 2.

![Image](image1.png)

Figure 4.6: SWNT device connected by more than 5 SWNT. (a) SEM image and (b) transfer curve at -0.5V for a device based on more than 5 SWNT. The on-current is high, but the device shows weak gate modulation.

To provide the full story, similar measurements were taken for 23 individual SWNT devices, 35 devices based on 2-3 SWNT, and 13 devices based on 4-5 SWNT. Statistics for on/off current ratio and subthreshold swing are shown in Figures 4.7a and 4.7b, respectively. The individual SWNT devices show clear peaks in desirable ranges for both on/off current ratio (average $5\times10^4$, median $6\times10^3$) and subthreshold swing (average 390 mV/dec), as consistent with the devices described in section 4.4.2. Devices based on 2-3 SWNT show more variation than individual SWNT, but have a median on/off current ratio of $2\times10^3$ and subthreshold swing of 600 mV/dec. With 4-5 SWNT connections, the median on/off ratio reduces to 15, and the
subthreshold swing increases to greater than 1000 mV/dec. The percentage of devices showing on/off ratio greater than 10 drops to 50%.

Figure 4.7: Multiple SWNT device statistics. (a) and (b) Histograms of the on/off current ratio and subthreshold swing for all devices based on an individual SWNT (23 devices), 2-3 SWNT (35 devices), and 4-5 SWNT (13 devices). Devices based on 2-3 SWNT also show high on/off ratio and low subthreshold swing, but devices based on 4 or more SWNT show less desirable electronic properties.

Therefore, it is possible to increase device yield by considering multiple connection SWNT devices. However, as the number of nanotube connections increases, nanotube-nanotube interaction begins to play a greater role in transport, and device characteristics suffer.
CHAPTER 5: CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

5.1 Summary

To conclude, we have developed a general strategy for fabrication of high-quality SWNT-FET with high yield. These devices were assembled using DEP in combination with a commercially available semiconducting-enriched solution, a simple and scalable method without the need for high-temperature growth. When optimizing for individual SWNT devices, assembly yield is 30%, and out of the 70 devices assembled, 99% showed semiconducting behavior (on/off current ratio greater than 10). Detailed electron transport characterization showed a median on/off ratio of $5 \times 10^4$ with a maximum of $8 \times 10^5$, while the median subthreshold swing was 300 mV/dec with a best value of 140 mV/dec. The local-gated devices show far reduced hysteresis and threshold voltage as compared to back-gated behavior. We also show that we can increase device yield to 85% by including devices where the source and drain electrodes are connected by 1-5 SWNT. However, when assembling more than four nanotubes, the interaction between SWNT plays a larger role, and the percentage of devices showing on/off ratio greater than 10 decreases to about 50%. This high-yield assembly, high-yield semiconducting SWNT-FETs large-scale fabrication of SWNT-based devices, and may pave the way for large scale fabrication of CMOS compatible nanoelectronic devices.
5.2 Suggestion for Future Work

This work has potential impact past high yield FET assembly. Our group does low-temperature measurement, including single electron transistors (SET) based on individual SWNT. The local gate can act as a mechanical template to introduce tunnel barriers into the SWNT, defining the size of a quantum dot [52]. Theoretical studies [53-54] have shown that metallic SWNTs are less susceptible to scattering compared to semiconducting SWNTs upon bending. Therefore, semiconducting SWNT can show increased probability to form SETs. By combining high-yield assembly of semiconducting SWNT with size-tunable quantum dots via controlling the width of the local gate, this could lead to high yield assembly of room-temperature SET based on SWNT.
CHAPTER 6: REFERENCES


