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TESTS Functional Description CDRL A002

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INSTITUTE FOR SIMULATION AND TRAINING

PREPARED UNDER CONTRACT NUMBER N61339-91-C-0100
for
NAVAL TRAINING SYSTEMS CENTER
and
NAVAL AIR TEST CENTER

TACTICAL ELECTRONICS SIMULATION TEST SYSTEM

TESTS Functional Description
CDRL A002

December 23, 1991

Institute for Simulation and Training
12424 Research Parkway, Suite 300
Orlando, FL 32826

and

Department of Electrical Engineering
University of Central Florida
Orlando, FL 32816

University of Central Florida
Division of Sponsored Research

IST

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**University of Central Florida
Division of Sponsored Research**

Approved:



**Michael Companion
Principal Investigator**

Edited:



Danette Carr

TABLE OF CONTENTS

	<u>PAGE</u>
SECTION 1. GENERAL	1-1
1.1 PURPOSE OF THE FUNCTIONAL DESCRIPTION	1-1
1.2 PROJECT REFERENCES	1-1
1.2.1 Technical Documentation.....	1-2
1.2.2 Programming and Documentation Standards	1-3
1.3 TERMS AND ABBREVIATIONS	1-3
1.3.1 Terms and Definitions	1-4
1.3.2 Acronyms	1-5
SECTION 2. SYSTEM SUMMARY	2-1
2.1 BACKGROUND	
2.1.1 Uses of Test and Evaluation Simulation	2-1
2.1.2 Purpose of TESTS	2-2
2.1.3 Tailoring TESTS to NAVAIRTESTCEN Requirements	2-2
2.1.4 TESTS Project Status	2-3
2.2 TESTS OBJECTIVES	2-4
2.2.1 General	2-4
2.2.2 Performance Objectives	2-4
2.2.3 Projects Goals	2-5
2.2.4 Anticipated Future Impact of TESTS	2-6
2.3 EXISTING METHODS AND PROCEDURES	2-7
2.4 PROPOSED METHODS AND PROCEDURES	2-10
2.4.1 Summary of Improvements	2-12
2.4.2 Summary of Impacts	2-13
2.5 ASSUMPTION AND CONSTRAINTS	2-14
SECTION 3. DETAILED CHARACTERISTICS	3-1
3.1 SPECIFIC PERFORMANCE REQUIREMENTS	3-1
3.1.1 Basic Capabilities	3-1
3.1.1.1 Signal Synthesis and RF Generation	
3.1.1.2 Simulation of Direct and Multipath Channel Effects	
3.1.1.3 Simulation of Multiple Transponders and Interrogators	

TABLE OF CONTENTS

	<u>PAGE</u>
3.1.1.4	Generation of RF Spread Spectrum Signals
3.1.1.5	Encoding and Decoding of Secure Transmission Modes
3.1.2	Timing3-5
3.1.2.1	Simulation Response Time
3.1.2.2	Simulation Response Time Accuracy
3.1.2.3	Scenario Update Rates
3.2	FUNCTIONAL AREA SYSTEM FUNCTIONS3-9
3.2.1	Simulator Component3-9
3.2.2	Stimulation Component3-9
3.2.3	Environment Component3-11
3.2.4	Operational Control Component3-11
3.2.4.1	Operational Control
3.2.4.2	Scenario Control
3.2.4.3	Diagnostic Control
3.3	HARDWARE/SOFTWARE FUNCTIONS3-14
3.3.1	Block Descriptions3-16
3.3.2	Supporting Discussion3-21
3.4	INPUT-OUTPUT REQUIREMENTS3-21
3.4.1	SWEG3-22
3.4.1.1	Shared Memory for SWEG
3.5	DATA BASE CHARACTERISTICS3-28
3.5.1	SWEG Data Bases3-28
3.5.1.1	Type Data Base
3.5.1.2	Terrain Data Base
3.5.1.3	Scenario Data Base
3.5.1.4	Environment Data Base
3.5.1.5	Runtime Data Base
3.5.1.6	Analysis Data Base
3.5.1.7	Model Kickoff Data Base
3.6	SECURITY3-30
SECTION 4.	DESIGN DETAILS4-1
4.1	SYSTEM DESCRIPTION4-1
4.2	SYSTEM FUNCTIONS4-4

TABLE OF CONTENTS

	<u>PAGE</u>
4.2.1 Accuracy and Validity	4-14
4.2.1.1 IFF Message Data	
4.2.1.2 Channel Effects	
4.2.2 Timing	4-16
4.2.3 TESTS Interface Bus Capacity Requirements ...	4-19
4.3 SYSTEM DATA	4-20
4.3.1 Inputs	4-20
4.3.1.1 SWEG Inputs	
4.3.1.2 Inputs from SWEG	
4.3.1.3 TESTS External Bus Message Inputs	
4.3.1.4 TESTS Operator Console Inputs	
4.3.2 Outputs	4-43
4.3.2.1 Internal TESTS Outputs to Signal Generation Hardware	
4.3.2.2 Data Collection and Analysis	
4.3.3 Internal TESTS Software Data Bases	4-47
SECTION 5. ENVIRONMENT	5-1
5.1 EQUIPMENT ENVIRONMENT	5-1
5.1.1 TESTS RF Receiver	5-1
5.1.2 TESTS Signal Generation Hardware	5-3
5.1.3 TESTS Signal Conditioning Devices	5-3
5.1.4 TESTS Host Computer and Interface Bus	5-5
5.1.5 SWEG Host Computer	5-6
5.1.6 SWEG Shared Memory Interface	5-6
5.1.7 TESTS Multiplexing Hardware	5-6
5.1.8 TESTS Data Collection Devices	5-11
5.1.9 TESTS Software Development Environment	5-12
5.2 SUPPORT SOFTWARE ENVIRONMENT	5-12
5.2.1 CASE Tools	5-12
5.2.2 Compilers	5-12
5.2.3 Assemblers	5-12
5.2.4 Configurational Management	5-13
5.2.5 Real-Time Operating System	5-13
5.2.6 SWEG	5-13
5.3 INTERFACES	5-16

TABLE OF CONTENTS

	<u>PAGE</u>
SECTION 6. SYSTEM DEVELOPMENT PLAN	6-1
6.1 SOFTWARE DEVELOPMENT APPROACH	6-1
6.2 HARDWARE DEVELOPMENT APPROACH	6-4
6.2.1 SWEG Hardware	6-4
6.2.2 Signal Generation, Modification and Distribution Hardware	6-4
6.2.2.1 Signal Conditioning Hardware	
6.2.2.2 Signal Generation Hardware	
6.2.2.3 Multiplexing Hardware	
6.2.3 Data Collection Hardware	6-5
6.2.4 TESTS Computer Hardware	6-5
6.2.5 Threat Hardware	6-6
6.2.6 Other Hardware	6-6
6.2.6.1 Crypto	
6.2.6.2 Calibration/Test Hardware	
6.3 VERIFICATION AND VALIDATION FOR TESTS	6-6

LIST OF FIGURES

	<u>PAGE</u>
Figure 2-1	Flight Test Data Analysis Requirements (1 of 2)2-8
Figure 2-1	Flight Test Data Analysis Requirements (2 of 2)2-9
Figure 2-2	TESTS Baseline Configuration for Transponder and Interrogator2-11
Figure 3-1	Overview of TESTS Hardware/Software Architecture3-2
Figure 3-2	Analysis of TESTS Pulse Sequences3-6
Figure 3-3	Approach to Updating TESTS Data Parameters3-8
Figure 3-4	TESTS Functional Components3-10
Figure 3-5	TESTS Functional Architecture3-15
Figure 3-6	SWEG Interface3-23
Figure 3-7	SWEG Shared Memory Architecture3-25
Figure 3-8	SWEG Mailboxes and Messages3-27
Figure 4-1	TESTS Top Level Software Architecture (1 of 2)4-2
Figure 4-1	TESTS Top Level Software Architecture (2 of 2)4-3
Figure 4-2	Task 1 Flow Diagram4-5
Figure 4-3	Task 2 Flow Diagram4-6
Figure 4-4	Task 3 Flow Diagram4-7
Figure 4-5	Task 4 Flow Diagram4-9-
Figure 4-6	Flow Diagram for Determination of Main Beam Active Target List4-10
Figure 4-7	Flow Diagram for Addition of Target to Active List4-11
Figure 4-8	Flow Diagram for Determination of Side Lobes Active Target List4-12
Figure 4-9	Flow Diagram for Task 54-13
Figure 4-10	TESTS External Bus Message Format4-15
Figure 4-11	TESTS Data Base Interactions with Tasks4-48
Figure 4-12	Transponder Object Data Base4-50
Figure 4-13	Path Object Data Base4-51
Figure 4-14	Output Message List4-53
Figure 5-1	Signal Generation Integrated Flow Diagram ...5-2
Figure 5-2	RF Signal Conditioner Block Diagram5-4
Figure 5-3	VMIC Multidrop Reflective Memory (1 of 2) ...5-7
Figure 5-3	VMIC Multidrop Reflective Memory (2 of 2) ...5-8
Figure 5-4	Systran SCRAMNet (1 of 2)5-9
Figure 5-4	Systran SCRAMNet (2 of 2)5-10
Figure 5-5	The SWEG Internal Data Structures and Memory Interfaces5-15
Figure 6-1	Overview of Real Time Systems Development Process6-2
Figure 6-2	Prototyping in MIL-STD-2167 Development Environment6-3

LIST OF TABLES

		<u>PAGE</u>
Table 4-1	Budget: Assumed Number of Operations per Process	4-17
Table 4-2	Preliminary Time Estimate	4-18
Table 4-3	Data Collection Parameters	4-44

SECTION 1. GENERAL

1.1 PURPOSE OF THE FUNCTIONAL DESCRIPTION

This Functional Description for the Tactical Electronics Simulation Test System (TESTS) is written to provide:

- a. The hardware and software development requirements that must be satisfied to achieve a simulation based test system that can be used to conduct Development Test and Evaluation of advanced Identification Friend or Foe (IFF) systems.
- b. Information on the performance requirements, preliminary design, and user impacts for the defined approach.

1.2 PROJECT REFERENCES

This section provides a general summary of the TESTS approach and the identification of project sponsor, target users, and operating centers where TESTS will be used. Additionally, a list of references applicable to the development of TESTS is provided.

The Tactical Electronics Simulation Test System is a scenario driven simulation/hardware based test and evaluation system designed to be used during developmental test and evaluation of advanced IFF systems. TESTS uses simulation techniques to emulate an ensemble of IFF systems to exercise an IFF system under test (SUT). This simulation emulates the interrogation and response environment for realistic IFF scenarios. The system also uses simulation techniques to calculate the environmental impact on signal transmission to provide realistic system performance. TESTS uses hardware to generate the simulated signals and modify the signal transmission characteristics under software control.

TESTS was initiated in 1990 by the Naval Air Test Center (NAVAIRTESTCEN), in conjunction with the Naval Training System Center (NAVTRASYSCEN), to support developmental test and evaluation of the MK XV IFF program. The MK XV IFF requirements specify almost a dozen functional modes, including embedded MK XII modes 1 - 4 and C, multiple MK XV time dependent formats and subformats, Mode S and Radar Mode Front End; a large number of environmental conditions, including Electronic Counter Measures (ECM) [benign, jamming], spoofing, weather/

atmospheric, ground [over water, over land, near land], density, and platform variations; and a variety of operational conditions, including altitude configurations [High Interrogator (IR) - High Transponder (XP), Low IR - High XP, High IR - Low XP]. Combination of these factors means that potentially, there are several hundred test cases to be considered. In addition, some tactical conditions requisite to testing the system without simulation can be unsafe or impractical because of degree of difficulty, safety or security considerations. It became clear that all Test and Evaluation Master Plan (TEMP) objectives for the MK XV IFF could not be evaluated during the developmental test and evaluation phase using only flight test or off the shelf test tools. Simulation provides a cost-effective and efficient way to subject the system to a large set of test conditions with accurately measured results.

TESTS was conceived to provide a high fidelity simulation test system that could be used to exercise a MK XV IFF during test and evaluation in an accurate and repeatable manner. TESTS had to not only generate valid MK XII and MK XV signals, but also degrade the signals in a manner that emulates real world environmental effects. TESTS was intended to operate as a stand-alone system or as an integral part of the NAVAIRTESTCEN Air Combat Environment Test and Evaluation Facility (ACETEF). The system would be operated by personnel from the NAVAIRTESTCEN NIFFTE (Naval IFF Test and Evaluation) laboratory. The data generated using TESTS would be analyzed in the NAVAIRTESTCEN IFF Data Center.

Secondary objectives of the TESTS effort were to develop a system that could also be used to support Operational Test and Evaluation of advanced IFFs and provide the foundation for the development of IFF simulation models which could be incorporated in training simulators. A unexpected benefit of TESTS is that many of the simulation models developed for TESTS can also be used to support the design and development of advanced IFFs. These models can be used to conduct design trade studies and evaluate the effect of various parameters on IFF performance prior to actual fabrication of the system.

1.2.1 Technical Documentation

Air Combat Environment Test and Evaluation Facility (ACETEF) Interface Document. BDM International, Inc., 26 September, 1990.

Functional Security Requirements Specification for Embedded COMSEC/TRANSEC Mark XV IFF System. National Security Agency (NSA) Document, 14 August, 1985. (Classified)

Mark XV Identification Friend or Foe (IFF) System Multi-Service Test and Evaluation Master Plan. DoD Mark XV TEMP, 13 March 1989.

Mode 4 Input/Output Data KIT/KIR-1A/TSEC. DoD Aims 64-900D, 8 March 1983.

Prime Item Development Specification for the Mark XV Identification Friend or Foe (IFF) Airborne Interrogator Subsystem. ASD/AEIE:60051-87S/P6510, 14 February 1989. (Classified)

Prime Item Development Specification for the Mark XV Identification Friend or Foe (IFF) Transponder Subsystem. ASD/AEIE:63522-87U/P6510, 14 February 1989. (Unclassified)

System Specification for the Mark XV Identification Friend or Foe (IFF) Equipment. ASD/AEIE:60048-87S/P6510, 14 February 1989. (Classified)

Tactical Electronics Simulation Test System, Feasibility Assessment Report. Institute for Simulation and Training, Technical Report, IST-TR-91-6, April 12, 1991.

Tactical Electronics Simulation Test System, Final Report: Phase I. Institute for Simulation and Training, Technical Report, IST-TR-91-21, June 30, 1991.

Technical Standard for the ATCRBS/IFF/Marks XII Electronic Identification System (AIMS), DoD Aims 65-1000B, 29 April 1983. [Classified supplement]

1.2.2 Programming and Documentation Standards

DOD-STD-2167A, Defense System Software Development

DOD-STD-2168, Software Quality Evaluation

Roetzhein, William. Developing Software to Government Standards, Prentice Hall, Englewood Cliffs, New Jersey, 1991.

1.3 TERMS AND ABBREVIATIONS

This section provides a listing of terms and definitions, and acronyms which are used in this document.

1.3.1 Terms and Definitions

Probability of Correct Identification - The system single scan and multiple scan probability of Friend Identification and Probability of Enemy Acceptance.

Anti-Jam Capabilities - The amount of performance degradation under various Electronic Counter Measures environments.

System Capacity/Interrogation Volume - The ability to identify friendly targets and adequately locate them in range/azimuth to correlate/associate with the primary sensor in an environment of increasing interrogation rates.

Code Validation - Percentage of proper code validations per interrogation, a ratio of times the interrogator correctly decodes the reply over the number of interrogations during the dwell on a target transponder.

Split Targets - Targets declared as multiple targets.

Diversity Performance - The capability of the transponder algorithms to determine through which antenna the reply should be sent. The reply is sent through the antenna receiving the strongest and/or first interrogation pulse.

Maximum Range - The maximum range in nautical miles at which consistent ID is lost.

Range Resolution - The minimum range separation of two targets where they are still distinguishable.

Minimum Range - The minimum range at which consistent ID is lost.

Range Accuracy - Accuracy of target range over entire range of system.

Azimuth Resolution - The minimum azimuth separation of two distinguishable targets.

Azimuth Accuracy - Evaluate accuracy of IFF reported target azimuth over the entire system range.

Multipath - Evaluate the impacts to system performance as a result of multipath effects, where multipaths are secondary signals generated by reflections of the primary signal from the ground or atmosphere.

Freindly Replies Unsynchronized in Time (FRUIT) Rate - Replies received by an interrogator which were intended for another interrogator.

Anti-Spoof - Resistance to exploitation of spoofing. Spoofing is the attempt to generate a signal which emulates a real signal to interfere with operation of a communication system.

Encryption - Techniques used to code an electronic transmission to prevent jamming and/or unauthorized reception of the transmitted message.

Interoperability and Compatibility - The ability of the MK XV IFF system to operate within the civil Air Traffic Control (ATC), current military IFF systems, and the NATO Identification System.

Electromagnetic Compatibility - The ability to operate simultaneously with other systems within the platform without degradation due to Electromagnetic Interference (EMI).

Channel Effects - Degradation or modification of an electronic signal as it propagates through the atmosphere.

Spread Spectrum - Modulation technique for communication signals in which the signal content is distributed and transmitted over a band of frequencies rather than a single frequency.

1.3.2 Acronyms

A - Attenuation

ACETEF - Air Combat Environment Test and Evaluation Facility

ACT - Acoustic Charge Transfer

ADM - Advanced Development Model

AIMS - Automatic Identification and Messaging System

ASEF - Aircrew Systems Evaluation Facility

ATC - Air Traffic Control

ATCRBS - Air Traffic Control Receiving and Beacon System
A-T-D-P-F - Attenuation, time delay, dispersion, phase and frequency shift
BIT - Built in Test
CASE - Computer Aided Software Engineering
CAL - Canadian Avionics Limited
CNIL - Communications, Navigation and Identification Laboratory
COMSEC - Communication Security
COTS - Commercial-off-the-shelf
CPU - Central Processor Unit
D - Dispersion
DEC - Digital Electronics Corporation
DoD - Department of Defense
DSG - Density Signal Generator
DT&E - Developmental Test and Evaluation
ECM - Electronic Counter Measures
EE - Electrical Engineering
EM - Electromagnetic
EMEGS - Electromagnetic Environmental Generation System
EMI - Electromagnetic Interference
E3TL - Electromagnetics Environment Effects Test Laboratory
EWISTL - Electronic Warfare Integrated System Test Laboratory
F - Frequency shift
FIBER - Friendly Interrogations but Enemy Replies
FRUIT - Friendly Replies Unsynchronized in Time
GFE - Government Furnished Equipment
HDBK - Handbook
ID - Identification
IFF - Identification Friend or Foe
IFX - Input-Output File Executive
IST - Institute for Simulation and Training
J - Jammers
KI - Krypto Identification
KIT - Krypto Identification Transmitter
KIR - Krypto Identification Receiver
MK XII - Mark XII Identification Friend or Foe
MK XV - Mark XV Identification Friend or Foe
MIPS - Million Operations Per Second
MPV - Multi Processor Version
NAVAIRTESTCEN - Naval Air Test Center

NAVTRASYSCEN - Naval Training System Center
NG - Noise Generators
NIFFTE - Navy IFF Test and Evaluation (laboratory)
NIS - NATO Identification System
NSA - National Security Agency
OS - Operating System
OSL - Offensive Sensors Laboratory
OT&E - Operational Test and Evaluation
P - Phase
PN - Pseudo-random Number
PRF - Pulse Repetition Frequency
PRI - Pulse Repetition Interval
PUT - Platform Under Test
RF - Radio Frequency
RFSC - Radio Frequency Signal Conditioner
SATCOM - Satellite Communication
SAW - Surface Acoustic Wave
SDP - Software Development Plan
SG - Signal Generator
SIF - Special Identification Features
STD - Standard
SUT - System Under Test
SWEG - Simulated Warfare Environment Generator
T - Time delay
TASS - Tactical Agile Signal Simulator
TASTEF - Tactical Avionics and Software Test and Evaluation Facility
TBD - To Be Determined
TEMP - Test and Evaluation Master Plan
TESTS - Tactical Electronic Simulation Test System
TRANSEC - Transmission Security
UCF - University of Central Florida
VMIC - VME Microsystems International Corporation
V&V - Verification and Validation
XMIT - Transmit

SECTION 2. SYSTEM SUMMARY

2.1 BACKGROUND

Researchers at the Institute for Simulation and Training initially became interested in developing TESTS in January 1990 when it was visited by personnel from the Systems Test Directorate, Naval Air Test Center, Patuxent River, Maryland. During the course of the visit, the Commander mentioned the facilities at NAVAIRTESTCEN, the present plans to upgrade the systems test capabilities, and the current difficulty in testing tactical electronics systems because of a lack of real-time simulation test tools and equipment. The specific problem of adequately testing the emerging MK XV IFF was discussed. Although the Institute had no previous projects which called for the development of real-time simulation software for test and evaluation (T&E) purposes, both parties agreed that further discussion might be warranted.

2.1.1 Uses of Test and Evaluation Simulation

The concept of developing a real-time simulation test tool intrigued a small group of researchers at the university, and they immediately began exploring how simulation was used in test and evaluation, what environmental models could be made available, and what obstacles existed in current software and hardware which would have to be overcome to build a dynamic simulation that would function at the speed of light. During late January 1990, the institute discussed the possibility of creating a team with the University of Central Florida's Electrical Engineering Department to address the NAVAIRTESTCEN requirement. The basic disciplines: Digital Signal Processing, RF Signal Generation, and EM Propagation Effects that the electrical engineering staff possessed combined with the Institute's expertise in simulation and systems design prompted the university to request more detail on the actual requirement at NAVAIRTESTCEN.

In response, a four man briefing team from NAVAIRTESTCEN visited the Institute on 6-7 February 1990 and conducted unclassified briefings on their requirements. The briefings focused on the inability to test advanced IFF systems to a level of confidence sufficient to meet defined Joint Test and Evaluation Master Plan (TEMP) objectives. The NAVAIRTESTCEN briefing team also provided sufficient unclassified material to permit a joint IST/EE technical team to further study the Navy's requirement. It became evident that the basic problem with using simulation for test and evaluation purposes is that the basic tools required to test to required levels of

confidence do not exist. The test community usually follows a "brute hardware" approach to testing (i.e., one signal generator, one signal). Additionally, nothing close to actual operational scenarios could be replicated because the requisite channel effects models are either non-existent or incomplete. Further, even if adequate channel effects simulations were developed, commercially available hardware was found to be incapable of accepting it. Despite the shortfalls in existing simulation test technology, there seemed to be no overwhelming technical difficulties in building a prototype TESTS, and the cost effectiveness of such a tool was obvious from the outset.

2.1.2 Purpose of TESTS

The purpose of TESTS is to provide a simulation test tool to test an emerging advanced IFF system to levels of required confidence in areas of testing not suited, not permitted, or not possible through actual flight testing or with the current test capabilities at NAVAIRTESTCEN. A secondary purpose is to develop a simulation test bed that will have application in testing other tactical electronics systems. As a result of the analysis, both IST and the EE Department gained sufficient insights to form a project team and inform the Navy that the University of Central Florida possessed the requisite expertise to initiate a program to fulfill the requirement. The university's joint IST/EE team then sent a letter to NAVAIRTESTCEN (dated March 26, 1990) stating a firm conviction that such a requirement could be met, expressing hope that a program could proceed in the interests of the public good, and expressing commitment by the university to meet the Navy's goals. A resultant proposal was then submitted to the Naval Training Systems Center (NAVTRASYSCEN) under solicitation BAA 90-01. It was proposed that a collaborative program be established to conduct a full technical feasibility assessment, including a site survey at NAVAIRTESTCEN, to determine the most cost-effective method in which to proceed. A Phase I contract for this initial effort was awarded on August 14, 1990. The key deliverable, the Tactical Electronics Simulation Test System (TESTS) Feasibility Assessment Report was delivered to the Navy on April 12, 1991.

2.1.3 Tailoring TESTS to NAVAIRTESTCEN Requirements

In order to ensure maximum cost-effectiveness, two early decisions were reached. First, the UCF/IST team had to start the project with a thorough understanding of what existing tools and facilities were available at NAVAIRTESTCEN and that these tools and facilities would be fully utilized in the TESTS final design. Second, the project would proceed in an orderly and logical fashion so that if, because of some

unknown reason, it would not be possible to proceed to development, the cost to the government would be minimized. Since the Institute is a non-profit entity, the UCF/IST team informed the government that if it were impossible to proceed, the government would be notified immediately and all expenditures against the TESTS project would cease. The approach reached as a consequence of these understandings included:

- A thorough site survey and laboratory briefings at NAVAIRTESTCEN
- In collaboration with the government, identification of software, hardware, and test facilities which could be used in development of TESTS
- A detailed development approach, including costs and schedule milestones, which would minimize government project risk
- A final report and briefing delineating all findings to determine whether or not subsequent phases were warranted

The site survey was thorough and enlightening; NAVAIRTESTCEN personnel allowed access to required information and provided invaluable insights into test procedures. Unfortunately however, very little in the way of simulation software and hardware was found which could be utilized in the design of TESTS. The ACETEF chamber and the SWEG software were the only elements of real value to the project. Although many of the laboratories are in the process of being significantly upgraded, the TESTS design, because it had to respond to a revolutionary new advanced IFF system, would have to include development of both new software as well as new signal generation equipment. It was determined, however, that during the development of TESTS, a high degree of software and equipment commonality could be achieved with ongoing upgrade programs at NAVAIRTESTCEN.

Based on the survey conducted in collaboration with the government, it was determined there are no real-time dynamic IFF simulations, nor has a spread spectrum waveform ever been simulated in real time. Since it is anticipated that most tactical communications systems will use a spread spectrum waveform, the development of TESTS could be valuable to assist in advanced systems design as well as testing.

2.1.4 TESTS Project Status

A subsequent briefing by the UCF TESTS team at NAVAIRTESTCEN convinced the Navy that proceeding to the next logical step in meeting the requirement was

warranted. A smaller effort was then contracted through NAVTRASYSCEN to produce a functional description of TESTS. Shortly after contract award to UCF, the Mark XV program was canceled, leaving the prime system to be simulated with undefined systems characteristics and performance parameters. By consensus with government, the TESTS team proceeded further into resolution of problems related to channel effects simulation, hardware related to RF signals generation, and the issue of signal modification/signal conditioning. Consequently, many areas of risk were reduced from medium to low risk levels. This report constitutes the final deliverable under this phase, which is scheduled to end December 25, 1991.

2.2 TESTS OBJECTIVES

The primary objective of TESTS is to provide a simulation test tool to test an emerging advanced IFF system to levels of confidence required by test and evaluation master plan (TEMP) defined objectives. These objectives include issues in areas of testing not suited, not permitted or not practical through actual flight testing or with the systems test capabilities currently available to NAVAIRTESTCEN. A secondary objective is to design and develop TESTS as a test bed that will have application in testing other tactical electronics systems.

2.2.1 General

Since the inception of the TESTS program, both the technical and programmatic objectives have remained unchanged. With the agreement of the government and because of some turbulence in the acquisition of the prime avionics subsystem (MK XV) on which TESTS is based, some minor deviations have been taken in how the objectives were to be ultimately achieved; however the objectives themselves have remained fixed since agreed upon early in Phase I. These technical and programmatic objectives will be reiterated/discussed briefly in this section.

2.2.2 Performance Objectives

Specific test objectives have been addressed in considerable detail in prior reports and include: antijam capability, systems capacity, code validation, prioritization, correct identification and others. Although the basis of discussion for the technical objectives were based on the MK XV TEMP which is now a canceled program; it is highly probable that whatever final decisions are reached on the advanced IFF system, the problem of testing an emerging IFF system to the necessary confidence levels will

remain the same. Therefore the rationale for the continuation of TESTS with the use of "real-time simulation" to assist in the achievement of TEMP objectives remains as strong as ever. However, now that the acquisition of an advanced IFF system has been delayed, there are some very real advantages which the TESTS program, if continued, now offers to the government over and above its use as a simulation test tool. One advantage is the virtual elimination of risk in the development of TESTS. The program can now be structured so that the first step in development will be to produce a dynamic, real-time simulation of the MK XII with selective key high resolution channel effects. Since the first portion of the simulation created will replicate an existing system, the simulation can be accurately evaluated and improved thus attaining credibility prior to development of the Advanced IFF simulation. Because any advanced IFF system that emerges must respond to "old" (MK XII), as well as new systems, neither time nor funds are wasted in this initial effort. What is gained is increased confidence and credibility in the simulation and, as stated previously, virtual elimination of technical risk.

2.2.3 Project Goals

From a programmatic standpoint, the program was initially established as a collaborative relationship with NAVAIRTESTCEN, NAVTRASYSCEN, and UCF/IST. This represented an important departure from the traditional contractor to government relationship. As part of the collaborative arrangement, NAVAIRTESTCEN provided the specific IFF descriptive material/expertise required for the project, and NAVTRASYSCEN will provide secure facilities, as required, convenient to the TESTS team for the production of the simulation software during full scale development. This joint effort will facilitate the implementation of a multi-phased prototyping effort for TESTS. In view of these factors, the three programmatic goals are: affordability, versatility, and risk reduction. These goals remain the same as they appeared in the TESTS Feasibility Assessment Report dated April 12, 1991:

Affordability - TESTS has to be cost-effective. A design-to-cost approach has been the project team's objective from the outset.

Versatility - TESTS must serve the Navy's needs regardless of whether the final prime system is an MK XV or an MK XII enhanced IFF or any variation which might occur downstream. It must also make the best possible use of existing facilities, simulation tools, and equipments.

Risk Reduction - Each successive project phase must reduce both technical and programmatic risk. An answer which solves one small piece of the problem without advancing the overall solution is not acceptable. No element of this project can be characterized as more than moderate risk and most of the technical issues have been reduced to low risk elements.

Since April 12, 1991, the TESTS team has identified existing software, hardware, and facilities for use in the development of the simulation test tool; this precise identification will result in considerable cost savings to the government. In the area of risk reduction, the technical issues have been addressed sufficiently that none now appear to exceed a low risk classification except for the RF Signal Conditioning hardware. A moderate risk remains for this element of the simulation tool development.

2.2.4 Anticipated Future Impact of TESTS

Continuation of the TESTS program will significantly contribute to the requirement to utilize simulation in design and in test and evaluation of emerging communications systems. Because the development starts with the simulation of an existing IFF system (MK XII), a verifiable and credible performance benchmark will provide early program confidence. Further, it will take a major step in increasing the role of simulation software as compared to present "brute force" hardware methods. The "one generator, one signal" syndrome may finally be broken. Because of the unanticipated delay in the advanced IFF program itself, an advantage which accrues to the government is that the simulation test tool can additionally be utilized to assist in the design and development, as well as perform the system test and evaluation function for the new, emerging IFF system. Furthermore, development of a TESTS program can significantly enhance future testing efforts by decoupling environmental effects from system performance. Validation and verification can assure this by comparing system performance to that of system analysis results using flight test data.

Finally, as anticipated, the emerging design of the IFF system will utilize a spread spectrum message waveform. All the high fidelity models, the "simulation" architecture, other performance methodology and verification methods of Phase I (MK XII) can be used to produce a cost effective simulation tool using spread spectrum technology with all of its inherent antijam advantages. Continuation of the TESTS program will make a vital impact on the final design of the Advanced IFF system.

2.3 EXISTING METHODS AND PROCEDURES

Although NAVAIRTESTCEN presently has significant upgrade programs ongoing in many of their current laboratories and facilities, the center still must rely heavily on flight testing and the data generated through flying to accomplish its mission. This fact especially impacts the Systems Test Directorate responsible for testing tactical electronics equipment to ensure performance across a broad band of parameters and in a large number of diverse environmental conditions. Existing test and evaluation methods at NAVAIRTESTCEN are limited by present constraints on flight testing which include: operational security concerns, resource availability, and safety. And further, in many of the TEMP objectives, flight testing cannot provide the requisite data for analysis because of the special requirements and/or restriction critical to each of these specific TEMP objectives. Nor are current ground testing methods at NAVAIRTESTCEN sufficient to compensate for these key flight test capability shortfalls.

The test and evaluation (T&E) of avionics system equipment at NAVAIRTESTCEN has predominately focused on the use of actual flight test data to evaluate the subsystem performance parameters, of particular systems under test (SUT). The error covariance values for these parameters are natural by-products of the analysis procedures and serve to determine the accuracy/effectiveness of "a flight data set" for the evaluation process. Figure 2-1 shows the analysis requirements existing for the data processing of flight test data.

A second method, employed at NAVAIRTESTCEN for T&E of IFF equipment, is a simulation implemented by the Electronic Warfare Integrated System Test Laboratory (EWISTL). In its prototype mechanization, it uses SWEG to define the emitter environment and a simulated test scenario for generating test signals to stimulate a system-under-test (SUT) installed in an anechoic chamber. In its present configuration the EWISTL stimulation system has successfully tested the MK XII IFF System in the anechoic chamber. This success has ultimately stimulated the current TESTS project; moreover, the demonstration of this simulation tool gave credibility and promise to the use of simulation in the T&E world. Armed with the experience gained in the EWISTL simulator project and the requirements necessary to fulfill the TEMP objectives, IST embarked on the TESTS project approximately one year ago.

Analysis Requirements Summary

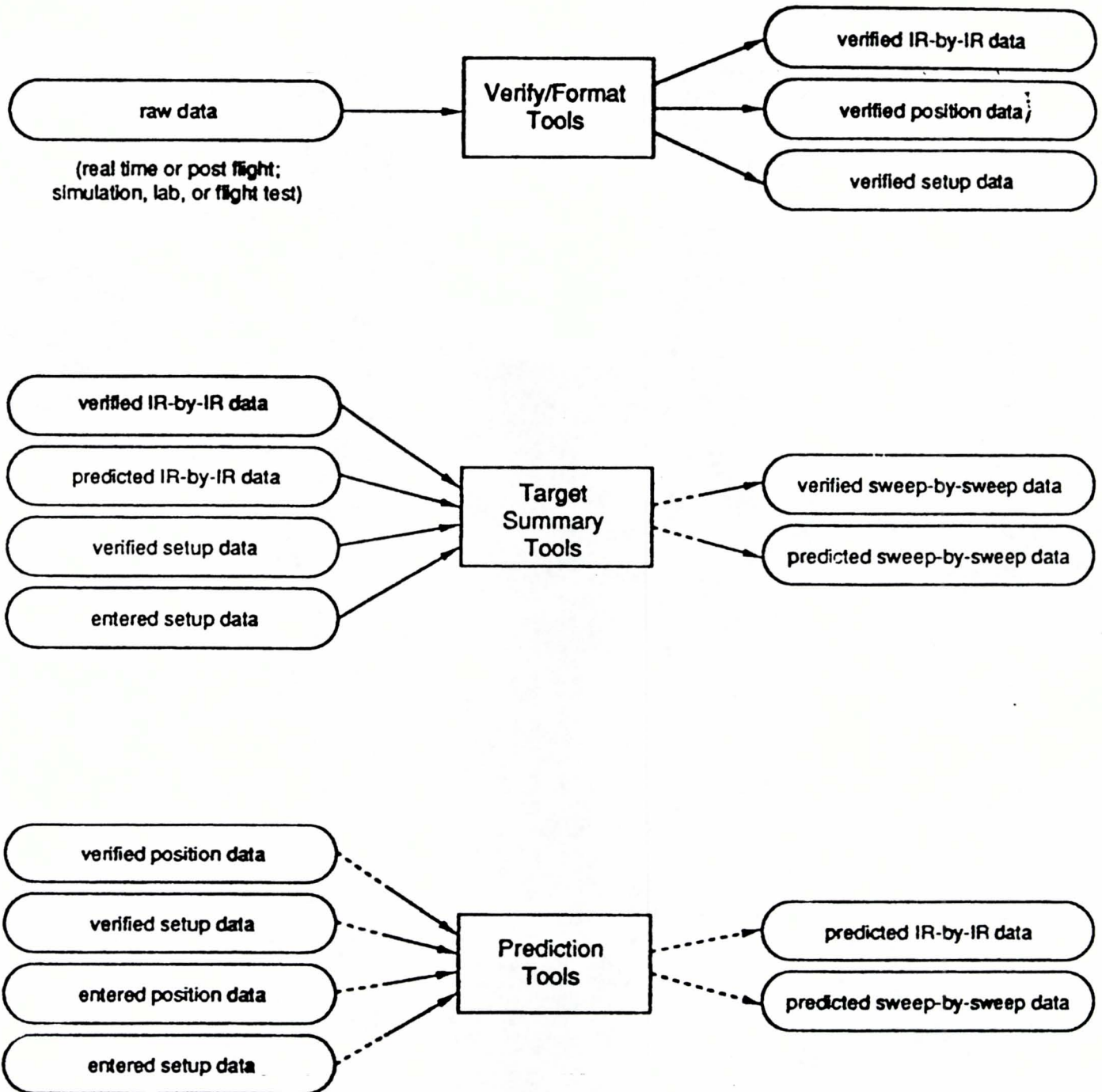


Figure 2-1. Flight Test Data Analysis Requirements (1 of 2).

Analysis Requirements Summary (con't)

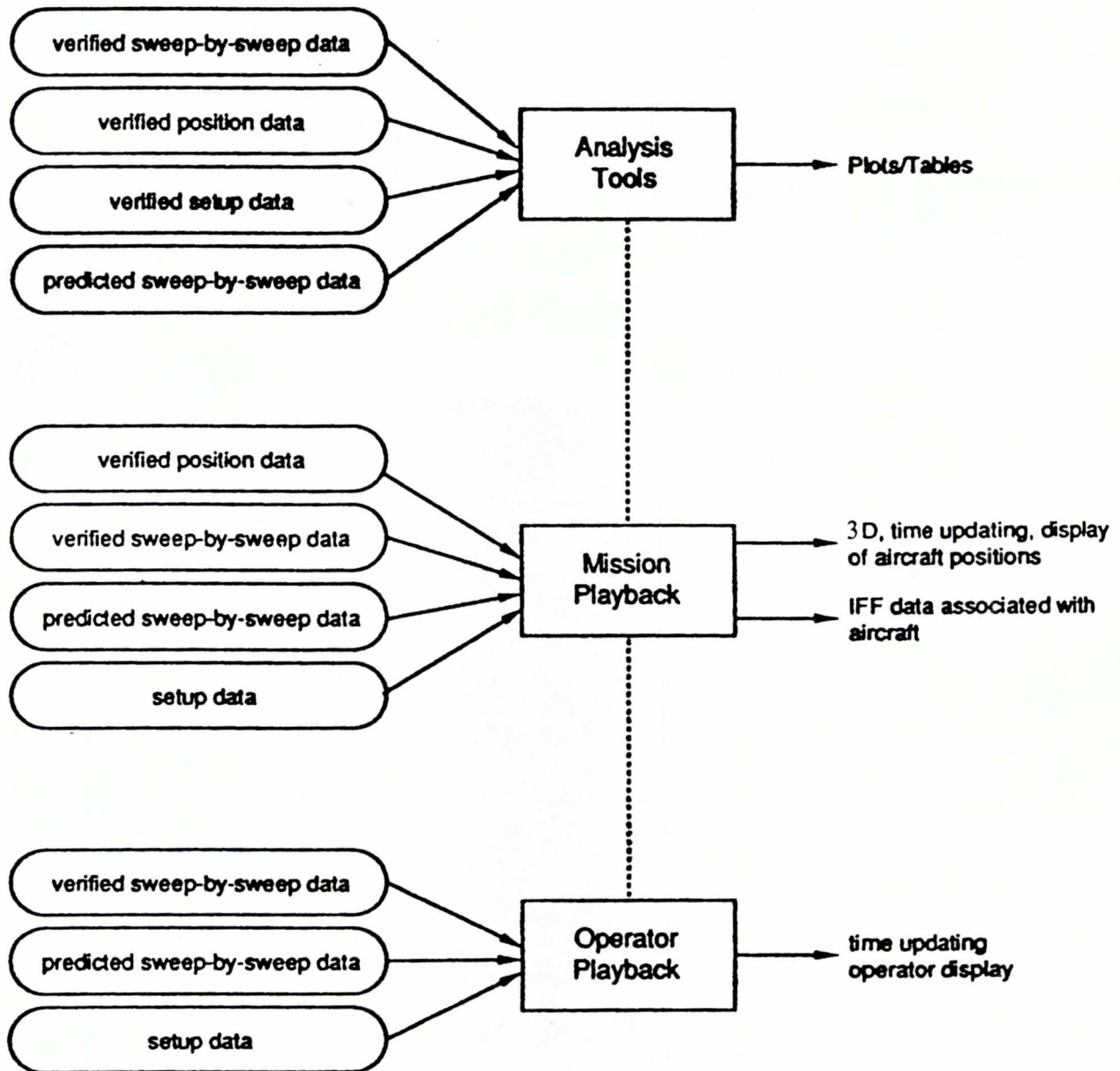


Figure 2-1. Flight Test Data Analysis Requirements (2 of 2).

2.4 PROPOSED METHODS AND PROCEDURES

The TESTS Feasibility Report laid out the recommended approach and design to implement a simulation tool to satisfy the TEMP objectives and to identify and explore the technical risks associated with this recommended design. This final report delves one level below the feasibility findings to describe the functional flow characteristics and design details of the proposed TESTS configuration. The primary approach taken to define a baseline configuration focuses on a requirement for a stand-alone capability. This approach could be used if one or more assets of the Aircraft Combat Environment Test and Evaluation Facility (ACETEF) were occupied in a higher priority test. Figure 2-2 describes the baseline configuration for the Transponder and Interrogator Simulators. Here, the SWEG simulator and its host computer are integral to the baseline configuration.

In addition, the requirement exists for TESTS be able to interface with ACETEF (in particular with the Communications, Navigation and Identification Laboratory (CNIL) to carry out its testing mission. This additional requirement necessitates the identification of an "alternate configuration." This configuration simply uses the ACETEF assets to host SWEG and communicate with the TESTS computer through a common shared memory interface. As long as the interface requirements between the TESTS & SWEG computers are the same, the "alternate configuration" is simply a subset of the "baseline configuration."

It is important to consider that, in the data reduction "multi-lateration" process (using flight test data procedures), the fidelity of the analysis models of each subsystem and their relationship to the other subsystems. The level of fidelity is directly related to how well the error sources of the subsystems can be uncoupled in the analysis itself. For example, if the attenuation of an IFF signal is measured during the flight test at the receiver, this measurement, along with the position/velocity of the signal source and receiver, is collected and available as part of the data set. Attenuation sources between the transmitter and receiver are attenuations due to such things as antenna pattern, propagation medium, fading, dispersion phenomenon, and the like. Each one of these potential error sources must be modeled and the total measured attenuation apportioned to each error source. The accuracy of this apportionment is dependent on the fidelity of the models and the "conditioning" of the data set. The resulting data reduction process, using this added dimension, would enhance the "Overall System Performance Analysis" and the partitioning of error sources in the "IFF Performance Steps" procedures.

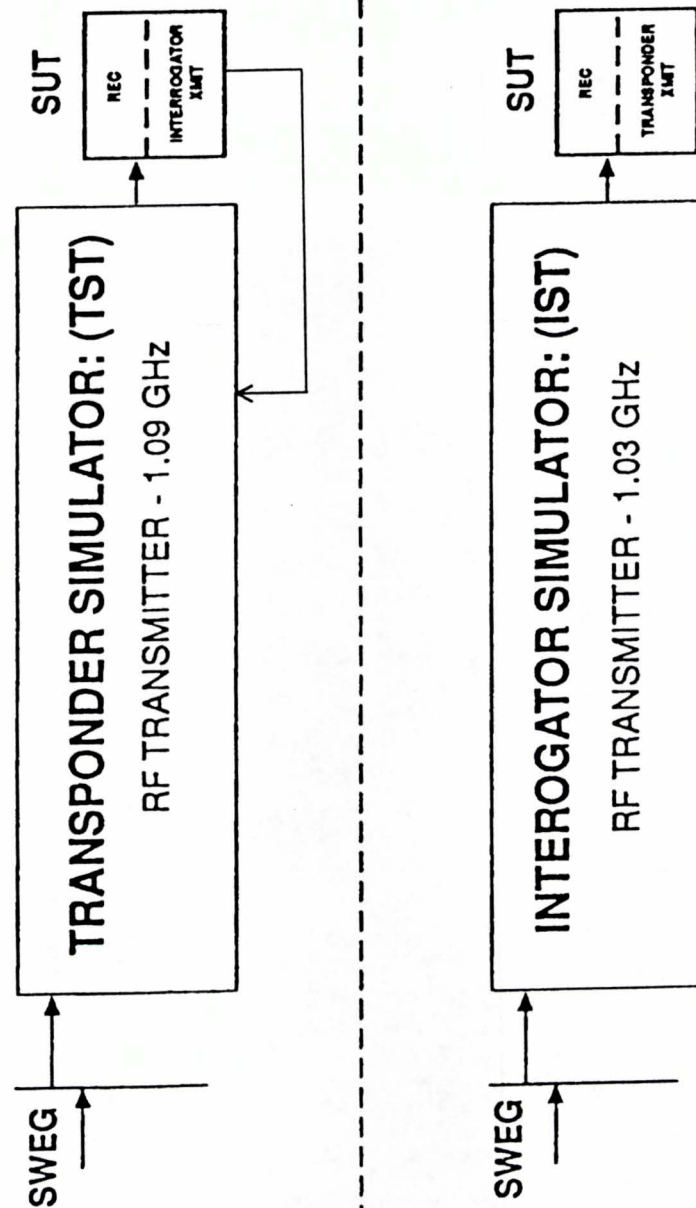


Figure 2-2. TESTS Baseline Configuration for Transponder and Interrogator.

The case-in-point to this discussion is that test and evaluation, using flight test data, is highly dependent on accurate, "well-conditioned" data sets and high fidelity models (with determined subsystem parameters) describing the error sources for each required parameter. As a result, there is a strong case that simulation modeling can greatly enhance the flight test data reduction process.

On the other hand, the "simulator" requires a calibration each time it is used. Also, the models need to be independently verified, and the system needs an overall validation and verification during the development phase of the TESTS project. Both of these requirements are met using flight test data. It is apparent that TESTS will complement/enhance the analysis of flight test data by incorporating the high fidelity TESTS models into the data reduction process. At the same time, TESTS is complemented by using the flight test data to calibrate and accomplish validation and verification (V&V) of the simulator.

The impact of this coupling of T & E procedures (flight-test to simulation) is to use the best quality of each method to reduce substantially (below 50%) the flight hours necessary to the T & E process of an IFF system. The added simulation capability will fulfill five additional TEMP objectives that the flight test method will not be able to accomplish because of aircraft or range restrictions and/or potential security difficulties. Also the creation of a large "emitter environment" is easy by simulation, but quite costly if literally deployed.

2.4.1 Summary of Improvements

Among the capabilities that TESTS will offer NAVAIRTESTCEN are:

- RF Signal Generation will provide "message level" commands from the simulator into conditioned RF signals to stimulate SUT.
- Multiplexing IFF signals from several different platforms on one signal generator can reduce the number of signal generators required.
- High fidelity models to simulate environmental channel effects. As previously noted, these "models" will also enhance the resolution of error sources in evaluating IFF emitters using flight test data.

- Integral to the simulation will be an RF conditioning device that will be controlling/conditioning the RF signal generator output to reflect existing channel effects(i.e. gain, phase, time delay and frequency changes). This hardware device will also provide for at least one multipath signal for each primary signal transmitted. Provisions for additional multipath signals may be added as future research dictates.
- A highly flexible simulator control monitor to operate and control the simulator test process through a wide range of input parameters. System diagnostic and set-up functions will be included.
- TESTS can provide a role in the Design phase of avionics equipment development. The high resolution, real-time characteristics of TESTS can determine the sensitivity of design parameters/identification of technical risk elements well in advance of freezing hardware designs.
- A subset of TESTS can be used to structure an “evaluation model” for the T&E team to use as a yardstick for evaluating the performance of the equipment to specification.
- The TESTS simulation tool can be transitioned to the Operational Test & Evaluation team by enhancing the user-friendly control mechanization and orienting the model usage to an operational oriented version.

2.4.2 Summary of Impacts

Among the impacts that TESTS will provide NAVAIRTESTCEN are:

- (a) Through the use of the “baseline configuration,” an IFF testing capability will be available that is “uncoupled” from ACETEF, thereby easing scheduling overlaps for the anechoic chamber.
- (b) TESTS will more fully exercise the SUT through TEMP objectives that flight testing can not or should not accomplish.

The impact of using the TESTS simulation tool across the entire development cycle of the program is intriguing. It would heighten program visibility and reduce program risk in the Design, Evaluation, DT&E and OT&E phases of the development process.

It is also apparent that there is cross-support between actual flight test data and the simulation architecture to consider. The actual flight data will be used to calibrate, refine and V&V the simulator, while the simulator architecture (high fidelity models) will refine the decomposition of the total error budget (obtained from flight test measurements) into identifiable subsystems. This results in a boot-strapping compatibility where the simulation tool enhances the flight test productivity, and the flight test data provides credibility to the simulation tool; this cross-support obtains optimal results for T&E.

2.5 ASSUMPTIONS AND CONSTRAINTS

To summarize, the simulation environment can become impractical if it is not bounded. Several assumptions and constraints are identifiable for TESTS. The simulation test environment should:

- be scenario driven
- parallel the operational test environment
- operate with existing facilities, but have the ability to operate stand-alone
- provide for transition between developmental DT&E and operational OT&E phases
- make use of existing hardware and software/simulation capabilities at NAVAIRTESTCEN and NAVTRASYSSEN.

SECTION 3. DETAILED CHARACTERISTICS

3.1 SPECIFIC PERFORMANCE REQUIREMENTS

Specific performance requirements for TESTS originated in an evaluation of the test objectives outlined in the MK XV Test and Evaluation Master Plan (TEMP). Whereas the MK XV program has been halted, the critical test objectives identified in that program for the proposed TESTS concept lead to a valid set of performance requirements for testing of any current generation (MK XII) or Next Generation IFF system. In basic terms, the TESTS simulation / stimulation tool must be able to receive and recognize any valid IFF transmission; it must be able to format and transmit the proper IFF responses, and it must be able to control the timing of such responses accurately enough to simulate the "real world" as it appears to the SUT. In addition, the TESTS tool must be capable of accurately calculating and applying the environmental channel effects to the RF signals returning to the SUT, and of simulating multiple platforms in space for the generation of IFF emitters. These basic requirements directly impact either the accuracy and validity requirements or the timing requirements of the proposed TESTS concept. These basic requirements are discussed below.

3.1.1 Basic Capabilities

TESTS requires a complex set of basic capabilities to provide the flexibility to support all DT&E objectives for a variety of platforms and IFF systems. The five primary capabilities which drive the TESTS design are described in the following paragraphs.

3.1.1.1 Signal Synthesis and RF Generation

The Conceptual TESTS Design, shown in Figure 3-1, shows the basic division between TESTS hardware and software components, with emphasis on the real-time communications loop between TESTS and the System Under Test (SUT). The SUT may be either an actual interrogator or an actual transponder mounted on its aircraft platform inside the shielded hangar or anechoic chamber. The TESTS tool will interface to the SUT via shielded cable connected to the RF transmit and receive ports of the SUT. The TESTS tool must provide a realistic simulation of the external environment as seen at this interface via combination of hardware and software components.

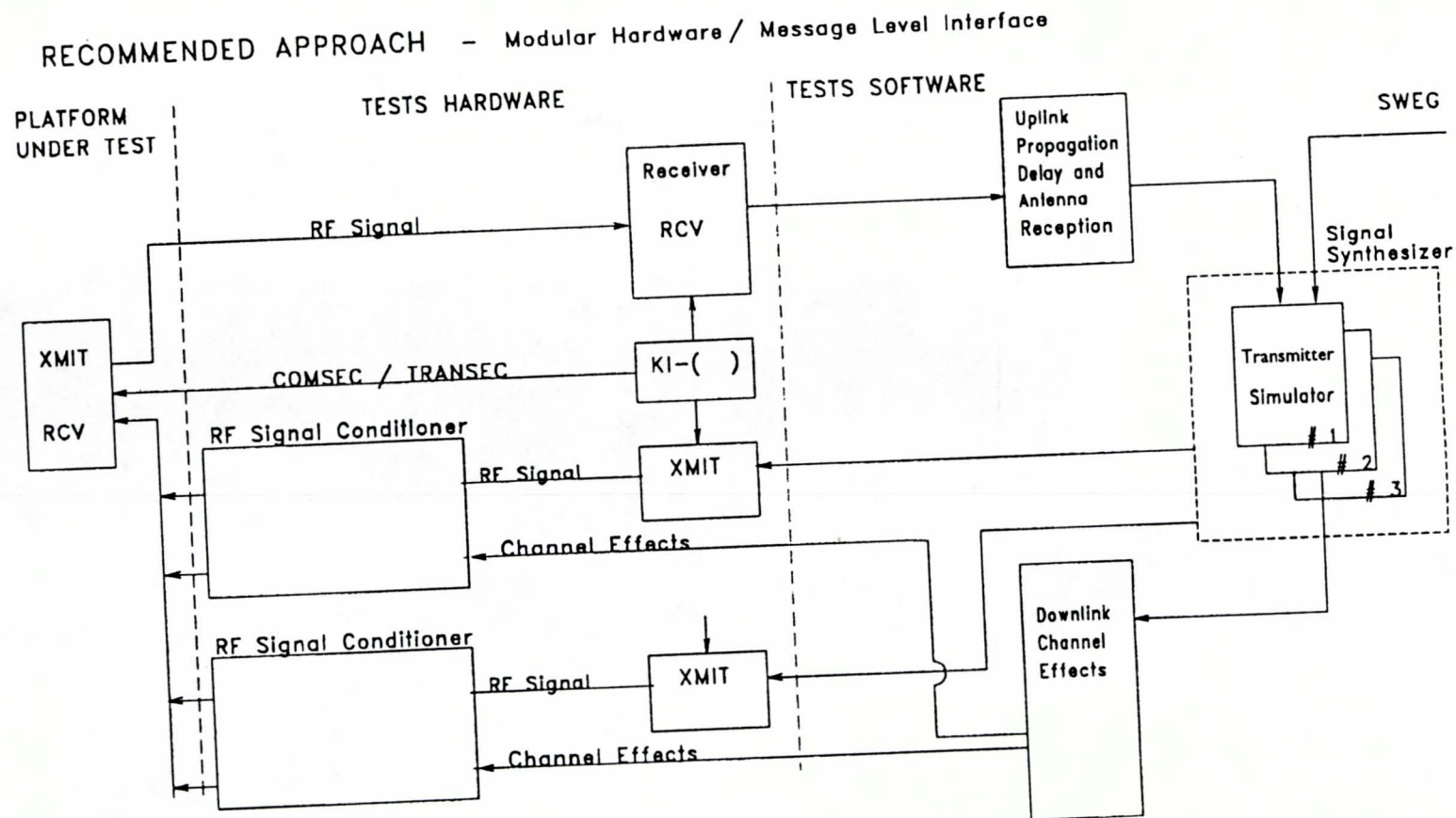


Figure 3-1. Overview of TESTS Hardware/ Software Architecture.

In order to fulfill the basic requirements for an IFF communications loop, the TESTS components must be able to determine the appropriate baseband IFF challenge or reply in order to stimulate or respond to the SUT. This determination will be dependent upon type and mode of IFF challenges received from the SUT for replies, or operator selected interrogation modes for challenges. Additional IFF replies will be generated to simulate the real world effect of Friendly Replies Unsynchronized in Time (FRUIT), and Friendly Interrogations but Enemy Replies (FIBER).

The TESTS RF Transmitter must then be able to create and modulate the uplink and downlink RF carrier frequencies to the appropriate waveforms of the MK XII or Next Generation (spread spectrum) IFF signals, and transmit them to the SUT. The accuracy of the RF waveform generation and modulation must be within the tolerances specified for pulse width, rise time, decay time, amplitude uniformity, etc., that are contained in the Mark XII or advanced IFF system specifications.

3.1.1.2 Simulation of Direct and Multipath Channel Effects

Channel effects will be calculated in software by the TESTS tool based on time and scenario dependent conditions which affect the electromagnetic transmission, propagation, and reception of the IFF signal waveforms. Channel effects include such physical phenomenon as: antenna pattern gains at the transmitter and receiver, electromagnetic propagation time delays, atmospheric absorption, refraction, and diffraction. In situations where multipath transmission effects are present, channel effects must be computed for the reflected as well as the direct transmission paths. Additionally, relative kinematic and orientation effects, such as platform antenna masking, polarization interference phenomenon, and doppler shift, must be computed.

Research efforts will define the complexity and fidelity of algorithms required to model these effects, resulting in the computation and application of distortions in the amplitude, phase, and frequency of the transmitted signal. The total time delay, plus amplitude, phase, and frequency distortions will be applied to the RF signal(s) by the special signal distortion devices which modify the synthesized RF signal between the output of the signal generation devices and the input to the SUT. Initial studies indicate that 48 dB of dynamic range (or 8 bits of accuracy) is adequate to represent the amplitude, phase, and frequency distortion channel effects.

Processing time delays and tolerances of the simulated IFF components must also be considered in conjunction with electromagnetic propagation delays, in simulating the closed loop time delay of the communication system. Accurate

simulation of multipath channel effects will often require the reflected path signal to be transmitted separately from the direct path signal by the TESTS RF transmitter; it would carry the same information and signal content, but different channel effects parameters. Initial studies indicate that multipath signal delays in the reflected path may vary from several nano-seconds to 40 μ seconds, relative to the direct path signal. Therefore, in order to represent over 6 orders of magnitude of timing resolution, a 32 bit representation for time delay is required.

3.1.1.3 Simulation of Multiple Transponders and Interrogators

Analysis of the MK XV TEMP Objectives reveals that a major benefit of the TESTS tool results from its ability to generate realistic test scenarios where many transponders and interrogators will be operating simultaneously. This results in high IFF signal densities with the potential for many overlapping or colliding IFF messages at the receiver of the SUT. System Specifications require the validation of performance as a function of interrogation rates if the SUT is a transponder, or as a function of reply rates, if the SUT is an interrogator. Interrogation rates on the order of five thousand per second, and total reply rates up to forty thousand per second may be required for such test scenarios.

As the number of IFF messages is increased (reply rate, or interrogation rate), the probability of message overlap at the receiver of the SUT likewise increases. It is important to be able to simulate this effect with high fidelity in order to test important features of the IFF receiver and processor which are designed to deal with message garble, prioritization, synchronization, intersymbol interference, etc. Therefore, the TESTS RF Transmitter must be able to generate multiple signals and their associated multipath components simultaneously. Preliminary stochastic analysis of the probability of IFF message overlap at the receiver of the SUT, indicate that by the use of multiplexing a relatively small number of independent signal generators (approximately ten) may be employed to simulate a reply rate up to 40,000 per second (see Section 5.1.7). However, the actual reply rate capability as a function of number of signal generators, is highly dependent upon the specific test scenario, and the reset capabilities and limitations of the signal generation and distortion hardware devices, which are not yet known.

3.1.1.4 Generation of RF Spread Spectrum Signals

It is assumed that the next generation of advanced IFF systems will utilize spread spectrum signals to enhance communication performance and security. The

sort of chip rates associated with spread spectrum signals severely limits the waveform manipulation and summation that can be performed in the TESTS host computer; this is due to the enormous processing requirements associated with performing convolutions and correlations on large data sets in real time. Thus, the requirement to generate multiple spread spectrum signals reinforces the decision to use multiple independent RF transmitters; the requirement also reinforces the decision to let the superposition of colliding signals occur in the hardware channel at RF carrier frequencies.

3.1.1.5 Encoding and Decoding of Secure Transmission Modes

Mark XII Mode 4 utilizes security codes generated by KIT/KIR equipment to provide secure and encrypted IFF transmissions. An advanced IFF will likewise require special communications and transmission security equipment to provide pseudo-random number (PN) code sequences and other security codes. In order to generate or decode valid encrypted IFF messages when interfacing with an actual transponder or interrogator as the SUT, the TESTS hardware will have to perform the complementary encryption / decryption functions. This will require an interface from the KIT/KIR equipment or advanced IFF security equipment in order for TESTS signal generation devices and RF receiver devices to perform in the secure transmission modes. Special test or maintenance codes may be employed by the security equipment to avoid the risk of exposure of classified operational modes. Nevertheless, security classification and access restrictions will likely be imposed upon the TESTS hardware and software components.

3.1.2 Timing

IFF systems exhibit extremely fast response times in the operational environment to accommodate high signal densities. Furthermore, advanced IFF Crypto systems incorporate highly complex timing synchronizations. As a result, timing requirements for TESTS are extremely critical. The achievement of a valid, real-time IFF simulation/stimulation tool is a critical challenge. Given the IFF capabilities required for TESTS, this issue requires a state-of-the-art computer software/hardware architecture.

3.1.2.1 Simulation Response Time

Figure 3-2 presents an analysis of the pulse sequences required to stimulate or respond to actual IFF equipment in real-time. In the real world, IFF communications are initiated by a query, which is transmitted by an interrogator. After a propagation

PULSE SEQUENCE ANALYSIS

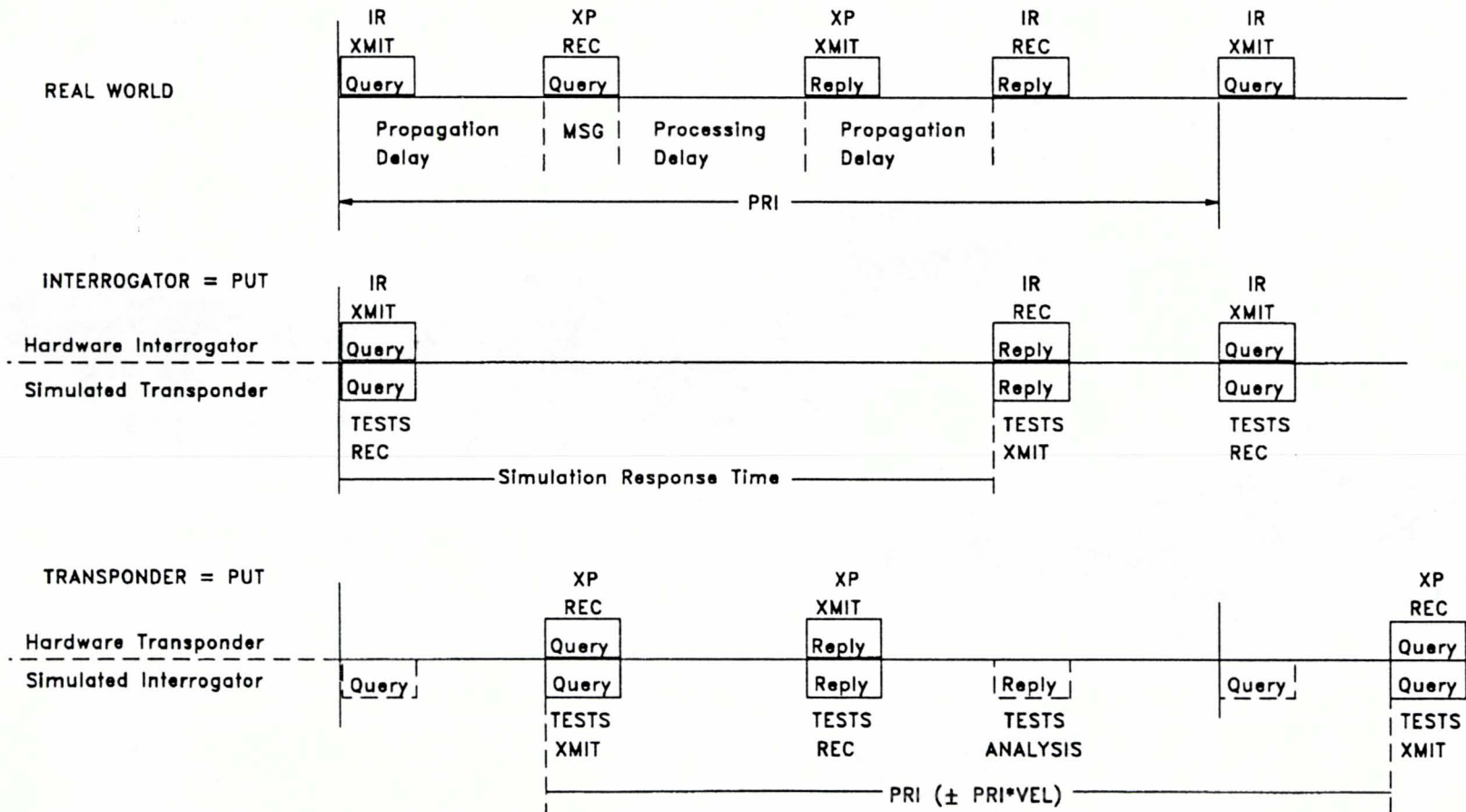


Figure 3-2. Analysis of TESTS Pulse Sequences.

delay, the query is received by a transponder. After a processing delay, the transponder transmits its reply, and after another propagation delay, the reply is received back at the interrogator. This process is repeated every Pulse Repetition Interval (PRI) determined by the interrogator. Figure 3-2 further illustrates how this process will be simulated by TESTS, where the System Under Test (SUT) may be either an interrogator or a transponder.

If the SUT is an interrogator, the required response time depends upon the round trip propagation delays, the message lengths and the transponder processing delay. For a worst case condition, at zero range, the TESTS simulator response time would have to be equal to or better than the processing time of an actual transponder. The MK XII transponder in basic SIF modes, for example, has a response time of about 3 microseconds. Round trip propagation delays add another 12 microseconds per nautical mile of slant range. If TESTS cannot meet the zero range requirement, the result is an increase in the minimum range at which the TESTS simulation can be effective.

If the SUT is a transponder, the PRI of the simulated interrogator is the critical factor, and for a high Interrogation Rate of 5000 / sec, this configuration yields a less stringent response time requirement of approximately 200 microseconds. Pulse to pulse changes in the response time due to target velocity (platform motion) have a negligibly small effect (on the order of .0001 %).

3.1.2.2 Simulation Response Time Accuracy

If the SUT is an interrogator, the timing accuracy of the TESTS simulator response is an issue, since every 100 nano-seconds of timing error translates into 50 feet of range error, as determined by the interrogator IFF analyzer. If the TESTS response time inaccuracy is very large, the interrogator analyzer may categorize valid IFF replies as FRUIT.

3.1.2.3 Scenario Update Rates

Simulation assets of SWEG may either be event driven or updated periodically. The update period for certain platform parameters, such as positions (latitude, longitude, altitude) and attitudes (pitch, roll, yaw), may be critical to the fidelity requirements of TESTS. Although additional study may be required, a preliminary analysis indicates that approximately 1.0 degrees of angular motion, and 50.0 feet of relative translational motion can be tolerated per simulation update cycle. Assuming

average aircraft angular rates of 30.0 degrees per second or less, and average closing velocities of 1500 feet per second or less, a simulation update rate of 30 times per second should be adequate for TESTS. Discussions with NAVAIRTESTCEN personnel indicate that SWEG platform position and attitude data is commonly updated at 60 to 120 times per second during scenario execution.

To meet response time requirements in a limited scenario update system, it may be required to incorporate a number of advanced simulation concepts into TESTS. Increases in response time without significant fidelity losses can be accomplished through the use of concepts developed for distributed interactive simulations. These approaches use internal data bases with predictive algorithms which are periodically updated based on real world changes, in this case SWEG. Figure 3-3 illustrates this update approach where data parameters are periodically updated based on current scenario information.

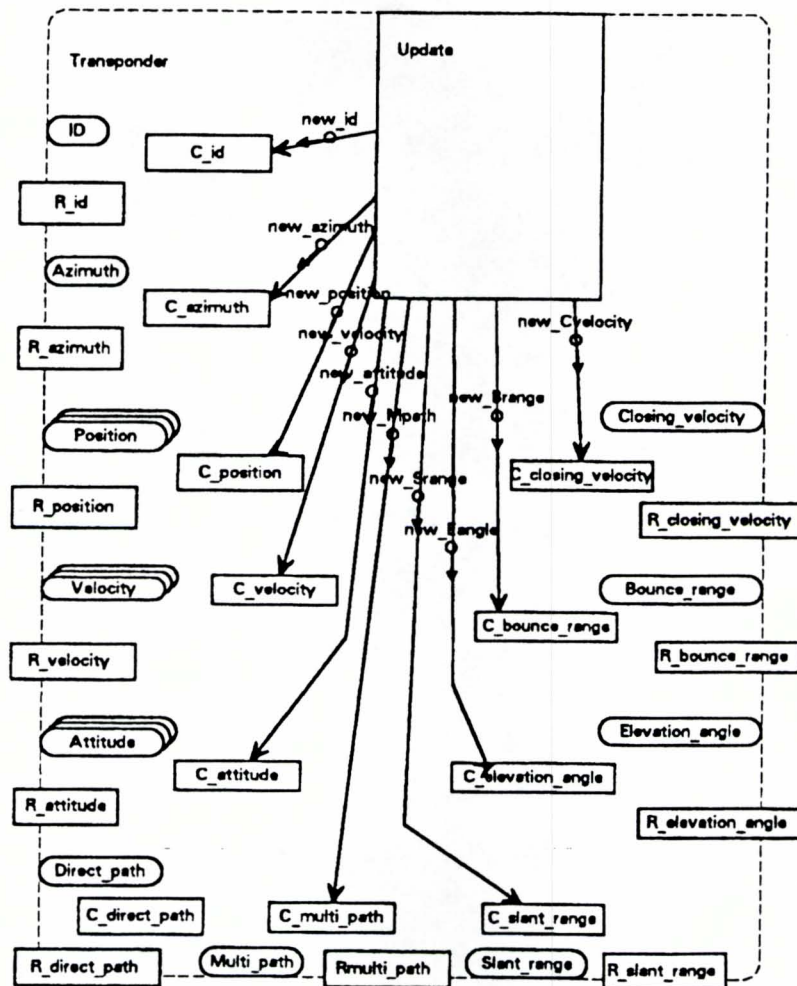


Figure 3-3. Approach to Updating TESTS Data Parameters.

3.2 FUNCTIONAL AREA SYSTEM FUNCTIONS

There are four major functional blocks within the overall TESTS architecture as shown in Figure 3-4. These major functional blocks within TESTS, which include supporting interface structures, consist of the TESTS simulator component, the TESTS stimulation component, the scenario control component and the environmental component. The first two components comprise the core functionality of TESTS. The latter two components are external capabilities required for TESTS to be fully functional.

3.2.1 Simulator Component

In the signal generation operation, the TESTS simulator component generates IFF messages, calculates propagation effects, etc., in software, and formats the simulation commands to the stimulation component. In the receiving operation, the simulator component decodes the received signal and passes it to the data capture facility.

The TESTS Host Computer and Interface Bus provides the hardware processor platform and high speed interface data bus required to execute the TESTS Software Components and provide the communications link between the TESTS Software Components, and the TESTS Hardware Components (TESTS RF Receiver, TESTS Hardware Signal Generators, and TESTS Signal Distortion Devices).

TESTS Software Components provide real-time calculation of IFF message content and signal channel effects for platform in the scenario as it responds or interrogates the SUT. These components provide the real-time link between the scenario data base driven by SWEG, and the TESTS Hardware Components that interface directly to the SUT. The TESTS Software Components are allocated into eight autonomous software tasks, which respond to system events under control of a real-time multitasking operating system kernel. A functional description of each software task is provided in Section 4.1

3.2.2 Stimulation Component

The stimulation component is the hardware RF generator portion of TESTS. It includes both the signal generation hardware and the signal distortion, i.e., channel effects, hardware. This component translates the message level simulation command into the appropriate signal signature(s), both data and characteristics, required to stimulate the SUT. On the receiving side, it demodulates the SUT signal and transforms the received signal into a format interpretable by the simulator module.

SIMULATOR COMPONENT (S/W)

SIGNAL SYNTHESIS:

- Generates IFF messages
- Calculates propagation effects
- Sends formatted command signals to stimulation component

RECEIVING OPERATION:

- Decodes received signal
- Sends to analysis section

STIMULATION COMPONENT (H/W)

RF SIGNAL GENERATION & CONDITIONS:

- Translates "message level" command from simulator into conditioned RF signal to stimulate SUT

RECEIVING OPERATION:

- Demodulates SUT signal
- Transforms to message format for simulator interpretation

OPERATIONAL CONTROL COMPONENT (SWEG/TESTS CONTROL MODES)

OPERATIONAL CONTROL:

- Sets up TESTS configuration
- Identifies parameters for test
- Controls operation in stand-alone configuration

SCENARIO CONTROL:

- Definition of DT&E scenario with SWEG

DIAGNOSTIC CONTROL:

- Inputs values to calibrate and test
- Tests hardware and software

ENVIRONMENTAL COMPONENT (JAMMERS/ECM)

PROVIDED BY EXTERNAL SOURCE:

- Jammer/ECM environment

PROVIDED BY TESTS:

- Interface to integrate into design

CAPABILITY PROVIDED (TESTS CONFIGURATION)

- Either by ACETEF through EWISTL or off-the-shelf hardware

Figure 3-4. TESTS Functional Components.

The TESTS Hardware Signal Generators are a bank of addressable IFF signal generation devices that can construct and modulate any of the required IFF signals at RF frequencies, including spread spectrum signals for an advanced IFF. The signal generator receives the desired message in discrete baseband format over the high speed Interface Data Bus from the TESTS host computer, and outputs the RF message to the TESTS Signal Distortion Devices which apply the channel effects to the signal prior to reception by the SUT. The hardware signal generators also receive crypto codes and PN sequences from the IFF Crypto unit, and apply these to the signal construction and modulation process when required for secure IFF transmission modes.

The TESTS Signal Distortion Devices are a bank of addressable, programmable hardware devices that impose channel effects parameters upon the RF signals produced by the TESTS Hardware Signal Generators. These devices receive the RF signals from the TESTS Hardware Signal Generators, modify the RF signal, and output the signals over a hardware coaxial interface to the RF input port of the SUT. Each device provides at least two parallel output signal paths to allow separate control for simulation of a direct path and a one indirect path (multipath) signal. Each device will also provide a summation input port to receive and mix the RF signals output by other TESTS Signal Distortion Devices when multiple Signal Generators are in use. Each device receives two sets of channel effects parameters from the TESTS host computer over the high speed Interface Data Bus. Each set of channel effects parameters contains an attenuation factor (gain), phase, dispersion, frequency offset, and time delay corresponding to both the direct and indirect signal paths. The channel effects are then implemented by programmable hardware components in each device that modify the incoming RF signal in the prescribed manner.

3.2.3 Environmental Component

The environmental component provides the jammer/ECM environment for TESTS. This component will be provided by external resources. TESTS will provide the appropriate interface to integrate this capability. Depending upon the TESTS configuration, this capability may be provided by ACETEF through EWISTL, CNIL or other off-the-shelf hardware.

3.2.4 Operational Control Component

The operational component provides the capability to set up the TESTS configuration, generate the test scenario, specify data collection requirements,

conduct diagnostics tests, and conduct calibration of the TESTS hardware and software. An operator workstation will be provided to control all TESTS specific features of the operational control. This workstation will be supplemented by the SWEG host computer which is used for scenario generation and control.

The primary scenario control element for TESTS is SWEG. SWEG provides operational information concerning platforms, and environmental data and terrain data required for multipath and other propagation effects determinations. This component also initializes the appropriate test conditions and provides the interface to other facilities, e.g., CNIL, ACETEF. SWEG will be augmented by a TESTS specific scenario control subcomponent if it is determined that all parameters required for TESTS can not be obtained from SWEG.

3.2.4.1 Operational Control

The operational control elements of this function include the capability to specify the current configuration of TESTS, select the operational mode for TESTS, and tailor the data collection requirements to the current test.

The TESTS configuration alternatives include a stand-alone configuration and configurations where TESTS is integrated with ACETEF. This subfunction is required to identify the source of SWEG data that TESTS will access. In addition, the configuration feature will also identify whether TESTS is operating in a benign configuration or whether it includes provisions for threat signals or other noise sources. This configuration will also be used to identify whether the SUT is a transponder or interrogator, and the specific IFF system being evaluated.

A second feature under operational control is the specification of data capture elements relevant to the current test. This feature is included to optimize the data capture and simplify data analysis requirements.

The third feature under operational control is the specification of the mode in which TESTS is operating. TESTS has both an operational mode and a diagnostic mode as described below.

3.2.4.2 Scenario Control

The primary source of scenario control for TESTS is provided through SWEG. The SWEG scenario is generated on a stand-alone computer which is interfaced to the

TESTS host computer through a shared memory interface. TESTS will provide the capability to augment the SWEG scenarios via the TESTS operator console to add any data elements required for TESTS that are not available within SWEG. (Several data required data elements are currently not implemented in SWEG, but are scheduled for addition in future SWEG updates). The addition of data to the SWEG data bases is feasible because of the well defined nature of the data bases. This capability requires supplementary data to be entered into shared memory.

3.2.4.2.1 SWEG

The SWEG Host Computer is the hardware processor that executes SWEG and updates the SWEG data base during operations with TESTS. Depending upon the test configuration, the SWEG Host Computer may be provided by ACETEF, by CNIL or by an independent workstation for stand-alone testing.

The SWEG Software Components provide the scenario and environmental simulations necessary for problem initialization and real-time generation of all platform data during TESTS operation. Platform positions, velocities, attitudes, antenna patterns and pointing angles, terrain elevation angles, and other such relevant information is calculated and maintained by various modules of SWEG. TESTS will utilize or upgrade existing SWEG simulation models whenever possible, and will conform to the conventions established for ACETEF regarding scenario preparation, initialization, execution, shutdown, and post processing phases of operation.

The SWEG Shared Memory Interface provides direct memory access to the data generated by SWEG in real-time. This interface also provides and enforces a standard format for the interface of the various assets of ACETEF, and defines the protocol for interactions between various components. The stand-alone configuration for TESTS will incorporate a shared memory interface for SWEG which parallels ACETEF. Properties of this interface are further discussed in Sections 3.4 and 4.4.

3.2.4.3 Diagnostic Control

The diagnostic control element in TESTS is used to calibrate the signal generation and conditioning hardware, and conduct tests of the TESTS software. The provision of BIT capabilities for software is included to ensure that the software has not been corrupted and to facilitate V&V of future software enhancements. Both automatic and operator initiated software capabilities will be provided.

The primary function of the diagnostic control is to provide the capability to test and calibrate TESTS signal generation hardware. This feature will be implemented through a series of menu driven diagnostic routines. The diagnostic tests will permit each of the signal generators to be tested independently and as a group. The diagnostics test is used to verify the operation of the signal multiplexing hardware. The diagnostic routines will also permit the user to enter selected levels of each signal conditioning parameter for the generation of selected conditions. These tests will verify the operation of each signal conditioning component, and by comparison to an unconditioned waveform permit the calibration of the signal conditioners. Capability will be provided for both pulse based and spread spectrum based signals.

It will be possible to record diagnostic data (signal waveforms) using the TESTS data collection system for later analysis and/or to serve as a calibration record.

3.3 HARDWARE/SOFTWARE FUNCTIONS

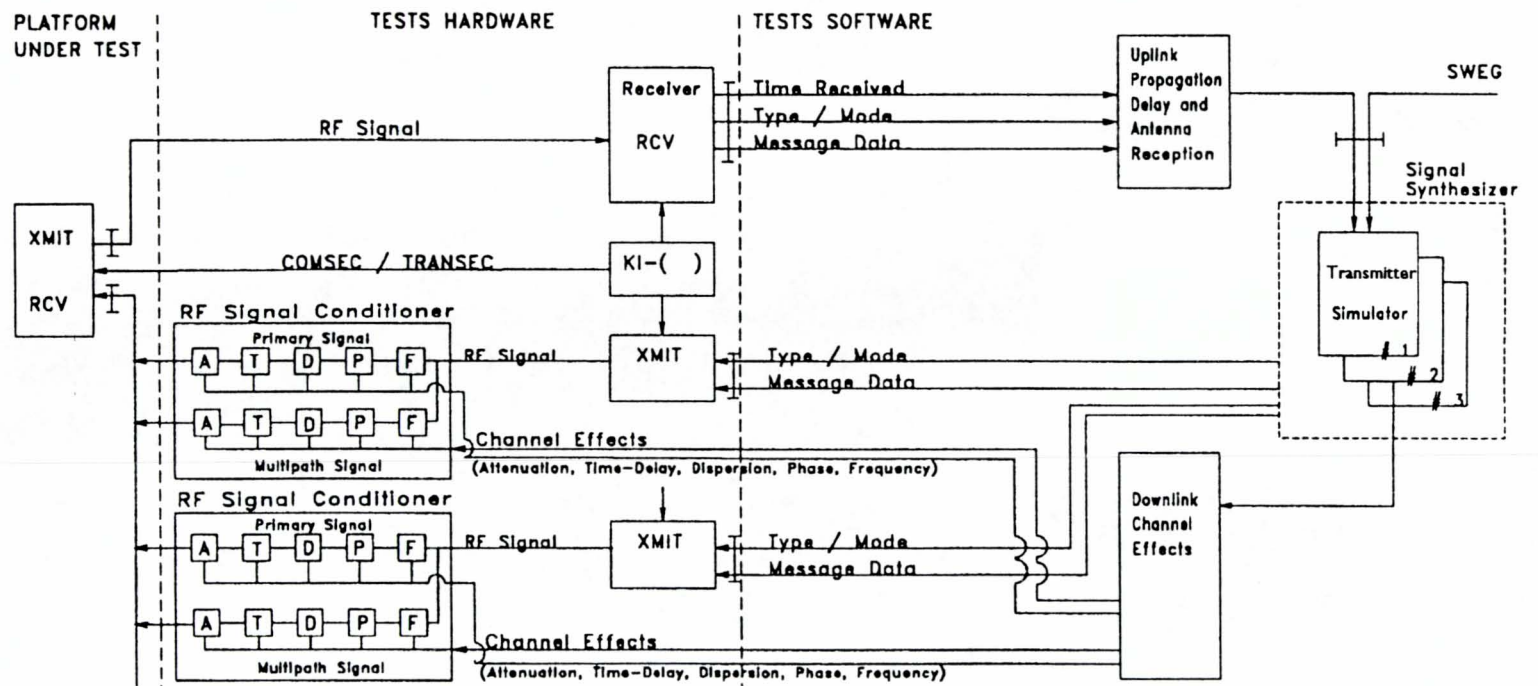
Figure 3-5 shows the major functional areas of the proposed TESTS system functions. The proposed TESTS system will consist of the SUT, IFF Crypto Unit, TESTS RF Receiver, TESTS Signal Generation Hardware, TESTS Signal Distortion Devices, TESTS Host Computer and Interface Bus, TESTS Software Components, SWEG Host Computer, SWEG Software Components, and SWEG shared memory interface.

Important aspects of the recommended approach to the TESTS hardware/software interface that are represented in Figure 3-5 are:

System Under Test (SUT) - either an IFF interrogator, or IFF transponder installed on the Platform Under Test (PUT), which may be located in either the shielded hangar or anechoic chamber facilities of ACETEF.

TESTS Receiver - Able to recognize each of the possible IFF signal types and modes, and to demodulate, decode, and despread the signal to determine message data content. It sends the decoded IFF signal in discrete baseband format, and the time that the IFF signal was received to the TESTS host computer over the high speed Interface Data Bus.

RECOMMENDED APPROACH - Modular Hardware / Message Level Interface



I - Data Collection Nodes

Figure 3-5. TESTS Functional Architecture.

KI-() - Real or simulated encryption device that provides the COMSEC / TRANSEC sequences to the TESTS Receiver, TESTS Signal Generators, and Platform Under Test. This unit will interface to the SUT as well as the TESTS RF Receiver and TESTS Signal Generation Hardware to provide real or simulated crypto codes for use in testing secure IFF transmission modes.

TESTS Signal Generators (XMIT) - Receives a complete message in binary (baseband) format from the TESTS host computer, and constructs the desired IFF message modulated at RF frequency for transmission over hardware channels to the Platform Under Test. The RF signal is then passed to the RF Signal Conditioner.

RF Signal Conditioner (A-T-D-P-F) - Special purpose hardware devices that can be used to dynamically introduce channel effects in the generated IFF signals. They contain programmable attenuation (A), phase (P), time delay (T), dispersion (D) and frequency shift (F) devices that can be directly controlled from the TESTS host computer. Separately programmable paths will be provided to allow for at least one direct and one indirect signal path to simulate multipath effects at the receiver of the Platform Under Test.

Platform Under Test (PUT) - This represents the RF transmit and receive hardware lines of the actual IFF equipment on the Platform Under Test.

3.3.1 Block Descriptions

PLATFORM UNDER TEST:

Interrogator

Functional Description:

SUT installed in an aircraft in an anechoic chamber or shielded hangar.

Block Inputs:

Interrogation requests from platform, KI-() COMSEC and TRANSEC coding information, RF reply waveforms.

Block Outputs:
RF interrogation waveforms.

Internal Operations:
Uses COMSEC/TRANSEC coding information to generate interrogation waveforms in response to platform interrogation requests. Uses COMSEC/TRANSEC coding information to interpret RF reply waveforms.

Transponder

Functional Description:
System under test (SUT) installed in an aircraft in an anechoic chamber or shielded hangar.

Block Inputs:
RF Interrogation WAVEFORMS, KI-() COMSEC and TRANSEC information.

Block Outputs:
RF reply waveforms.

Internal Operations:
Uses COMSEC/TRANSEC coding information to interpret interrogation waveforms and generate, when appropriate, reply waveforms.

TESTS HARDWARE:

Signal Receiver

Functional Description:
Detects RF IFF signals from SUT, converting them to a message level data format.

Block Inputs:
SUT IFF system output waveforms; COMSEC/TRANSEC information.

Block Outputs:

Message level data format RF signal description.

Internal Operations:

Message level signal recognition and demodulation including despreading, decoding and/or decryption.

Signal Transmitter

Functional Description:

Converts software generated message level data format signals into RF SUT stimulus signals.

Block Inputs:

Message level data format RF signal descriptions; COMSEC/TRANSEC information.

Block Outputs:

RF SUT stimulus signals.

Internal Operations:

Message level modulation including spreading, encoding and/or encryption.

KI-Q

Functional Description:

Crypto unit which interacts with MK XV or Navy Advanced IFF Subsystem to provide COMSEC/TRANSEC information to IFF Subsystem and TESTS host processor.

Block Inputs:

Time of day information and key codes.

Block Outputs:

COMSEC/TRANSEC codes via shielded cable.

Internal Operations:

Actual internal operation is classified and may be replaced in some test cases with an unclassified substitute.

RF Signal Conditioner

Functional Descriptions:

Implementation of channel effects on RF signals.

Block Inputs:

Control signals originating in software.

Block Outputs:

Perturbations on RF signals.

Internal Operations:

Programmable time delay would respond to predetermined control signals with predetermined amounts of uniform group delay. Programmable phase and gain blocks would similarly apply variable levels of carrier phase and signal attenuation.

TESTS SOFTWARE:

Uplink Propagation Delay and Antenna Reception

Functional Description:

Computes propagation delay to message level data format SUT RF signal descriptions and passes data if it was received in the antenna's reception lobe.

Block Inputs:

Message level data format descriptions of SUT RF signals.

Block Outputs:

Message level data format signal descriptions modified for propagation delay.

Internal Operations:

Addition of propagation delay via message level data format descriptions computed for direct and reflected signals. Rejects data if it was not received in the antenna's reception lobe.

Transponder Simulator

Functional Description:

Receives TESTS interrogations and formats replies appropriate to the test function and time dependent scenario conditions.

Block Inputs:

IFF message types, modes and content.

Block Outputs:

New IFF message types, modes and content.

Internal Operations:

Follows test scenario to simulate individual IFF platforms.

Downlink Channel Effects

Functional Description:

Computes channel effects to message level data format.

Block Inputs:

Simulation scenario environment information.

Block Outputs:

Control signals for programmable time delay, dispersion, frequency shift, phase and attenuation blocks.

Internal Operations:

Computes channel effects and sends commands to RF Signal Conditioner to implement these changes.

3.3.2 Supporting Discussion

In the Message Level Interface approach, the entire IFF message is represented in digital data format. The TESTS Hardware consists of a receiver and a bank of signal transmitters. The Recommended Concept receiver is designed to detect, demodulate, decode and despread interrogations from the SUT (when operating in the transponder mode). The message contained in the interrogation is then passed on to TESTS software along with the time received and the type of interrogation employed. TESTS signal synthesizer software components can then work directly with digital baseband data to formulate appropriate responses. The signal transmitters in TESTS hardware may be invoked by TESTS software to send given replies to the SUT under given modulation types or modes. The Recommended Concept TESTS software components accomplish scenario simulations by tracking platform positions and computing uplink and downlink channel effects. These effects are introduced via a software driven hardware interface subsystem which has been labeled an RF Signal conditioner. This TESTS hardware subsystem is comprised of programmable TESTS hardware attenuation blocks, phase blocks, dispersion, frequency changers and time delay lines. Similar functions are performed when operating in the interrogator mode, except that interrogations are initiated by the TESTS software components, and replies from the SUT are recorded for analysis.

3.4 INPUT-OUTPUT REQUIREMENTS

TESTS has a detailed set of input-output requirements. The inputs to TESTS are derived from the TESTS operator console/workstation and SWEG. The outputs from TESTS can be divided into two classes: those that are passed to the TESTS stimulation hardware and those which are collected for later data analysis.

The inputs requirements derived from SWEG provide the scenario, platform and terrain data required for TESTS. Additional inputs to TESTS are provided through the TESTS operator console/workstation. These additional inputs are used to control the operation of TESTS and conduct diagnostics tests. Operational control inputs include the configuration of the TESTS system, stand-alone or integrated into ACETEF, other signal sources (jammers), and data collection requirements. These inputs will be entered via a series of start-up menus. The operator workstation is also used to conduct testing and calibration of TESTS hardware and software. These functions will permit assessment that TESTS software is not corrupted and that the hardware is generating and/or modifying RF signals within specifications.

The primary TESTS outputs involve the data collection requirements. The specific data collected will vary depending upon whether TESTS is operating in an operational or diagnostics mode. The parameters collected in the operational mode will provide sufficient data to enable assessment of the SUT against TEMP objectives. The available parameters for operational DT&E are identified in Section 4.0.

3.4.1 SWEG

The primary input interface of TESTS during testing will be provided by SWEG. SWEG has been updated to control and coordinate tactical engagement simulations and provides a rich library of platform and emitter models. SWEG provides a standard format for the shared memory interface between the various components, and defines the protocol for interactions between components, Figure 3-6. The software components of TESTS will interface to the SWEG shared memory for required scenario simulation data, such as platform positions, attitudes, velocities, terrain elevation data, antenna pattern directional attenuations, antenna scan rates, etc.

3.4.1.1 Shared Memory for SWEG

There exist three major issues that TESTS must address in the use of a shared memory interface for SWEG:

- Structure of shared memory and techniques used to manage it.
- Read/Write conflicts.
- The use of mailboxes and messages for some types of information passing.

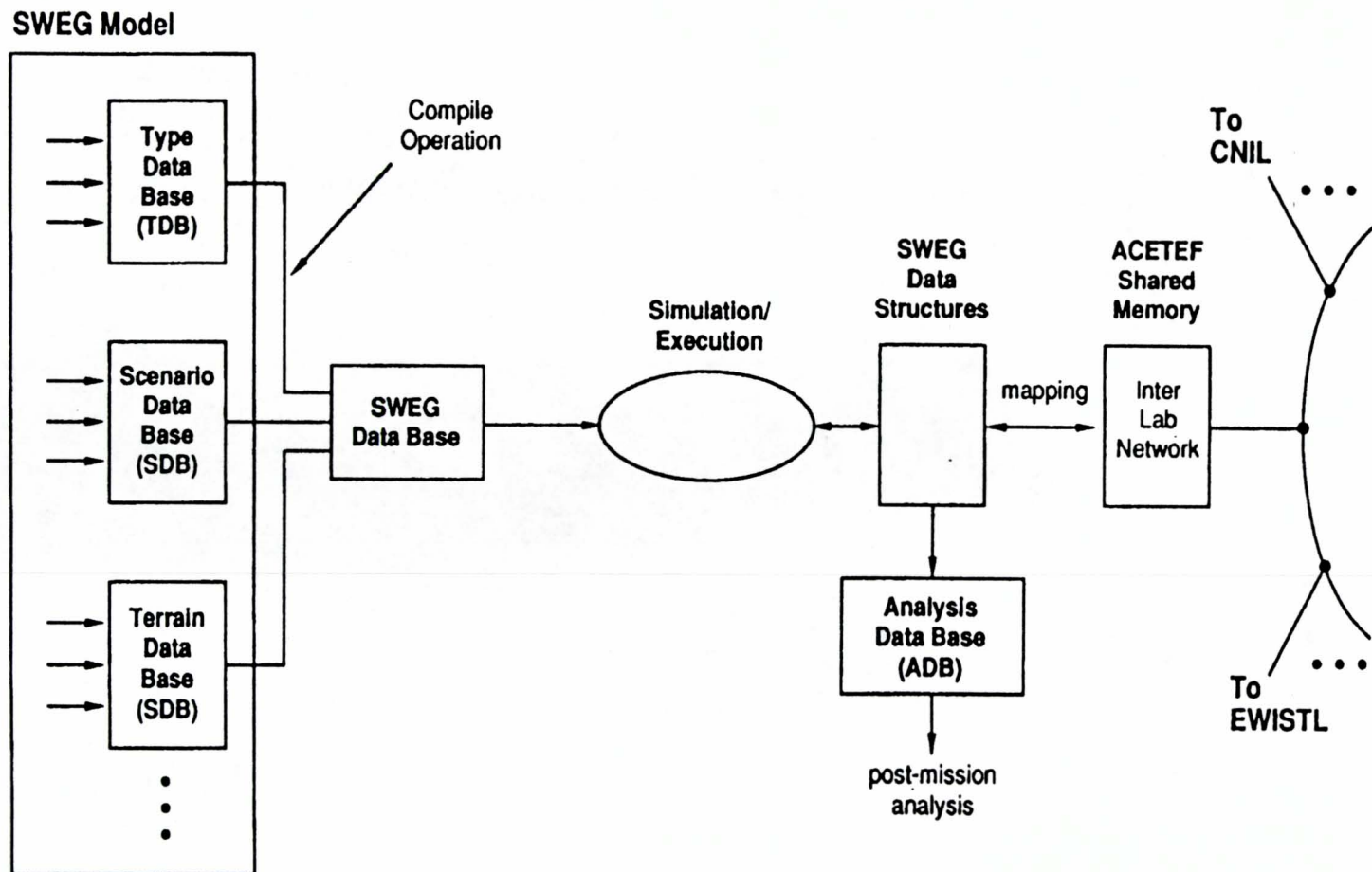


Figure 3-6. SWEG Interface.

3.4.1.1.1 Shared Memory and Management Techniques

The structure of shared memory as used within SWEG is illustrated in Figure 3-7. Data in SWEG shared memory has four primary characteristics that must be accommodated in the SWEG TESTS interface:

FUNCTION OF THE DATA: The data in the shared common memory has one of three functions: [1] Administrative (internal control of data space management/SWEG); [2] Global shared data (used by two or more assets); [3] Data unique to an asset.

DATA PERFORMANCE: One of the most difficult technical issues is the description of rules for when and where reading and writing to the shared memory can occur, and which assets have what privileges for which data blocks. Static data blocks, once set up, will not move (the pointer to their location is constant or fixed). In addition, the values in the data block will not change. Changeable data blocks will not move once they are set up, but the values within the data block can possibly change. Volatile data blocks can come and go (they may or may not exist, and the pointer to them will not be constant).

DATA LOCATION: The location of data within shared memory can either be absolute, or relative. Except for the master data block pointer (1), all of the other data blocks are relative. This characteristic of the data blocks makes it easier to modify and upgrade ACETEF, since none of the interfacing software is allowed to assume that data (except for the master data block) will remain in the same place from run to run.

SIZE OF DATA BLOCKS: Data blocks are either of constant fixed length, varying fixed length, or variable length. Constant fixed length data blocks have the same length everywhere, for each instance of that type block. Varying fixed length blocks, for a given type of data block, have a constant fixed length for each instance, but between instances the lengths may vary. Variable length data blocks have a dynamically calculated length that cannot be estimated before runtime. This last characterization is the most difficult to manage, and variable length data blocks will be avoided, especially when they have the data permanence characterization of volatile.

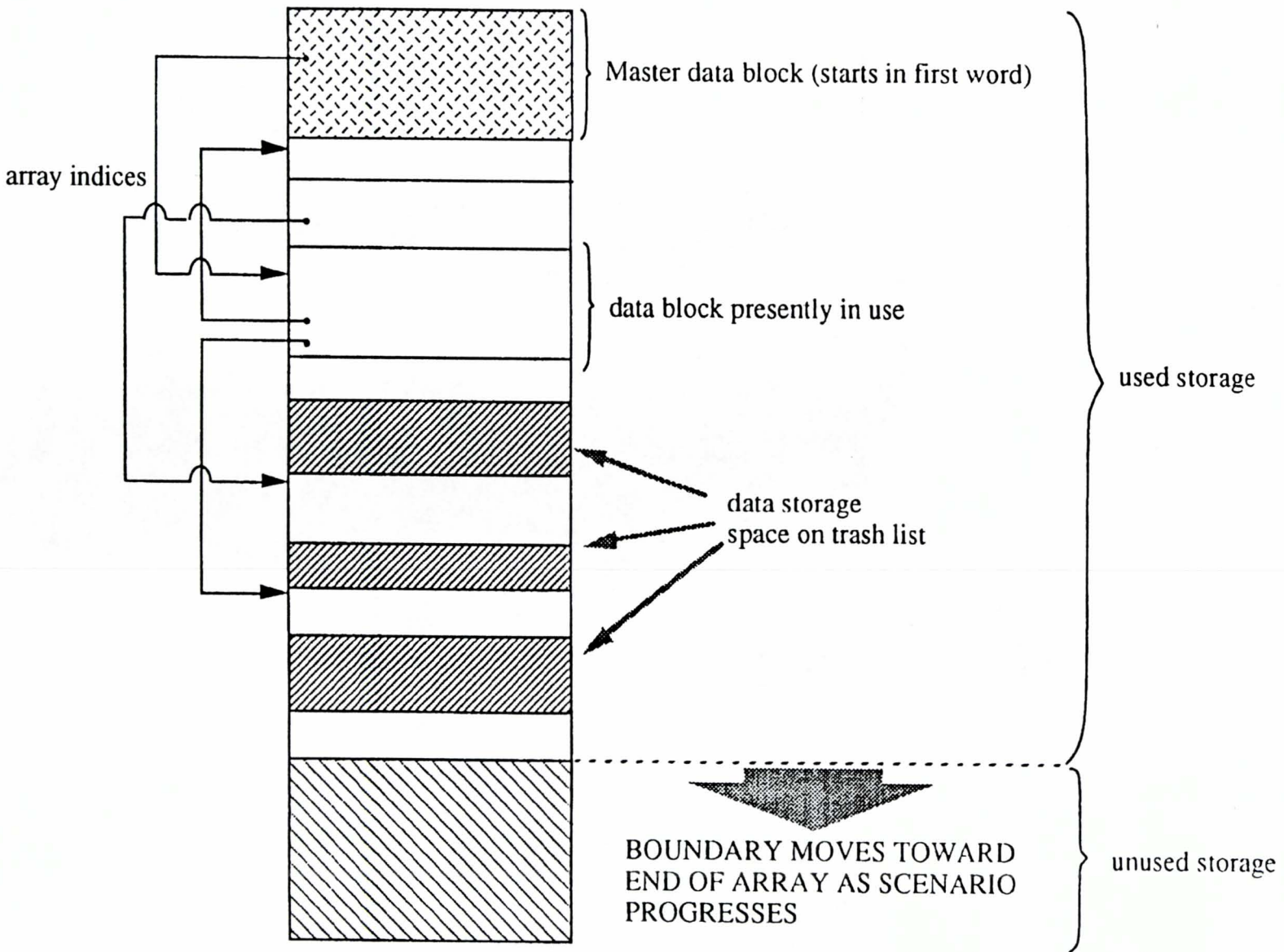


Figure 3-7. SWEG Shared Memory Architecture.

3.4.1.1.2 READ/WRITE Conflicts

Common access static data blocks are not subject to read/write conflicts, since the values do not change. Changeable or volatile data blocks can potentially be subject to read/write conflicts. It is possible that one process may be reading a data block at the same time that another process is writing to, updating or deleting the data block. Therefore, TESTS must consider read/write conflicts as they impact input data integrity, currency and validity.

TESTS SWEG access routines must be designed to accommodate both periodic and aperiodic update rates within SWEG data bases. Updates happen periodically in some cases, and aperiodically in other situations. There are different requirements for the two cases. The update rates and access rates also affect read/write contention. The worst case might be assumed to be a high update and a high access rates, but this is not in actuality the worst case. High rates for updates and accesses usually happen for "reality" data: Positions and Velocities. There will be only one writer and possibly a large number of readers. Even if during one read operation an old x-coordinate value and new y- and z-coordinate values were read, the effect is almost unnoticeable.

3.4.1.1.3 SWEG Mailboxes

SWEG uses mailboxes and messages to minimize multiple read and write conflicts where necessary (see Figure 3-8). Each asset that can receive information from another asset has a mailbox in shared memory. Some assets might have several mailboxes. SWEG, for example, will have a mailbox for each other asset in the scenario. A mailbox, then represents a one-way connection between exactly two assets. If the connection is two-way, then each asset will have a mailbox.

Each mailbox has a set of blank message forms which are allocated at initialization. There are one or more blank messages for each type of incoming message that the asset might receive. The number of blank messages are meant to handle worst-case situations where more than one message of a given type are awaiting processing. The sender will look for blank messages in the recipient's mailbox, fill out one of the messages, and set a flag. Once the message has been read, the recipient will erase the message by turning the flag off. Although it has not been needed, SWEG can add additional blank messages to someone's mailbox when the scenario dynamics demand it.

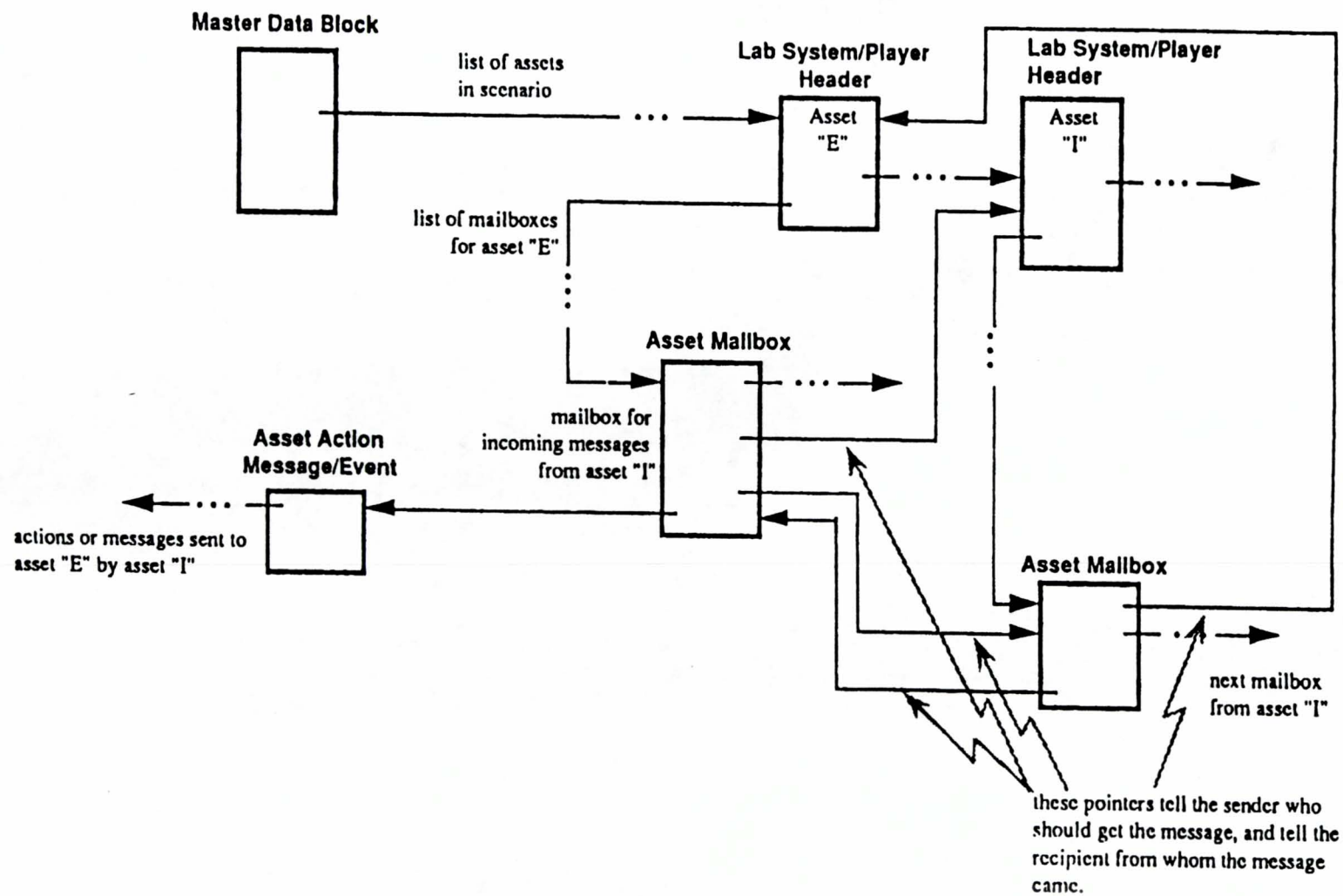


Figure 3-8. SWEG Mailboxes and Messages.

Mailboxes are useful for sending stimuli, responses, and captured data. They are not useful for sending high volume periodic updates, like position changes. They are often times not useful for status changes, which can be made to shared memory data structures directly.

3.5 DATA BASE CHARACTERISTICS

TESTS utilizes both internal and external data bases. The internal data bases are temporary data bases created by the TESTS software to pass data between processing tasks. The preliminary requirements for the internal data bases are outlined in Section 4.4. The primary data bases associated with TESTS are those developed by SWEG. SWEG provides detailed scenario information which is utilized by TESTS. The following subsections provide brief descriptions of the data bases provided by SWEG.

3.5.1 SWEG Data Bases

SWEG uses seven different internal data bases to structure its data. The use of smaller data bases is used to enhance data updates generated by SWEG.

3.5.1.1 Type Data Base

Type Data Base (TDB) Instructions contains data associated with kinds or classes of players. Any data that might have to be repeated for every player or for all players of a given type are candidates for this data base. Following the TDB instructions is an annex which provides a detailed explanation of selected TDB data items that share common formats. Besides reducing the work of the user, it also increases the reliability of the total input data base, and makes it easier to modify the data.

3.5.1.2 Terrain Data Base

Terrain-Related Instructions defines the processed terrain area to be used with a scenario. Within this instruction group are actually two sets of instructions: DMA Instructions (to process digitized Defense Mapping Agency (DMA) terrain files into binary files) and EDB Instructions (to decompose the binary terrain data into triangles).

3.5.1.3 Scenario Data Base

Scenario Data Base (SDB) Instructions contains information specific to each player, such as its location, movement path, mode of control, engagement zones, communication nets, etc. It can be considered as limiting the order of battle for each side involved in the conflict, along with some administrative information. Repetitive data, as much as possible, are contained in the Type Data Base. The output file data from this data base forms part of the input for the Runtime Data Base processor.

3.5.1.4 Environment Data Base

The Environment Data Base conceptually governs all input data that are not strictly associated with any of the modeled forces. This includes weather, rivers, roads, buildings, terrain, etc. Presently, only terrain data are entered, and then only the altitude data. Further, these altitude data points are employed only for line of sight checks between sensors, disruptors, communication receivers and transmitters, and targets.

3.5.1.5 Runtime Data Base

The purpose of the Runtime Data Base processor is to reorganize the input files that have been checked for spelling and grammatical errors into data structures that will maximize the execution efficiency and minimize the memory requirements of the Model Execution. It serves to decouple the requirements for the user interface from the software requirements of the model properly.

3.5.1.6 Analysis Data Base

Analysis Data Base (ADB) Instructions defines the data to be summarized from the scenario run, how the data should be filtered, and what output statistics are desired.

3.5.1.7 Model Kickoff Data Base

Model Kickoff Instructions define the instructions for executing the scenario and the data to be saved for analysis.

3.6 SECURITY

TESTS will operationally be used within shielded facilities so the use of TEMPEST equipment is not required. However, software models, data bases and/or scenarios may contain classified information or parameters. Hence, TESTS will be design to meet classified requirements for secure data. This will be accomplished through use of removable mass storage media and volatile RAM. TESTS software will also incorporate techniques to prevent unauthorized access to data and modifications of the software.

SECTION 4. DESIGN DETAILS

This section describes how TESTS software will meet the functional requirements specified in Sections 2 and 3. Further, it discusses critical development issues. The system described will be developed through a number of incremental builds which provide increasing capability and diversity in the number of platforms and signals to be generated. This evolutionary approach will allow early closed loop testing and validation of the TESTS system with existing IFF systems such as the MK XII, and provide a low risk transition to more advanced IFF systems utilizing spread spectrum signals.

4.1 SYSTEM DESCRIPTION

TESTS consists of both hardware and software. Figure 4-1 shows the top level diagrams of the system hardware and software along with the connections to SWEG and the SUT. The hardware portion receives a message from the SUT which it demodulates and decrypts if necessary. It passes this information to the software which determines the necessary response. Finally the hardware generates, encrypts, and modulates the appropriate message.

The software portion is a multitasking environment consisting of eight prioritized tasks. Task 1, having the highest priority tells the TESTS hardware what signal to generate. Task 2 responds to the SUT. It places the information regarding the incoming signal into shared memory and sets a timer for Task 1. As the time between the arrival of a signal from the SUT and the departure of the reply to the SUT is so small, Tasks 1 and 2 must be able to retrieve the necessary information from shared memory without doing the calculations or waiting for them to be done. These calculations are geometry dependent and can be completed by other tasks prior to the arrival of signal from the SUT.

Task 3 determines the signals to be sent as Friendly Responses Unsynchronized In Time (FRUIT). It also sets timers for Task 1 for these signals. Task 4 handles the majority of the calculations. It first determines the emitters in the beam of the SUT, then calculates the travel times, attenuations, and phase shifts of the propagating signals. These emitters could be ground-based or airborne. Task 5 provides for interaction with the operator during initialization and execution of the simulation. Tasks 6 and 7 monitor and record data for real-time and later analysis respectively. Task 8, a background task, provides analysis of system timing and any real-time periodic BIT functions.

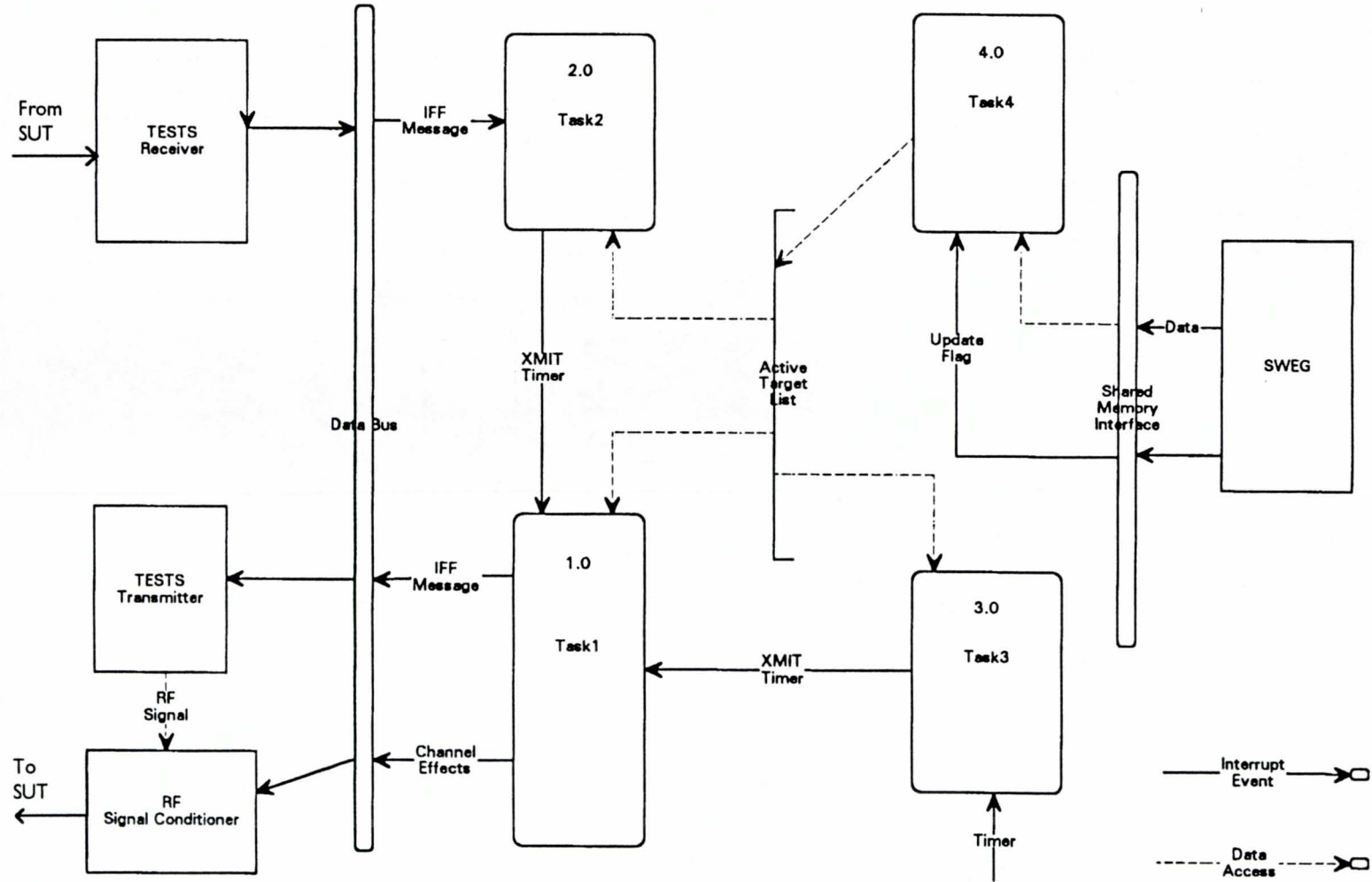
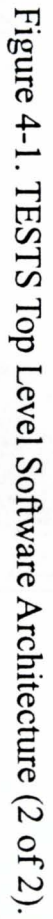


Figure 4-1. TESTS Top Level Software Architecture (1 of 2).



Task 2 differs slightly depending on whether the SUT is an interrogator or transponder. The description above is for a SUT as an interrogator. For a transponder, the SUT only sends a signal as a response to interrogation and does not expect a return signal. Thus, Task 2 only stores the signal information that is sent by the SUT. It does not set any timers for Task 1.

4.2 SYSTEM FUNCTIONS

This section discusses each software task individually with greater detail. It addresses questions of accuracy, validity, and timing.

Task 1 - Figure 4-2 shows the top level diagram for Task 1. This task is triggered by a timer set in Task 2 or Task 3. It goes to an internal data base and gets the signal information needed to generate the signal. This information is sent to the transmitter. It also adjusts the RF signal conditioners to produce the correct channel effects.

Task 2 - Figure 4-3 shows the top level diagram for Task 2. This task is triggered to start by an interrupt from the TESTS receiver upon the arrival of an RF signal from the SUT. The task first stores the signal information along with the time at which the signal is received. For an interrogator, it then determines the internal clock time at which Task 1 must generate the direct and multipath signals from each emitter to the SUT. (Task 4 calculates this time before hand as it is a lengthy calculation--Task 2 only uses it.) This calculation requires knowledge of the timing requirements of the hardware in signal generation. Task 2 sets a timer for Task 1 at the appropriate time to generate the signal.

Task 3 - Figure 4-4 shows the top level diagram of Task 3. This task is triggered by a timer from the operating system (OS). The frequency of the timers is dependent on the FRUIT rate which is set during initialization of the program. It first determines an appropriate random message to be sent to the SUT by each of the emitters in the main and side lobes of the SUT. It then sets the corresponding timers for Task 1.

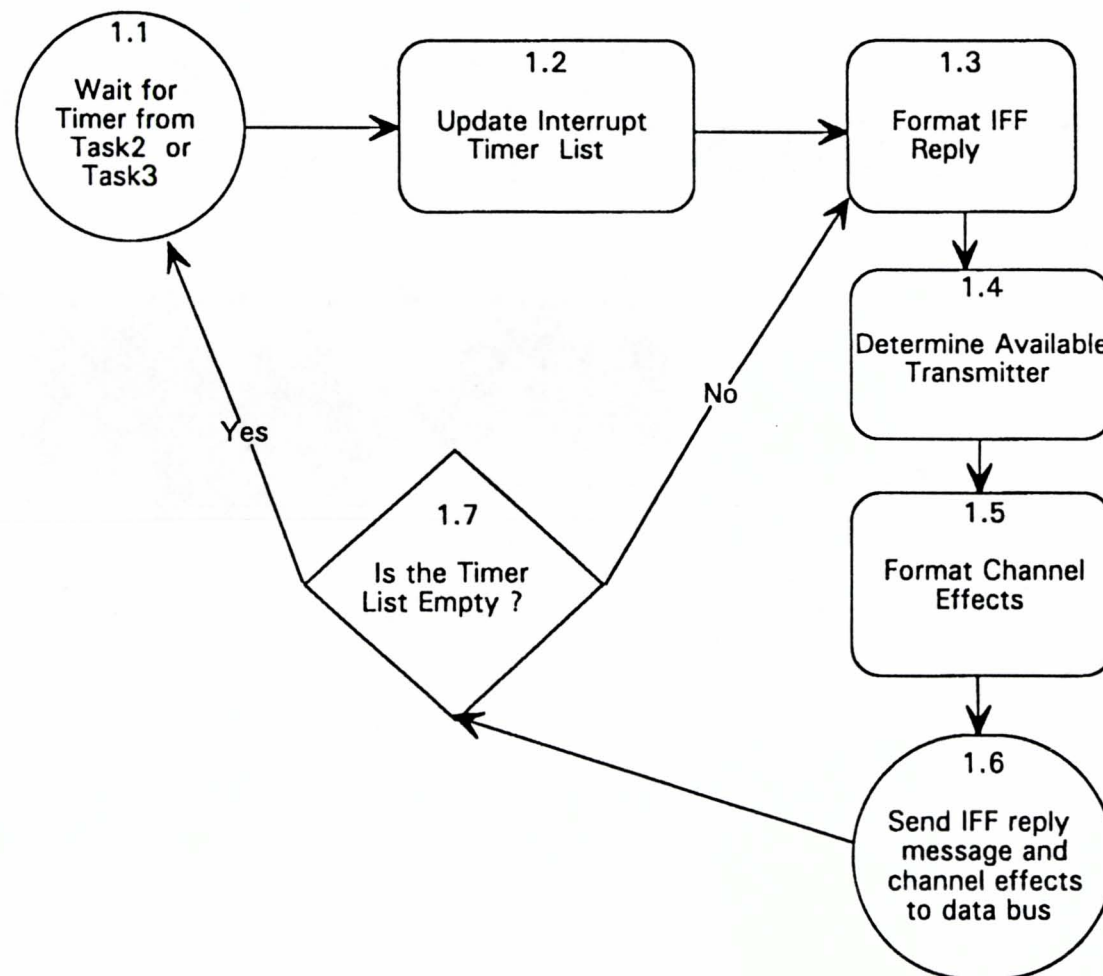
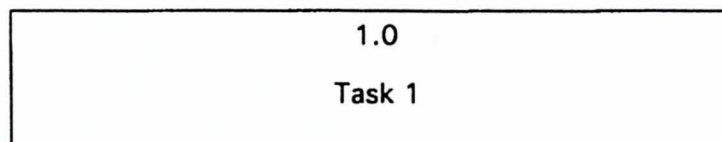


Figure 4-2. Task 1 Flow Diagram.

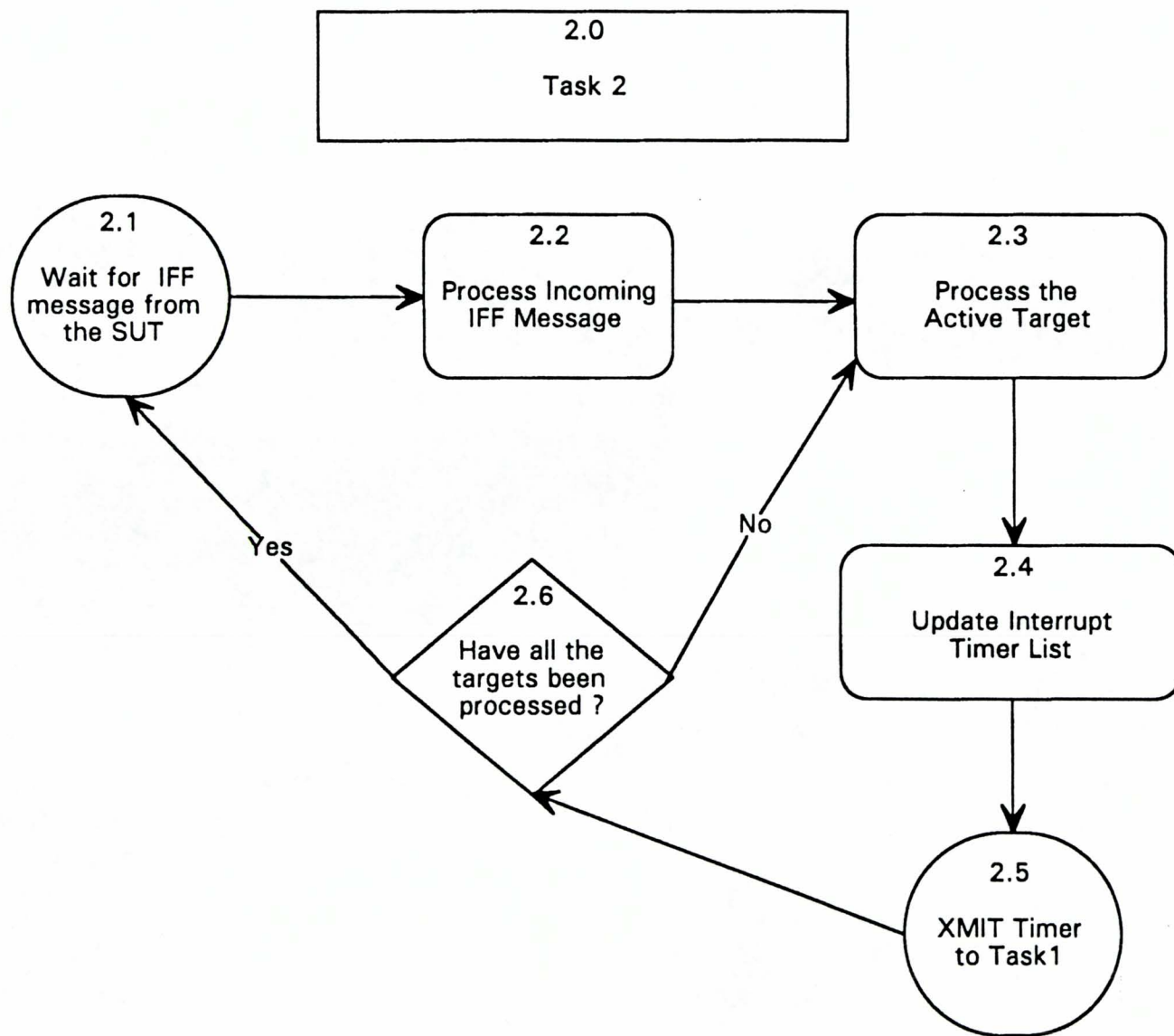


Figure 4-3. Task 2 Flow Diagram.

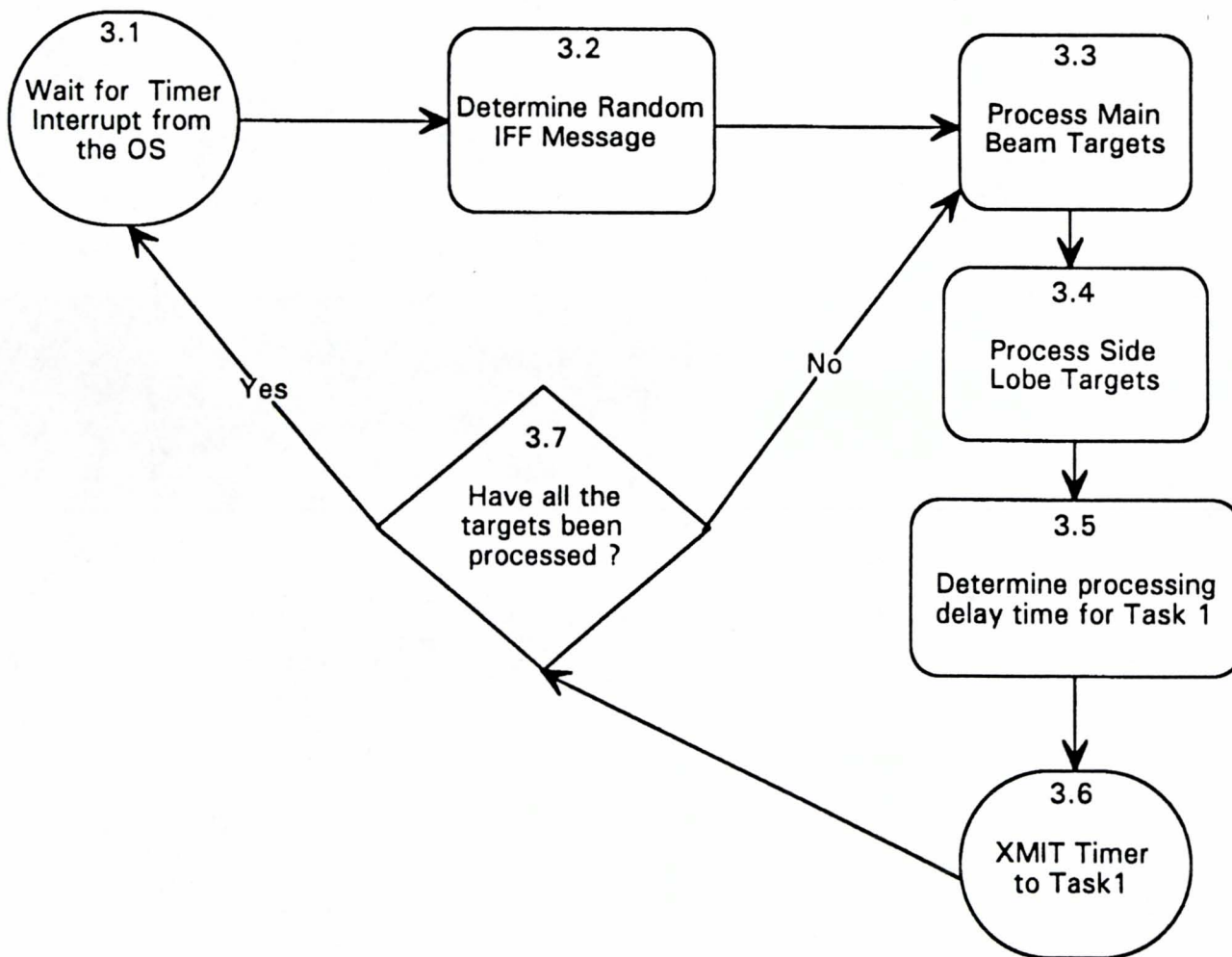
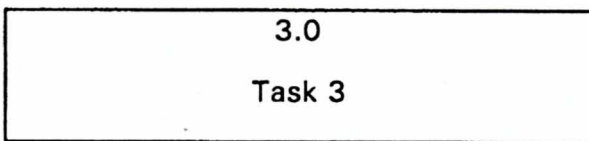


Figure 4-4. Task 3 Flow Diagram.

Task 4 - Figure 4-5 shows the first level diagram of Task 4. The task first updates platform and terrain data. It then determines those emitters in the main beam of the SUT and adds them to the active target list, as shown in Figures 4-6 and 4-7. For each of these emitters, it determines the uplink and downlink channel effects - the round-trip traveltimes for the direct signals, the multipath reflection points, the round-trip times for the multipath signal (direct signal out and reflected signal back) and corresponding attenuations, doppler shifts, and relative phase shifts. Finally, Task 4 determines those emitters in the side lobes of the SUT, Figure 4-8, and performs similar channel calculations.

Task 5 - Figure 4-9 shows the top level diagram for Task 5. This task controls interaction with the operator console during the initialization and execution of the program. It first displays the main menu consisting of three options; initialization of parameters, analysis of system status, and real time data monitoring. During initialization parameters such as FRUIT rate are set. The analysis includes amounts of time the processor spends on each task. The monitoring option will include graphical displays of the scenario for both the interrogator and transponder modes of operation.

Task 6 - This task converts the emitter's coordinates as given by the output of the SUT to a form suitable for real-time display when requested by Task 5. It also prepares for display any "Friend labels" attached to emitters. **Task 7** - This task records relevant data into a database to be used for off-line analysis.

Task 8 - This is a "background" or "slack" task that is always runnable and provides for analysis of system timings, and resource utilization.

4.0
Task 4

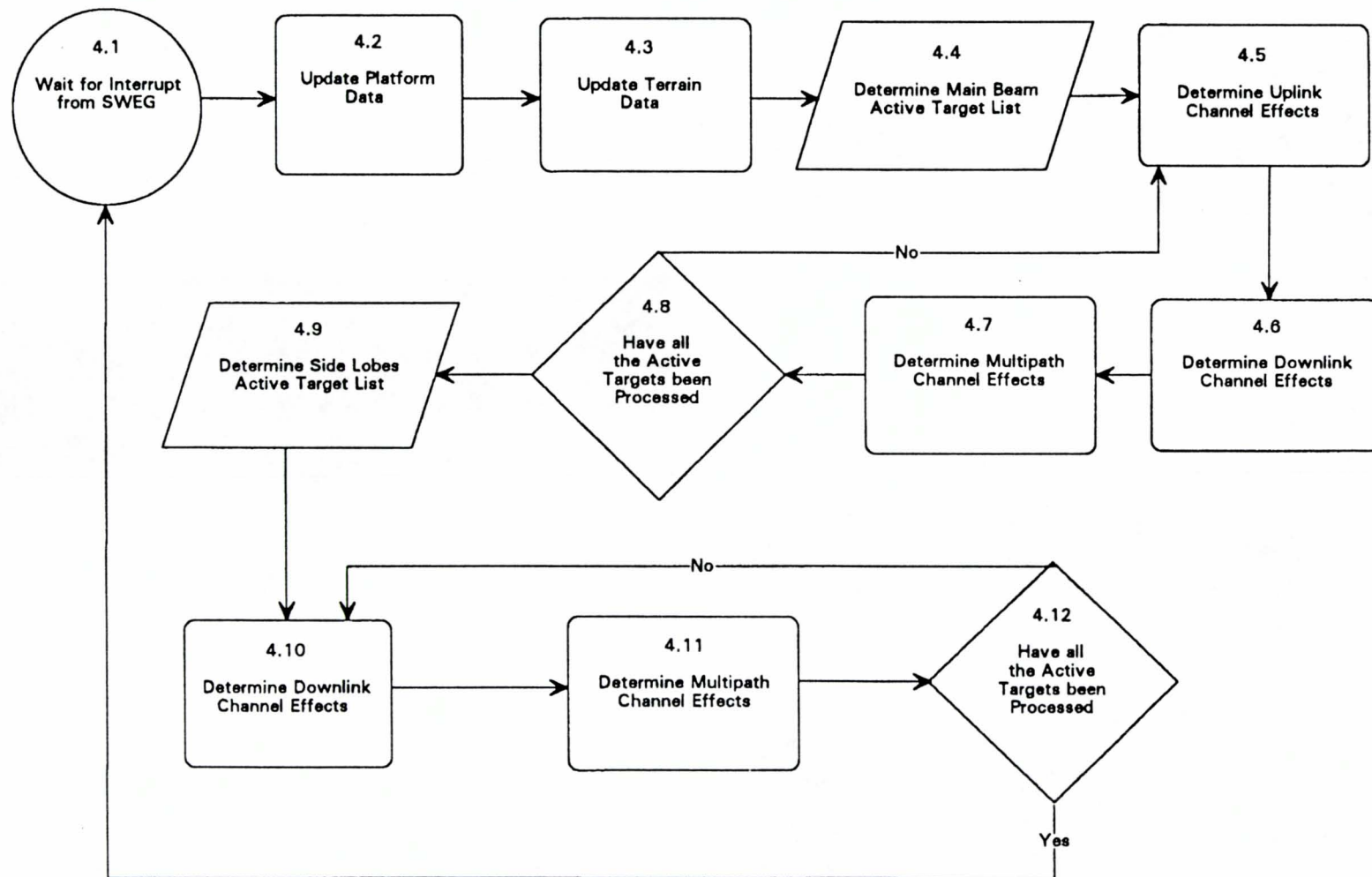


Figure 4-5. Task 4 Flow Diagram.

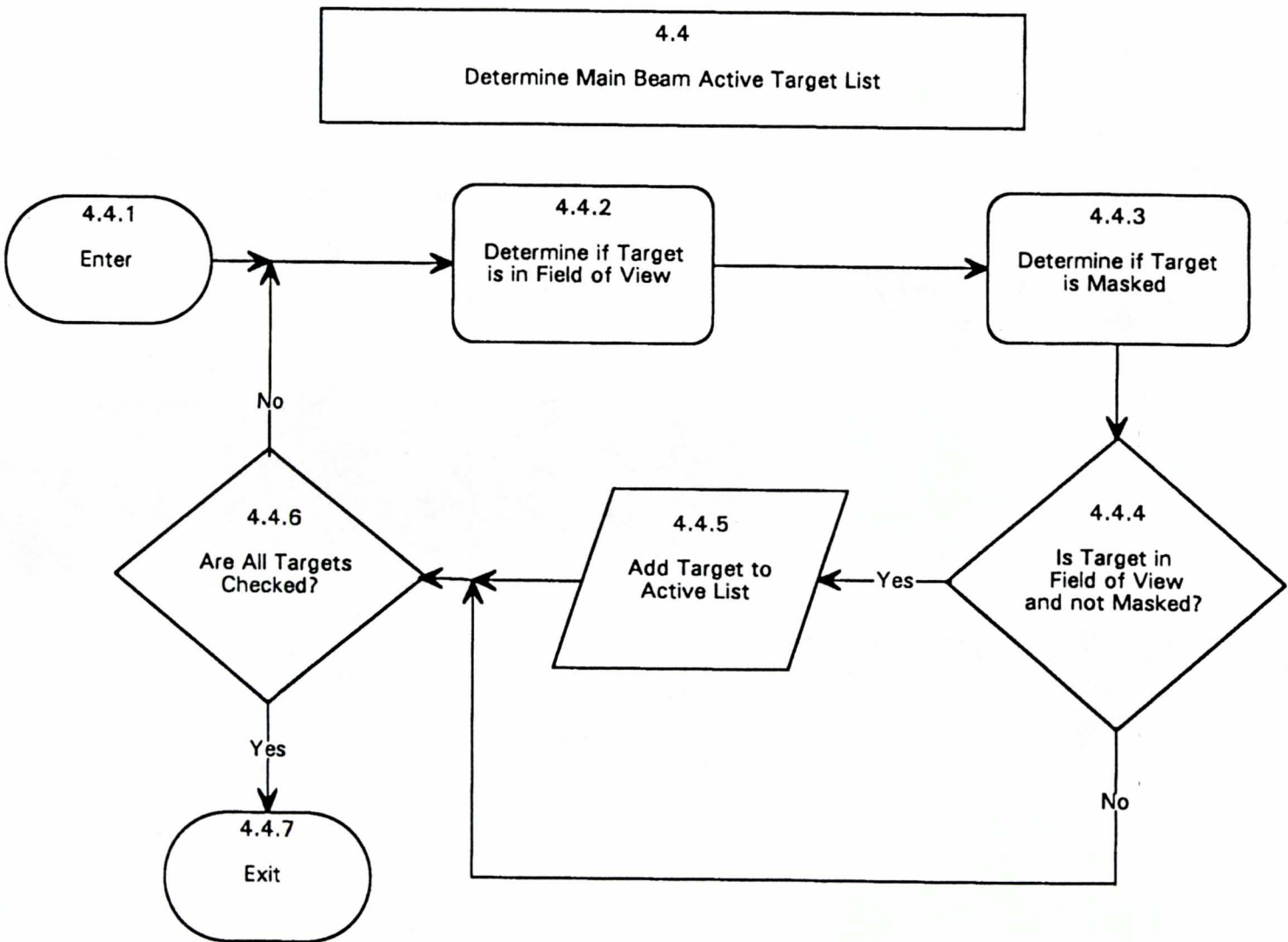


Figure 4-6. Flow Diagram for Determination of Main Beam Active Target List.

4.4.5
Add Target to Active List

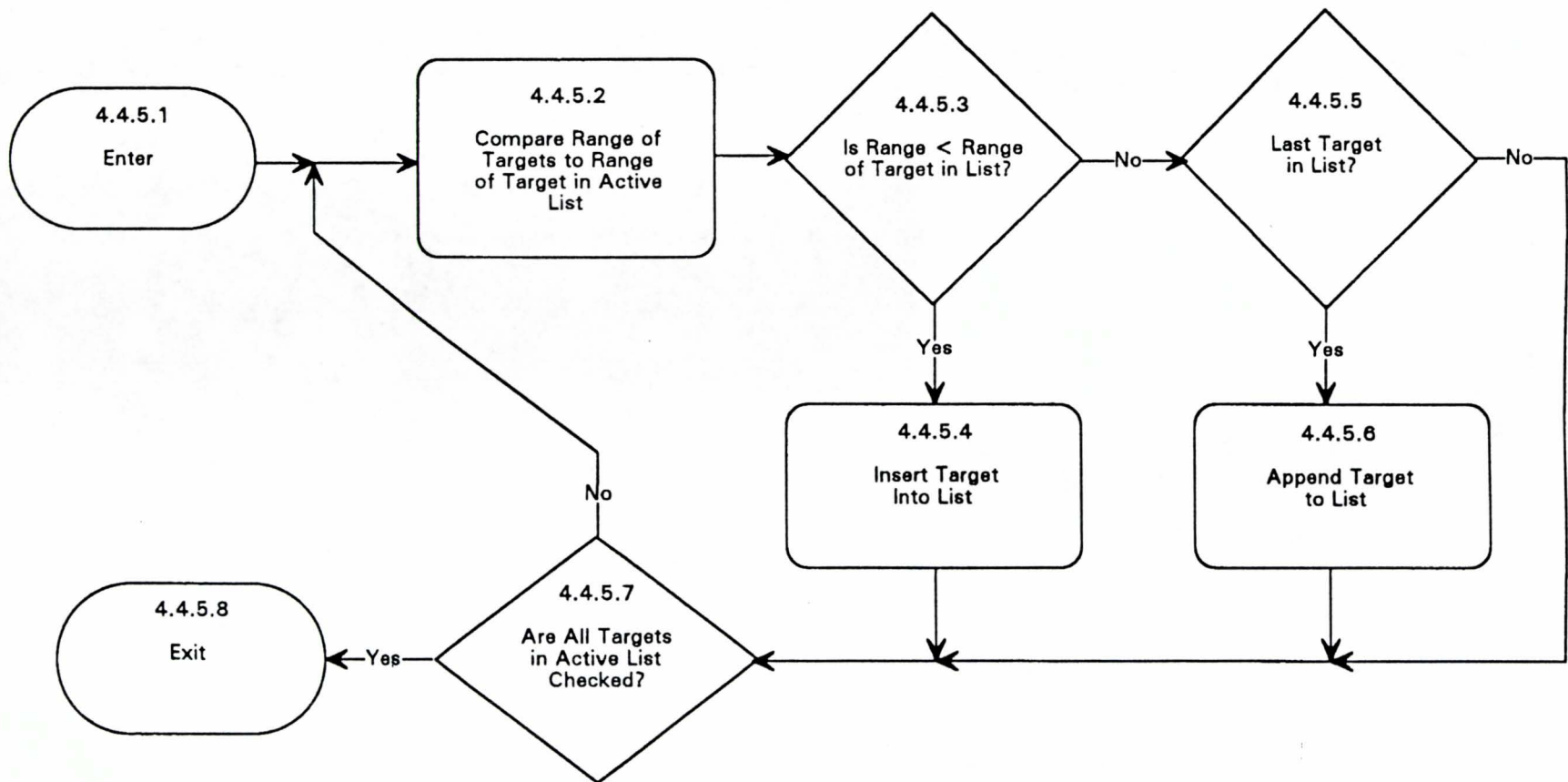


Figure 4-7. Flow Diagram for Addition of Target to Active List.

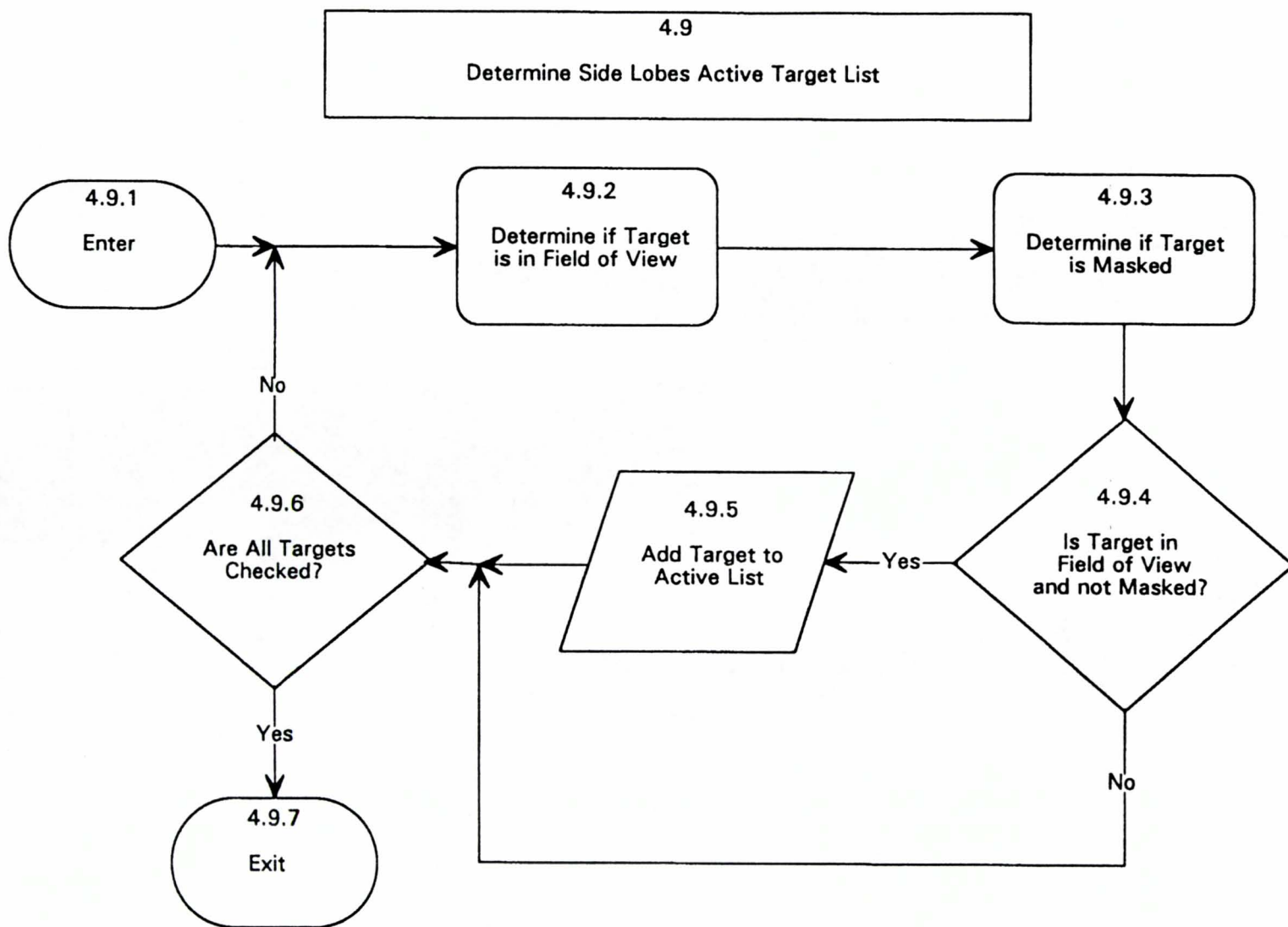


Figure 4-8. Flow diagram for Determination of Side Lobes Active Target List.

5.0
Task 5

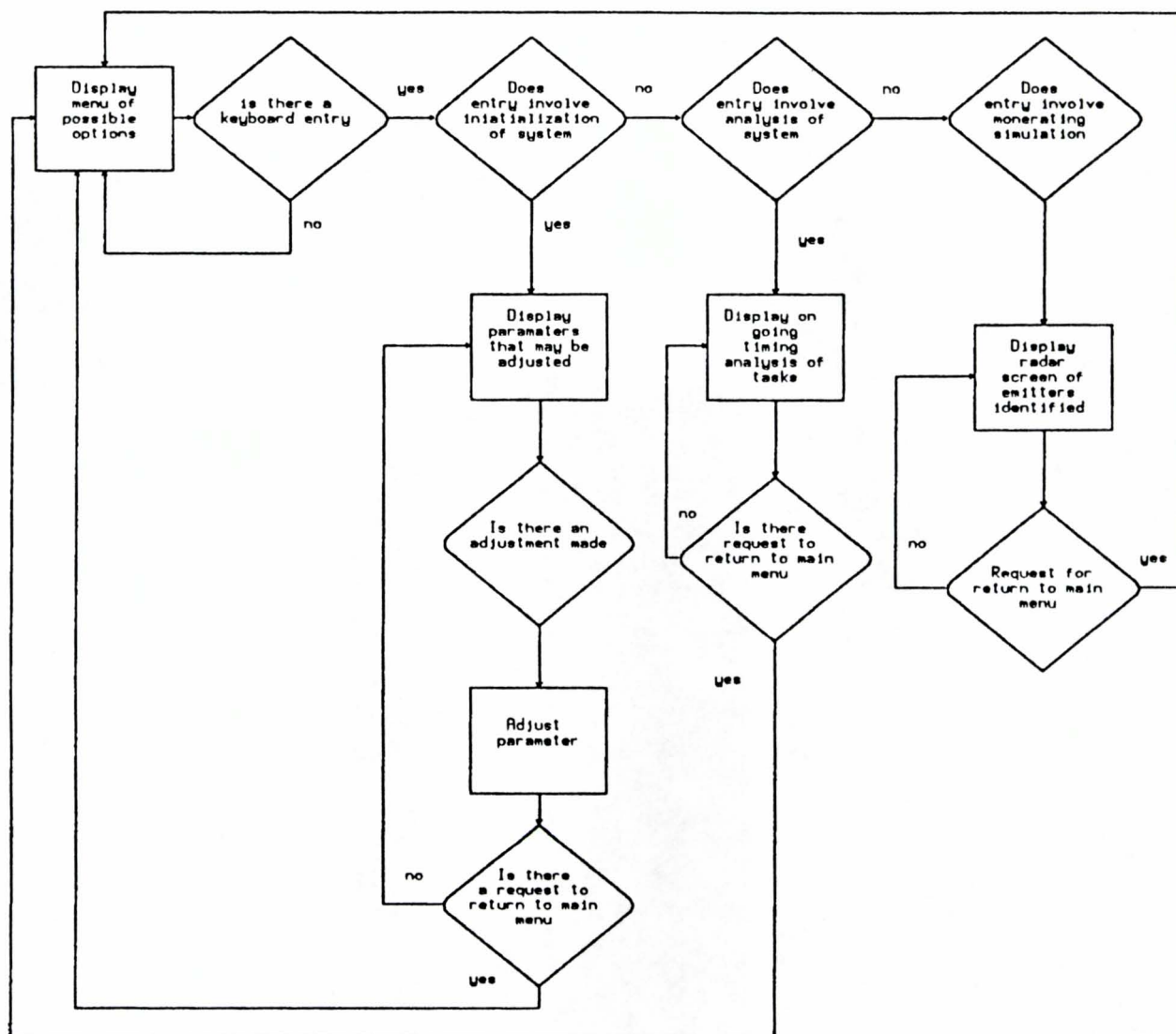


Figure 4-9. Flow Diagram for Task 5.

4.2.1 Accuracy and Validity

The accuracy and validity requirements for TESTS software components are addressed in a general manner in the following paragraphs.

4.2.1.1 IFF Message Data

The content of all IFF messages computed by TESTS must be accurate to the least significant bit required by the applicable IFF message format. For example, MK XII Mode C replies contain encoded altimeter data, which must be computed and converted to a number of bits of accuracy and format specified by the MK XII system specification. Also, IFF message formats must be compatible with the requested modes in order to be valid, and the generated RF waveforms must meet the IFF system specifications for tolerance on rise time, pulse widths, etc.

4.2.1.2 Channel Effects

The computation of signal distortion parameters that will control the RF signal conditioner hardware devices must meet the following general accuracy requirements, in order to be consistent with the output data accuracy shown in Figure 4-10.

- + or - .1563 db for attenuation factors
- + or - .7032 degrees for phase parameters
- + or - .100 micro seconds for time delay parameters

Equations and algorithms that model environmental conditions leading to the computation of these channel effects must be accurate enough to support the above mentioned tolerances. However, the overriding validity of such channel effects computations depends upon the fidelity to which the real-time models and algorithms match the real-world in so far as actual input conditions can be duplicated.

TESTS EXTERNAL BUS MESSAGE FORMAT

Data Item	# Bits	LSB	Units	Description
OUTPUT				
Time to Xmit	32	10^{-6}	sec	Time to transmit IFF message to SUT
Type	8	--	--	IFF message type
Mode	8	--	--	IFF message mode
Message Data	16	*	*	IFF message data (Alt., ID, etc.) (* Mode dependent)
<u>Channel Effects</u>				
Gain	8	.3125	dB	Attenuation factor (0 - 80 db)
Phase	8	1.4063	deg	Phase shift (0 - 360 deg)
Time Delay	8	.0039	msec	Residual time delay (0 - 1 msec)
Gain Dispersion	8	.3125	dB/MHz	Amplitude dispersion (+/- 40 dB/MHz)
Phase Dispersion	8	1.4063	deg/MHz	Phase Dispersion (0 - 360 deg/MHz)
Frequency Offset	8	.3906	MHz	Doppler frequency shift (+/- 50 MHz)
INPUT				
Time Received	32	10^{-6}	sec	Time IFF message received from SUT
Type	8	--	--	IFF message type
Mode	8	--	--	IFF message mode
Message Data	16	--	*	IFF message data (Alt., ID, etc.) (* Mode dependent)

Figure 4-10. TESTS External Bus Message Format.

4.2.2 Timing

A preliminary timing budget has been constructed for the TESTS Software Components that are critical to the real-time IFF communications loop with the System Under Test. This budget, as presented in Table 4-1 is defined in terms of the number of operations assumed for each major function of the software Tasks 1 through 4, plus certain critical functions of the real-time operating system kernel. These operations represent average number of basic machine instructions required to perform each function. Floating point operations, such as multiplies or divides, typically require 5 to 10 of such basic instruction cycles.

Table 4-2 shows the results of a computer simulation that was run using the timing budgets of Table 4-1 to estimate the total number of operations (or processor throughput) that would be required for a stressing scenario. In this scenario it was assumed that the System Under Test was an interrogator operating at a PRF of 500 per second, that there were 20 IFF platforms in the main beam of the SUT, and 10 IFF platforms in the side lobes of the SUT. It was further assumed that all platforms were also interrogated by other friendly systems operating at an combined effective PRF of 1000 interrogations per second, to provide a FRUIT rate of 30,000 per second. It was also assumed that there were 200 total platforms being tracked in the system, and that the SWEG interface data items were updated at a rate of 100 times per second.

Table 4-2 then shows the total number of operations required by each major function of each task (for Tasks 1 through 4) and the total number of entries into each major function. Similar statistics are also shown for major functions of the operating system kernel required to receive and transmit external bus messages, and to set and handle internal software timer interrupts between tasks. Operations required to perform task swapping (context switching) were included in the budget estimates in Table 4-1 for the operating system functions required to Receive External Bus Message, and Wait for Internal Timer Interrupt, and are therefore included in the total operations shown in Table 4-2.

The scenario presented required slightly over 26 million operations to complete one second of actual time, yielding a throughput requirement of about 26 Mega Operations per Second (26 MIPS). The proportion of time used by the operating system required about 20.0 % of the total operational time as shown by the data in Table 4-2.

TABLE 4-1
BUDGET : ASSUMED NUMBER OF OPERATIONS PER PROCESS

<u>Operating System</u>	<u>Operations</u>
Receive External Bus Message	50 (task swapping)
Transmit External Bus Message	30
Set Internal Timer Interrupt	10
Wait for Internal Timer Interrupt	30 (task swapping)
 <u>Task 1 - Reply to SUT</u>	 <u>Operations</u>
Update Interrupt Timer List	20
Format IFF Reply	25
Determine Available Transmitter	25
Format Channel Effects	25
 <u>Task 2 - Receive from SUT</u>	 <u>Operations</u>
Process Incoming IFF Message	20
Process Active Target	20
Update Interrupt Timer List	20
 <u>Task 3 - Simulated Interrogators</u>	 <u>Operations</u>
Determine Random IFF Message	20
Process Main Beam Targets	20
Process Side Lobe Targets	20
Update Interrupt Timer List	20
 <u>Task 4 - Update Scenario</u>	 <u>Operations</u>
Update Platform Data	200 / platform
Update Terrain Data	500 total / update
Determine Main Beam Active Target List	20 / platform
Determine Side Lobes Active Target List	20 / platform
Add Target to Active List	20 / active target
Determine Uplink Channel Effects	200 / active target
Determine Downlink Channel Effects	1000 / active target
Determine Multipath Channel Effects	1000 / active target / path

TABLE 4-2
PRELIMINARY TIMING ESTIMATE -
NUMBER OF MEGA OPS PER SECOND

INPUT PARAMETERS

Start Time = 1.000	Stop Time = 1.000
SUT PRF = 500/sec	Scenario Update = 100/sec
Main Beam: Range (mi.) = 100.00	Number Targets = 20
Side Lobes: Range (mi.) = 30.00	Number Targets = 10
Total Number Platforms = 200	

Time = 1.000

<u>Operating System</u>	<u>Operations</u>	<u>Total Entries</u>
Receive External Bus Message	25000	500
Transmit External Bus Message	3600000	120000
Set Internal Timer Interrupt	410000	41000
Wait for Internal Timer Interrupt	1233000	41100
TASK TOTALS =	5268000	202600

<u>Task 1 - Reply to SUT</u>	<u>Operations</u>	<u>Total Entries</u>
Update Interrupt Timer List	800000	40000
Format IFF Reply	1000000	40000
Determine Available Transmitter	1000000	40000
Format Channel Effects	2000000	80000
TASK TOTALS =	4800000	200000

<u>Task 2 - Receive from SUT</u>	<u>Operations</u>	<u>Total Entries</u>
Process Incoming IFF Message	10000	500
Process Active Target	200000	10000
Update Interrupt Timer List	200000	10000
TASK TOTALS =	410000	20500

<u>Task 3 - Simulated Interrogators</u>	<u>Operations</u>	<u>Total Entries</u>
Determine Random IFF Message	20000	1000
Process Main Beam Targets	400000	20000
Process Side Lobe Targets	200000	10000
Update Interrupt Timer List	600000	30000
TASK TOTALS =	1220000	61000

<u>Task 4 - Update Scenario</u>	<u>Operations</u>	<u>Total Entries</u>
Update Platform Data	4000000	20000
Update Terrain Data	50000	100
Determine MainBeam Active Target List	400000	20000
Determine SideLobes Active Target List	400000	20000
Add Target to Active List	60000	3000
Determine Uplink Channel Effects	400000	2000
Determine Downlink Channel Effects	000000	3000
Determine Multipath Channel Effects	000000	6000
TASK TOTALS =	14310000	74100

Total FRUIT = 30000

FRUIT Rate = 30000

TOTAL OPERATIONS = 26008000

TOTAL MEGA OPS / SEC = 26.008

This data however only addresses the requirements for the tasks critical to the real-time IFF communications loop. In extrapolating this data to determine operational system requirements, one should double the 26 MIPS to allow for processing time for operator console commands, real-time data monitoring, and real-time data collection tasks (Tasks 5, 6, and 7). An additional 50 % pad should also be added to account for spare time (Task 8), potential growth requirements, and uncertainty in the timing budgets at this stage of the process. Therefore, a total processing speed in the neighborhood of 75 to 80 million operations per second will be required for the TESTS host processor.

4.2.3 TESTS Interface Bus Capacity Requirements

Another critical design issue for TESTS is the capacity requirements of the data bus that interfaces the TESTS host computer with the TESTS RF signal receiver, and the IFF signal generation and distortion devices. A high speed data bus, utilizing either VME or new reflective memory configurations, is assumed. Channel capacity for such data busses varies from about 40 to 150 Mega Bits per Second (MBit/sec). However, maximum channel utilization is usually no greater than about 90% of channel capacity. Furthermore, for each packet, or message, or user data transmitted, there is a significant overhead of additional information including address, identification, parity, control, and age.

An example bus message format taken from the SYSTRAN Corporation SCRAMNET 150 MBit/sec shared memory system is shown below.

SCRAMNET Data Bus Message Format

Parity	9 bits
Control	3 bits
Data	32 bits
Address	22 bits
Age	8 bits
ID	8 bits
Total = 82 bits	

Thus for each 32 bits of user data, an additional 50 bits of overhead information must also be transmitted. Spacing requirements between bus messages only allow for about 90% utilization of the 150 MBit/sec capacity (135 MBit/sec), which allows a maximum of 1.64 million messages per second. Thus 150 MBit/sec channel capacity provides a transmission rate of only 49.2 MBit/sec of user data.

Using the TESTS External Bus Message Data requirements shown in Figure 4-10, TESTS will require 2 data bus messages (of 32 usable data bits each) for each input IFF message received from the SUT, and 5 data bus messages for each IFF message (with channel effects for both direct and multipath signals) sent to the SUT. The high reply rate scenario described in the previous section assumes an interrogator as the SUT operating at 500 interrogations per second. Twenty targets in the main beam respond to give 10,000 replies per second, which combined with a reply rate of 30,000 per second, gives a total reply rate of 40,000 replies per second.

For this scenario TESTS would receive 1,000 data bus messages per second (2 messages x 500 interrogations per second), and would transmit 200,000 data bus messages per second (5 messages x 40,000 total replies per second). For the SCRAMNET system described above, this would translate into approximately 16.5 MBits/sec channel utilization, requiring a minimum channel capacity of 18.33 MBits/sec.

However, a conservative design must allow for significant additional capacity to provide for additional output of test and diagnostic data, and to provide for design uncertainty and potential growth. Therefore, it is recommended that a minimum requirements be established at 32 MBit/sec of channel utilization, or equivalently 35 MBit/sec channel capacity for the TESTS interface data bus.

4.3 SYSTEM DATA

This section describes the various inputs and outputs and internal data base requirements of TESTS.

4.3.1 Inputs

TESTS software components receive inputs from three primary sources: SWEG via shared memory interface, the TESTS RF receiver via the external data bus, and the operator console keyboard over direct serial link.

4.3.1.1 SWEG Inputs

Because TESTS is designed to operate in conjunction with SWEG, it is considered as part of TESTS for the purpose of this functional description. The scenario

definition for TESTS is provided via SWEG. The input parameters to SWEG and its operational requirements are fully described in the ACETEF Infterface Document. Since SWEG is being updated, the specification of the inputs to SWEG in this document will only be made by reference to the ACETEF Interface Document. The latest version of this document is included by reference to provide the most accurate definition of the SWEG inputs.

4.3.1.2 Inputs From SWEG

The following section describes data elements that reside in shared memory which can be both read from and written to. These elements are initiated by SWEG and are updated by SWEG. Whereas TESTS will be able to access any data required in shared memory, it is expected that only a small portion of the following data items that are relevant to platform positions, velocities, attitudes, etc., will be used as inputs to TESTS. These data elements are listed in detail because they are not readily identifiable within existing SWEG documentation.

1. Data Element Name: JNR
Definition: Integer array containing data structures, i.e. Linked List, Queue.
2. Data Element Name: GRL
Definition: Real array equivalenced to JNR.
3. Data Element Name: LAAMEF
Definition: Pointer (index) to message in mailbox (MPM 19)
4. Data Element Name: TGAME
Definition: Present Game Time.
5. Data Element Name: LCDIR
Definition: Pointer to central directory (1) of created player.
6. Data Element Name: LABANL
Definition: Pointer to asset birth announcement list (248)
7. Data Element Name: LAAME
Definition: Pointer to message in mailbox (MPM 19)

8. Data Element Name: LPLAT
Definition: Pointer to SWEG platform (MPM 3)
9. Data Element Name: LPFRM
Definition: Pointer to platform (2)
10. Data Element Name: TDELTA
Definition: Elapsed game time until next update.
11. Data Element Name: LSWEG
Definition: Pointer to SWEG header (240).
12. Data Element Name: TCMPAR
Definition: Comparison time for allowable wall clock time to use.
13. Data Element Name: TWALL0
Definition: Reference time for wall clock time at start of game.
14. Data Element Name: TXTRA
Definition: Extra slack time anticipated for next event.
15. Data Element Name: LPLAR
Definition: Pointer to SWEG player (8).
16. Data Element Name: NDXSIT
Definition: Offset to situation output (36).
17. Data Element Name: LMSGH
Definition: Pointer to message header (28).
18. Data Element Name: LCDIRR
Definition: Pointer to central directory of recipient (1).
19. Data Element Name: MPMMSG
Definition: MPM message flag (2=send MPM message, 1=ignored MPM message, 0=SWEG message).
20. Data Element Name: LAILE
Definition: Pointer to event being processed (33).

- 21. Data Element Name: LPIIE
Definition: Pointer to MPM platforms involved in event (MPM 21).
- 22. Data Element Name: ITSBAD
Definition: Bad message flag (0=OK, 1=Bad)
- 23. Data Element Name: LCDIR
Definition: Pointer to player central directory (1).
- 24. Data Element Name: LTRGT
Definition: Pointer to perceived target (17).
- 25. Data Element Name: LSEHE
Definition: Pointer to direct source sensor header (46).
- 26. Data Element Name: IACTN
Definition: Action to be taken (1=start/update, 2=stop/delete)
- 27. Data Element Name: LAILE
Definition: Pointer to event node (33).
- 28. Data Element Name: LPFRMV
Definition: Pointer to victim platform (2).
- 29. Data Element Name: LPFRMT
Definition: Pointer to transmitter platform (2).
- 30. Data Element Name: LSETX
Definition: Pointer to transmitter system data (48).
- 31. Data Element Name: LSEHE
Definition: Pointer to sensor header (46).
- 32. Data Element Name: IACT
Definition: Action code (1=update, 2=delete).
- 33. Data Element Name: LNTERT
Definition: Pointer to interaction key (39) for target.

- 34. Data Element Name: IDTGT
Definition: Target platform global identifying number.
- 35. Data Element Name: LNTERS
Definition: Pointer to interaction key (39) for sensor.
- 36. Data Element Name: IDSNR
Definition: Sensor platform global identifying number.
- 37. Data Element Name: LTOP
Definition: Pointer to top node in tree structure.
- 38. Data Element Name: ICODE
Definition: Type code (of entity described).
- 39. Data Element Name: IPNT
Definition: Offset to parent pointer.
- 40. Data Element Name: IDWN
Definition: Offset to down pointer in tree node.
- 41. Data Element Name: NOFF
Definition: Offset for sibling pointer.
- 42. Data Element Name: NWDS
Definition: Number of words in tree node.
- 43. Data Element Name: LAILE
Definition: Pointer to event being processed (33).
- 44. Data Element Name: KNDACT
Definition: Type of action (1=intercept, 2=abort).
- 45. Data Element Name: LPFRM
Definition: Pointer to target platform (2).
- 46. Data Element Name: TARRIV
Definition: Scheduled intercept time.

- 47. Data Element Name: LPFRM
Definition: Pointer to platform (2) that is to move.
- 48. Data Element Name: LMRIN
Definition: Pointer to remove related information (42) for platform.
- 49. Data Element Name: MOVFLG
Definition: Type of movement flag (1=initiate, 2=update).
- 50. Data Element Name: LSCNDY
Definition: Pointer to secondary target (256).
- 51. Data Element Name: LINST
Definition: Pointer to instructions (154).
- 52. Data Element Name: LLIST
Definition: Pointer to input list (102).
- 53. Data Element Name: LPARH
Definition: Pointer to parser header.
- 54. Data Element Name: LPASI
Definition: Pointer to ADB situation data block (166).
- 55. Data Element Name: NDXSIT
Definition: Index to specific incident.
- 56. Data Element Name: LSUPH
Definition: Pointer to supplemental data header (21 case 14).
- 57. Data Element Name: KODICN
Definition: Incident verb name semantic code.
- 58. Data Element Name: LPARH
Definition: Pointer to parser header.
- 59. Data Element Name: LRSYS
Definition: Pointer to runtime system (4).

- 60. Data Element Name: LSYST
Definition: Pointer to runtime system (4).
- 61. Data Element Name: NOPOFF
Definition: New status (2=off, 4=nonoperational).
- 62. Data Element Name: XPT
Definition: x-coordinate of translated point.
- 63. Data Element Name: YPT
Definition: y-coordinate of translated point.
- 64. Data Element Name: SCALE
Definition: Scaling factor for determining unit of length.
- 65. Data Element Name: NUMDIG
Definition: Number of digits in address tree index.
- 66. Data Element Name: NUMADR
Definition: desired number of tree indices (either 1 or 7).
- 67. Data Element Name: LNODES
Definition: Address tree node index (array of 1 or 7 indices)
- 68. Data Element Name: CTRLON
Definition: Longitude of scenario center in radians.
- 69. Data Element Name: CTRLAT
Definition: Latitude of scenario center in radians.
- 70. Data Element Name: CTRLON
Definition: Longitude of scenario center in radians.
- 71. Data Element Name: CTRLAT
Definition: Latitude of scenario center in radians.
- 72. Data Element Name: PTLON
Definition: Longitude of point to be translated in radians.

- 73. Data Element Name: PTLAT
Definition: Latitude of point to be translated in radians.
- 74. Data Element Name: VALIN
Definition: Value to be converted.
- 75. Data Element Name: MEAS
Definition: Units of measure to be used.
- 76. Data Element Name: KASE
Definition: UOM case (1=internal unit, 2=external unit).
- 77. Data Element Name: IWID
Definition: Width of output file.
- 78. Data Element Name: IOUT
Definition: Logical unit number of output file.
- 79. Data Element Name: NDNT
Definition: Number of spaces to indent.
- 80. Data Element Name: IWR
Definition: Flag indicating whether to write a line (1=yes, 0=no).
- 81. Data Element Name: CXFER
Definition: Character string to be transferred to output.
- 82. Data Element Name: LPTR
Definition: Pointer to character buffer (243).
- 83. Data Element Name: NWRD
Definition: Number of word.
- 84. Data Element Name: LCHRCV
Definition: Pointer to character conversion table (29/2).
- 85. Data Element Name: NUM
Definition: Integer to be converted.

- 86. Data Element Name: ISP
Definition: Number of spaces to be used (when>0).
- 87. Data Element Name: LCHRS
Definition: Pointer to character string (243).
- 88. Data Element Name: LCHRH
Definition: Pointer to integer character header (246).
- 89. Data Element Name: CLINE
Definition: Character string to be transferred.
- 90. Data Element Name: NBEG
Definition: Index into string to start transfer.
- 91. Data Element Name: NEND
Definition: Index into string to stop transfer.
- 92. Data Element Name: LNTRNL
Definition: Pointer to block or subblock containing packed string.
- 93. Data Element Name: LSCHD
Definition: Pointer to central directory (1).
- 94. Data Element Name: LFREN
Definition: Pointer to subordinate (10).
- 95. Data Element Name: LTRGT
Definition: Pointer to perception (17) block for target.
- 96. Data Element Name: LNTERC
Definition: Pointer to interaction key (39) of commander.
- 97. Data Element Name: LTHEL
Definition: Pointer to thinking element (23).
- 98. Data Element Name: LPTRS
Definition: Pointer into code values.

- 99. Data Element Name: LTABL
Definition: Pointer to physical data base table (150).
- 100. Data Element Name: NEXTRA
Definition: Extra words of storage desired at top of runtime blocks.
- 101. Data Element Name: LTMPL
Definition: Pointer to table template.
- 102. Data Element Name: P1
Definition: Initial point of finite line segment.
- 103. Data Element Name: T1
Definition: Time corresponding to P1.
- 104. Data Element Name: P2
Definition: Terminal point of finite line segment.
- 105. Data Element Name: T2
Definition: Time corresponding to P2.
- 106. Data Element Name: PC
Definition: Position of center of circle.
- 107. Data Element Name: RHO
Definition: Radius of circle.
- 108. Data Element Name: AX,Y
Definition: x,y-coordinate of endpoint A on first line segment.
- 109. Data Element Name: BX,Y
Definition: x,y-coordinate of endpoint B on first line segment.
- 110. Data Element Name: CX,Y
Definition: x,y-coordinate of endpoint C on first line segment.
- 111. Data Element Name: DX,Y
Definition: x,y-coordinate of endpoint D on first line segment.

- 112. Data Element Name: PKILL
Definition: Probability of attack success on target group.
- 113. Data Element Name: LGRUP
Definition: Pointer to target group (3).
- 114. Data Element Name: ITSDED
Definition: Flag indicating whether platform was destroyed (1=yes).
- 115. Data Element Name: JNRSIZ
Definition: Number of words in master array.
- 116. Data Element Name: LENTER
Definition: Interaction key pointer (39) for dead friendly unit.
- 117. Data Element Name: KODSIT
Definition: Incident situation code.
- 118. Data Element Name: LPARH
Definition: Pointer to parser header (54).
- 119. Data Element Name: LGLOB
Definition: Pointer to top instruction block (186).
- 120. Data Element Name: LPFRM
Definition: Pointer to platform (2).
- 121. Data Element Name: TIME
Definition: Time at which position is needed.
- 122. Data Element Name: INEED
Definition: Flag set equal to 1 when unit velocity vector is needed.
- 123. Data Element Name: IP1
Definition: Pointer to path entry (119) or (446) before desired time.
- 124. Data Element Name: DELTIM
Definition: Time interval between desired time and FPL entry IP1.

- 125. Data Element Name: DELFPL
Definition: Time interval from FPL entry IP1 to next entry.
- 126. Data Element Name: LUV
Definition: Unit velocity vector (only if INEED=1).
- 127. Data Element Name: LUZ
Definition: Unit up (z) vector (only if INEED=1).
- 128. Data Element Name: X
Definition: x-coordinate of new flight path point.
- 129. Data Element Name: Y
Definition: y-coordinate of new flight path point.
- 130. Data Element Name: Z
Definition: z-coordinate of new flight path point.
- 131. Data Element Name: S
Definition: Speed of mover at the new point.
- 132. Data Element Name: R
Definition: Turn radius up to this point.
- 133. Data Element Name: IUSERS
Definition: Flag showing if this point was user specified (1=yes).
- 134. Data Element Name: ITURN
Definition: Turn direction preference (1=right, 2=left, 3=shorter).
- 135. Data Element Name: LPREV
Definition: Pointer to future entry (119) before this addition.
- 136. Data Element Name: LNEW
Definition: Pointer to future entry (119) after this addition.
- 137. Data Element Name: R
Definition: Radius of circular arc in plane of maneuver(meters).

138. Data Element Name: C(i)
Definition: Location of the center of arc in the plane of maneuver.
139. Data Element Name: LEL
Definition: Unit vector from center of arc to new point.
140. Data Element Name: SIZEL
Definition: Magnitude of vector from center to new point.
141. Data Element Name: LEN
Definition: Unit vector normal to plane of maneuver.
142. Data Element Name: LERHO
Definition: Unit vector from previous point to center of arc.
143. Data Element Name: LMRIN
Definition: Pointer to move-related info (42).
144. Data Element Name: L1
Definition: Pointer to path point (119) or (446).
145. Data Element Name: L2
Definition: Pointer to a second path point (119) or (446).
146. Data Element Name: LCAND
Definition: Pointer to candidate list (24 case 5).
147. Data Element Name: LTRGT
Definition: Pointer to target perceived (17).
148. Data Element Name: LSCNDY
Definition: Pointer to secondary threat (256).
149. Data Element Name: KNDACT
Definition: Type of action (1=add, 2=drop).
150. Data Element Name: LVALUS
Definition: Pointer to add/drop candidate values (153).

- 151. Data Element Name: LTRGT
Definition: Pointer to target perceived (17).
- 152. Data Element Name: LEMIT
Definition: Pointer to secondary threat (256).
- 153. Data Element Name: LCAVA
Definition: Pointer to candidate values (153).
- 154. Data Element Name: LTRGTP
Definition: Pointer to target perceived (17).
- 155. Data Element Name: LSYSTI
Definition: Pointer to system (4) for (47), (60), or (92).
- 156. Data Element Name: ISTAT
Definition: Status change code (0=off, 1=on, 2=non-op).
- 157. Data Element Name: LATN8
Definition: Pointer to attenuation data (150).
- 158. Data Element Name: FREQ
Definition: Energy frequency.
- 159. Data Element Name: ALT1
Definition: Altitude of one object.
- 160. Data Element Name: ALT2
Definition: Altitude of other object.
- 161. Data Element Name: DIST
Definition: Ground distance between objects.
- 162. Data Element Name: LPOSNR
Definition: Pointer to location block (5) for receiver.
- 163. Data Element Name: LANPO
Definition: Pointer to antenna pointing info (201) for receiver.

- 164. Data Element Name: LANTP
Definition: Pointer to antenna pattern table (150 case 2) for receiver.
- 165. Data Element Name: LPOSNT
Definition: Pointer to location block (5) for transmitter.
- 166. Data Element Name: FREQOP
Definition: Operating center of frequency.
- 167. Data Element Name: LADST
Definition: Pointer to add/drop criterion storage (124).
- 168. Data Element Name: LREVA
Definition: Pointer to resource type values (24 case 5).
- 169. Data Element Name: LPLOCM
Definition: Pointer to my perceived location (196).
- 170. Data Element Name: LFREN
Definition: Pointer to perceived resource (10).
- 171. Data Element Name: LEMITS
Definition: Pointer to secondary (emitter) target (256).
- 172. Data Element Name: LREVAL
Definition: Pointer to list of subordinate types and values (24 case 5).
- 173. Data Element Name: LFINS
Definition: Pointer to list of instructions (154).
- 174. Data Element Name: KNDCSN
Definition: Type of decision (3=jam, 7=assign).
- 175. Data Element Name: LPFRMR
Definition: Pointer to resource platform.
- 176. Data Element Name: LREVAE
Definition: Pointer to subordinate types and values entry (24 case 5).

177. Data Element Name: LREVA
Definition: Pointer to resource type values (24 case 5).
178. Data Element Name: LPFRMR
Definition: Pointer to platform (2) belonging to jammer resource.
179. Data Element Name: LMRIN
Definition: Pointer to mover related information (42).
180. Data Element Name: TURN
Definition: Turn radius at point (=0 means no turn).
182. Data Element Name: IOFF
Definition: Offset for storing table pointer.
183. Data Element Name: ITYP
Definition: Table type code.
184. Data Element Name: LPENT
Definition: Pointer to TDB system (143), group (144), Player (145).
185. Data Element Name: LSTOR
Definition: Pointer to data block where table pointers are to be stored.
186. Data Element Name: LPQEN
Definition: Pointer to pending queue entry (27).
187. Data Element Name: LWEPN
Definition: Pointer to weapon status (51).
188. Data Element Name: LXPEN
Definition: Pointer to expendable to use (238).
189. Data Element Name: NROUND
Definition: Number of rounds in salvo to fire.
190. Data Element Name: IDELE
Definition: Target element global ID.

- 191. Data Element Name: KNDPLN
Definition: Plan name for ordnance, when disaggregation.
- 192. Data Element Name: TNEXT
Definition: Time to check for fuel remaining (-1. = use FUELFT).
- 193. Data Element Name: FUELFT
Definition: Fuel remaining threshold (-1. = use TNEXT).
- 194. Data Element Name: LPLEL
Definition: Pointer to future path entry to start FPL update (119).
- 195. Data Element Name: LSYST
Definition: Pointer to mover system (4).
- 196. Data Element Name: LANTN
Definition: Pointer to antenna pointing/facing info. (201).
- 197. Data Element Name: LLOCT
Definition: Pointer to target's location (5).
- 198. Data Element Name: LRNG
Definition: Pointer to 3-D vector from target to antenna (142).
- 199. Data Element Name: LURNG
Definition: Pointer to normalized vector from target to antenna (142).
- 200. Data Element Name: KODE
Definition: Scan plane (1=freq driven, 2=physical scan).
- 201. Data Element Name: LLOCA
Definition: Pointer to antenna's location (5).
- 202. Data Element Name: LLOCT
Definition: Pointer to target's location (5).
- 203. Data Element Name: LTERAN
Definition: Pointer to terrain processing block (323).

- 204. Data Element Name: LPOINT
Definition: Pointer to terrain vertex (325).
- 205. Data Element Name: LPTR
Definition: Pointer to point to be converted.
- 206. Data Element Name: IZ
Definition: Flag indicating whether to store altitude (flag > 0 = yes).
- 207. Data Element Name: LSTOR
Definition: Pointer to storage for x/y/z data.
- 208. Data Element Name: LINES
Definition: Pointer to set of lines (183).
- 209. Data Element Name: XT
Definition: x-coordinate of start of line to be checked.
- 210. Data Element Name: YT
Definition: y-coordinate of start of line to be checked.
- 211. Data Element Name: XG
Definition: x-coordinate of end of line to be checked.
- 212. Data Element Name: YG
Definition: y-coordinate of end of line to be checked.
- 213. Data Element Name: LNEW
Definition: Pointer to node added to or found on tree.
- 214. Data Element Name: LLPAR
Definition: Pointer to listing parameters (15 case 12).
- 215. Data Element Name: MATCH
Definition: Incident matches situation (>0=yes, 0=no).
- 216. Data Element Name: PTLON
Definition: Longitude of point to be translated in radians.

217. Data Element Name: PTLAT
Definition: Latitude of point to be translated in radians.
218. Data Element Name: CHGD2R
Definition: Angle in radians.
219. Data Element Name: VALOUT
Definition: Converted value.
220. Data Element Name: LIRRT
Definition: Pointer to run-time table created by segment.
221. Data Element Name: KODE
Definition: = 0 if no intersection occurs, = 1 if intersection occurs.
222. Data Element Name: PP1
Definition: Earliest segment point within circle.
223. Data Element Name: TT1
Definition: Time corresponding to PP1.
224. Data Element Name: EX,Y
Definition: x,y-coordinate of intersection (only if IFLAG=1).
225. Data Element Name: IFLAG
Definition: Intersection found (0=no intersection, 1=intersection).
226. Data Element Name: ALPH
Definition: Factor used to compute intersection point.
227. Data Element Name: BETA
Definition: Factor used to ensure intersection exists.
228. Data Element Name: KEMIT
Definition: Turn off tracker flag (1=yes, 0=no).
229. Data Element Name: DYNLOC
Definition: Pointer to location (5).

- 230. Data Element Name: XPOS
Definition: x-coordinate of the location.
- 231. Data Element Name: YPOS
Definition: y-coordinate of the location.
- 232. Data Element Name: ZPOS
Definition: z-coordinate of the location.
- 233. Data Element Name: SPEED
Definition: Speed of mover at desired time (only if INEED=1).
- 234. Data Element Name: LEN
Definition: Unit vector normal to plane of maneuver.
- 235. Data Element Name: LERHO
Definition: Unit vector from previous point to center of arc.
- 236. Data Element Name: LBFOR
Definition: Pointer to FPL (119) at time less than or equal to TIME.
- 237. Data Element Name: DELTIM
Definition: Time interval between desired TIME and FPL entry LBFOR.
- 238. Data Element Name: DELFPL
Definition: Time interval from FPL entry IP1 to entry IP2.
- 239. Data Element Name: LBGIN
Definition: Pointer to beginning of orbit (119) if LBFOR on orbit.
- 240. Data Element Name: RHOMAG
Definition: Magnitude of arc radius, (0.0=straight ahead, -1.0=behind).
- 241. Data Element Name: DIST12
Definition: Linear distance between FPL points L1 and L2.
- 242. Data Element Name: ERGATN
Definition: Attenuation factor in decibels.

243. Data Element Name: GAIN
Definition: Gain.
244. Data Element Name: RANGE
Definition: Range from transmitter to receiver.
245. Data Element Name: LBFOR
Definition: Pointer to FPL point at or before TGAME (119).
246. Data Element Name: TORBT
Definition: Time at which orbit began (=0. means not orbiting).
247. Data Element Name: FLTGET
Definition: Pointer to new FPL point (119).
248. Data Element Name: LRADHO
Definition: Pointer to resource allocation header (13).
249. Data Element Name: TOUT
Definition: Game time when fuel = FUELFT (<0 = never gets this low).
250. Data Element Name: XOUT
Definition: x-coordinate when fuel = FUELFT.
251. Data Element Name: YOUT
Definition: y-coordinate when fuel = FUELFT.
252. Data Element Name: ZOUT
Definition: z-coordinate when fuel = FUELFT.
253. Data Element Name: FUELRM
Definition: Fuel remaining at time TNEXT.
254. Data Element Name: KEMIT
Definition: Turn off tracker flag (1=yes, 0=no).
255. Data Element Name: DIST12
Definition: Linear distance between FPL points L1 and L2.

256. Data Element Name: LERHO
Definition: Unit vector from first point (L1) to center of arc.
257. Data Element Name: INSIDE
Definition: Point inside (1) or not (0) flag.
258. Data Element Name: GEOCRS
Definition: Intersection found (0=no intersection, 1=intersection).

4.3.1.3 TESTS External Bus Message Inputs

For each IFF message received from the SUT, the time received, message type, message mode, and message data will be received over the external message data bus from the TESTS RF receiver. The format of this data was shown earlier in the lower portion of Figure 4-10.

4.3.1.4 TESTS Operator Console Inputs

4.3.1.4.1 Data Supplements to SWEG

SWEG does not currently contain all the data parameters required for TESTS. For example, it is currently not possible for the IFF mode to be specified for a platform. Planned updates of SWEG for CNIL are designed to eliminate these deficiencies. However, TESTS will provide input provisions to supplement SWEG data bases with required data parameters which are not provided in the baseline SWEG at the time of TESTS implementation.

4.3.1.4.2 Configuration Data

The operator console will be used to set the mode of TESTS operation and define the configuration for TESTS. These options may affect the data collection routines and parameter sampling routines within TESTS.

1. Data Element: Mode
Options: Operational or BIT
2. Data Element: Operational Configuration
Options: Stand-alone, CNIL or ACETEF

3. Data Element: Threat Signals
Options: Active or not-active
4. Data Element: Noise
Options: Active or not-active
5. Data Element: SUT
Options: Transponder or interrogator
6. Data Element: Data Collection
Options: Selection of data parameters to be collected during the current test

4.3.1.4.3 TESTS BIT

Several input parameters will be entered using the operator console during TESTS BIT and calibration. Other parameters required for BIT, such as antenna pattern, will be entered through SWEG. These parameters will be used to systematically check out the signal generation, RF signal conditioning and multiplexing hardware.

1. Data Element: Calibration Parameters
Parameters: Attenuation
Time Delay
Dispersion
Phase
Doppler Shift
2. Data Element: Test Conditions
Parameters: Number of Platforms
IFF Mode(s)
Signal Generator #
Location of Platforms (X,Y,Z)

4.3.2 Outputs

4.3.2.1 Internal TESTS Outputs to Signal Generation Hardware.

These data items will be output to the TESTS signal generation hardware: Time to transmit, type, mode, message data, for each IFF message to be transmitted to the SUT. A channel effects message for each direct and reflected path will be sent to the signal distortion devices which contain the attenuation, phase, time delay, and dispersion parameters. The format of these data items was shown earlier in the upper portion of Figure 4-10.

4.3.2.2 Data Collection and Analysis

TESTS data collection and analysis functions must be constructed to support integration, calibration and check out of the various TESTS components during hardware and software development phases, as well as support actual testing activities with an IFF System Under Test.

During actual IFF system testing, the primary data recorded should be IFF messages going to and from the SUT extracted directly from the RF waveforms by RF data recording devices. Data will also be collected after the receiver portion of the SUT to determine what the SUT detected in order to isolate performance decrements. Signal demodulation and message analysis will be conducted off-line.

During system development, and as supplementary operational testing data, additional IFF message data at baseband can be obtained by recording the message traffic on the TESTS external data bus. The channel effects (signal distortion) parameters are also available on this bus and may also be recorded. Note however, at this interface, there is no indication of how the RF signals will actually look to the SUT after distortion, encryption, spread spectrum modulation, and signal mixing occurs.

Within the TESTS host computer, a special software component (Task 7) will be devoted to collecting, time tagging, and recording necessary data items on magnetic storage media during program operations. The exact nature and composition of such data items is yet to be determined, and may vary from one test to another. Table 4-3 presents a summary of the data collection parameters identified for TESTS.

Table 4-3: Data Collection Parameters

Categories	Data Parameters	Sources				Uses		
		SUT		SWEG Common DB	TESTS DB	V & V	Calib.	System Eval.
		Input	Output					
TSPI, Target Position (All Platforms)	Latitude			*		*		*
	Longitude			*		*		*
	Altitude			*		*		*
	Velocity/Airspeed			*		*		*
	Pitch			*		*		*
	Roll			*		*		*
	True Heading			*		*		*
Interrogator Setup ¹ - Switch Settings - Antenna Positions	Correct Code Enable	*			*		*	*
	IR Enable	*			*		*	*
	IR Type Select	*			*	*	*	*
	IR Format / Mode Select	*			*	*	*	*
	Azimuth ²		*	*		*	*	*
	Elevation		*	*		*	*	*
Transponder Setup ¹ - Switch Settings	Mode / Format	*			*		*	*
	Enable Status	*			*		*	*
	Diversity Status		*		*	*	*	*
Misc. Setup ¹ - Jamming Platform	Jamming Type/Modulation (CS, FM, etc.)	*				*		*
	Jamming Bandwidth	*				*		*
	Jamming ERP	*				*		*
Miscellaneous	Weather Conditions			*	*	*	*	*
	Sea State			*	*	*	*	*
<p>Note 1 - All setup parameters must be time tagged, resolution should be at least 0.5 sec.</p> <p>Note 2 - Antenna azimuth must be recorded to an accuracy of +/- 0.5 microsec with resolution of 0.5 microsec.</p>								

Table 4-3: Data Collection Parameters (Cont'd)

Categories	Data Parameters	Sources			Uses			
		SUT		SWEG Common DB	TESTS DB	V & V	Calib.	System Eval.
		Input	Output					
Interrogator Performance ¹ - Transmitted	Type (XV, XII, Both)	*	*					*
	Interrogator Format/Mode	*	*					*
	High Power Request	*	*					*
	Enabled (Y/N)	*						*
	Signal Amplitude (dB)	*	*		*	*	*	*
	- Reply Received							
	Type				*	*	*	*
	Range ²				*	*	*	*
	Code				*			*
	Signal Amplitude (dB)				*	*	*	*
	- Reply Evaluator							
	Type				*			*
	Integration Format/Modes				*			*
	Range				*			*
	Azimuth				*			*
	ID Status				*			*
	ID Confidence				*			*
	Hit Count				*			*
	Validity				*			*
	Width / Amplitude				*	*	*	*
Transponder Performance ¹ - Interrogator Rec'd	Decod Status (Y, N) (Disparity, Authen., Fail)	*					*	*
	Decode Type (XV, SIF)	*					*	*
	Decode Format/Mode		*				*	*
	- Reply Transmitted							
	Type (XV, SIF)	*				*		*
	Format Mode		*	*		*		*
	Code		*	*				*
	High Power (Y/N)		*			*		*
	Antenna (Top/Bottom)		*	*		*		*

Note 1 - All setup parameters must be time tagged,
resolution should be at least 0.5 microsec.

Note 2 - Reply range recorded to a 50 ft accuracy

Table 4-3: Data Collection Parameters (Cont'd)

Categories	Data Parameters	Sources				Uses		
		SUT		SWEG Common DB	TESTS DB	V & V	Calib.	System Eval.
		Input	Output					
Simulator (Internal) - H/S Interface (RVC/TESTS Comp.) - Input Xmit ¹ - Input RF Signal Conditioner ²	Type				*		*	
	Format / Mode				*		*	
	Message Data				*		*	
	Type				*		*	
	Message Data				*		*	
	Amplitude Change				*	*	*	
	Dispersion Change				*	*	*	
	Phase Change				*	*	*	
	Time Delay (Trimming)				*	*	*	
	Frequency Change				*	*	*	

Note 1 - Parameters for all messages multiplexed per signal generator.

Note 2 - Parameters for all RF signal conditioners and multipath inputs per RF - SG.

4.3.3 Internal TESTS Software Data Bases

Internal data base items for TESTS are organized into three major groupings: The Main Beam Object, the Side Lobe Object, and the Output Message List. Figure 4-11 shows the interaction between these data structures and the real-time tasks (1-4). The Main Beam and Side Lobe data objects are continually updated by TESTS to contain information about the active transponder platforms within the main beam or side lobe beams of the SUT. The Output Message List is a doubly linked list structure that contains the time ordered commands for Task 1 to transmit IFF messages. Tasks 2 and 3 update this list by adding messages, in order of their time to transmit, and Task 1 removes messages from the head of this list as they are serviced. Following is a description of each of these data structures, for the transponder mode of operation,

1. Title: Main Beam Object
Description of content:
The Main Beam Object consists of many Transponder Objects in the Main Beam of the SUT.
Number of records: 1
Storage media: Random Access Memory
Data retention: Static
2. Title: Side Lobe Object
Description of content:
The Side Lobe Object consists on many Transponder Objects in all the side lobe beams of the SUT.
Number of records: 1
Storage media: Random Access Memory
Data retention: Static

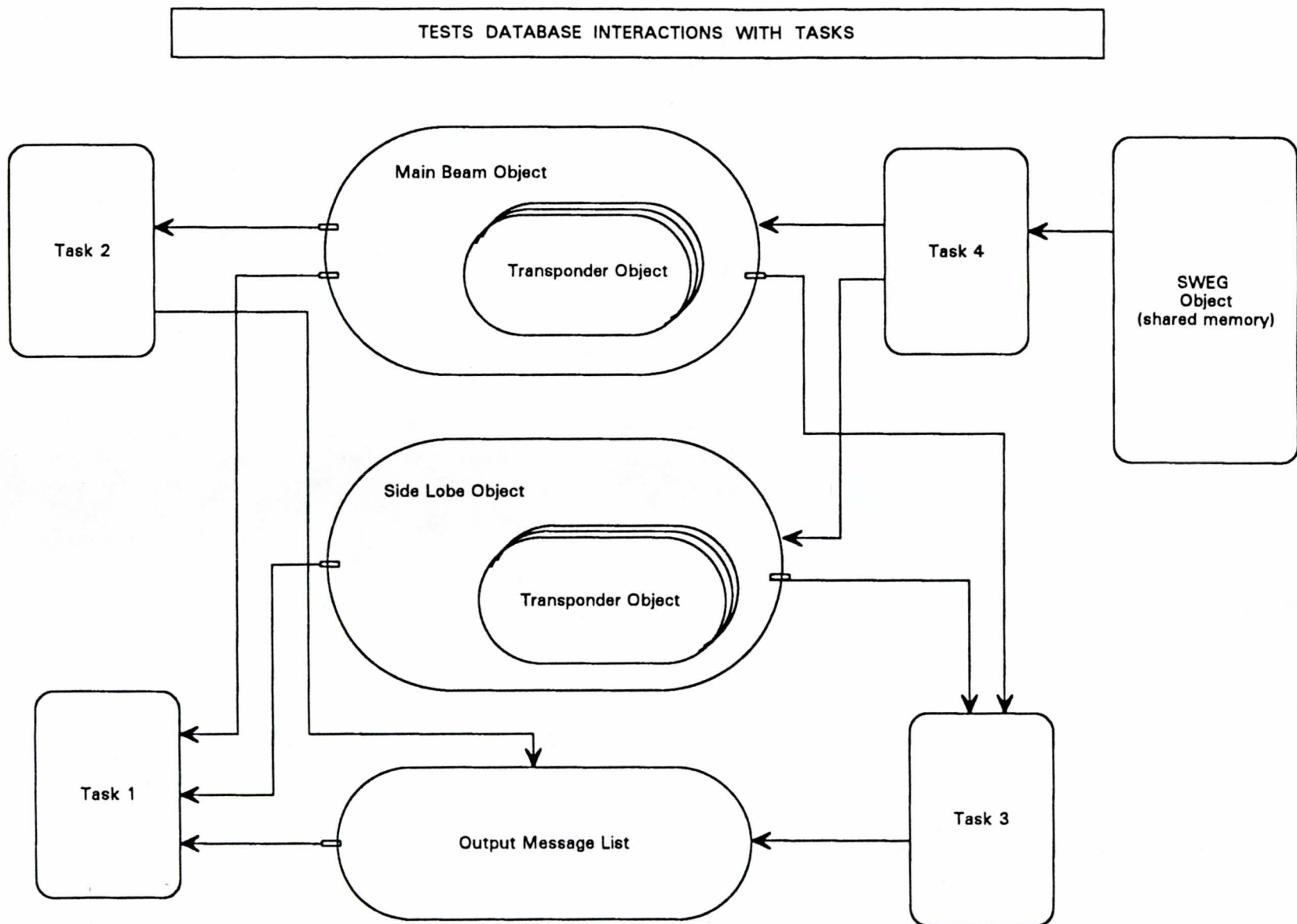


Figure 4-11. TESTS Data Base Interactions with Tasks.

3. Title: Transponder Object

Description of content:

The Transponder Object consists of two instances of the Path Object (i.e., Direct Path and Multipath), and the following data elements. Refer to Figure 4-12.

- a. ID
- b. Azimuth
- c. Slant Range
- d. Elevation Angle
- e. Bounce Range
- f. Closing Velocity
- g. Velocity
- h. Position
- i. Attitude

Number of records: Variable during runtime

Storage media: Random Access Memory

Data retention: Dynamic

4. Title: Path Object

Description of content:

The Path Object consists of the following data elements. Refer to Figure 4-13.

- a. Time Delay
- b. Phase
- c. Gain
- d. Dispersion

Number of records: Twice the number of Transponder Objects.

Storage media: Random Access Memory

Data retention: Dynamic

TransponderObject

Transponder Object

ID

Elevation Angle

Path Object

MultiPath

Direct Path

Azimuth

Bounce Range

Slant Range

Closing Velocity

Position

Velocity

Attitude

Figure 4-12. Transponder Object Data Base.

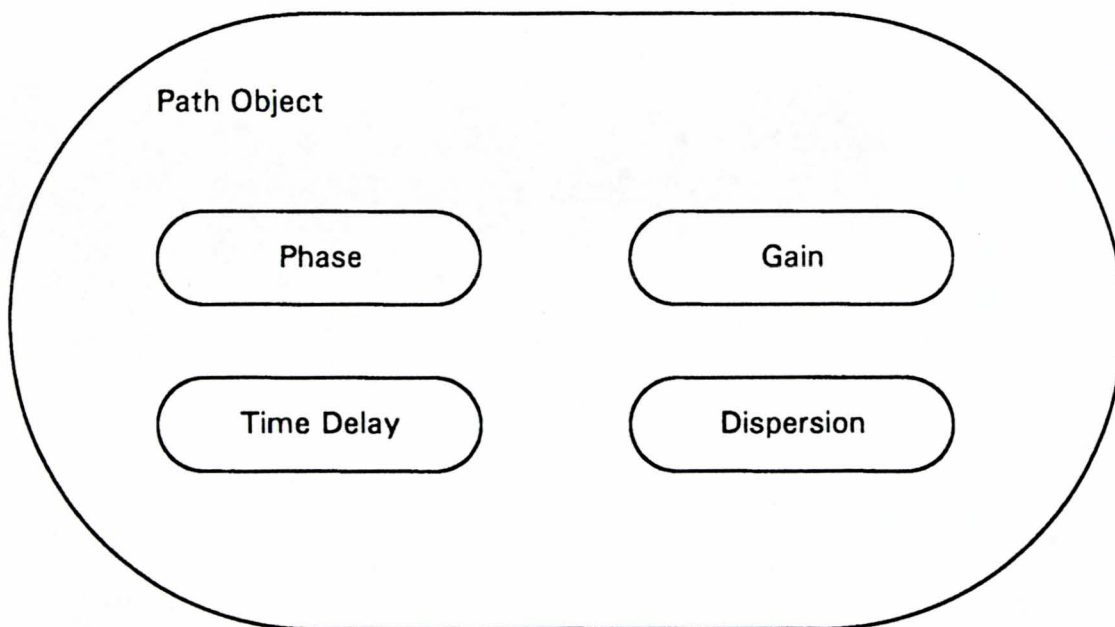
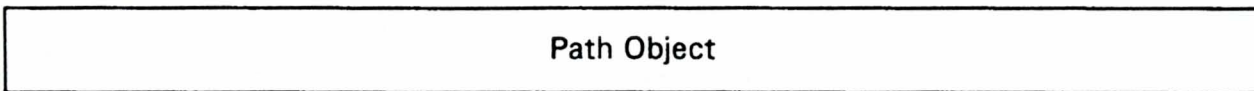


Figure 4-13. Path Object Data Base.

5. Title: Output Message List

Description of content:

The Output Message List is responsible for waking up Task 1. Each element in the list consists of the following data elements. Refer to Figure 4-14.

- a. Time to XMIT
- b. Platform ID
- c. Beam Object Pointer
- d. IFF Message Type/Mode

Number of records: Variable during runtime

Storage media: Random Access Memory

Data retention: Static

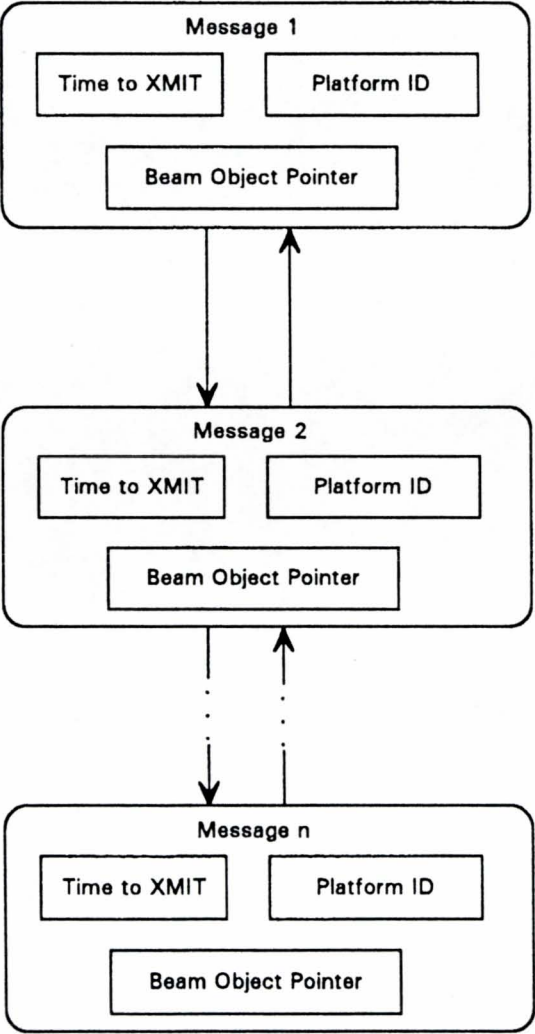
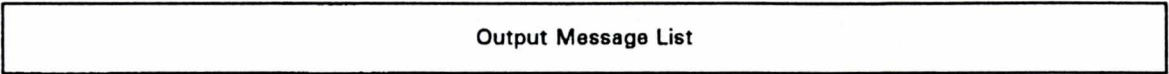


Figure 4-14. Output Message List.

SECTION 5. ENVIRONMENT

The TESTS environment will be a combination of hardware and software linked together to provide a measured stimulation and simulation of the SUT. The proposed approach includes the flow and interfaces as shown in Figure 5-1. The Signal Generator (SG), RF Signal Conditioner (RF-SC), Jammers (J) and the Noise Generators (NG) are envisioned to be hardware; all of these are computer controlled devices with input signals D_1 , D_2 , D_3 , and D_4 for an fully functional TESTS configuration.

The jammer will be a signal generator capable of generating pulsed signals, frequency hopped or direct sequence spread spectrum signals, or continuous wave jamming signals. The computer will drive the jammer.

The noise processor will be capable of generating white noise and possibly other types of signals or systems to be determined in the future by the Navy.

5.1 EQUIPMENT ENVIRONMENT

The operational equipment required for the proposed TESTS system will consist of the SUT, IFF Crypto Unit, TESTS RF Receiver, TESTS Signal Generation Hardware, TESTS Signal Conditioning Devices, TESTS Host Computer and Interface Bus, SWEG Host Computer, and SWEG shared memory interface. The System Under Test and the IFF Crypto Unit are considered GFE or user supplied during actual operation. During TESTS system development, additional equipment for the software development environment as well as special devices for hardware testing and calibration will be required. Anticipated equipment needs are outlined in the following paragraphs.

5.1.1 TESTS RF Receiver

The TESTS simulator will use existing hardware for the RF receiver. In the case of the MK XII prototypes, these subsystems are already available and could be furnished by the government. In the advanced IFF (previously MK XV), the modified, advanced development model (ADM) test equipment incorporating RF receiver subsystems are available at Bendix (at least ten subsystems on hand) and could be furnished by the government. These devices are fast enough and qualify under bench test to perform the RF signal receiver function within the simulator.

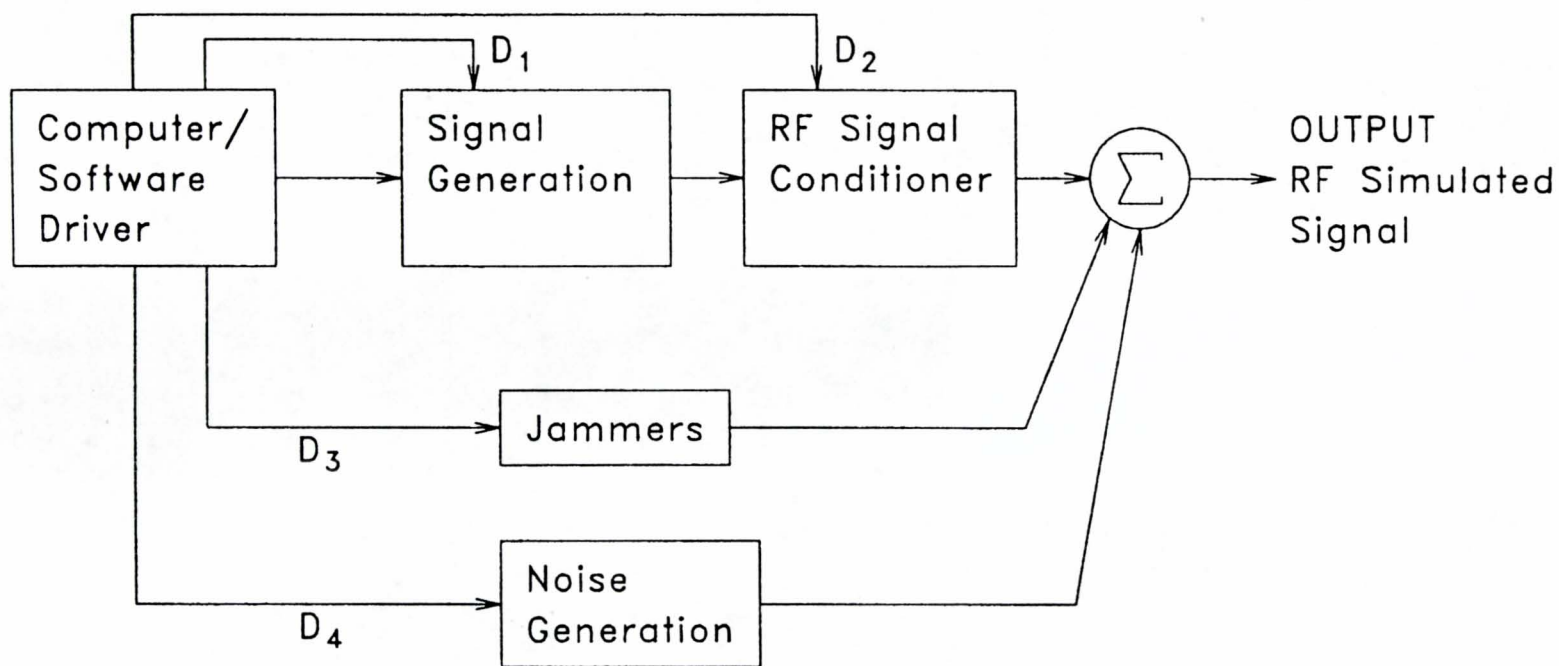


Figure 5-1. Signal Generation Integrated Flow Diagram.

5.1.2 TESTS Signal Generation Hardware

TESTS will require a number of signal generators that operate at 1.03 and 1.09 GHz for carrier frequency stimulation. It is expected that each of these signal generators will be used to simulate multiple emitters and their multipaths (2 - 40, as workload permits) through the use of multiplexing devices. The options to be considered for the selection of a signal generation device for TESTS will first evaluate existing or modified existing equipment before defaulting into a custom option. The candidates already evaluated for signal generation hardware are:

- Modified (ADM) Density Signal Generator (DSG) - Bendix
- SG Subsystem from "Compact Simulator" - ViaSat
- HP 8791 Agile Frequency Generator - Hewlett Packard
- SG Subsystem from Tactical Signal Generator (TASS) - CAL

The order of priority at this juncture is as indicated. A hardware development plan (Section 6.0) will be necessary to finalize the specification and proceed through the selection process. The criteria will focus primarily on the capability requirements to satisfy TESTS objectives, but to also consider schedule need and cost implications.

5.1.3 TESTS Signal Conditioning Devices

The RF signal conditioner will take the ideal signal and condition/modify it via known inputs from the computer (modifications due to channel effects). There are a finite number of signal parameters which will model all first order environmental changes; as well as second order effects, namely (see Figure 5-2): (a) Amplitude (ΔA), (b) Phase (ΔP), (c) Time Delay (ΔT), (d) Frequency Offset (ΔF), and dispersion (second order effect) as (e) Phase Dispersion dP_1/df , and (f) Amplitude Dispersion dA_1/df . Each of these devices will be developed to handle one primary signal and one multipath signal and will work in conjunction with each signal generator.

This RF signal conditioning device is a critical area to be developed for TESTS. The ability to have arbitrary amplitude gain and phase dispersion, as well as time delay mechanization has not yet been demonstrated. Hence, early focus on this element (see Section 6.0 for development plan options) is mandatory for a successful TESTS.

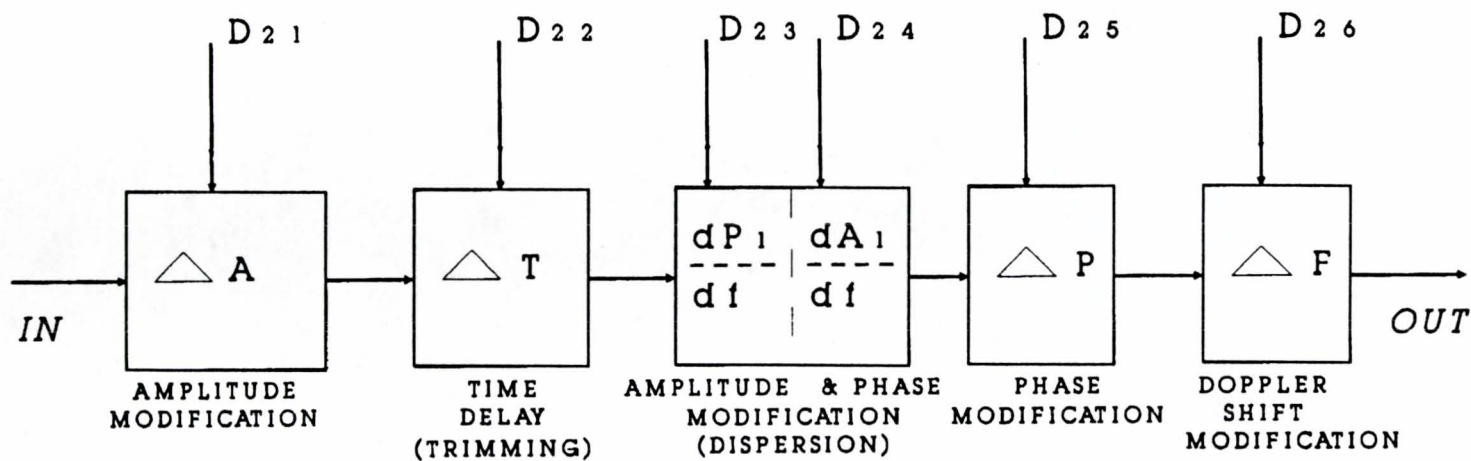


Figure 5-2. RF Signal Conditioner Block Diagram.

It has been confirmed from various manufacturers that this device can be developed inexpensively (less than \$5000 each) and would be possible to use multiple (one for each signal generator) units to simulate multiple transmitters, fading (dispersion), and multipath interference. The technology risk is now moderate (after initial research findings and industrial contacts) for this device.

Since this module is an analog device being driven by digital signals from the TESTS computer, an optimal development mechanization of the RF Signal Conditioner should only require state-of-the-art ranges of time delay and response times for each element identified. As an example, alternative mechanizations for analog time delay reveal that high resolution devices (ACT and/or SAW) are now available, but are limited in the range of delay possible (up to 2 microseconds). Therefore, it is planned that time delay will be split into two parts, with the course/large changes made on the digital side and the finer adjustments made in the RF Signal Conditioner.

The other consideration is the tradeoff between the response time of each element of the RF Signal Conditioner and the number of multiplexed signals that can be processed by each RF-SC. Current research indicates that response times of less than 3 microseconds are reasonable to expect, therefore, the impact on the design may only require an additional signal generator (worst case) to synthesize the spectrum of emitters. Additional research is necessary to calibrate this during the development process.

5.1.4 TESTS Host Computer and Interface Bus

As previously discussed in Section 4.2.2 the operational TESTS Host Computer will require processing speeds (throughput) on the order of 75 to 80 Million Instruction per Second (MIPS). A low cost work station environment that can meet these processing requirements consists of a Sun Sparc Station with Sky Vectorizing Processor Accelerators. This configuration can achieve processing rates of 80 MIPS. Manufacturer product information and product specification bulletins have been obtained for this system.

The Interface Bus linking the TESTS Host Computer, the TESTS RF Receiver, and the TESTS Signal Generation and Signal Distortion equipment will require high data transmission capacity on the order of 35 MBits per second. While standard VME busses yield data rates from 5 to 8 MBytes per second (40 to 64 MBits / sec.), recent developments utilizing a reflective memory configuration with linked fiber optics

channels appear able to meet the requirements. Two product announcement sheets are shown for reflective memory devices which are VME bus compatible, and which support data transmission rates of 120 MBits / sec., by VME Microsystems International Corp. (VMIC), and 150 MBits / sec, by SYSTRAN Corp., in Figures 5-3, and 5-4. The use of a reflective memory interface will also make it easy to link additional workstation processors to the network if it becomes necessary to achieve total throughput requirements through parallel processing.

5.1.5 SWEG Host Computer

In the Integrated ACETEF environment, the SWEG Host Computer will be provided by CNIL or other assets of ACETEF. In the stand-alone configuration or during TESTS system development, SWEG will initially be hosted on a DEC 3100 workstation.

5.1.6 SWEG Shared Memory Interface

The SWEG Shared Memory Interface with the TESTS host computer which has been discussed functionally in previous sections, will be configured to meet the same specifications for the TESTS stand-alone and for the Integrated ACETEF environment. The hardware configuration utilizes a standard VME bus interfacing to the shared memory modules.

5.1.7 TESTS Multiplexing Hardware

The multiplexing hardware will be required to control the message flow from the TESTS computer and direct it to one of the signal generators. A simple control algorithm will be used to distribute the optimal message traffic to the array of signal generators so that a normal distribution can be approximated across the signal generator modules. The capacity for multiplexing is a function of the message length and the hardware response time. The multiplexor will have to operate at baseband or a selected intermediate frequency.

NEW PRODUCT ANNOUNCEMENT

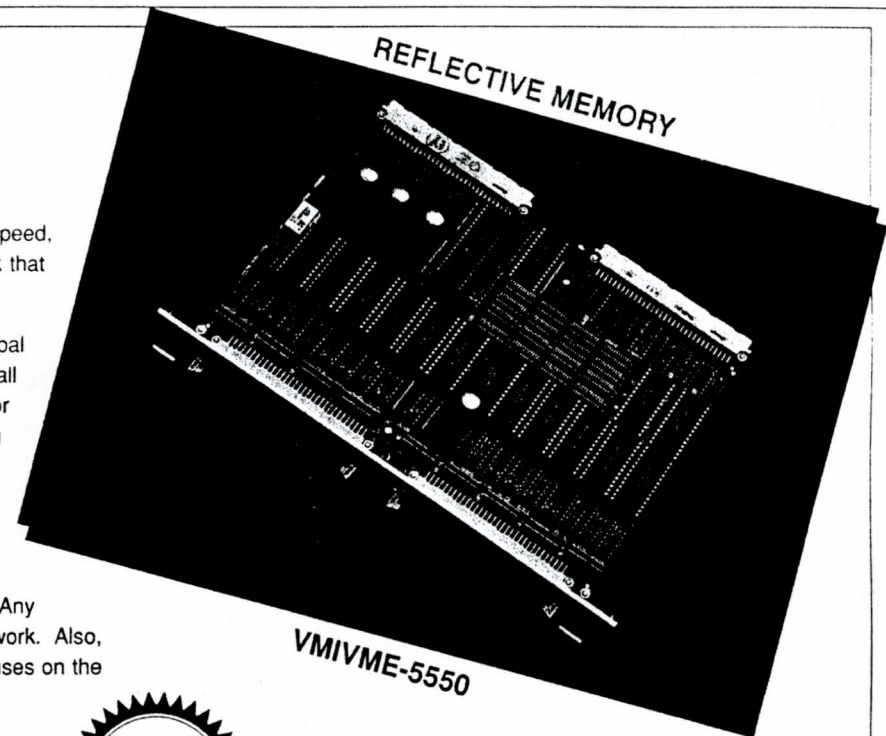
MULTIDROP REFLECTIVE MEMORY WITH INTERRUPTS

VMIC's new Reflective Memory, Model No. VMIVME-5550, is a high-speed, high performance, 16 chassis multidrop VME-to-VME parallel network that features data transfers at 20 Mbytes/s, transfer FIFOs, and interrupts.

The new Reflective Memory transfers data by writing to on-board global RAM. Data written into 1 Mbyte of reflective memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data transfers from memory locations on sending nodes to corresponding memory locations on receiving nodes.

In addition to transferring data between nodes, the Reflective Memory will allow any processor in any chassis to generate a VMEbus interrupt on any other chassis. Three interrupts are available. The user may define function, priority, and vector for each interrupt. Any processor can generate an interrupt on any other VMEbus on the network. Also, any processor on the network can generate an interrupt on all VMEbuses on the network simultaneously.

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Figure 5-3. VMIC Multidrop Reflective Memory (1 of 2).

MULTIDROP REFLECTIVE MEMORY WITH INTERRUPTS FUNCTIONAL BLOCK DIAGRAM

VMIVME-5550 FEATURES

- HIGH-SPEED PARALLEL NETWORK
- DATA WRITTEN TO MEMORY IN ONE CHASSIS IS ALSO WRITTEN TO MEMORY IN ALL CHASSIS ON THE NETWORK
- MULTIDROP CAPABILITY (UP TO 16 CHASSIS)
- DATA TRANSFERRED @ 20 MBYTES/S (5-foot CABLE)
- ANY CHASSIS ON THE NETWORK CAN GENERATE AN INTERRUPT IN ANY OTHER CHASSIS ON THE NETWORK OR IN ALL NETWORK CHASSIS SIMULTANEOUSLY
- NO PROCESSOR OVERHEAD
- NO PROCESSOR INVOLVEMENT IN THE OPERATION OF THE NETWORK
- UP TO 1 MBYTE OF REFLECTIVE MEMORY
- DIFFERENTIAL LINE DRIVERS AND RECEIVERS PROVIDE ± 7 V OF NOISE IMMUNITY
- A24:A32:D32:D16:D8 MEMORY ACCESS
- 16:A24:A32:D8 STATUS AND CONTROL ACCESS
- SINGLE 6U BOARD

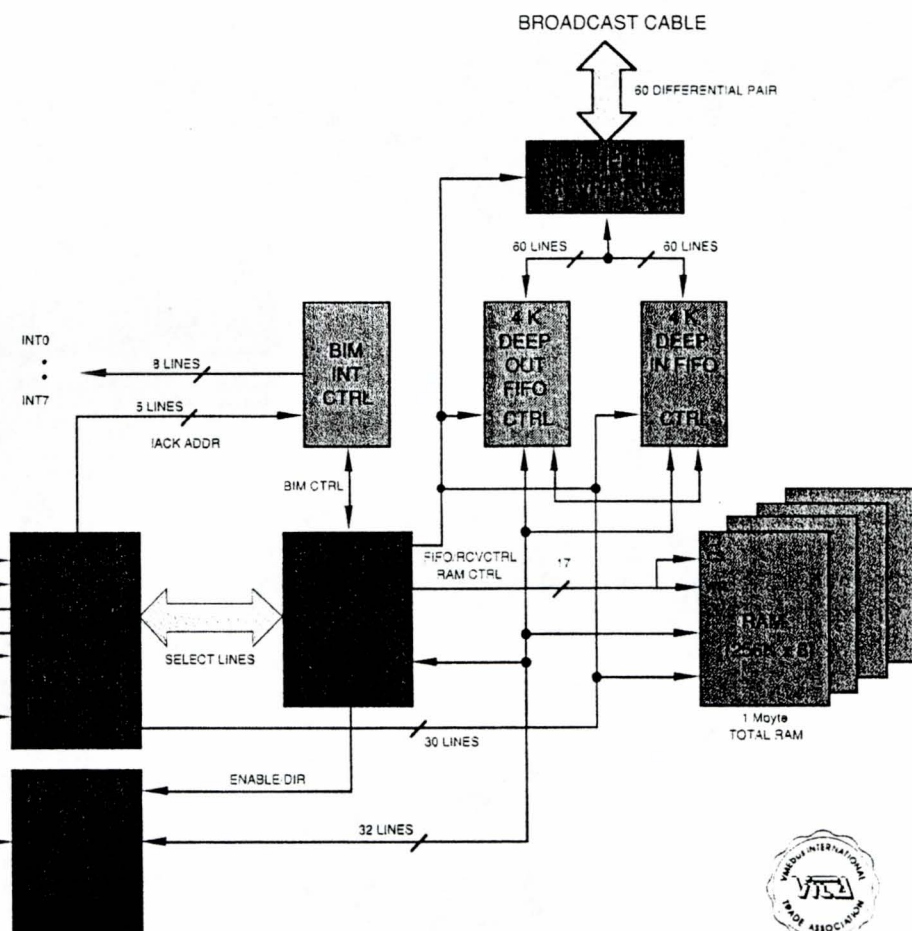
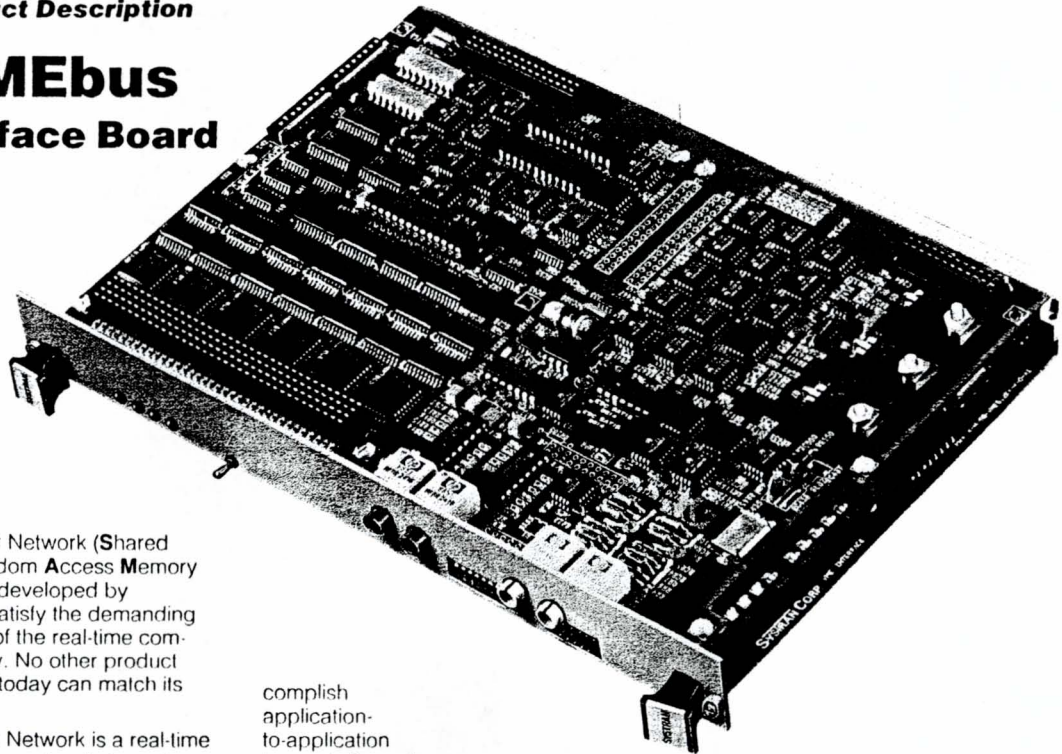


Figure 5-3. VMIC Multidrop Reflective Memory (2 of 2).

SCRAMNet™ Network **Product Description**

VMEbus **Interface Board**



Introduction

- The SCRAMNet Network (Shared Common Random Access Memory Network) was developed by SYSTRAN to satisfy the demanding requirements of the real-time computing industry. No other product on the market today can match its performance.
- The SCRAMNet Network is a real-time communications network, based upon a replicated, shared-memory concept. It is optimized for the high-speed transfer of data between multiple, real-time computers that are all solving portions of the same real-time problem. It was originally developed to solve the ultra-fast, real-time requirements of aircraft simulations, but its capabilities extend equally well to virtually all other real-time applications.
- The SCRAMNet Network is also based upon a "data-filtered" concept, which can significantly reduce network traffic for many applications. The SCRAMNet Network hardware implements this key feature and transmits only data which have changed in value each computing cycle.
- Most other networking systems are designed for file or block transfers between computers and use extremely complex and time consuming software and hardware protocols. These systems can require many milliseconds for application-to-application transmissions. However, the SCRAMNet Network can ac-

complish application-to-application transmissions at memory speeds (microseconds). This revolutionary speed advantage is derived from the state-of-the-art, real-time communications link discipline designated as the GOLD RING™ (Guaranteed Access, Optimized, Low-overhead, Deterministic RING) protocol.

Features/Benefits

- New and revolutionary, memory-speed communication technology
- Low-overhead, deterministic ring network protocol (GOLD RING protocol)
- High-speed, 150 Megabit/second line transmission rate
- No host computer time used for network protocol
- No operating system software needed to support network communications
- No network-dependent application software needed other than for initialization
- Up to 256 nodes per single network ring
- Data-filtering feature eliminates redundant transmissions

- High reliability and EMI/RFI protection with fiber optic transmission lines
- Automatic, built-in hardware error detection and recovery with fast retransmission capability
- Availability of a wide variety of other host interfaces allows integration of multiple vendors' computers on a single network
- Ease of system reconfiguration since all network data are in shared memory area
- Real-time control via Control & Status Registers
- Fully redundant network configuration option

Available From

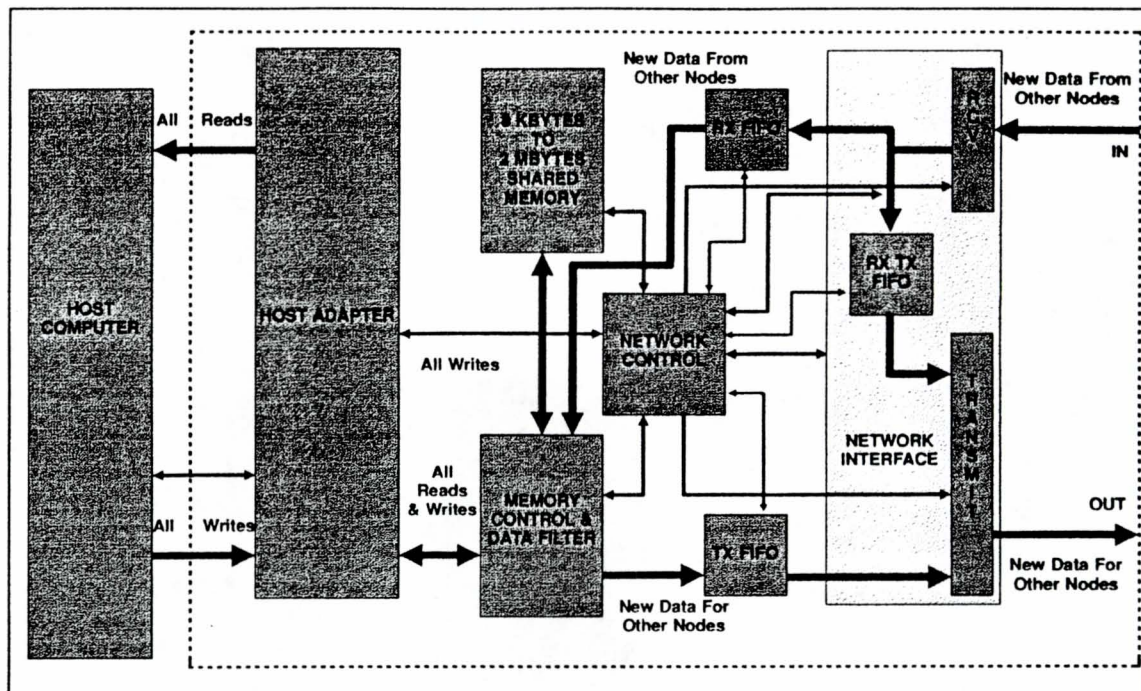
SYSTRAN CORPORATION
The Problem Solving Company

Corporate Headquarters
 4126 Linden Avenue
 Dayton, Ohio 45432-3068
 Phone: 513-252-5601

Network Sales Phone: 800-252-5601
 FAX: 513-258-2729

Figure 5-4. Systran SCRAMNet (1 of 2).

Functional Block Diagram



Specifications

- **Hardware Compatibility:** VMEbus
- **Physical Dimensions:** 6.30" x 9.19" (6U Eurocard, two slots). Optional 9U adaptor available.
- **Electrical Requirements:** +5 VDC/10.5A
- **Operating Temperature:** +15° to +35°C
- **Operating Humidity:** 10% to 90% (noncondensing)
- **Replicated Shared Memory:** Basic System, 128 Kbyte; option to 512 Kbyte, 1 Mbyte and 2 Mbyte. Dip-switch selectable (8 Kbyte minimum).
- **Network Line Transmission Rate:** 150 Mbits/second
- **Transmission Medium:** Dual Fiber Optic Cable
- **Message Length:** 83 Bits
- **Error Correction Time:** Typical for ten node ring; maximum, 10.5 micro-

seconds; minimum, 1.8 microseconds

Maximum Number of Nodes on Ring: 256

Maximum Node Separation: Limited by cable attenuation and bandwidth (700 m typical, greater distances with repeaters)

Node Latency: 220 nanoseconds/node typical

Effective Per-Node Bandwidth: Typical for a ten node ring; maximum, 32 bit word/2.8 microseconds; minimum, 32 bit word/6 microseconds

Cables: Network cables not included

Support Items: Shipped with Installation Manual and Cabinet Kit

Optional Fiber Optic By-Pass Switch

Models Available & Ordering Information

H-AS-VME128K#-6: Two slot board

assembly with 128 Kbyte memory. Specify cabinet used.

H-AS-VME512K#-6: Two slot board assembly with 512 Kbyte memory. Specify cabinet used.

H-AS-VME1M###-6: Two slot board assembly with 1 Mbyte memory. Specify cabinet used.

H-AS-VME2M###-6: Two slot board assembly with 2 Mbyte memory. Specify cabinet used.

H-SB-VME6U9U: 6U-to-9U card adaptor assembly. Specify cabinet used.

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Doc. A-T-SH-VMEIFB01-A-0-A2 (5/15/90)

Figure 5-4. Systran SCRAMNet (2 of 2).

5.1.8 TESTS Data Collection Devices

Data collection and data collection modes will be designated to retrieve information from the simulator. This information will be necessary to carry out the following requirements:

- perform diagnostic analysis in the system development phase
- initialization of the simulator and conduct of start-up testing (BIT)
- simulator calibration
- selected data collection for use in performance evaluation of the SUT

Use of the LORAL data collection system, as selected for the CNIL, is planned for the TESTS ACETEF integrated environment. For the uncoupled or stand-alone configuration, a parallel LORAL data collection system will be considered to minimize the internal difference between the two configurations. In addition, consideration will be given to routing selective data from internal and SWEG data bases through Task 7 as a data collection option. Loading on the TESTS CPU will be of critical importance in evaluating this alternative.

It is envisioned that the nodes for data collection will, at a minimum, include the input and output of the SUT (RF collection). It is also expected that data will need to be collected after the receiver portion of the interrogator or transponder to isolate the cause of performance decrements. The other nodes will be on the computer side and will monitor and collect data from the TESTS computer data base and the SWEG common data base.

5.1.9 TESTS Software Development Environment

During initial phases of TESTS System Development, several Intel 80486 based PC systems will be utilized for software prototyping and software development activities. This provides a low cost path for initiating software design and component development which can easily be rehosted to the TESTS operational environment. During later phases of TESTS development, the operational TESTS Host Computer system (refer to Section 5.1.4) will be utilized for software development.

5.2 SUPPORT SOFTWARE ENVIRONMENT

TESTS Support Software Environment includes software required for program CSCI development as well as operational support software. Development support software includes such things as CASE tools, compilers, assemblers, and library management tools. Operational support software includes operating systems, run-time applications support environment, and run-time library support.

5.2.1 CASE Tools

The preliminary phases of software design and development will be assisted by the acquisition of Object Maker, a CASE tool by Mark V Software. Object Maker provides off-the-shelf support for over 20 object oriented and structured design methods. Language support modules have been purchased which provide automatic code frame generation for both C Language and Ada. Object Maker is currently hosted on the Intel 80486 based PC platform, and is actively used to prepare high level software design diagrams.

For the operational software support environment, it is recommended that the AGE/ASA System Specification Environment and AGE/GEODE Software Design tools be purchased and hosted on the Sun SPARC work stations. These tools provide a complete system for detailed software specification and full code generation in a multitasking/ multiprocessing environment. The tools also provide automatic test code generation, full 2167A documentation, and compatibility with several real time operating system kernels including VRTX.

5.2.2 Compilers

Initial software development will require both Ada and C Language compilers. The Ada Z Compiler, by Meridian Software, and Turbo C++ Compiler by Borland have been acquired, and are presently hosted on the Intel 80486 software development platforms.

5.2.3 Assemblers

Due to the special requirements of real-time software development and debugging, it is anticipated that an assembly language compiler (assembler) and in-line debugger will be required for the operational software environment. This compiler will be hosted on the Sun SPARC work stations.

5.2.4 Configuration Management

Either commercial or custom software packages will be utilized to maintain configuration management of the TESTS operational software in accordance with the tailored MIL-STD-2167A as presented in the Software Development Plan. Strict configuration management is essential to the Evolving Prototype Plan as presented therein regarding the TESTS software life cycle. The configuration management tools, which have yet to be identified, will include library management functions for multi-user, multi-version software development. Restricted access and security procedures will be implemented to the level required by appropriate DoD guidelines. Configuration management will be applied at the highest level available for either CASE file, source file, or assembly file modules. Program archival and both on-site and off-site program backups will be maintained. Automatic program Build and Make functions will be implemented for accurate compilation and assembly of all program versions.

5.2.5 Real-Time Operating System

In order to meet the real-time simulation response and timing accuracy requirements discussed in Section 4.2.2, a high performance real-time multitasking operating system will be required for the operational TESTS software environment. A probable candidate to meet these needs is provided in the VRTX/OS real-time operating system components by Ready Systems, Inc. VRTX32 implements a real time kernel that provides high level language interaction for task management, memory management, communications, synchronization, clock management, and interrupt servicing. This kernel has been thoroughly tested, and provides excellent flat response, in the microsecond range, versus system loading. A full range of support software and options are available with VRTX, such as an Input-Output File Executive (IFX), a Multiprocessor version (MPV), a Real-Time Multitasking Debugger and System Monitor (RTscope), and a portable C Runtime Library. These products are available for both the Intel 80486 microprocessor and Sun SPARC station environments, and are compatible with the Sky Computer vectorizing accelerator boards.

5.2.6 SWEG

One of the critical areas that must be given careful consideration is SWEG. The primary interface of TESTS to the other components of ACETEF required during testing will be provided by SWEG. SWEG is derived from a battlefield simulation

called SUPPRESSOR which is approximately ten years old. An outgrowth of the SUPPRESSOR simulation program, SWEG has been updated to control and coordinate tactical engagement simulations in ACETEF, and provides a rich library of platform and emitter models. SWEG provides a standard format for the shared memory interface between the various components of ACETEF, and defines the protocol for interactions between components. The software components of TESTS will interface to the SWEG shared memory for required scenario simulation data, such as platform positions, attitudes, velocities, terrain elevation data, antenna pattern directional attenuations, antenna scan rates, etc. Note that TESTS will utilize some subset of SWEG capabilities to provide scenario preparation and execution, even when operating in a stand-alone configuration in the shielded hangar. It is anticipated that all interactions between TESTS software components, and other components of ACETEF will take place via the SWEG shared memory interface.

The Navy version of SWEG is still in development and the final level of capability is still undetermined. The ability to upgrade or modify any software package that old represents a degree of technical risk. Short cuts also tend to be adopted in updating software which might compromise performance if not fully tested. For example, SUPPRESSOR utilized metric conventions for all units, i.e., meters rather than feet. Selected parts of SWEG have been modified to use English units, i.e., feet. This is necessary since most of the Navy's measurements are in feet. However, an examination of the SWEG source code indicates that not all units have been changed, only those directly related to certain input parameters. Hence, there is a mixture of measurement units in the current version of SWEG. Conversion between units within SWEG could introduce an unknown degree of error simply because of round off errors. There will also be a need to supplement SWEG with a TESTS specific database. SWEG appears to have the basic capability to support TESTS and provides as much fidelity as any available scenario simulation package. SWEG is undergoing significant modification under contract to the CNIL. Variables are being added which will permit communication and IFF systems to be specified more precisely and the coordinate system is be modified to a polar system to accommodate satellite players within the scenario, i.e., SATCOM, etc. The CNIL version of SWEG should be used for TESTS. Until SWEG is fully upgraded and validated within ACETEF, it represents a potential unknown impact on TESTS. Hence, modifications of SWEG will need to be closely monitored. Furthermore, the documentation on SWEG is somewhat limited, so TESTS researchers will need to discuss SWEG operations directly with BDM personnel to ensure that SWEG is fully understood.

While TESTS can operate in a stand-alone configuration or integrated through CNIL to ACETEF, SWEG will always be required. In the stand-alone configuration SWEG will need to be hosted at a workstation level, such as a VAXstation. When integrated with CNIL/ACETEF, TESTS will receive SWEG inputs through the appropriate level of shared memory. In the CNIL/ACETEF integrated configuration TESTS may require two interfaces to the shared memory. In order to meet real time processing requirements for multipath calculations, a second direct access interface to the SWEG terrain data base will be required. The need for this second access to shared memory will depend upon the final architecture for the CNIL.

Figure 5-5 illustrates the internal data structures and memory interfaces inherent in SWEG.

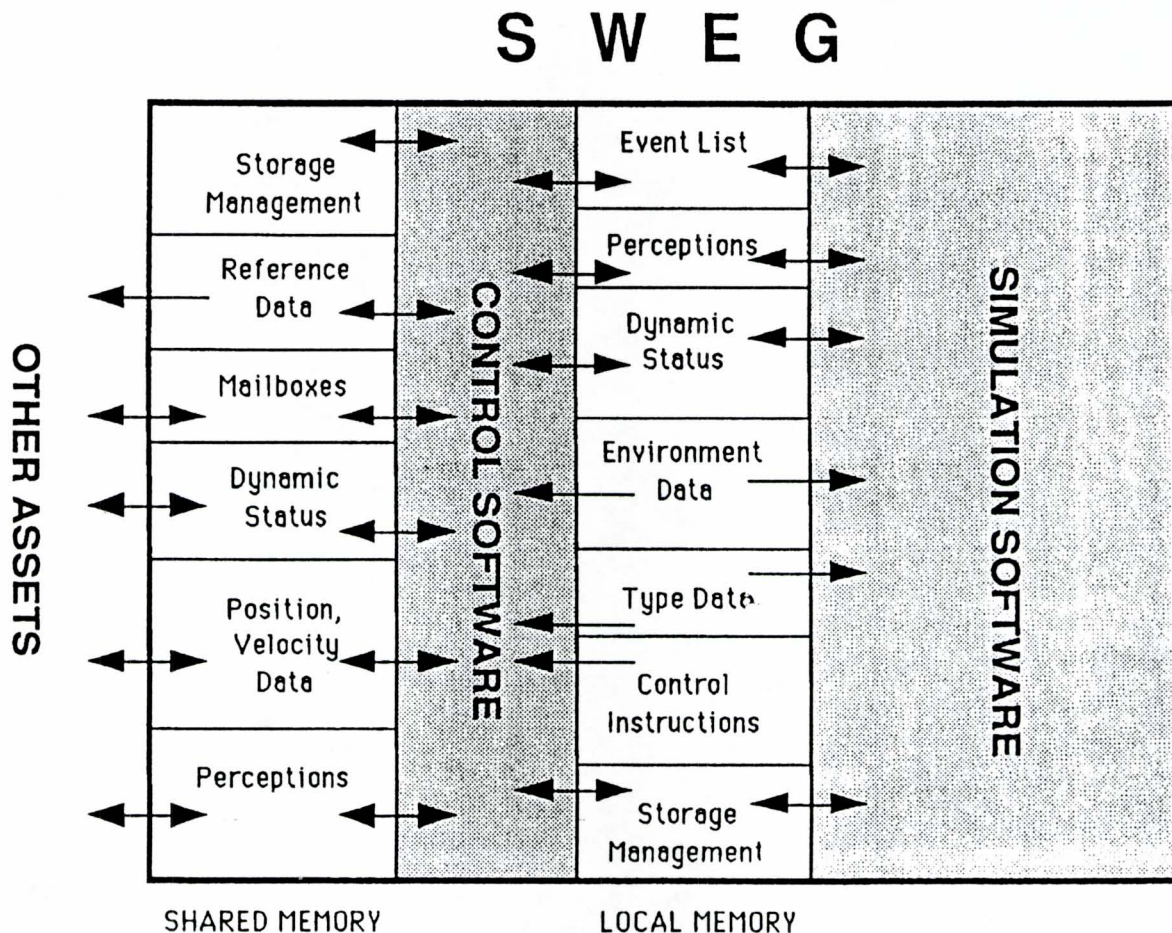


Figure 5-5. The SWEG Internal Data Structures and Memory Interfaces.

5.3 INTERFACES

The ACETEF provides a controlled environment for integrated testing of aircraft avionics systems at the NAVAIRTESTCEN. ACETEF provides a suite of laboratories and facilities that can interact to provide a variety of electromagnetic test environments and stimulations for actual avionics systems mounted on an aircraft and radiated in an anechoic chamber. An adjacent shielded hangar provides additional space for hard wired testing of several aircraft. Presently there are several operational elements of ACETEF, such as the Aircrew Systems Evaluation Facility (ASEF), the Electronic Warfare Integrated Systems Test Laboratory (EWISTL), the Electromagnetic Environmental Generation System (EMEGS), and the Tactical Avionics and Software Test and Evaluation Facility (TASTEF). Other planned facilities include the Communications, Navigation, and Identification Laboratory (CNIL), the Offensive Sensors Laboratory (OSL), the Electromagnetics Environment Effects Test Laboratory (E³TL), and others. TESTS will integrate into the expanding capabilities of ACETEF, initially to provide Development Testing of the MK XII / advanced IFF system, and eventually to provide full Operational Testing of IFF systems as part of the CNIL.

It is anticipated that TESTS will be employed in at least four different configurations:

1. as a stand-alone benign test tool to provide IFF testing on aircraft in the shielded hangar,
2. as a stand-alone test tool integrated with additional equipment such as the Tactical Agile Signal Simulator (TASS), used to provide an ECM/jamming environment,
3. integrated in CNIL with CNIL operating independently of ACETEF, or
4. in a fully integrated ACETEF testing environment utilizing several assets at once to test aircraft systems in the anechoic chamber.

SECTION 6. SYSTEM DEVELOPMENT PLAN

TESTS shall be a computer-based system tool to simulate prototype models of advanced tactical electronic systems. The simulation environment selected as a test case involves the Identification Friend or For (IFF) with emphasis on the MK XII and MK XV or comparable advanced IFF systems. It is proposed that the TESTS tools be designed to interface with various platforms under test (PUT) through simple, potentially off-the-shelf interfaces. The proposed TESTS software is a combination of Commercial-off-the-shelf (COTS) software, simulator operational software, and Government furnished SWEG software. There may also be reusable software as the prototypes evolve from simple to more complex IFF features and modes, and from the Mark XII to the advance IFF simulations.

In order to provide a low risk, high confidence, and low cost approach to the design, purchase, fabrication, and integration of the hardware and software components of the TESTS system, an evolving Prototype Build Plan will be adopted. This plan uses a number of incremental builds which provide increasing capability and diversity in the number of platforms and signals to be generated, and simultaneously, increasing fidelity in the environmental and channel propagation effects to be simulated by TESTS. This evolutionary approach will allow early closed loop testing and validation of the TESTS system with existing IFF systems such as the MK XII, and provide a low risk transition to more advanced IFF systems utilizing spread spectrum signals.

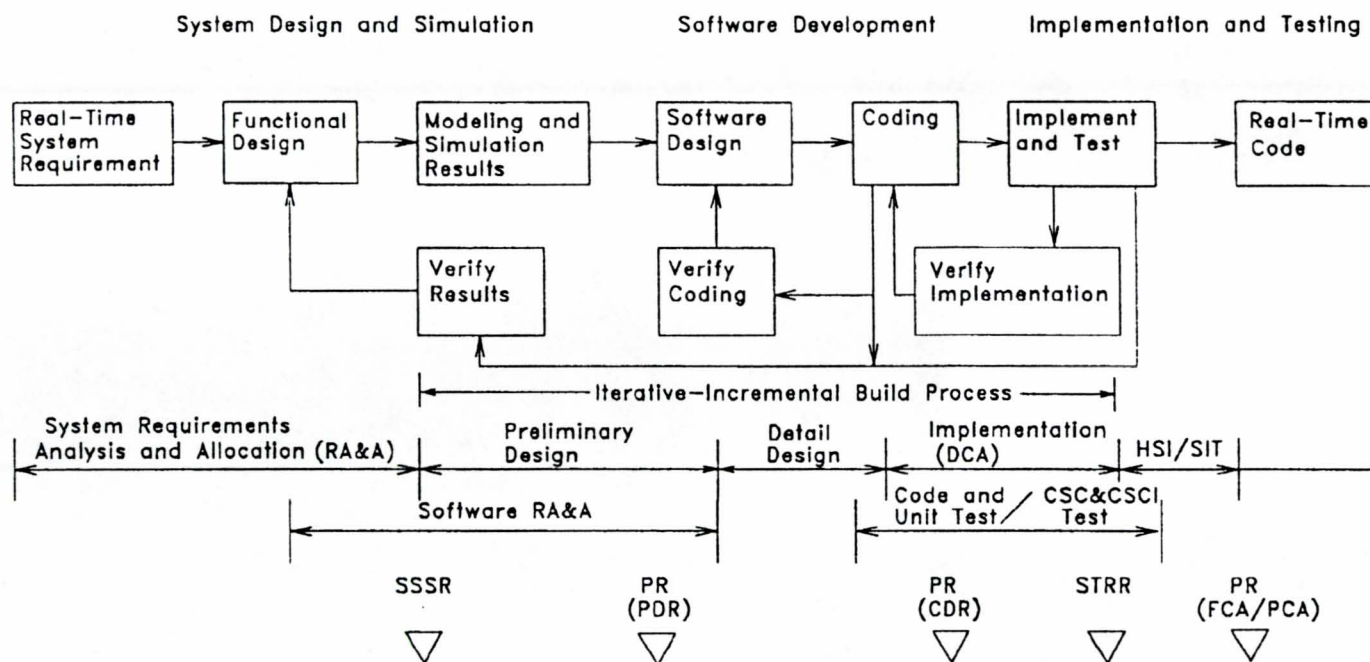
6.1 SOFTWARE DEVELOPMENT APPROACH

The TESTS project will utilize a tailored MIL-STD-2167A software development approach. A tailored approach to DoD software development standards is proposed to accommodate the prototyping approach to the TESTS development, accommodate the research aspects of TESTS and maintain the cost effectiveness of the TESTS concept. Figure 6-1 provides an overview of the real time system development process which will be implemented in TESTS. It depicts major design, development and test activities, major project milestones.

The term prototype as used herein refers to an instance of a software version that does not exhibit all properties of the final system as defined in DoD-HDBK-287. It is an intermediate stage to the development of the final product. TESTS will be developed following an evolving prototype approach. This approach has the advantage of intermediate stage to the development of the final product.

Figure 6-1. Overview of Real Time Systems Development Process

REAL-TIME SYSTEM DEVELOPMENT PROCESS



Notes on Tailoring:

1. 2167A and 1521B call out 9 major reviews as minimum plus potentially separate HW-SW PDRs/CDRs: Schedule above shows 5 reviews but assumes the PDR, CDR, & FCA/PCA could be replaced by a Progress Review (PR)
2. 2167A calls out 17 Data Items and 490A implies A, B and C specs. A potential plan for SW Development would be to combine the SSS (Aspec) and the PIDS/CIDS (B/C) and the SSDD into the Functional Description (FD), DI-E-30104B, with a contractor defined RTM.

TESTS will be developed intermediate stage to the development of the final product. TESTS will be developed following an evolving prototype approach. This approach has the advantage of following an evolving prototype approach. This approach has the advantage of providing continual feedback on the progress and operation of TESTS. This approach has been successfully used in a number of major DoD programs. While not the standard MIL-STD-2167A approach to system development, the evolving prototype approach is compatible with and can be implemented in compliance with the requirements of MIL-STD-2167A. Figure 6-2 depicts the flow of an evolving prototyping approach within MIL-STD-2167A.

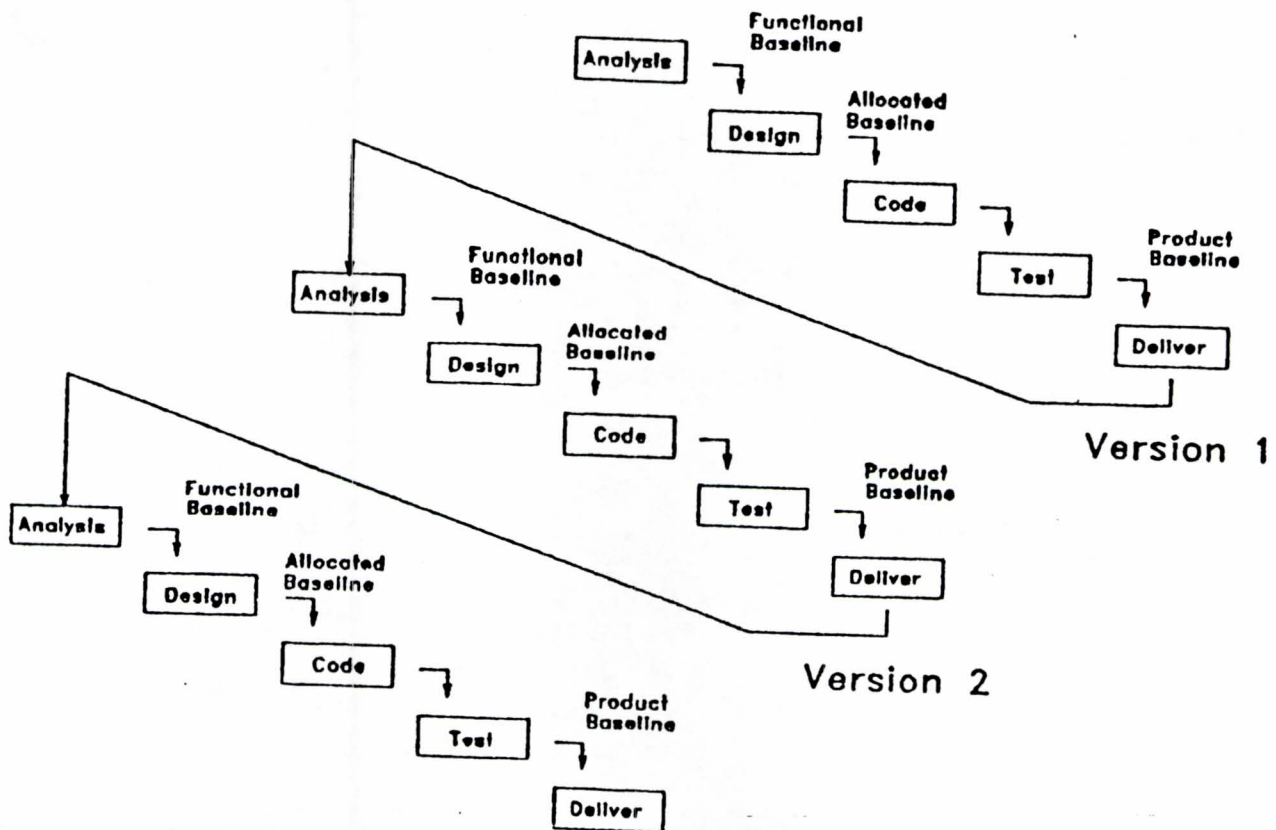


Figure 6-2. Prototyping in a MIL-STD-2167 Development Environment.

6.2 HARDWARE DEVELOPMENT APPROACH

A combination of off-the-shelf and custom hardware will be required for implementation of TESTS. COTS equipment will be used where practical. Custom equipment or custom modifications of existing equipment will be required for the stimulation portion of TESTS.

The development of custom TESTS hardware will be initiated as early in the design process as feasible to reduce program risk. The hardware development will be accomplished in parallel with the software development as previously shown in Figure 6-1. IST will develop the specifications for the hardware. The detail design and fabrication of the custom hardware will be competitively bid. Several qualified vendors have been identified to develop the custom hardware, including ViaSat and CAL. The custom hardware components will be bid independently. Initial analysis of vendor capabilities indicates that a team of support vendors may be desirable to capitalize on various vendor strengths and experience.

6.2.1 SWEG Hardware

COTS computer hardware will be used to implement SWEG in the development and stand-alone configurations. A DEC computer workstation will be used to host the SWEG software. The shared memory required to run SWEG will be implemented using standard VME hardware. The final selection of the vendor for the shared memory hardware will be based on competitive bid.

6.2.2 Signal Generation, Modification and Distribution Hardware

There are three components in the TESTS stimulation hardware. One component performs the actual signal generation. The second component implements the channel effects on the generated signals. The final component distributes the TESTS messages across the available signal generators. Hardware will be modular for ease of configuration and reconfiguration. The modularity will also permit ease of upgrade from the initial MK XII capability (pulse signal) to the advanced IFF capability (spread spectrum).

6.2.2.1 Signal Conditioning Hardware

The RF Signal Conditioner will be built to IST specifications by a commercial vendor. The development of the RF Signal Conditioner will be initiated at the start of

the TESTS full scale development. The signal conditioning hardware is required by the initiation of the second TESTS prototype to achieve program objectives.

6.2.2.2 Signal Generation Hardware

Signal generation hardware for TESTS will be developed in two stages. The first phase of the development will focus on the core capability required to generate pulsed MK XII signals. This initial version of the hardware will be used to support the first TESTS prototype which will emulate the MK XII. The second phase of the signal generation hardware development will expand the capability to generate multiple spread spectrum signals for an advanced IFF.

The signal generation hardware will be developed to IST specifications by a commercial vendor. Signal generation approaches implemented in the NAVAIRTESTCEN ACETEF CNIL will be used as guidance to maximize hardware commonality.

6.2.2.3 Multiplexing Hardware

A custom signal multiplexor will be developed for TESTS. This component may be developed by a commercial vendor or developed internally by the UCF Department of Electrical Engineering. The choice of developer will be based on cost and schedule.

6.2.3 Data Collection Hardware

For the stand-alone configuration of TESTS, the data collection system developed by LORAL that has been selected by NAVAIRTESTCEN for the ACETEF CNIL will be utilized. This selection assures commonality with other NAVAIRTESTCEN capabilities and minimizes data collection interface requirements for TESTS.

6.2.4 TESTS Computer Hardware

TESTS computer hardware will utilize COTS host computers and accelerator boards. Selected hardware will be modular and provide for easy growth capability through the addition of additional coprocessor to accommodate increases in computing requirements or new features.

6.2.5 Threat Hardware

When required, threat signals will be introduced using Navy selected equipment. TESTS will not include an internal threat capability, but will provide the interface provisions to external threat generation systems through standard computer interfaces.

6.2.6 Other Hardware

Other hardware that may be required for TESTS includes Crypto hardware, network interfaces, and other data interfaces. These requirements can not be determined until the detail design phase of TESTS.

6.2.6.1 Crypto

If computer-based implementations of the advanced IFF Crypto device can not be developed in collaboration with NSA, TESTS will include provisions for interface with actual Crypto hardware to code generation and timing synchronization.

6.2.6.2 Calibration/Test Hardware

A minimal suite of off-the-shelf signal analysis other related hardware will be required for TESTS. Initially, this hardware will be used for validation and verification (V&V) tests and calibration of the TESTS hardware as it is developed and integrated into the system. This hardware will be selected to support calibration requirements once TESTS is developed and installed at NAVAIRTESTCEN.

6.3 VERIFICATION AND VALIDATION FOR TESTS

A strong requirement exists in the TESTS project to conduct a rigorous V&V activity from the software unit level through the consolidated system level. As a consequence of this desire, the requirement traceability will be included in the approval process for the three configuration baselines, namely, functional, allocated and product.

Verification matches the new baseline against the requirements identified in the previous baseline to ensure that all requirements have been satisfied. Validation matches the new baseline against the original requirements for the system to ensure that the final product will meet the end user objectives. V&V relies on documentation

reviews, contractor test monitoring, and independent testing to evaluate the products making up each of the baselines.

The testing is divided into two categories: (1) Development Test & Evaluation (DT&E), and (2) Operational Test & Evaluation (OT&E). DT&E is conducted to verify that design objectives have been met, that minimum risk has been attained and that functional performance of the final system has been properly estimated. Emphasis is on validation. OT&E, on the other hand, is conducted by the end user to verify that the final system meets the end user objectives and to determine impacts, if any, on end user operations when the system is installed. The emphasis here is on verification.

During the DT&E phase of TESTS the sequence of V&V tasks are applied to the required phases of DT&E:

- (1) During the "concept exploration phase" alternative system concepts, technologies, and designs will be accomplished and validated.
- (2) During the "demonstrated and validation phase" the preferred technical approach, including the identification of technical risks and feasible solutions will be determined.
- (3) During the conduct of the "full scale development phase", (i.e., that the design meets its required specifications in all areas).
- (4) After final system completion.

The method of implementation of the testing portion of these V&V tasks will be twofold. The first will entail the generation of unit "drivers" to stimulate the units under test and validate the functional accuracy of the outputs. The units will be sequentially put together with intermediate validation by known driver inputs until the entire system is assembled and similarly validated end-to-end.

The second method is to use actual flight data to V&V as many of the subunit modules as possible. The use of existing flight test data will be maximized during the formulation and execution of the V&V test plan. It is anticipated that requirements for additional parameter measurements of already planned flight tests will be needed to V&V intermediate stages of the simulation tool TESTS. These requirements will be consolidated and identified early in the preparation of the functional specifications. Both methods will be planned and used to conduct a rigorous V&V program.

The second method (i.e. the use of actual flight data) for the implementation of the OT&E testing is recommended for the verification process. An outside organization should be considered to conduct an "Independent V&V" during this final phase. A selected number of actual flight tests will be necessary to test the "envelope of performance" of TESTS and to verify as many of the TEMP objectives as possible.

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