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Effects Of Deposition Temperature And Post Deposition Annealing On The Electrical Properties Of Barium Strontium Titanate Thin Film For Embedded Capacitor Applications

Ranganathan, Ravip Peelamedu

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EFFECTS OF DEPOSITION TEMPERATURE AND POST DEPOSITION ANNEALING ON
THE ELECTRICAL PROPERTIES OF BARIUM STRONTIUM TITANATE
THIN FILM FOR EMBEDDED CAPACITOR APPLICATIONS

by

RAVIPRAKASH PEELAMEDU RANGANATHAN
B.S. Bharathiyar University, 2000

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the Department of Electrical and Computer Engineering
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2004
ABSTRACT

A higher degree of system level integration can be achieved by integrating the passive components into semiconductor devices, which seem to be an enabling technology for portable communication and modern electronic devices. Greater functionality, higher performance and increase in reliability can be achieved by miniaturizing and reducing the number of components in integrated circuits. The functional potential of small electronic devices can be enormously increased by implementing the embedded capacitors, resistors and inductors. This would free up surface real estate allowing either a smaller footprint or more silicon devices to be placed on the same sized substrate.

This thesis focuses on the effect of deposition temperature and post deposition annealing (PDA) in different gas ambient on the electrical properties of sputter deposited ferroelectric Barium Strontium Titanate (Ba$_{0.5}$St$_{0.5}$) TiO$_3$ thin film capacitors. Approximately 2000Å of Barium Strontium Titanate (BST) thin film was deposited at different substrate temperatures (400, 450, 500 and 550°C) on cleaned silicon substrates. These BST films were then annealed separately in 100% N$_2$, 100% O$_2$ and 10% O$_2$ + 90% N$_2$ at 575°C in sputtering machine (PVD anneal) and a three zone annealing Lindberg furnace. The objective of this thesis was to compare the effect of PDA on the electrical properties of BST films deposited at different substrate temperatures between PVD annealing and furnace annealing.

For this work, tantalum thin film was used as top and bottom electrode to fabricate the capacitors. BST thin film capacitors were fabricated and characterized for leakage current and
dielectric breakdown. Roughness study on pre and post annealed BST films were done using optical profilometer. The capacitors were tested using HP impedance analyzer in the frequency range from 10Hz through 1 MHz. From the experiments, 100% O2 annealed furnace annealed BST thin film seem to have better dielectric constant, higher breakdown voltage and nominal capacitance density.
Dedicated to my parents
ACKNOWLEDGMENTS

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CHAPTER ONE: INTRODUCTION

The ever increasing functionality, speed, portability and increased use of the internet in consumer electronics is putting tremendous pressure on designers and manufacturers to pack more circuitry into smaller spaces [1,2]. Recordable minidisks, hard drives, radio, MP3 players and browsers are now integrated into a portable and compact package which is the size of a thumb. The number of Integrated Circuits (I.C) and passive components in a package increases drastically as the functionality of the components increases. As the operation speed of the computers is increased to make full use of the internet, capacitors are needed to be placed as close to the I.C. as possible to avoid parasitic inductance effects. The active components include ICs, transistors and diodes. Passive components refer to non-active elements, including capacitors, resistors and inductors, and usually ten to hundreds of discrete passive components are mounted on the circuit board inside a contemporary electronic device [2]. In typical electronic packages, 80% of total electronic components are passives, and they can take up to 50% of the Printed Wiring Board (PWB) area [3]. All this leads to the fact that the size of a device is now becoming more often a function of the circuit board or module size than anything else. The question begs therefore, how will all these future features be contained in products that will still fit in your hand? [1] The solution may very well be the elimination of the passive components on the surface of the circuit by burring them within the inner layers of the PWB. Integration of the passive components within the PWB is referred to as “Embedded Technology”.
1.1 Embedded Passive Components

The primary structural blocks for most of the electronic systems are active and passive components and their interconnecting substrates. The substrate can be either laminate, ceramic, metal or silicon with an interconnection pattern. A cellular phone for instance, may consist of only about few integral circuits (IC) compared to 300-400 passives. Figure 1.1 shows the backside of a circuit board from a PC with surface mount capacitors all around the chip's pins.

![Figure 1.1 Backside of a circuit board from a PC with surface mount capacitors all around the chip's pins][4]

In recent electronic packages the ratio of passive to active devices are rapidly increasing, and shown in Table 1.1. Thus the system cost, size, and reliability are substantially influenced by
the passive components. Alternatives are necessary to meet the smaller, faster, more reliable, lighter and cheaper next generation electronic packaging.

Table 1.1 Comparison of ratio of passive to active components in consumer products [2]

<table>
<thead>
<tr>
<th>Product</th>
<th>IC</th>
<th>Passive Component</th>
<th>Total Component</th>
<th>Passive : Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desktops</td>
<td>182</td>
<td>1066</td>
<td>1285</td>
<td>6:1</td>
</tr>
<tr>
<td>Laptops</td>
<td>53</td>
<td>820</td>
<td>900</td>
<td>15:1</td>
</tr>
<tr>
<td>Pen pager</td>
<td>15</td>
<td>437</td>
<td>460</td>
<td>29:1</td>
</tr>
<tr>
<td>PCS Phones</td>
<td>15</td>
<td>322</td>
<td>380</td>
<td>21:1</td>
</tr>
</tbody>
</table>

1.1.1 Embedded Capacitor

Presently the surface mount or through-hole technologies based discrete capacitors are the workhorse for the capacitor technology. Singular capacitor enclosed inside a single case, mounted on an interconnecting substrate using a solder joint, is referred to as “discrete capacitor”. However, higher packaging density, improved electrical performance and reliability at potential reduced manufacturing cost can be achieved by integrating the capacitors within the PWB, package module or multilevel metallized IC chips. Integration of embedded thin film capacitors is beneficial at on-chip and off-chip level. The embedded capacitors can be singulated or can be distributed as an entire plane of capacitance between the ground plane and the power of the distribution system as shown in Figure 1.2. The main objective of the embedded passive
components is to eliminate surface mount technology (SMT) or soldered parts, from the printed circuit board and to embed those components within the board thickness.

Since the majority of the passive components used on a circuit board are capacitors and resistors, a high level of present interest is primarily focused on them. Capacitors are a vital component in nearly every military and commercial high performance system. Military and
commercial aircraft manufacturers, the medical industry and power utilities use high
temperature, high energy density capacitors. The major contribution of the capacitor is employed
for decoupling, or as bypass capacitors. The noise arising due to numerous drivers switching
simultaneously in digital or mixed applications are suppressed using decoupling capacitors.
Decoupling is an ideal initial application for embedded capacitors. It can solve many of the
performance problems associated with the inductance of present surface mount capacitors, free
up board space, and eliminate solder joints. NEMI (National Electronics Manufacturing
Initiatives Inc.) roadmap, another index widely used for electronic component industry, also
shows that the embedded passive based technology could significantly improve reliability and
cost effectiveness is shown in Table 1.2.

Table 1.2  Embedded passive implementation plan [5]

<table>
<thead>
<tr>
<th></th>
<th>1999</th>
<th>2002</th>
<th>2005</th>
</tr>
</thead>
<tbody>
<tr>
<td>C density</td>
<td>&lt; 3 nF / in²</td>
<td>30 nF / in²</td>
<td>200 nF / in²</td>
</tr>
<tr>
<td>C cost</td>
<td>$ 0.05 – 0.30 / in²</td>
<td>$ 0.20 / in²</td>
<td>&lt; $ 0.10 / in²</td>
</tr>
<tr>
<td>R density (mixed R values)</td>
<td>20 / in²</td>
<td>60 / in²</td>
<td>200 / in²</td>
</tr>
<tr>
<td>R cost (with trim)</td>
<td>$ 0.20 – 0.30 / in²</td>
<td>$ 0.20 – 0.30 / in²</td>
<td>$ 0.08 – 0.25 / in²</td>
</tr>
<tr>
<td>R resistivity</td>
<td>To 100Ω/□</td>
<td>To 1 MΩ/□</td>
<td>To 1 MΩ/□</td>
</tr>
</tbody>
</table>

A capacitor dielectric placed between the power and ground plane would lower noise and
acts as blocking capacitors for filtering applications. Resistors could also be embedded,
providing similar advantages. Additional advantages gained would include a large reduction in the number of solder joints leading to improved reliability. So, with all these benefits, why hasn’t there been a widespread adoption of embedded passive technology? The answer lies partly in design, prototyping, test and infrastructure issues associated with the manufacture of circuits with embedded passives. A recent report by Prismark Partners [6] suggests that the major obstacles are the availability and adoption of smaller discrete components delaying the need and the fact that embedded passive technology currently does not offer the component density or tolerances necessary for widespread replacement of discrete components. Uses are therefore, currently limited to niche applications.

1.2 Embedded Capacitor Applications

From an application point of view, capacitors can be broadly classified as: decoupling, blocking and precision capacitors.

1.2.1 Decoupling Capacitor

A capacitor is an electrical device capable of storing electric charge and consists of two metal conductors isolated by an insulated or non-conducting layer. The usefulness of the capacitor is determined by its ability to store electric energy. Ideally, could be represented just by a capacitive component as shown in Figure 1.3.
Parasitics of the real capacitor are the equivalent series resistance (ESR, $R_C$) and equivalent series inductance (ESI, $L_C$). Figure 1.4 shows an equivalent circuit for real capacitor. In other words, the value of the lumped impedance is measured and from this value the equivalent circuit capacitance is calculated.

![Series equivalent representation of a real capacitor](image)

**Figure 1.4** Series equivalent representation of a real capacitor

Signal decoupling in both digital and analog systems is the most important application of capacitors in electronic packages. Figure 1.5 represents the schematic diagram of a coupling capacitor that acts as a sink for charges due to decoupling the IC from the power supply. In common most of the electronic circuits share a power supply. During switching, a logic circuit draws current from the power supply, and is likely to cause voltage fluctuation across the power supply.
This power distribution noise is increased with simultaneous switching of several drivers in digital or mixed signal application circuits [7, 8, 9, 10]. Decoupling capacitors are inserted into a circuit in order to reduce the noises due to circuit switching.

1.3 Embedded Capacitor Vs Surface Mount Capacitors

For future electronic devices embedded thin film capacitor technology offers a substantial solution by integrating the capacitors within the chip or the printed wiring board. The major advantage of using embedded capacitor over surface mount capacitor is to reduce the decoupling effect. The two jobs of a decoupling capacitor are:

1. By using a very high value capacitor the current required to run the chip for one clock cycle can be achieved without its voltage dropping.

2. Ramping the charge and delivering that charge at high level can be achieved by introducing a low-inductance capacitor placed close to the chip.
The overall circuitry inductance can be reduced by using the decoupling capacitors in the circuits. In a surface mount technology (SMT) the inductance can be reduce by fabricating the capacitors with less parasitic inductance and placing them closer to the chips to decrease the inductance of the vias and metal electrodes or traces connecting them to the chip's power and ground pins. The above strategy in SMT is reaching its limit. The solution for this problem could be switching to embedded passive technology.

The current flow is like a loop in case of a SMT capacitor, where it travels from the power/ground planes into the board, up to the surface, through the capacitor, and back down into the board. A simple circular loop 1 mm in diameter would give about 2 nH of inductance, and that's a lot in high-frequency decoupling [4]. The inductance associated with this loop current can be isolated by installing a dielectric directly in between the power and ground planes. The current loop is smaller for an embedded capacitor because it is planar and in the same plane as what it decouples, especially if the capacitor's plates are very close together. The inductance of the planar embedded capacitors is less than that of a surface mount capacitor because of the way current is directed inside the device. The left side of Figure 1.6 shows how the current in a typical surface mount capacitor travels in the same direction in the plates due to the fact that the leads are on opposite ends of the unit.
Currents flowing in the same direction create fields that reinforce each other and amplify the effects of inductance [11]. In an embedded capacitor, the current is fed in and drawn out of the same side so the current travels in opposite directions in the plates. Hence the field produced due to the opposite current flow cancels each other, lowering the inductive effect. Inductance for embedded caps can be even further decreased by connecting the plates along the entire length of their sides, avoiding the current crowding associated with point contacts. Embedded capacitance is capable of being implemented in circuits in such a way to greatly decrease the inductance from both of these sources (cap and location), and is a natural next step in board technology [14]. The main advantages of using the embedded capacitors over the SMT are:

1. Free up surface real estate allowing either a smaller footprint or more silicon devices to be placed on the same sized substrate, thereby enormously increasing the function potential of small electronic devices

2. Materials cost saving
3. Improved reliability, due to reduced solder joints in package

4. A simplified board construction can be achieved by placing the capacitors directly underneath the active components they support and reducing the number of layers and interconnecting vias thereby, reducing costs and lower parasitic inductance and cross talk.

Though, integration of embedded capacitors into semiconductor devices is seen as an enabling technology, it faces issues and challenges which are discussed in the next section.

1.4 Challenges and Issues in Embedded Capacitors

The overall electrical performance of embedded thin-film capacitors is dictated by intrinsic materials and electrical properties of the thin film dielectric used in them, such as dielectric constant, dielectric loss, dielectric dispersion, breakdown field etc. Though, it is impossible to have an ideal dielectric material, a trade-off among the electrical properties of thin film dielectric materials, which determines whether or not a dielectric material can be optimally used for a particular application. The key drivers in the embedded capacitor research and development are:

1. Long term reliability
2. On-chip and off-chip level integration scheme
3. New testing procedures and test vehicles to characterize the electrical performance of thin film capacitors
4. Cost-effective process to fabricate high-K material over a wide range of film thickness.
Integration of embedded capacitors into power devices or into device lead structure has at least two orders of magnitude lower than the parasitic lead inductances. Remarkable interest is growing these days in extending the embedded thin film capacitor technology from the realm of well developed signal electronic domain to the power and automotive electronics applications [13]. Thin film capacitors must comply with an additional requirement of high breakdown voltage, varying from 10V to 1000V in order to meet the specifications for most of the electronic and automotive applications.

In case of embedded capacitor using metal-insulator-metal (MIM) configuration, strict control on different set of electrical properties is required. Current transients caused by simultaneous switching of on-chip and off-chip drivers can be supported only if the capacitance of the decoupling capacitor is large. Based on guidelines provided by Semiconductor Industry Association (SIA), Chahal et al. [12] estimated that capacitance densities in the range of 13-72 nF/cm$^2$ are required for hand-held and cost performance applications over the next decade. This was computed according to the formula,

$$P = p(C_T V_{DD}^2 f)$$

where, $P =$ consumed power, $p =$ power transition occurring probability, $f =$ clock frequency (Hz), $C_T =$ effective capacitance of the chip, and $V_{DD} =$ device voltage (V). Higher breakdown voltage (>10V) and lower current density (<10$^{-6}$ A/cm$^2$ at 1MV/cm) are required from both functionality and reliability viewpoints.
1.5 Objective of This Work

The placement/integration scheme and the overall capacitor structure property mainly influence the electrical performance of the embedded capacitors. Design considerations for placing the embedded capacitors in packages or chips are vital to minimize the parasitic series inductance in the pH range. In order to ensure long term electrical reliability of the overall capacitor structure, the scope of interaction of different electrode metal with dielectric films needs to be evaluated. To avoid any premature electrical breakdown of the dielectric film minimum interface roughness is required. This leads to the question, whether the embedded passives or integrated passives are replacing SMT components soon? With the available new enabling technology, penetration will be slow, starting with high performance systems and descending gradually towards commodity products. And all this depends on how fast the technological issues are cleared.

Other applications of a capacitor such as a blocking capacitor, separating two dc circuits, requires severe limits on leakage current density along with high capacitance and low series inductance. Capacitors integrated in DRAMs require high charge storage density (as high as $25\text{fF}/\mu\text{m}^2$) along with extremely low dc leakage (<10-100 pA at 5V) [14]. Capacitors used for RF applications need to have good capacitance matching, low voltage coefficients, GHz range dispersion, and precise control of capacitor values. Integration of polymer based embedded decoupling capacitors in the advanced packaging or chips require low temperature processing, basically influenced by the thermal stability of the polymers, which is one of the major concern. Thin film deposition process with low processing temperature has to be developed since; the integration of decoupling capacitors in multilevel metallization for on-chip decoupling is also
limited by low thermal budgets for back end of line processing. A sound understanding of effects of the various process parameters on the electrical and material properties of the deposited thin films is necessary.

Combining all these requirements into one capacitor puts a great deal of demand on dielectric materials. The development of novel high-k dielectric materials that are compatible with already compatible silicon and polymer (organic substrates) processing technologies is the key driver for the research in capacitor technology. Currently, most of the embedded capacitor studies are concentrated on the low temperature co-fired ceramic (LTCC) and ceramic/polymer composites for MCM application. Both of the above approaches are commercially available in the market, however, in the end, the technology with lower manufacturing cost, better processing margin and the materials with higher dielectric constant, would be necessary in the following decades. In terms of higher dielectric constant, ferroelectric compositions, like BaTiO$_3$ and (Ba,Sr)TiO$_3$, are better than the conventional capacitor materials (SiO$_2$, Ta$_2$O$_5$ etc).

This thesis focuses on the fabrication and electrical characterization of sputtered thin films as dielectrics for embedded thin film capacitor applications. The dielectric film investigated as part of this thesis is Barium Strontium Titanate (Ba,Sr)TiO$_3$. Tantalum has been used as an electrode material for bottom electrode with silicon as substrate. The overall purpose of this research is to explore and quantify the potential of sputtered high-k dielectric films for capacitors used in embedded capacitor applications in terms of their electric performance.

Chapter 2 of this work presents an overview of the various high dielectric constant material and ferroelectric material options for embedded capacitor application.
An overview of sputtering and the AJA sputtering system used for this thesis work, process conditions for sputtering dielectric and tantalum electrode films, methods for sputtering process optimization have been discussed in chapter 3.

In Chapter 4, material and electrical characterization results of (Ba,Sr)TiO$_3$ has been presented. The electrical characterization results of the fabricated capacitors have been presented over a varied film thickness and operating frequencies (100Hz to 10MHz). The electrical properties investigated in this chapter are dielectric constant, dielectric loss, and breakdown voltage and leakage current density.

In Chapter 5, conclusions of this thesis are summarized and discussed. Future work and remaining challenges related to this thesis work are also listed.
CHAPTER TWO: OVERVIEW OF HIGH K MATERIAL

The charge storage capacity of a dielectric material can be defined by a parameter called dielectric constant, which is usually denoted by an alphabet “k”. Consequently, it also defines capacitance, C, of any capacitor comprising of a layer of dielectric sandwiched between two metal plates. In the figure 2.1 size of the upper plate defines area of the capacitor contact (A).

![Figure 2.1 Illustration of an ideal MIM capacitor](image)

With all other parameters equal, k would define the extent of capacitive coupling between two conducting plates, or simply, it would determine the capacitance of the above structure. With “high” k dielectric such coupling would be strong, and with “low” k dielectric being obviously weak. In Si technology the reference is a value of k of silicon dioxide, SiO$_2$, which is 3.9. Dielectrics featuring k>3.9 are referred to as “high” k dielectric while dielectric featuring k<3.9 are defined as “low” k dielectrics. To implement the full functionality of very high density ICs both high k and low k dielectrics are needed, although, for drastically different reasons. In
embedded stacks high-k dielectrics are needed to maintain sufficiently high capacitance for decoupling.

Increasingly smaller and higher performance devices are prodding the search for novel high k materials. As the device dimensions of the very large scale integration (VLSI) integrated circuits continue to scale down, several problems associated with the dielectric films become apparent [16,17,18]. In order to make either useful devices (capacitors, for example) or a meaningful fundamental investigation, the films must possess physical continuity, i.e. pinholes etc. must be avoided; mechanical stability, i.e. the films must not be in a highly stresses state or cracking as a short circuit can result, since many of the properties of a dielectric depends sensitively on the film thickness. Dielectric thin films serve important functions for semiconductor devices and integrated circuits. The most important applications of dielectric films are:

1. as a gate dielectric for MOSFETs and
2. as a dielectric for capacitor application

Since one of the principle applications of the dielectrics is in the thin film capacitors, it is desirable to use materials with as high a value of permittivity as is practically realizable. The range of the materials used is wide and encompass plastics, oxides and ferroelectrics, all of which can be deposited by conventional technique [19].
2.1 High-K Material Options for Thin Film Capacitor

High-K materials that have been actively pursued for capacitor dielectrics and for gate dielectrics can be categorized into two groups. The first group consists of the "simple" high dielectric-constant (K) materials which has compounds of a single metal and oxygen with atomic composition similar to that of SiO$_2$. Tantalum pentoxide (Ta$_2$O$_5$), Hafnium Oxide (HfO$_2$), Aluminum Oxide or Alumina (Al$_2$O$_3$), Zirconium Oxide (ZrO$_2$) and Titanium Oxide (TiO$_2$) are some of the first group simple dielectric constant materials. The dielectric constant of these materials ranges from 8 to 160.

2.1.1 Tantalum Pentoxide

Tantalum pentoxide (Ta$_2$O$_5$) is a high K material that has reasonably low leakage current and higher breakdown strength. Corrosion resistance, piezoelectricity and high refractive index are some of the interesting properties of Ta$_2$O$_5$. Compared to dielectric constant of perovskite structured films such as SrTiO$_3$, Pb$_x$Zr$_{1-x}$TiO$_3$, (Ba$_x$Sr$_{1-x}$) TiO$_3$, the dielectric constant of Ta$_2$O$_5$ is much lower. Although, Ta$_2$O$_5$ has been preferred for DRAM applications due to the following advantages:

1. There is only a slight dependency of the dielectric constant of Ta$_2$O$_5$ over the applied voltage as compared to other high k films and ferroelectric films.

2. Compared to other high k films the Ta$_2$O$_5$ has a higher dielectric breakdown strength and lower leakage current.

3. The Ta$_2$O$_5$ films stoichiometry can be easily controlled.
2.1.2 Zirconium Oxide

Monoclinic, orthorhombic, tetragonal and cubical are the four different crystalline modifications of ZrO$_2$, based on preparation techniques. Under atmospheric pressure, around 1150°C the monoclinic low temperature phase transforms into tetragonal ZrO$_2$. This phase is stable up to 2350°C after that the tetragonal phase transforms to cubic ZrO$_2$. High refractive index, high dielectric constant, low thermal conductivity are some of know physical properties of ZrO$_2$. Some of the techniques used to produce thin films of ZrO$_2$ are sol gel, evaporation, sputtering and Chemical Vapor Deposition.

2.1.3 Hafnium Oxide

Hafnium oxide, HfO$_2$ is very similar to ZrO$_2$ in physical and chemical properties. The HfO$_2$ and ZrO$_2$ phases are isostructural, but there are some differences in the atomic positions and transition temperatures. For HfO$_2$, the monoclinic to tetragonal transition takes place between 1620 and 1650°C and tetragonal to cubic at 2700°C.

As expected, HfO$_2$ has the same excellent material properties as ZrO$_2$: extreme chemical and thermal stability, good electrical properties and a high refractive index. Thin films of HfO$_2$ can be made using Laser ablation, ion beam sputtering, sol-gel, ALD and CVD.
2.1.4 Aluminum Oxide

Aluminum Oxide, $\text{Al}_2\text{O}_3$ possesses strong ionic interatomic bonding giving rise to its desirable material characteristics. It can exist in several crystalline phases which all revert to the most stable hexagonal alpha phase at elevated temperatures. Its high hardness, excellent dielectric properties, refractoriness and good thermal properties make it the material of choice for a wide range of applications. $\text{Al}_2\text{O}_3$ films can be made using ALD, sputtering and sol gel processes.

2.2 Ferroelectric Materials

The second group of high dielectric constant materials consists of the "ferroelectric" thin films. A ferroelectric material exhibits an electric dipole moment even in the absence of an external electric field [16]. The physical properties of ferroelectric materials are related to dielectric, elastic, piezoelectric, pyroelectric, ferroelectric, optical and other parameters. Structural symmetry of a crystal affects the physical parameters of the ferroelectric material. Depending on the structural symmetry with respect to the point, crystals can be classified into 32 crystal classes, 11 of which have a center of symmetry. Of the remaining 21 noncentric crystal classes, all except one class exhibits electrical polarity when subjected to stress. This effect is termed as “piezoelectric effect” and is linear, with reversal of the stimulus resulting in a reversal of the response. Among the 20 piezoelectric crystal classes, 10 crystal classes have only one unique polar axis. Such crystals are called “polar crystals”, since they display spontaneous polarization or electric moment per unit volume. This spontaneous polarization is in general
temperature dependent, and the variation of the charge density can be detected by observing the
flow charge to and from the surfaces on change of temperature. This is the “pyroelectricity”
crystals that exhibit spontaneous polarization. Most pyroelectric crystals exhibit spontaneous
polarization, Ps in certain temperature range, and the direction of Ps can be reversed by an
external electric field. Such crystals are called “ferroelectric crystals”. If the material is
paraelectric at room temperature, it behaves very much like a normal dielectric material. The
Curie temperature depends on the composition of these ferroelectric materials. The dielectric
constant of bulk ferroelectric materials is in range of 1000 or more and that for thin film is in
range of 200-800 [20].

In recent years ferroelectric materials, such as Barium Strontium Titanate (Ba, Sr) TiO$_3$
Strontium Titanate (SrTiO$_3$) and Lead Titanate (PbTiO$_3$), have been widely investigated in a
variety of technologies that require high charge storage density materials in thin film devices.

2.2.1 Strontium Titanate (SrTiO$_3$)

Strontium Titanate behaves as a parelectric material at room temperature, but transforms
to tetragonal form above 105K [22]. The dielectric constant of this material ranges from 225 to
250. SrTiO$_3$ belongs to a family of compounds with the general formula ABO$_3$, where A is the
divalent ion and B is the quadrivalent ion [23]. The strontium titanate is the first material for
which the dielectric at low temperature was associated with a low frequency optical mode. At
low temperatures SrTiO$_3$ films exhibit superconductivity and quantum paraelectric behavior
[24]. SrTiO$_3$ films can be prepared by sol-gel, sputtering, laser ablation and metal-organic
solution methods.
2.2.2 Lead Titanate (PbTiO$_3$)

Lead Titanate has many useful properties like large piezoelectric, pyroelectric and electro-optic coefficients. Lead titanate based thin films including PbTiO$_3$ (PT) is a promising candidates for a lot of potential applications such as non-volatile memory, sensors, and more recently, optical waveguide devices. Several methods have been used for growing PbTiO$_3$ thin films including metal organic chemical-vapor deposition (MOCVD), Sol–gel process and pulsed-laser deposition (PLD).

2.2.3 Barium Strontium Titanate (BaSrTiO$_3$)

Among them BST is a promising dielectric material because of it unique mixture of high dielectric constant, good thermal stability, low leakage current density and low dielectric loss. BST thin films are potentially important material for variety of applications such as infrared pyro-electric sensors, dynamic random access memory, decoupling capacitors, microsensors, microwave devices and other integrated technologies. Thin film ferroelectrics offers more advantages over the bulk film for these applications.
In general, ferroelectric materials must achieve a crystalline or polycrystalline state in order to exhibit higher dielectric constants than paraelectrics. This may require anneal temperatures in the range of 500-700°C. This precludes their use on many common microelectronic substrates [2, 21] such as polymeric2 substrates, etc. In contrast, most paraelectric materials can also be deposited at low temperatures and are suitable for applications where the fabrication schemes demand low processing temperatures. In addition, paraelectric materials exhibit stable values of dielectric constants with respect to operating frequency, voltage and temperature [2, 21, 22]. General properties of ferroelectric and ferroelectric materials are compared in Table 2.2.
As a result, paraelectrics are more suitable for decoupling capacitors requiring minimum dispersion in the GHz range and other high-tolerance applications, such as filtering, timing, RF, wireless etc where predictable and constant capacitance is required. Ferroelectrics are better for high capacitance applications (operating at low frequencies) such as energy storage where high tolerance and stability is not important as long as minimum capacitance is provided. Currently ferroelectric materials are widely used in DRAM memory cells.

Thus high dielectric constant material such as BaSrTiO$_3$ is suitable candidates for embedded capacitor applications operating over wide range of frequencies (dc to GHz range) and voltages. In the following section, the general properties of the dielectric films that can be sputtered and used for embedded capacitors have been discussed. The next section discusses the deposition methods that can be used to deposit these dielectric films.
Table 2.1 Dielectric constants of important paraelectric and ferroelectric dielectric materials

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Composition</th>
<th>Dielectric Constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polyimide</td>
<td>Organic</td>
<td>3.6</td>
</tr>
<tr>
<td>Silicon Oxide</td>
<td>SiO₂</td>
<td>3.9</td>
</tr>
<tr>
<td>Silicon Nitride</td>
<td>Si₃N₄</td>
<td>6.9</td>
</tr>
<tr>
<td>Aluminum Nitride</td>
<td>AlN</td>
<td>9</td>
</tr>
<tr>
<td>Aluminum Oxide</td>
<td>Al₂O₃</td>
<td>9.1</td>
</tr>
<tr>
<td>Silicon Carbide (3C &amp; 6H)</td>
<td>SiC</td>
<td>9.7</td>
</tr>
<tr>
<td>Amorphous Tantalum Oxide</td>
<td>Ta₂O₅</td>
<td>25</td>
</tr>
<tr>
<td>Barium Strontium Titanate</td>
<td>BaSrTiO₃</td>
<td>Up to 1000</td>
</tr>
<tr>
<td>Lead Zirconate Titanate</td>
<td>PbZrₓTi₁₋ₓO₃</td>
<td>Up to 2000</td>
</tr>
<tr>
<td>Barium Titanate</td>
<td>BaTiO₃</td>
<td>Up to 5000</td>
</tr>
</tbody>
</table>
Table 2.2 Comparison of Paraelectric & Ferroelectric dielectrics

<table>
<thead>
<tr>
<th>Property</th>
<th>Paraelectrics</th>
<th>Ferroelectrics</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\varepsilon_r$ (Dielectric Constant)</td>
<td>2-50</td>
<td>From ~15 up to 1000’s</td>
</tr>
<tr>
<td>$\varepsilon_r$ vs. T</td>
<td>Little dependence, $&lt; 550$ ppm/°C</td>
<td>Highly dependent on T due to crystal phase transitions and ion mobility</td>
</tr>
<tr>
<td>$\varepsilon_r$ vs. Frequency</td>
<td>Little dependence</td>
<td>Decreases significantly above a few GHz</td>
</tr>
<tr>
<td>$\varepsilon_r$ vs. Bias</td>
<td>No Dependence</td>
<td>Decreases with dc bias</td>
</tr>
<tr>
<td>$\varepsilon_r$ vs. Film Thickness</td>
<td>No Dependence</td>
<td>Highly dependent due to thickness dependent crystal structures</td>
</tr>
<tr>
<td>Dielectric fatigue</td>
<td>None</td>
<td>$\kappa$ can decrease significantly with cycles and time</td>
</tr>
<tr>
<td>$\varepsilon_r$ vs. Film structure</td>
<td>Little or no dependence</td>
<td>Must be crystalline to exhibit high dielectric constant</td>
</tr>
<tr>
<td>Cure requirements</td>
<td>None</td>
<td>500-700°C (typically in O$_2$)</td>
</tr>
</tbody>
</table>
CHAPTER THREE: THIN FILM DEPOSITION TECHNIQUES

3.1 Overview of Deposition Techniques

Mainly, techniques for the thin film deposition can be classified into either purely physical, such as evaporative methods, or purely chemical such as gas and liquid phase chemical processes. Physical methods cover deposition techniques which depend on the evaporation or ejection of material from a source, i.e. evaporation or sputtering, whereas chemical methods depend on a specific chemical reaction [25]. Apart from the above processes, there are combined physical and chemical reactions based on reactive sputtering and glow discharge processes; these overlapping processes can be grouped as physical-chemical methods.

3.2 Chemical Deposition Techniques

3.2.1 Chemical Vapor Deposition

Chemical Vapor Deposition (CVD) is a process where the substrate is placed directly inside a reactor or a chamber to which different gases are supplied. The basic principle of the process is that a chemical reaction takes place between the process gases and a thin film or a powder is formed on the substrate. The two important CVD techniques used in the semiconductor industry are Plasma Enhanced Chemical Vapor Deposition (PECVD) and Low
Pressure Chemical Vapor Deposition (LPCVD). LPCVD are performed at high temperatures, usually greater than 600°C. The layers deposited with this process have excellent uniformity of thickness and material characteristics. The main problems with the process are the relative slower deposition rate and high deposition temperature. PECVD deposition causes the reaction or the process gases to decompose via the electrical discharge. This allows the PECVD process to operate at lower temperatures (down to 300°C) thanks to the additional energy supplied to the gas molecules by the plasma in the reactor. However, the film quality tends to be inferior to the films deposited at higher temperatures.

3.2.2 Thermal Oxidation

Thermal Oxidation is one of the most commonly used deposition technique. Films can be formed on a larger variety of metal substrates by heating them in gases of the required type (oxygen for oxides, nitrogen for nitrides, CO carbides) [19]. The uniqueness of this deposition technology is that the growth of the film takes place by diffusion of oxygen into the substrate and consuming the substrate during processing. Which means the film growth is actually downwards into the substrate. The films obtained, however, are limited in thickness because the reactions are generally self-limiting and become very slow as the film thickness increases. To speed up the process the temperature of the process is raised to 800°C-1100°C. This process is naturally limited to materials that can be oxidized, and it can only form films that are oxides of that material.
3.2.3 Anodisation

Anodisation (more formally called as Anodic oxidation) can be done using aqueous or non-aqueous solution or by using an oxygen plasma. In aqueous phase anodization, the substrate is immersed in an electrolyte solution and oxidation is carried out using a fixed current density and potential. The main growth mechanism of the oxide is due to high field ionic conduction in the oxide. The main advantage of this process is that the oxide can be grown at room temperature and it is homogeneous with reproducible thickness. However the anodic oxide formed by this method can contain impurities from the electrolyte solution which increase the leakage current and hence degrade electrical performance. In non aqueous (gas) phase anodization, the electrolyte solution is replaced by oxygen plasma. The plasma is created using a parallel plate structure with an ion cathode as the source of negative ions. When the substrate is floating with respect to the plasma, it is called plasma oxidation and when the substrate is positively biased it is called plasma anodization. High oxidation rates can be achieved using this technique, but the oxides produced contain significant density of defects which need to be removed by annealing.

3.2.4 Atomic Layer Deposition

The Atomic Layer Deposition (ALD), previously known by the name Atomic Layer Epitaxy (ALE), is a deposition method by which precursor gases or vapors are alternately pulsed on to the substrate. Chemical reaction takes place at the surface of the substrate due to the introduction of the precursor gases. These chemical reactions at the substrate surface are carried out in a controlled manner. This allows the uniform distribution of active species on the
substrate. The reactants are injected in the reactor in the form of vapor pulses. In between the two reactant pulses, the reactor is flushed. Hence ALD can be used to get very uniform films. The thickness of the films depends on the number of reactant cycles used. Low deposition rate is the main drawback of this method.

3.3 Physical Deposition Techniques

3.3.1 Evaporation

Evaporation techniques are extensively used in the preparation of thin dielectric films and a variety of materials in either oxygen ambient or directly in an extremely clean environment in the vacuum chamber [26]. Evaporation rate can vary with respect to the material used and the distance between the substrate and the source. The uniformity and step coverage in the evaporation is poor compared to sputtering.

3.3.2 Sputtering

Sputter deposition (more formally called sputtering) is a relatively simple process which involves bombardment of a metal target source by energized particles, typically Ar+ in plasma environment. In sputtering process, unlike many other vapor phase techniques there is no melting of the material. Dislodging of metal atoms from the target takes place and deposits onto an adjacent substrate. The adhesion of the sputtered films is typically much better than a evaporated metal, because of the increased energy imparted to sputtered metal atoms. However, undesirable
substrate heating is a common problem, but can be controlled by the use of DC magnetrons to confine electrons in the plasma. Sputtering deposition rates are much lower than those for evaporation and source utilization can be irregular due to uneven flux distribution.

Sputtered metal atoms are knocked free from the source surface is essentially random directions, resulting in a conformal deposited film, with good step coverage of features. Uniformity of the sputtered film is directly related to the relative sizes of the source and substrate and the throat distance between them. Very large substrates are typically difficult to sputter coat with uniform films. Contamination of the substrate surface can degrade adhesion and can be removed by ion milling or RF sputtering. These processes ablate several hundred Å of the substrate surface prior to deposition, removing organic contaminants and may also improve adhesion through surface roughening or an increase in the surface energy of the substrate. Figure 3.1 shows how the impact of an atom or ion on a surface produces sputtering from the surface as a result of the momentum transfer from the in-coming particle.

Figure 3.1  Basic sputtering process showing how an energized atom sputters the atom from the target [3]
The sputter yield, $Y$, is the ratio of the number of emitted particles to the number of bombarding ones [2].

$$Y = \frac{\text{(Number of ejected particles)}}{\text{(Number of incident particles)}} \quad (3.1)$$

Sputtering techniques are based on the cathodic erosion due to the bombardment of ionized gases form a plasma discharge. Fig. 3.2 shows the basic schematic for a DC sputtering system. As shown in Fig. 3.3 Ions from the plasma are attracted towards the target of the material to be deposited, the ions strike the target physically knocking the atoms loose and the target atoms then land on the wafer.

Out of the numerous techniques available today for depositing thin films, sputtering is one of the most versatile techniques to prepare thin films of almost any material -metal or dielectric. Some of the many important advantages, sputtering has over other methods are high uniformity of thickness of the deposited films, good adhesion to the substrate, better reproducibility of films, ability of the deposit to maintain the stoichiometry of the original target and relative simplicity of film thickness control.
Sputter guns create low pressure plasma by bombarding an inert gas (typically argon) contained at 1 to 30 millitorr in a vacuum chamber. This process extracts energetic ions which accelerate toward the cathode target, striking it with kinetic energy up to several hundred eVolts. Energy transfer then ejects material from the target with approximately 90% leaving as neutral atoms and 10% as ions. Gas phase collisions between target atoms and argon atoms scatter the ejected material into a distributed cloud. As the cloud migrates towards the substrate, the randomized approach angles result in deposition of a uniform film, even on surfaces that have micron-sized vertical structures.
3.4 Glow Discharge Technology

3.4.1 DC Diode Sputtering

DC diode sputtering is the oldest technique used for sputter deposition. This is a simplest kind of plasma device, a diode, simply an anode and cathode placed inside a vacuum system. Figure 3.4 shows a simple diode sputtering device. Under the right conditions, with adequate gas pressure, the gas will breakdown into a plasma discharge. The potential of the plasma due to this discharge is spatially uniform and is slightly higher than the anode potential. A dark space or
sheath with very large electric field is created near the cathode. Ions are accelerated rapidly across the sheath and strike the cathode. Due to this collision, which causes sputtering, secondary electrons are emitted from the surface of the target. These electrons are accelerated back across the dark space where they gain energy, which is used to form more ions to sustain the discharge.

Figure 3.4 Shows a simple dc diode sputtering system

Presently this process is not used much because of its high operating pressures. The higher pressures not only present problems for the vacuum pumps but also results in a severe rate and efficiency loss due to gas phase scattering of the sputtered material.
3.4.2 RF Diode Sputtering

Visually an rf diode and dc diode are the same, except for an rf diode device a high frequency operating power supply is used. 13.56 MHz is the frequency that is most commonly used. The rf diode operates slightly different than a dc diode for a small part of the rf cycle, the anode and cathode are electrically reversed. This eliminates the charge buildup on an insulating surface by providing an equal number of ions, then electrons, then ions, and so on. This allows the metals and insulators to be sputtered into the reactive environment. The advantage of the rf diode system is that the oscillation of the fields in the plasma results in additional electron motion within the plasma. The end result of enhancing the electron movement is that the plasma density of the rf diode is increased. This increased density results in higher ion current to the cathode and a faster sputtering process. An impedance matching circuit is required for the rf diode system to operate most efficiently. This matching circuit or network is used to optimize the transfer of power from the power supply. Figure 3.5 show the most commonly used matching network in an rf diode sputtering system.

3.4.3 Ion Beam Sputtering

This technique makes use of broad beam ion sources. One advantage of the technique is that the source term, the sputter target and the substrate are decoupled. This allows a high degree of independent control. The downside of the technique is that the broad beam ion sources themselves are somewhat fragile.
3.4.4 Magnetron Sputtering

DC and RF Magnetron sputter devices are crossed field plasma devices that not only reduces impedance and permits operation at relatively low pressure but also substantially reduces substrate bombardment. RF Magnetron sputter sources operate in much the same manner as DC Magnetron sputter sources. Magnetron based sputter tools operates at much lower pressure and deposits thin films at much higher rate than the diodes. A DC magnetron is basically a magnetically enhanced diode in which the spatial relationship of electric (E) and magnetic (B) fields is engineered to confine secondary electrons produced by Ar$^+$ bombardment on the target. The high deposition rates result from the high power that can be applied at nearly optimal target potentials. There are, however, some important complicating factors and the operating point for the RF magnetron source is generally located at a higher potential than that of the DC magnetron source. DC and RF magnetron sputtering techniques have been used for this thesis work. A brief description and physics of magnetron source is given in the next section.

3.5 Magnetron Source

Nowadays magnetron sputter sources are the most commonly used for sputtering. Magnetron sources can be classified with their construction geometry but the most common arrangement is the planar magnetron source. A planar magnetron source is a planar diode source with an array of magnets added behind the cathode (target) surface. The planar magnetrons have be designed for a variety of target shapes e.g., square, rectangle, wedge and circular. However,
the circular shape is widely used in IC production because it matches the circular geometry of the wafer. This circular pattern also lends itself to rotating the magnet arrays that are employed to improve the target utilization and uniformity. These magnets generate a magnetic field of around 50-500 gauss parallel to the target surface. A closed looped electron traps are formed in front of the target surface due to the combination of electric field and magnetic field. The drift of the electrons is in \(-E \times B\) direction due to “Hall Effect” but superposed on this drift is cycloidal motion as shown in Figure 3.5. The gyro radius of their orbits is given by

\[ \rho = \frac{mv_{\perp}}{qB} \]  

(3.1)

where \(m\) and \(q\) are the mass and charge on the electron respectively and \(B\) is the magnetic field, and \(v_{\perp}\) is the component of the electron velocity that is perpendicular to the flux lines. This radius is typically of the order of a few millimeters or less for most sputtering systems. An electron encircles the lines of flux until it is scattered by another particle. Practically, a magnetron exists when the \(-E \times B\) path is closed and the electrons remain trapped for several trips around the loop.

This confinement of electrons results in enhanced ion bombardment and sputtering rates for both DC and RF discharges. In general, a magnetron discharge is much more efficient, with either DC or RF excitation, than one that does not utilize magnetic trapping.

For the most common magnet arrangement, the resulting shape of plasma is toroidal. This is due to the fact that ring of magnets confines the electrons in to an annular closed path, which in turn produces an annulus of intensified sputtering plasma. This results in a donut shaped erosion pattern on the target with only about 30% of the target being used. One way to increase target material utilization is to move the target with respect to magnets (swept field magnetron) during deposition. Other methods involve departing from the planar geometry and
changing the shape of the target and/or arrangement of the magnets so that the plasma bombards
the target more uniformly over its entire surface. The other alternative to the basic sputtering
setup is Ion beam sputtering. In this technique, a low voltage discharge is established within the
ion source. The entire source is biased to a high DC potential, on the order of 1 KV. An ion beam
is extracted from this source and directed onto a sputtering target, possessing a maximum kinetic
energy equal to the DC bias of the source.
Figure 3.5 The Planar Magnetron Arrangement (a) Annular design of magnetron and as a result of which an erosion groove is formed on the surface of the target. (b) For both DC and RF sputtering, a static magnetic flux is created perpendicular to the electric field. (c) The electrons drift in the -E x B direction executing a cycloidal path.
3.6 Description of AJA Sputtering Machine

The magnetron sputtering system from AJA International is an ultra high vacuum system with three 3" magnetron sources inside an 18" diameter and 17" high cylindrical stainless steel chamber. It also consists of a rotating substrate holder a sample insertion load-lock chamber with a magnetic transfer arm. The substrate holder is fitted with a motor that can rotate the holder at variable speeds that allows a uniform film deposition.

The AJA system has a multiple gas injection configuration. All the process gases are injected to the vacuum chamber through the lamp heater assembly except the argon in injected from the bottom of the main process chamber. At base pressure of about 2 x 10⁻⁸ Torr is achieved by pumping the system using a turbo pump backed by a mechanical pump. The load lock vacuum is in the range of low 10⁻⁶ Torr. The main vacuum chamber is water cooled. Three different targets can be installed at a time in the three guns with a +/- 45° in-situ rotation capability. The system can be operated in two modes of power supplies DC and RF, with a maximum power output of 500W. A lamp based heater above the substrate holder can be used for heating the substrate from ambient to 600°C.

Deposition of dielectric films like BaSrTiO₃ and Al₂O₃ from composite targets requires an RF power source to deliver energy to the argon atoms. Electrically conductive materials such as metals can be deposited by a dc power source in which the target acts as a cathode and the substrate(s) are mounted on a system anode, thus directing the deposited material from target to substrate. The other way to deposit dielectric films is to use DC reactive sputtering in which a reactive gas in addition to Argon is injected in the chamber.
Figure 3.6 (a) AJA Sputtering System schematic (b) AJA sputtering system main chamber (open) (c) View inside the main chamber showing the three target guns (shutters open)
3.7 Presputtering

Generally, presputtering is done prior to film deposition to clean and equilibrate the target surface. It has been found that if the target has been in frequent use, a few minutes of presputtering time is necessary for the metal target. For pure metal targets, oxides on the surface are removed, the target is brought to thermal equilibrium and the system is out gassed. Due to sputtering of oxides and breakdown of gaseous contaminants (especially H₂O), the discharge current is increased. It gradually decreases when the contaminants are removed from the system and/or covered up with film material. Presputtering can be terminated once the discharge current falls to the normal value.

3.8 Sputtering of Tantalum and Dielectric Films

The optimum process conditions to deposit stoichiometric films that exhibit superior and reliable electrical properties while maintaining suitable deposition rates is one of the major challenges in depositing the dielectric films. RF sputtering BST films were deposited for this thesis work. Tantalum was deposited using DC sputtering. A very low deposition rate is the major issue with the RF sputtering. The low deposition rate can be overcome by using reactive DC sputtering from metallic targets in a mixed gas environment of argon with a small percentage of oxygen.

Number of test runs and design of experiments are conducted to determine the optimum deposition condition for tantalum and BST films.
3.8.1 Choosing the Sputtering Gas

It is much easier to ionize atoms when they are in gaseous state, and easy to accelerate ions to the energies. Inert gases are chosen for this purpose as they do not react with the target or the films. Argon is the gas of choice for sputtering as it is cheaply available in high purity (99.99%).

3.8.2 Choosing the Gas Pressure

A vacuum gas enables one to control the operating pressure inside the sputtering system. Operating pressure limitations are imposed by the requirements of both glow discharge and film deposition. The glow discharge sets the lower limit. The discharge is sustained by the electrons making collision in the gas. The number of ionizing collisions will decrease with decreasing the gas density or pressure. A different problem arises from the high density or pressure because when electrons undergo collision, the sputtered material from the target collides with the gas atoms on its way to the substrate, and will increase the gas pressure. The result of the collision is to deflect the sputtered atom, and hence decrease the deposition rate.

For AJA sputtering system, Ar gas pressure of 5 mTorr was found to be optimum for deposition of films using both DC and RF sputtering. Ta films for electrodes were deposited using DC sputtering at a power of 200W at 300°C. The films were then annealed inside the main chamber using the substrate heater to ~500°C to remove any stresses induced in the film during the deposition. It was found that unannealed Ta films peeled off due to residual stress in the films.
For RF sputtering of BST and Al$_2$O$_3$ films, films were deposited at a RF power of 300W at 400°C with argon flow rate of 20scm at 5 mTorr pressure. It was found that annealing of RF sputtered films did not yield any improvement in the quality of the films.
CHAPTER FOUR: EXPERIMENTS AND RESULTS

4.1 Substrate Preparation

The substrates used for the experiments were p-type Silicon <100> wafers with the sheet resistivity in the range of 7-14Ω.cm. Native oxide on the substrate was removed by immersing the wafers in a 9:1 buffered oxide etch solution for 30 seconds. In order to prevent the contamination of the semiconductor equipment and to obtain high performance and good reliability semiconductor devices the contaminants present on the surface of the Si wafers, or accumulated during the process have to be removed. SC1 and SC2 cleaning (modified RCA cleaning) was used to remove organic, ionic and heavy metal contaminants from the silicon wafers.

The SC1, SC2 procedure has two major steps executed sequentially:

2. Removal of ionic and heavy metal atomic components using a solution of 6:1:1 H₂O/H₂O₂/HCl solution.

The SC1 solution was prepared by heating the solution of NH₄OH and H₂O in the ratio of 6:1 till a temperature of 80°C. 1 part of H₂O₂ was then added to the solution just prior to immersing the Si wafers. The wafers were cleaned for 10 minutes. This was followed by a DI water rinse for 5 minutes.

SC2 solution was prepared by heating the HCl and H₂O in the ratio 6:1 to 80°C. H₂O₂ was added just prior to immersing the SC1 cleaned wafers in the solution. A 10 minutes SC2 clean was
followed by 5 minutes DI rinse, after which the wafers were blown dry using a N$_2$ gun. The cleaned Si substrates were then stored for further processing.

### 4.2 Options for electrode material

#### 4.2.1 Tantalum as an Electrode Material

Tantalum is used as an electrode material for thin film capacitors in miniaturized electrical circuitry. Tantalum based capacitors provide higher volumetric capacitance with high reliability characteristics over a wide range of temperatures ranging from -55°C to 125°C. Moreover, Ta is a refractory metal and is corroded only by reagents that attack the oxide film on its surface including strong alkalis, fuming sulfuric acid containing free SO$_3$ or SO$_2$ and HF. The resistivity of Ta has been compared to other metals used as capacitor electrodes in Table 4.1.
Table 4.1 Comparison of electrical resistivity of different metals used as electrodes

<table>
<thead>
<tr>
<th>Metal</th>
<th>Bulk Resistivity (µΩ.cm)</th>
<th>Thin film resistivity (µΩ.cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mo</td>
<td>5.2</td>
<td>7.5-12</td>
</tr>
<tr>
<td>Ag</td>
<td>1.6</td>
<td>1.6</td>
</tr>
<tr>
<td>Au</td>
<td>2.4</td>
<td>4.1</td>
</tr>
<tr>
<td>Al</td>
<td>2.65</td>
<td>2.7</td>
</tr>
<tr>
<td>Cu</td>
<td>1.7</td>
<td>2.1</td>
</tr>
<tr>
<td>Ta</td>
<td>13</td>
<td>24-50</td>
</tr>
<tr>
<td>W</td>
<td>5.6</td>
<td>10-14</td>
</tr>
</tbody>
</table>

For this thesis, sputtered Ta thin films have been used as top and bottom electrodes to develop capacitors that can withstand very low temperatures.
4.3 Fabrication of the Test Devices

4.3.1 Sputtering Parameters

Approximately 1800Å of Al₂O₃ barrier film was deposited on the cleaned silicon substrates. This film was used as a barrier layer to isolate the substrate from bottom Ta electrode. 2000Å of bottom Ta electrode was sputtered on the barrier Al₂O₃ layer. For both the Al₂O₃ and Ta sputtering Ar gas was used as the carrier gas. 2000Å BST film was deposited on the Ta electrode at 400,450,500 and 550°C substrate temperatures. 1000Å BST films were deposited at 400 and 500°C substrate temperatures. For both 1000 and 2000Å BST films the process gas was 10% O₂ + 90% Ar at 5mTorr pressure. Table 4.2 shows the sputtering process parameters used for fabricating the test vehicles.

Film microstructure and stoichiometry are of critical importance for dielectric thin films capacitors. In order to fabricate a high quality thin film with a good reproducibility these two properties have to be carefully controlled. Nature of the substrate, deposition temperature, deposition process gases, system vacuum and post deposition processing has a strong influence on the quality of the films deposited. Even a small deviation from stoichiometry in the film can affect the film property and increase the leakage current properties of the dielectric. It also may lead to some inferior dielectric and insulating properties issues. Defects such as pinholes, voids and porosity tend to decrease the dielectric properties and increase the dielectric loss of the film. Also, incorporation of contamination (such as carbon residue) into the growing film can adversely affect material properties. A dense and smooth microstructure is another important
requirement for obtaining optimum dielectric properties. The surface analysis of the dielectric films was done using a VEECO NT 3300 Optical profilometer shown in Figure 4.1.

Table 4.2 Sputtering process parameters

<table>
<thead>
<tr>
<th>Sputtering process parameters</th>
<th>Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;</th>
<th>Ta</th>
<th>Ba0.5Sr0.5TiO&lt;sub&gt;3&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>250W RF</td>
<td>250W DC</td>
<td>180W RF</td>
</tr>
<tr>
<td>Pressure</td>
<td>5 mTorr</td>
<td>5 mTorr</td>
<td>5 mTorr</td>
</tr>
<tr>
<td>Ar flow rate</td>
<td>20 sccm</td>
<td>20 sccm</td>
<td>10% O&lt;sub&gt;2&lt;/sub&gt; + 90% Ar</td>
</tr>
<tr>
<td>Deposition Temperature</td>
<td>400°C</td>
<td>300°C</td>
<td>400, 450, 500 &amp; 550°C - 2000Å</td>
</tr>
<tr>
<td>Thickness</td>
<td>1800Å</td>
<td>2000Å</td>
<td>1000Å and 2000Å</td>
</tr>
</tbody>
</table>
4.4 Surface roughness measurements

Surface roughness of the dielectric films is an important factor in determining their reliability. Degradation in dielectric properties occurs when the thickness is reduced to the point that the surface roughness of the dielectric becomes comparable the film thickness. When the RMS roughness of the dielectric exceeds 20% relative to the film thickness then thin spots in the dielectric film can start to dominate the capacitance and leakage thus leading to premature breakdown of the thin film capacitors. The surface profilometry of the deposited films was done using VEECO NT3300 Optical profilometer. The NT3300 is a non-contact surface profiler which was used to measure the thickness and surface roughness of the sputtered dielectric and metal films. This profilometer uses two different technologies to measure a wide variety of surface heights. Phase shifting interferometry (PSI) is reliable for smooth surfaces and small
steps in which the height change between two adjacent points is not more than 160 nm [27]. The vertical resolution for PSI mode is 3Å for a single measurement and 1Å for multiple averaged measurements. Vertical scanning interferometry (VSI) allows measurement of rough surface profiles and steps up to a few millimeters high. The vertical resolution is 3nm for a single measurement and <1nm for averaged multiple measurements.

The average roughness and peak to valley roughness was measured for BaSrTiO$_3$ film. Average roughness ($R_a$) represents the two dimensional roughness average, the arithmetic mean of the absolute values of the surface departures from the mean plane.

\[
R_a = \frac{1}{MN} \sum_{j=1}^{M} \sum_{i=1}^{N} |Z_{ji}|
\]  

(4.1)

where M and N are the number of data points in the X and Y direction, respectively of the array, and Z is the surface height relative to the surface reference mean plane.

Peak to valley roughness ($R_t$), the maximum height of the surface is the vertical distance between the highest ($R_p$) and lowest ($R_v$) points as calculated over the entire dataset. It is defined by

\[
R_t = R_p + R_v
\]  

(4.2)
Table 4.3 Operational differences between PSI and VSI measurement

<table>
<thead>
<tr>
<th>Vertical Scanning Interferometry</th>
<th>Phase Shifting Interferometry</th>
</tr>
</thead>
<tbody>
<tr>
<td>Neutral Density filter for white light</td>
<td>Narrow bandwidth filtered light</td>
</tr>
<tr>
<td>Vertically scans- the objective actually moves through the focus</td>
<td>Phase-shift at a single point- the objective does not move.</td>
</tr>
<tr>
<td>Processes fringe modulation data from the intensity signal to calculate surface heights.</td>
<td>Processes phase shift data from the intensity signal to calculate surface heights</td>
</tr>
<tr>
<td>Primarily used to measure step heights</td>
<td>Primarily used to measure roughness of the films</td>
</tr>
</tbody>
</table>

The roughness measurements were made in PSI mode at a resolution using a 5X objective. The profilometer was calibrated using the mirror calibration sample before measurements were taken. The table 4.4 shows the measured values for BaSrTiO$_3$ film. Several measurements were made to check the accuracy of measurements.

4.5 Annealing Methods

During film growth, inter layers and specific grain structures are developed that cause serious problems of high leakage and low dielectric constant in thin films. Ferroelectric materials must achieve a crystalline or polycrystalline state in order to exhibit higher dielectric constants than paraelectric material. For crystallization anneal temperatures in the range of 500-700°C are required. Figure 4.2 shows the capacitor stack used for annealing.
Table 4.4 Roughness values for 2000Å BST films post anneal in Lindberg Furnace using different gas ambient at 575°C

<table>
<thead>
<tr>
<th>BST Deposition Temp</th>
<th>Measurement Mode</th>
<th>Ra(nm)</th>
<th>Rt(um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>No anneal</td>
<td>2.8558497</td>
<td>32.365535</td>
</tr>
<tr>
<td>400</td>
<td>100% N₂</td>
<td>52.22225</td>
<td>39.412638</td>
</tr>
<tr>
<td>400</td>
<td>100% O₂</td>
<td>3.3077603</td>
<td>73.44860967</td>
</tr>
<tr>
<td>400</td>
<td>10% O₂</td>
<td>2.8123997</td>
<td>58.31712867</td>
</tr>
<tr>
<td>450</td>
<td>No anneal</td>
<td>3.105328</td>
<td>61.47935</td>
</tr>
<tr>
<td>450</td>
<td>100% N₂</td>
<td>3.731453</td>
<td>176.3794</td>
</tr>
<tr>
<td>450</td>
<td>100% O₂</td>
<td>127.3588</td>
<td>7094.798</td>
</tr>
<tr>
<td>450</td>
<td>10% O₂</td>
<td>3.179595</td>
<td>98.12139033</td>
</tr>
<tr>
<td>500</td>
<td>No anneal</td>
<td>5.4638233</td>
<td>103.407624</td>
</tr>
<tr>
<td>500</td>
<td>100% N₂</td>
<td>62.970207</td>
<td>758.318329</td>
</tr>
<tr>
<td>500</td>
<td>100% O₂</td>
<td>76.628952</td>
<td>484.486504</td>
</tr>
<tr>
<td>500</td>
<td>10% O₂</td>
<td>81.517532</td>
<td>492.127838</td>
</tr>
<tr>
<td>550</td>
<td>No anneal</td>
<td>8.3400977</td>
<td>127.351797</td>
</tr>
<tr>
<td>550</td>
<td>100% N₂</td>
<td>98.147521</td>
<td>1445.00633</td>
</tr>
<tr>
<td>550</td>
<td>100% O₂</td>
<td>63.095162</td>
<td>954.098167</td>
</tr>
<tr>
<td>550</td>
<td>10% O₂</td>
<td>35.300946</td>
<td>958.596611</td>
</tr>
</tbody>
</table>
Post deposition annealing was performed on all the samples using PVD and Lindberg three zone furnace. PVD annealing was done inside the vacuum chamber of the sputtering machine. Furnace anneal was done using a three zone filament heating quartz tube furnace. Figure 4.3 (a) and (b) shows the PVD machine and Lindberg furnace used for annealing.

The annealing was performed in different gas ambient at 575°C for 20 minutes. Following are the gases that were used for annealing the BST films in PVD and furnace:

- 100% O₂
- 100% N₂
- 10% O₂ + 90% N₂
Figure 4.3 Shows the equipments used for annealing the BST films (a) PVD system (chamber open position) (b) Lindberg three zone furnace

In both the annealing equipment the temperature was ramped to 575°C at a rate of 25°C/min. PVD annealing was done after the BST deposition inside the vacuum chamber. In case of the Lindberg furnace the quartz tube was first flushed or purged with the annealing gas for 15minutes before the sample was placed inside the tube. Purging with the annealing gas evacuates the other gases inside the tube. After purging, the sample was placed inside the quartz tube and the temperature was ramped till the required annealing temperature (575°C) was attained. At this temperature the annealing was done for 20 minutes. Then the furnace was switched off and was allowed to cool down below 100°C. Once the temperature of the tube was below 100°C the annealing gas was turned off and the samples were slowly removed from the furnace. Pre annealing and post annealing roughness measurements were taken using optical profilometer.
4.6 Electrical Measurements

Thin film capacitors with the highest capacitance density and highest breakdown voltage are desired in most applications. However, a trade-off exists between these two properties of interest. Both breakdown voltage and capacitance density of a capacitor are determined by: (a) intrinsic material properties of the dielectric used in the capacitor, i.e., capacitor area and dielectric thickness. Figure 4.4 shows the MIM capacitor stack used for electrical testing.

Factors such as electrode-dielectric interface roughness, electrode metal diffusion into the dielectric etc., can further degrade the breakdown of the capacitors. Section 4.6.1 discusses the dielectric properties and section 4.6.2 discuses the electrical breakdown and leakage current density of the fabricated structures. Figure 4.5 shows the picture of the annealed samples which are ready for electrical testing.

Figure 4.4 Illustration of a Metal – Insulated – Metal stack used for electrical testing
Figure 4.5 shows the picture of the annealed samples which are ready for electrical testing.
A simplified circuit for a thin film capacitor is shown in the figure below.

\[ C = \frac{\varepsilon_0 \varepsilon_r A}{d} \]  

(4.3)

where \( C \) is the capacitance, \( \varepsilon_0 \) and \( \varepsilon_r \) are permittivities of the free space and that of the dielectric material respectively, \( A \) is the area of capacitor plates and \( d \) is the spacing between the electrode plates. Dissipation factor is a measure of the losses of the capacitor under AC operation and is given by

\[ DF = \frac{ESR}{X_c} \]  

(4.4)

For a multilayer capacitor, say with three layers having dielectric constants \( \varepsilon_{r1}, \varepsilon_{r2}, \varepsilon_{r3} \) with thickness \( d_1, d_2 \) and \( d_3 \) respectively as shown in Figure 4.6, the total capacitance is
\[
\frac{1}{C} = \frac{\varepsilon_0}{A} \left[ \frac{d_1}{\varepsilon_{r_1}} + \frac{d_2}{\varepsilon_{r_2}} \right]
\] (4.5)

Figure 4.8 shows the HP impedance analyzer used for testing the capacitance and dissipation factor.

Figure 4.7 (a) Simple parallel plate capacitor structure (b) Multilayer capacitor structure

Figure 4.8 HP impedance analyzer used for measuring capacitance and dissipation factor
4.6.2 Measurement of Leakage Current and Breakdown Voltage

Measurement of extremely low leakage currents is also an important requirement for a dielectric material in embedded capacitors. In order to measure the leakage current characteristics, a *dc* bias was applied to the parallel plates of the capacitor. A Keithley–6487 picoammeter/ voltage source (Figure 4.9) was used to measure the currents which are typically of the order of a few pico-amperes. The current densities were calculated by dividing the measured current by the area of the electrode as measured by an optical microscope. The dependence of leakage currents on the applied bias was measured by interfacing computer with the picoammeter.

Figure 4.9 Leakage current measurement test setup using Keithley 6487 Picoammeter/ Voltage Source. [27]
4.7 Results and Discussion

The top Ta electrode was deposited on all the annealed BST samples and electrical characterization (capacitance, dissipation factor and leakage current measurements) was done on all the samples. For the capacitance and dissipation factor measurements, the frequency was swept from 10Hz to 10MHz. The leakage current and breakdown voltage measurements were done with a voltage sweep from 0V till an avalanche breakdown ($V_{BD}$) occurred. The voltage sweep was performed with a 0.5V increment. Capacitance density (nF/mm$^2$) Vs annealing gas, $V_{BD}$ (V) Vs annealing gas, current density (A/cm$^2$) Vs annealing gas plots were plotted for the all the samples annealed in both furnace and PVD. Figure 4.10 shows the capacitance density plots at 100Hz for furnace and PVD annealed 2000Å BST deposited at 400°C and PDA at 575°C.

![Graphs showing capacitance density vs annealing gas ambient plots](image)

Figure 4.10 Capacitance density Vs annealing gas ambient plots (2000Å BST, 400°C deposition temperature for (a) Furnace (b) PVD)
From the plots it can be observed that the capacitance density of the furnace annealed sample is lower than the PVD annealed sample.particularly the 10% O\textsubscript{2} annealed PVD sample has highest capacitance. Figure 4.11 shows the leakage current density plot of 2000 Å BST, 400°C deposition temperature for furnace and PVD samples. Leakage current density for 10% O\textsubscript{2} furnace annealed sample is less than $10^{-4}$ A/cm\textsuperscript{2} while as the leakage current density of the 10% O\textsubscript{2} PVD annealed sample is in milliamps range. The average breakdown voltage of the 10% O\textsubscript{2} furnace annealed sample is ~ 50V. Figure 4.12 and 4.13 shows the $V_{BD}$ plot and average roughness plots with respect to annealing gas of 2000 Å BST, 400°C deposition temperature for furnace and PVD annealed samples.

![Figure 4.11 Current density Vs Annealing gas ambient plots (2000Å BST, 400°C deposition temperature for (a) Furnace (b) PVD)](image)

Figure 4.11 Current density Vs Annealing gas ambient plots (2000Å BST, 400°C deposition temperature for (a) Furnace (b) PVD)
Figure 4.12 Breakdown Voltage ($V_{BD}$) Vs Annealing gas ambient plots (2000Å BST, 400°C deposition temperature for (a) Furnace (b) PVD)

Figure 4.13 Average roughness ($R_a$) Vs Annealing gas ambient plots (2000Å BST, 400°C deposition temperature for (a) Furnace (b) PVD)
From the surface roughness plots in Figure 4.14 it can be seen that the 100% O2 anneal sample has a better average surface roughness (Ra) ~ 3.3 nm compared to that of 10% O2 anneal sample which is 7.7 nm.
Figure 4.14 Surface roughness analysis pictures of 2000Å BST, 400°C deposition temperature, Furnace annealed in (a) 100% O2 (b) 10% O2

From the capacitance and the breakdown voltage plots it can be observed that at 400°C deposition the 10% or partial oxygen anneal give a good capacitance both in a PVD and furnace anneal. But the leakage current is high for partial anneal sample, where it is opposite for a 100% annealed sample compared to 10% O2 annealed sample.
Figure 4.15 Capacitance Density (nF/mm²) Vs Annealing gas ambient plots 2000Å BST, 450°C deposition temperature for (a) Furnace anneal (b) PVD anneal

Figure 4.15 shows the capacitance density plot with respect to annealing gas of 2000 Å BST, 450°C deposition temperature for furnace and PVD anneal sample. From the plot 100% O₂ furnace annealed sample has the lowest capacitance ~ 2 nF/mm² where the 10% O₂ furnace annealed sample has a capacitance density of ~ 6nF/mm². Similarly the partial O₂ PVD annealed sample has a better capacitance density compared to 100% O₂ and 100% N₂ PVD annealed samples. The capacitance density of both the PVD and furnace annealed sample deposited at 450°C is lower than the 400°C deposition sample. There is an increase in the breakdown voltage of the 450°C compared to the 400°C deposition sample.
Figure 4.16 Breakdown Voltage Vs Annealing gas ambient plots 2000Å BST, 450°C deposition temperature for (a) Furnace anneal (b) PVD anneal

From the breakdown voltage plot in figure 4.16, the 100% O₂ furnace annealed sample has the better average breakdown voltage of ~15V compared to all other gas annealing in both furnace and PVD annealing. No data was obtained from the 450°C, 100% N₂ PVD annealed sample because the sample got blistered after annealing in the PVD machine. The blistered BST film can be clearly seen in figure 4.17.
Figure 4.17 Surface roughness analysis picture showing the blistered 2000Å BST film, 450°C deposition temperature annealed in 100N₂ in PVD

Figure 4.18 Current Density (A/cm²) Vs Annealing gas ambient plots 2000Å BST, 450°C deposition temperature for (a) Furnace anneal (b) PVD anneal
Figure 4.19 Average Roughness Ra (nm) Vs Annealing gas ambient plots 2000Å BST, 450°C deposition temperature for (a) Furnace anneal (b) PVD anneal

Figure 4.18 and 4.19 shows the current density and the average roughness plots with respect to the annealing gas for the 450°C BST deposition samples annealed in PVD and furnace. Plots show that the 100% N₂ and partial O₂ annealed sample has higher leakage current density in range of $10^{-6}$ A/cm². Comparing to 400°C sample the 450°C BST deposition sample has a lower leakage current density and better breakdown voltage.
Figure 4.20 Capacitance Density (nF/mm²) Vs Annealing gas ambient plots 2000Å BST, 500°C deposition temperature for (a) Furnace anneal (b) PVD anneal

Figure 4.21 Current Density (A/cm²) Vs Annealing gas ambient plots 2000Å BST, 500°C deposition temperature for (a) Furnace anneal (b) PVD anneal
Figure 4.22 Breakdown Voltage (V) Vs Annealing gas ambient plots 2000Å BST, 500°C deposition temperature for (a) Furnace anneal (b) PVD anneal

Figure 4.23 Average Roughness (Ra) Vs Annealing gas ambient plots 2000Å BST, 500°C deposition temperature for (a) Furnace anneal (b) PVD anneal
Figures 4.20, 4.21, 4.22 and 4.23 show the capacitance density, current density, breakdown voltage and average surface roughness with respect to different annealing gas for 2000Å BST, 500°C deposition temperature sample annealed in furnace and PVD.

Figures 4.24, 4.25, 4.26, 4.27 show the capacitance density, current density, breakdown voltage and leakage current plots with respect to different annealing gases for 2000Å BST, 550°C deposition temperature annealed in PVD and furnace.

Figure 4.24 Capacitance Density (nF/mm²) Vs Annealing gas ambient plots 2000Å BST, 550°C deposition temperature for (a) Furnace anneal (b) PVD anneal
Figure 4.25 Current Density (A/cm²) Vs Annealing gas ambient plots 2000Å BST, 550°C deposition temperature for (a) Furnace anneal (b) PVD anneal

Figure 4.26 Breakdown Voltage Vs Annealing gas ambient plots 2000Å BST, 550°C deposition temperature for (a) Furnace anneal (b) PVD anneal
PVD annealed sample in 100% O$_2$ has an average capacitance of ~ 15nF and an average breakdown voltage of 68V compared to all other samples. The furnace annealed 100% O$_2$ sample has an average breakdown voltage of ~ 119V where as the average capacitance is in range of ~ 2 nF. The drop in the overall capacitance of the 550°C BST deposition sample annealed in furnace can be due to the formation of the interfacial sub Ta$_x$O$_y$ layer between the bottom electrode and the BST film. The formation of the interfacial layer reduces the capacitance of the dielectric film. The oxide of tantalum starts to form above 500°C. This is evident from the breakdown voltage plots. Because the 550°C, 100% O$_2$ furnace annealed sample has the highest $V_{BD}$ voltage compared to all other deposition temperature samples. Formation of the tantalum oxide at 550°C is aided by the excess oxygen diffused through the BST film to the bottom electrode. Figure 4.28 shows the average capacitance graph with respect to frequency of
500°C, 2000Å BST films for (a) furnace anneal and (b) PVD anneal. At 100 Hz the capacitance of the BST film under all different annealing gas ambient have a high value compared to other frequencies. The capacitance above 100 Hz till 100 KHz the value is steady and it increases after 100 KHz. The same trend is can be observed in 550°C sample as shown in Figure 4.29 (a) and (b).
Figure 4.28 Average Capacitance Vs Frequency graphs 2000Å BST, 500°C deposition temperature for (a) Furnace anneal (b) PVD anneal
Average Capacitance Curves

- No anneal
- 550°C - 100% N2 anneal
- 550°C - 100% O2 anneal
- 550°C - 10% O2 anneal

(a)
Figure 4.29 Average Capacitance Vs Frequency graphs 2000Å BST, 500°C deposition temperature for (a) Furnace anneal (b) PVD anneal
Figure 4.30 Leakage current Vs Frequency graphs 2000Å BST, 550°C deposition temperature for
(a) PVD (b) Furnace anneal
CHAPTER FIVE: CONCLUSION

In this thesis, Barium Strontium Titanate dielectric films were sputter deposited and characterized for material and electrical properties. The PVD and Lindberg furnace annealing effects on the properties of the BST film were compared. The following were the main highlights and conclusions from this work.

Since the fabricated capacitors have to be used for very low temperature applications, Ta was used as an electrode for the fabricated capacitors due to its low thermal coefficient and superior properties at low temperatures.

From the breakdown voltages and current density plots it is clear that the furnace annealing is better than the PVD annealing. Current density of $<10^{-6}$ A/cm$^2$ was obtained for sputtered BST films. The breakdown voltage was in the range of 0.5 to 4 MV/cm at leakage current of $10^{-6}$A/cm$^2$. The capacitance density of the PVD annealed of 2000A sample shows high values in range of thousands. This shows that there is a difference between the PVD and Lindberg furnace anneal. This may be due to the fact that the annealing performed under PVD are subjected to partial pressure of the ambient gases, where as the furnace anneal is done under atmospheric pressure conditions. It was found that, with the deposition temperature in range of 500C and 550C followed by a post deposition annealing in O$_2$ ambient increases the formation of sub oxides of Ta$_{x}$O$_{y}$ on the electrode layer which contributes to the increased breakdown strength of the film. Also the capacitance density of the film was very low compared to the films deposited 400C and 450C. This is evident from source that the tantalum forms tantalum oxide.
above 500°C. It was found that adding an additional TaₙOₙ interfacial layer have a significant impact on the electrical properties of the stack.

For future work, other electrode materials with lower resistivity than tantalum such as Copper or Platinum can be studied and the electrical properties of BST can be compared with the present BST films for embedded capacitors. Other ferroelectric films can be studied under the same conditions and the results can be compared with the present BST results. The formation of the interfacial layer between the tantalum electrode and the BST can be prevented by introducing an oxygen barrier layer such as TiAl between BST and the bottom electrode. Some initial studies on TiAl cosputtered alloy film for oxygen barrier layer. Studies performed using TiAl barrier layer gave a poor quality capacitor, due to the formation of pinholes and defects during PDA. More study has to be done to improve the TiAl properties for getting a good oxygen barrier layer.


5. T. Kim, “Lead zirconate titanate (pzt) based thin film capacitors for Embedded passive applications” dissertation, Department of Material Science, North Carolina State University.


