Modeling And Simulation Of Long Term Degradation And Lifetime Of Deep-submicron Mos Device And Circuit

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MODELING AND SIMULATION OF LONG TERM DEGRADATION
AND LIFETIME OF DEEP-SUBMICRON MOS
DEVICE AND CIRCUIT

by

ZHI CUI

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Science
in the Department of Electrical & Computer Engineering
in the College of Engineering & Computer Science
at the University of Central Florida
Orlando, Florida

Spring Term
2005

Major Professor: Juin. J. Liou
ABSTRACT

Long-term hot-carrier induced degradation of MOS devices has become more severe as the device size continues to scale down to submicron range. In our work, a simple yet effective method has been developed to provide the degradation laws with a better predictability. The method can be easily augmented into any of the existing degradation laws without requiring additional algorithm. With more accurate extrapolation method, we present a direct and accurate approach to modeling empirically the 0.18-µm MOS reliability, which can predict the MOS lifetime as a function of drain voltage and channel length. With the further study on physical mechanism of MOS device degradation, experimental results indicated that the widely used power-law model for lifetime estimation is inaccurate for deep submicron devices. A better lifetime prediction method is proposed for the deep-submicron devices. We also develop a Spice-like reliability model for advanced radio frequency RF MOS devices and implement our reliability model into SpectreRF circuit simulator via Verilog-A HDL (Hardware Description Language). This RF reliability model can be conveniently used to simulate RF circuit performance degradation
ACKNOWLEDGMENTS

At first, I would like to gratefully acknowledge the enthusiastic supervision of my
professor Dr. J. J. Liou during this work.

I specially thank Dr. Yun Yue for the technical support and discussion.

I thank my dissertation committee for their interest and time: Dr. J.J. Liou, Dr. Kalpathy B.
Sundaram, Dr. Takis C. Kasparis, Dr. Thomas Xinzhang Wu, and Dr. Yun Yue.

I am grateful to all my friends from Micron electronic Lab: Xiaofang Gao, Ji Chen, Hao
Ding, Yue Fu, Javier Salcedo, Lifang Lou, and Xiang Liou.

Finally, I am forever indebted to my parents and my wife for their understanding, endless
patience and encouragement when it was most required.
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1. INTRODUCTION

1.1 Introduction

Lilienfeld and Heil conceived the insulated-gate field-effect transistor in the 1930s. An insulated-gate transistor is distinguished by the presence of an insulator between the main control terminal and the remainder of the device. Ideally, the transistor draws no current through its gate. This is sharp contrast to bipolar junction transistors that require a significant base current to operate. Unfortunately, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) had to wait nearly 30 years until the 1960s when manufacturing advances made the device a practical reality. Since then, the explosive growth of MOSFETs in electronics became ever more prevalent when “complementary” types of MOSFET devices were combined by Wanlass in the early 1960s to produce logic that required virtually no power except when changing state. MOSFET processes that offer complementary types of transistors are known as Complementary Metal Oxide Semiconductor (CMOS) processes, and are the foundation of the modern commodity electronics industry.

The dimensions of metal-oxide-silicon field effect transistors (MOSFETs) have been decreasing due to the continuous demand for higher packing densities and faster circuit speeds. Hot-carrier induced degradation of MOS devices has become more severe as the device size continues to scale down below 0.1 μm. As a consequence, the degree of reliability concern is increased when advanced MOSFETs are used in modern electronics systems.
1.2 Hot-Carrier Injection Phenomenon

A brief overview of the hot-carrier injection phenomenon and the resulting device degradation will be provided in this section. The cross-section of a typical n-channel MOSFET operating in saturation is shown in Figure 1. The large voltage drop across the pinch-off region results in a high lateral electric field close to the drain region. The carriers traversing this high field region reach energies, which are considerably higher than the equilibrium thermal energy in the semiconductor lattice. These high-energy carriers are called hot-carriers. Hot-carriers with energies above the impact-ionization threshold (1.6eV) [2] can generate electron-hole pairs in this region through impact-ionization. Some of these carriers, with energies large enough to overcome the potential barrier between Si and SiO2 and their momentum directed towards the Si-SiO2 interface, can get injected into the gate oxide [4]. As shown in Figure 2, the energy barrier for injection of electrons (3.1eV) is considerably smaller than that for holes (4.8eV) making hole-injection a less probable event as compared to electron-injection. The exact barrier at any given point along the channel is affected by the transverse electric field at that point due to the Schottky effect [3]. A large proportion of the injected electrons reaches the gate terminal and contributes to the gate current. However, some of the injected electrons can also get trapped at certain defects present in the gate oxide [5, 6]. Similarly, the injected holes can reach the gate and contribute to the gate current. However, as the hole mobility in SiO2 is considerably smaller than that of electrons [7], holes have a higher probability of getting trapped. In addition to getting trapped in the gate-oxide, the injected carriers can also result in increase in the density of interface traps present at the Si-SiO2 interface [8, 9, 10]. The presence of charge in the gate-oxide and at the Si-SiO2 interface of a MOSFET results in modulation of the surface
potential and carrier mobility at the surface of the semiconductor. These phenomena alter the device current characteristics, which can significantly reduce the operating lifetime of these devices [11].

As mentioned earlier, the injection of carriers into the gate-oxide is a significant concern for assuring the long-term reliability of modern digital CMOS circuits. As these degradation processes are relatively slow during circuit operation, in order to characterize the hot-carrier response of devices within short times they are often subjected to much larger biases than those present in real circuits. The presence of higher biases results in acceleration of the degradation processes and hence such experiments are called accelerated stressing experiments. The extrapolation of the results obtained from the accelerated stressing experiments to real-life circuit operation is a subject of other chapters later in this dissertation.

Figure 1  Hot carrier generation in nMOS devices.
1.3 Thesis Outline

The various characterization techniques, which are used to monitor the device degradation during accelerated stressing experiments and attribute it to the underlying physical mechanisms, will be presented in Chapter 2.

Chapters 3 present a new and simple extrapolation method for the MOS lifetime prediction, which can be readily applied to any existing degradation law for better accuracy and predictability. In order to predict the impact of hot-carrier induced device degradation on the circuit operation as well as to optimize the parameter shifts due to hot-carrier injection, we need to accurately model the time dependence of these parameter shifts. Chapter 3 also presents an overview of some of the popular models and discusses their applicability to deep-sub-micron technologies.
Basing on extrapolation method in Chapter 3, we present a simple yet effective approach to modeling the 0.18-μm MOS reliability empirically. Short-term stress data are first measured, and the well-known power law is used to project the MOS long-term degradation and lifetime. These results are then used as the basis for the development of an empirical model to predict the MOS lifetime as a function of drain voltage and channel length. The study focuses on the worst-case stress condition, and both the linear and saturation operations are considered in the modeling. The approach developed has useful applications to the empirical modeling of MOS and other semiconductor devices. This study provides useful design guides concerning MOS reliability issues, and the approach developed can be readily extended to the empirical modeling of other semiconductor devices. This work will be presented in Chapter 4. As a part of this work, a set of stressing experiments is suggested to study the various aspects of device degradation in n-channel MOSFETs comprehensively.

With deep study on submicron MOSFETs, experimental results are presented to indicate that the widely used power-law models for lifetime estimation are questionable for deep submicron (< 0.25 μm) MOS devices, particularly for the case of large substrate current stressing. This observation is attributed to the presence of current components, such as the gate tunneling current and base current of parasitic bipolar transistor, that do not induce device degradation. A more effective extrapolation method is proposed as an alternative for the reliability characterization of deep-submicron MOS devices. Chapter 5 is focus on a more effective extrapolation method for the reliability characterization of deep-submicron MOS devices. This method will account into the effect of gate tunneling current and base current of parasitic bipolar transistor that do not induce device degradation. A simple and accurate empirical expression
correlating the MOS lifetime with the ratio of gate to substrate current has been proposed in this chapter. This model also gives better physical insights than the existing power-law models.

In the final part of the thesis, we found the conventional modeling for hot-carrier aging is questionable for deep-submicron devices, and a systematic method is needed for predicting the lifetime of the devices and circuits. In this chapter, we develop a Spice-like reliability model for advanced radio frequency RF MOS devices and implement the model into SpectreRF circuit simulator via Verilog-A HDL (Hardware Description Language).
2. CHARACTERIZATION TECHNIQUES

2.1 Introduction

The injection of hot-carriers into the gate-oxide of MOSFETs triggers carrier trapping and interface trap generation processes. The presence of interfacial and bulk charge in the gate-oxide affects the DC current characteristics and AC properties of these devices. The alteration of the current characteristics effectively results in variations in some of the parameters extracted from them such as the threshold voltage, subthreshold slope and the transconductance [11, 12, 13]. These parameter shifts can be used as measures of the degradation as well as a key to understand the underlying physical mechanisms. The drain current characteristics (\(I_{DS-}\text{V}_{GS}\) and \(I_{DS-}\text{V}_{DS}\)) can be utilized to provide accurate information about the degradation processes when the hot-carriers are injected uniformly along the channel of the device, such as during substrate hot-carrier injection experiments [14, 15]. For example, the variations in the \(I_{DS}\) vs \(V_{GS}\) characteristic measured in saturation can be used to obtain the contributions due to interface traps and fixed charge in the oxide using techniques such as the midgap method [16]. These techniques assume that the change in subthreshold slope is entirely due to interface traps under uniform injection conditions, it can be assumed that the threshold voltage at each point along the channel of the device shifts by the same amount. The threshold voltage of the complete device is equivalent to that of any point along the channel under this condition.

At the same time, it is sometimes possible to explain the observed degradation under non-uniform carrier injection by different combinations and spatial distributions of interface trap density and fixed oxide charge [17]. Due to the limitations in the correct interpretation of the
variations in drain-current characteristics, certain other characterization techniques, such as charge pumping and substrate current characteristics, have been used in some literature. Some of the most commonly used device characterization techniques which are used to monitor and understand the device degradation under channel hot-carrier injection will be described in this chapter.

2.2 Drain Current Characteristics

The drain current characteristics as a function of the drain bias as well as the gate bias have been used extensively in literature to extract parameters, which can be used as degradation monitors. The commonly used parameters include $V_T$, $G_m$ and $I_{DS}$. The physical meaning of each of these parameters can be defined on the basis of a simplified theory of operation of MOSFETs [3]. While performing experiments, the drain current characteristics are obtained in terms of two-dimensional arrays of numbers. The above parameters need to be extracted numerically from these data and the extracted values may not directly correlate to the physical definitions of these parameters.

Each of the above parameters, for example, can be measured from drain current characteristics obtained in either linear or saturation regions of operation. The two most important parameters, which are extracted numerically from measured data, are the threshold voltage and the channel transconductance. The definitions of these parameters and the techniques used to extract them numerically from measured data will be presented.
Figure 3  The device terminals used to measure mode parameters relative to the terminals used during hot-carrier stressing experiments.

The classical definition of the MOSFET threshold voltage is based on the one-dimensional analysis of a MOS capacitor [3]. According to this analysis the threshold voltage is defined as the gate bias which results in a surface potential $\psi_B$, at the SiO$_2$ interface which is equal to $2\psi_B$, where $\psi_B$ is the potential difference between the bulk Fermi-level, $E_{F,Bulk}$, and the intrinsic Fermi-level, $E_i$.

The threshold voltage is extracted experimentally from the $I_{DS}$-$V_{GS}$ characteristics. In the linear mode of operation, the $I_{DS}$-$V_{GS}$ characteristics for long channel devices can be approximated using:

$$I_{DS} = \frac{W}{L} \mu c_{ox} (V_{GS} - V_T) V_{DS}$$  \hspace{1cm} (2.1)

The threshold voltage can be extracted from the measured $I_{DS}$-$V_{GS}$ characteristics by extrapolating the curve in the high $V_{GS}$ region to $I_{DS} = 0$. The intersection of this extrapolated curve with the $V_{GS}$-axis gives the threshold voltage Figure 4 The threshold voltage obtained using this
technique is called the linear extrapolated threshold voltage. A similar extrapolation can be performed on $I_{DS}-V_{GS}$ measurements in saturation using the approximate relation:

$$\sqrt{I_{DS}} = \sqrt{\frac{W}{2L}} \mu C_{ox} (V_{GS} - V_T)$$

(2.2)

Once again, the extrapolation of the $\sqrt{I_{DS}-V_{GS}}$ curve to $I_{DS} = 0$ gives the saturation extrapolated threshold voltage. Figure 5.

![Figure 4 Linear threshold voltage extraction from plot of $I_{DS}$ vs $V_{GS}$](image)
Figure 5  Saturation threshold voltage extraction from plot of $I_{DS}$ vs $V_{GS}$

The threshold voltage of a MOSFET represents the gate bias at which the device turns on. In other words, at any given drain bias, the drain current of an ideal device will be zero at gate biases below the threshold voltage and increase with the gate bias when it goes above the threshold voltage. As the threshold voltage defines the amount of drain current in a MOSFET, it is common to define the threshold voltage as the gate bias, which results in a certain amount of drain current. The threshold voltage extracted using this definition is called the constant current threshold voltage, $V_{T,ci}$ is defined as the gate bias for which

$$I_{DS} = \left(\frac{W}{L}\right) \times 1 \mu A$$  \hspace{1cm} (2.3)

While equation 2.1 and 2.2 work well for long channel devices, short channel effects tend to deviate the characteristics of modern devices from these approximate equations. The typically
linear $I_{DS}$-$V_{GS}$ characteristics of a 0.18 $\mu$m n-channel MOSFET before and after stress are shown in Figure 6 and 7. As can be seen from Figure 7, for large values of the gate bias, the drain current does not increase linearly with the gate bias. The extrapolated threshold voltage is usually extracted from such curves using the same approach as before assuming that equation 2.1 holds at the point of maximum slope along the curve Figure 7. A more precise method to extract the threshold voltage would be to fit an accurate model for the device characteristics of sub-micron devices, such as the BSIM3 model [18], to the measured characteristics. However, this approach is considered impractical while analyzing stressing experiments performed on a large volume of devices due to the high computational complexity of the curve fitting process. Obviously, no such problem exists in extracting the threshold voltage from equation 2.1 2.2 and 2.3.,

Figure 6  The $I_{DS}$-$V_{DS}$ characteristics measured before and after a typical hot-carrier stress in n-channel MOSFETs.
2.3 Channel Transconductance and Mobility

The channel transconductance is defined as the rate of change of the drain current as a function of the gate bias at a given drain bias [3]:

$$G_m(V_{DS}) = \left[ \frac{\partial I_{DS}}{\partial V_{GS}} \right]_{V_{DS}=\text{const}} = \frac{W}{L \mu C_{ox}} V_{DS}$$  \hspace{1cm} (2.4)

The transconductance can be easily extracted for long channel devices by taking the numerical derivative of the drain current with respect to the gate bias using the measured $I_{DS}-V_{GS}$ characteristics. In short channel devices, however, the derivative do not have a constant value and shows a non-monotonic nature with $V_{GS}$ as shown in Figure 8. The channel transconductance in

Figure 7  The $I_{DS}-V_{GS}$ characteristics measured before and after a typical hot-carrier stress in n-channel MOSFETs.
short channel devices is usually taken as the maximum value of this derivative and sometimes referred to as the maximum transconductance for clarity. Obviously, the mobility can be easily derived from equation 2.4 by know \( G_m \).

![Graph showing transconductance and mobility extraction from plot of IDS vs VGS](image)

**Figure 8**  transconductance and mobility extraction from plot of IDS vs VGS

### 2.4 Stress conditions and Effect of Hot-Carrier Injection on MOS devices

In general, we have those following assumptions when talk about nMOS device degradation-hot carrier lifetime. Avalanche hot-carrier injection due to impact ionization at the drain, rather than channel hot-electron injection composed of “lucky electrons,” imposes the severest constraints on device design. Device degradation (\( V_{th} \) shift and \( G_m \) change) resulting from drain avalanche hot carrier injection has a strong correlation with impact ionization-induced
substrate current, $I_{SUB}$. That is, the gate bias condition which caused the largest degradation which yields the peak substrate current [19-23].

In our experiment, we chose $V_{GS}$ at maximum $I_{SUB}$ substrate current as our stress conditions, which can generate fast degradation in short term stress and keep a consistent stress effect for different stress conditions.

The typical $I_{DS}$-$V_{DS}$ and $I_{DS}$-$V_{GS}$ characteristics of an n-channel MOSFET before and after hot-carrier stressing experiment are shown in Figure 6 and Figures 7 respectively [2].

The post-stress $I_{DS}$-$V_{DS}$ characteristics join the pre-stress characteristics as the device goes into saturation. This can be explained by the fact that the device damage is localized near the drain region of the device. As the pinch-off region extends over the damaged region $I_{DS}$-$V_{DS}$ characteristics, the damaged region stops affecting the device characteristics.

2.5 Conclusion

The various characterization techniques discussed in this chapter were used in our work.
3. A NEW EXTRAPOLATION METHOD FOR LONG-TERM DEGRADATION PREDICTION OF DEEP-SUBMICRON MOSFETs

3.1 Degradation Law

Hot carrier-induced degradation is a major concern for deep-submicron MOS devices. To characterize the MOS long-term degradation and lifetime, stress tests are normally carried out within a relatively short time frame to observe the change of MOS behavior (i.e., change of transconductance $G_m$), and time-dependent degradation laws are then applied to extrapolate the long-term degradation results [24]. Several time-dependent degradation laws have been reported in the literature. The most widely used is the power law proposed in the 1980s [25]. To include the saturation behavior frequently found in the stress data, the saturation law was later proposed [26]. Marchand et al. developed the federative law which has been used in the stress-induced leakage current (SILC) analysis [27]. Recently, Szelag et al. proposed the mixed law for deep-submicron devices [28]. Table I lists the expressions of the four different time-dependent degradation laws and the parameters associated with these laws.

Table I

<table>
<thead>
<tr>
<th>Degradation Law</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power law [2]</td>
<td>$\frac{dY(t)}{Y(0)}=A.t^n$</td>
</tr>
<tr>
<td>Saturation law [3]</td>
<td>$\frac{dY(t)}{Y(0)}=A.\log(t)-B$</td>
</tr>
<tr>
<td>Federative law [4]</td>
<td>$\frac{dY(t)}{Y(0)}=1-\exp(-B.t^n)$</td>
</tr>
<tr>
<td>Mixed law [5]</td>
<td>$\frac{dY(t)}{Y(0)}=A.[\log(t)]^n$</td>
</tr>
</tbody>
</table>
3.2 New extrapolation method

Unfortunately, the long-term degradation phenomena observed experimentally do not obey exactly any of the laws mentioned above, unless the parameters associated with the degradation laws are extracted correctly from the short-term stress data measured. In this chapter, a new extrapolation method will be developed and introduced to provide the degradation laws with a better MOS lifetime predictability. Data measured from an NMOS and PMOS will be included and analyzed in support of the model development. The method developed is simple yet highly effective for the characterization of MOS reliability.

We propose a method called the exponential–exponential scale method to improve the accuracy of the existing degradation laws. Conventionally, the stress data are placed on the log–log scale, and least squares algorithm is used to fit the data and to extract the parameters associated with the degradation law. Such an approach puts more weight on earlier data points (data measured at earlier time frame). In reality, however, the long-term degradation is more critical to the device lifetime, and thus the later data points should play a more important role on the lifetime prediction. The exponential–exponential scale method proposed here puts the stress data on the exponential–exponential scale. This in essence reverses the priority of the log–log scale and places more emphasis on the later data points. As will be demonstrated later, this method, when augmented into the existing degradation laws, improves significantly the accuracy of the MOS lifetime prediction. To better illustrate the concept of the exponential–exponential scale method proposed, let us consider an arbitrarily selected function

\[ f(x) = 20 + 2x + 0.2x^2 \]  

(3.1)

And its approximation
Where \( A \) and \( B \) are parameters to be extracted. The original function \( f(x) \) in (3.1) is analogous to the exact degradation (i.e., measured data) of MOSFET, while the approximated function \( f'(x) \) in (3.2) is analogous to one of the power laws used to simulate the MOSFET long-term degradation. Take a few data points of the original function at relatively small \( x \) (these data points are analogous to those obtained from the short-term stress test of MOSFET), and these data points can be arranged either

On the log–log or exponential–exponential scale. Using the least square fitting to these data, different values for the parameters of \( A \) and \( B \) in (3.2) can be extracted. For example, using data points from \( x = 0 \) to 10000, \( A \) and \( B \) were extracted to be \( -81.26733 \) and \( 101.03287 \) from the log-log scale method and \( -15999868.27 \) and \( 3601.99 \) from the exponential–exponential scale method. Putting these values in (3.2), one can then predict the trend of the original function at relatively large \( x \) based on the approximated function. Figure 9 compares the results of the original function, the approximated function with the log–log scale method, and the approximated function with the exponential-exponential scale method for \( x \) up to 40000. Clearly, the approximated function with the exponential-exponential scale method compares more favorably with the original function than that with the log-log scale method.

3.3 MOS data analysis and degradation prediction

Let us first focus on the widely used power law, which in principle fits the data on the log–log scale linearly. The devices considered were NMOS with a channel length of 0.18 \( \mu \)m and channel width of 10 \( \mu \)m, stressed using the HP Network Analyzer (4156B) controlled by a PC.
with Labview, under the bias condition of drain voltage \( V_D = 2.2 \) v and gate voltage \( V_G = 1.4 \) v. Note that the substrate current reaches its peak value at this bias condition (i.e., worst stress condition). Figure 10(a) shows the measured \( dG_m/G_m(0) \) versus time characteristics on the log–log scale for a relatively short stress time of 50000 s. The least squares fitting is also shown, which is linear and appears to be accurate for the stress time considered. From the fitting, the parameters \( A \) and \( n \) associated with the power law (see Table 1) were extracted to be 0.00000424 and 0.68908, respectively. These parameters, together with the power law, can then be used to predict the long-term degradation.

Figure 9 Comparison of the original function \( f(x) \), the approximated function \( f'(x) \) with the log scale method, and the approximated function \( f'(x) \) with the exponential scale method. The approximated function were calculated based on the data points of the original function from \( x=0 \) to 10000
Figure 10  (a) Log-log scale and (b) exponential exponential scale (present method) fitting the measured $dG_m/G_m(0)$ characteristics up to 50000s.
As will be illustrated later, however, this approach gives rise to considerable errors in predicting the $G_m$ degradation at a relatively long stress time. On the other hand, instead of the log–log scale, the exponential–exponential scale method (hereafter called the present method) arranges the same measured stress data on the exponential–exponential scale, as shown in Figure 10(b). From this, together with the least squares algorithm, a new set of parameter values of $A = 0.00077$ and $n = 0.39498$ is extracted, and a more accurate long-term degradation prediction is obtained.

It would be necessary to provide more explanations for the exponential-exponential scale method shown in Figure 10(b). The tic marks on the x and y axis are based on exponential scales. For example, the scale between 0 and 36889 tic marks on the x axis is exponential [i.e., opposite to the log scale between the tic marks in Figure 10(a)]. The same applies to the y axis. Using the same eight stress data points in Figure 10(a) but arranging them on this exponential–exponential scale, together with the least squares fitting scheme, a more accurate set of parameters for the power law can be extracted. These parameters are then put into the power law to predict long-term degradation of MOS devices. Figure 11 compares the long-term $dG_m/G_m(0)$ characteristics (up to about 250000 s) obtained from measurements, log–log scale method with power law (i.e., power law), and present method with power law. In the fitting schemes, we used the first 50000 s data [as shown in Figure 10(a) and (b) to predict the next 200000 s degradation behavior. Clearly, the power law overestimates the $G_m$ degradation at relatively long stress time. Using a 10% $G_m$ drop as the definition for the MOS lifetime, we obtained lifetimes of about 78000 and 210000 s from the power law and present method, respectively.
As mentioned earlier, the better accuracy associated with the present method stems from the fact that such a method reverses the importance of the short-term stress data in the conventional log–log scale method. In other words, the later data points obtained from the short-term stress play a more important role in determining the parameters in the present method than that in the log–log scale method. Since the MOS lifetime is a result of the long-term degradation, such a reversal of importance in the present method gives rise to a more accurate prediction of the MOS lifetime. The above discussions also brings an interesting question as to whether the accuracy of the log–log scale method could be improved if one or more initial stress data points are not considered, thus shifting the emphasis toward later data points. This is indeed the case, as the error of the power law using the log–log scale method for predicting the MOS lifetime is reduced from 62% to 12% if the first data point measured at 100 s [see Figure 10(a)] is removed from consideration. Note that the error associated with the present method, without eliminating any data point, is about 6%. The approach of removing initial data points, however, is quite subjective and difficult to follow. This is because it is sometimes hard to know how many initial data points need to be removed in order to achieve a reasonable accuracy, or if the first data point is to be removed, at what stress time this data should be measured. If the first data point is measured at a very small stress time, then the removal of this data may not improve the accuracy of the log–log scale method. On the other hand, if the first data point is measured at a relatively large stress time, the accuracy can be improved, but the subsequent data points will have to be measured at even larger stress time, thus increasing the time needed for the initial stress measurements. Moreover, a sufficiently large number of short-term stress data is often needed to ensure consistent parameter extraction, and the removal of initial data may require additional
data to be measured at a larger stress time, which again prolongs the stress measurements. The proposed exponential–exponential scale method eliminates these uncertainties and drawbacks.

An equally important issue to consider is how the selection of different numbers of short-term data points, or the different short-term stress time, affects the accuracy of the long-term degradation prediction. To address this, we have chosen four different short-term stress times to predict the MOS long-term degradation using the power law with the log-log scale method (i.e., power law) and with exponential-exponential scale method (i.e., present method). Taking the measured lifetime of about 200000 s (see Figure 11) as the norm value, the lifetime errors associated with the different short-term stress times were calculated and summarized in Table 2. Obviously, the present method requires a much shorter stress time and thus much less data points to obtain a reasonable accuracy in predicting the MOS long-term degradation than the power law. For example, for the device under study, a stress time of 30000 s is sufficient for the present model to predict the MOS lifetime with an error of less than 9%, whereas a nearly ten-fold error is found in the power law based on the same stress data.
Figure 11 Comparison of \( \frac{dG_m}{G_m(0)} \) characteristics of a 0.18-\( \mu \)m NMOS up to 250000 s measured and predicted from the power law, saturation law, and the two laws with the present exponential-exponential method based on the short-term stress data (stress time of 50000s).

The present method can also be expanded to optimize other existing degradation laws. Also shown in Figure 11 are the extrapolations of the saturation law (i.e., saturation law with the log–log scale method) and the present method (i.e., saturation law with the exponential–exponential scale method). It is illustrated that the saturation law can underestimate considerably the long-term Gm degradation of deep-submicron MOS devices. Figure 12 shows \( \frac{dG_m}{G_m(0)} \) versus time characteristics obtained from measurements and from the fittings of the federative law, mixed law, and the two laws with the exponential–exponential scale method. The data here were taken from an SOI PMOS stressed under the bias conditions of \( V_D= -4.25 \) V and \( V_G=V_D/2 \) [29]. In the fitting schemes, the first 10000 s data were used to extrapolate the next
40000 s $G_m$ degradation. The improved predictability of the present method is clearly demonstrated. For this particular device, the mixed law appears to be more accurate than the federative law.

Table 2 Errors of MOS lifetime associated with the power law and present method using data measured for stress times up to 5000, 10000, 30000, and 50000s.

<table>
<thead>
<tr>
<th></th>
<th>Stress time 5000 sec</th>
<th>Stress time 10000 sec</th>
<th>Stress time 30000 sec</th>
<th>Stress time 50000 sec</th>
<th>Measured lifetime (sec, norm value)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power law</td>
<td>90.6</td>
<td>85.7</td>
<td>72.5</td>
<td>62.0</td>
<td>200000</td>
</tr>
<tr>
<td>Present method</td>
<td>56.1</td>
<td>53.6</td>
<td>8.7</td>
<td>6.6</td>
<td></td>
</tr>
</tbody>
</table>

It should be mentioned that it is possible to fit the long-term $G_m$ degradation reasonably well using the existing degradation laws if the entire measured data points (i.e., up to 200000 s in Figure 11 and up to 50000 s in Figure 12) are considered. On the other hand, when augmented with the present method, these laws can predict the MOS long-term degradation accurately with a relatively small number of short-term data points. In other words, using the present method, the stress time required for predicting the MOS long-term degradation can be greatly reduced.

To further verify the present method, we analyzed the degradation of another NMOS with a channel length of 0.18 $\mu$m stressed at $V_D=2.1$ v and $V_G=1.33$ v. Only the power law was considered here, and a longer stress test was conducted to truly demonstrate the long-term applicability of the model. Figure 13 shows $G_m$ degradation results up to 420000 s obtained from measurements and calculated from the power law with the log–log scale method (i.e., power law) and with the exponential-exponential scale method. The calculation results were
based on the short-term stress data measured up to 5000 s. The advantage of the exponential–exponential scale method is again illustrated.

Figure 12  Comparison of \( \frac{dG_m}{G_m(0)} \) characteristics of an SOI PMOS [6] up to 50000 s measured and predicted from the fedrative law, and the two laws with the present exponential method based on the short-term stress data (stress time of 10000 s).
Figure 13 Comparison of $G_m$ degradation characteristics of 0.18-$\mu$m NMOS up to 400000 s measured and predicted from the power law and the power law with the present exponential method based on the short-term stress data (stress time of 5000 s)

3.4 Conclusion

In summary, a new and simple extrapolation method for the MOS lifetime prediction has been developed. The method can be readily applied to any existing degradation law for better accuracy and predictability. Stress data measured from three different MOS devices have been analyzed, and the improved accuracy of the present method over the existing method has been presented.
4. EMPIRICAL RELIABILITY MODELING FOR 0.18 μm MOS DEVICES

4.1 Introduction

Long-term hot-carrier induced degradation of MOS devices has become more severe as the device size continues to scale down below 0.1 μm. As a consequence, the level of reliability concern is increased when advanced MOSFETs are used in modern electronics systems. From the designers’ perspective, it is imperative to have a simple and accurate reliability MOS model which can predict the lifetime of MOSFET subject to different bias conditions.

Many physics-based MOS reliability models have been reported in the literature [30-31]. These models have the advantages of providing the physical insights into the degradation mechanism in MOS devices, but they tend to have non-straightforward expressions and may not be accurate due to the complicated short-channel and hot-carrier effects in the devices. Empirical models developed based on experimental data, on the other hand, possess simple expressions and provide accurate predictions, but they need to be re-developed for different MOS technologies.

This paper seeks to develop an accurate empirical reliability model for MOS devices fabricated from the 0.18-μm technology. The model will be sufficiently versatile to account for the effect of different channel lengths and different bias conditions. MOS devices having three different channel lengths will be considered, and stress measurements on these devices under different bias conditions will be conducted. The experimental data will then used as the basis of parameter extraction and empirical model development.
4.2 Measurement procedure

The devices under study are n-channel MOSFETs fabricated from the 0.18-\(\mu\)m CMOS technology, and the following channel lengths are considered: 0.5, 0.25, and 0.18 \(\mu\)m. The channel width is 10 \(\mu\)m, and device make-ups include P-well, N-well, threshold-adjust implant, and retrograde doping profiles. These devices are stressed over a relatively short period of time at different bias conditions, and the degradation of transconductance \(G_m\) is measured in both the linear and saturation regions. Based on these short-term stress data, the long-term degradation and lifetime are then projected based on a time-dependent degradation law. The lifetime is defined as the time when \(G_m\) degrades 10\% from its initial value.

To predict the long-term \(G_m\) degradation and thus the MOS lifetime, we use the well-known power law, which has the form of [32]

\[
\frac{\Delta G_m}{G_m} = C \times \tau^n \quad (1)
\]

An extraction method is needed to determine the values of the two parameters (C and n) associated with the power law. The conventional way to do this is to arrange the short-term stress data on the log-log scale, as shown in Figure 14(a), and use the least-square fitting. Recently, we have developed an improved extraction method which arranges the short-term data on the exponential-exponential scale [34], as shown in Figure 14(b). In the figures, the short-term data are measured up to 50000 sec. The different extraction methods will give rise to different parameter values and thus to different long-term degradation results predicted by the power law. Figure 15 compares the MOS long-term degradation characteristics (up to 200000 sec) obtained
from measurements (symbols) and predicted from the power law using the conventional and improved extraction methods. Clearly, the improved method gives a much better accuracy than the conventional method. Using the improved extraction method, together with the power law, the lifetime of a particular MOSFET subject to a particular bias condition can be determined.

(a)
Figure 14  Short-term (up to 50000 sec) stress transconductance data measured and fitted based on (a) log-log scale and (b) exponential-exponential scale.

Figure 15  Long-term (up to 200000 sec) transconductance degradation obtained from measurements, power law with log-log method, and power law with exponential-exponential method.
4.3 Empirical model development

Our task here is to develop an empirical reliability model for the 0.18-μm NMOS devices having different channel lengths \( L \) and different drain voltages \( V_D \) under the worst-case stress condition. This means that, for a MOS device having a particular \( L \) and \( V_D \), the stress is done in such a condition that the gate voltage \( V_G \) is adjusted until the substrate current \( I_B \) is maximum. As such, \( V_G \) is a hidden variable and does not appear in the empirical model.

Let us first focus on the MOS degradation in the linear region (MOS devices stressed under the worst-case and measured at a drain voltage of 0.1 v). To develop the empirical model, we will first look into the relationship between MOS lifetime \( \tau \) and substrate current \( I_B \). It has been observed experimentally that \( \tau \) versus \( I_B \) characteristics are not a function of \( L \). This is because \( I_B \) is related to the maximum electric field \( E_m \) near the drain junction, which gives a direct measure of the stress level [34]. Once \( I_B \) is fixed, \( E_m \) is almost insensitive to the channel length \( L \). To illustrate this, we have carried out device simulation and shown the electric field contours in MOS devices having the same \( I_B \) of 4.4x10^{-6} A, but three different channel lengths of 0.5, 0.25, and 0.18 μm in Figure 16(a)-(c), respectively. Note that different drain voltages are needed to arrive at the same substrate current for the MOS devices with three different \( L \). Very similar maximum fields of 6.1x10^5, 6.3x10^5, and 6.4x10^5 V/cm are found in these devices. This clearly indicates that \( E_m \) is almost independent of \( L \) when \( I_B \) is constant. In other words, once \( I_B \) is fixed, the stress level, and thus the MOS degradation, is almost the same for MOS devices having different \( L \). An expression has been suggested to relate the lifetime \( \tau \) and \( I_B \) [30]:

\[
\tau = K \times I_B^{-B} \quad (4.2)
\]
Where \( K \) and \( B \) are constant parameters. We have measured \( \tau \) versus \( I_B \) characteristics in the linear region and used the data to extract the parameters \( K \) and \( B \) associated with the expression in (4.2). These yields

\[
\tau = 4.312 \times 10^{-5} \times I_B^{-1.91898} \quad (4.3)
\]

Figure 17 shows the measured and simulated \( \tau \) versus \( I_B \) characteristics. Good agreement is found. Note that the trend is not a function of \( L \).

Our next step is to relate \( I_B \) and \( V_D \). To this end, we have measured \( I_B \) versus \( V_D \) characteristics and have obtained empirical expressions for the three different \( L \) considered. The general expression is

\[
I_B = \exp(-A - \frac{B}{V_D}) \quad (4.4)
\]

Where \( A \) and \( B \) are -0.4481 and 30.77448, -1.1709 and 25.64196, and -1.5739 and 22.88929 for \( L = 0.5, 0.25, \) and \( 0.18 \) \( \mu m \), respectively. Figure 18 shows the measured and simulated \( I_B \) versus \( 1/V_D \) characteristics.

Note that the values for the two parameters, \( A \) and \( B \), associated with the \( I_B \) vs \( 1/V_D \) characteristics are for particular \( L \). We will now develop empirical relationships between these parameters and \( L \). Fitted from the data, the expressions for \( A \) and \( B \) are obtained as

\[
A = -0.25501 - 0.8427 \times \ln(L - 0.06585) \quad (4.5)
\]
\[ B = 36.54878 \times (L - 0.09393)^{0.19081} \quad (4.6) \]

Figure 19 (a) and (b) compare the measured and fitting data of A and B, respectively.

We can now combine the above expressions and obtain an empirical model for MOS lifetime as a function of \( V_D \) and \( L \). Specifically, we put (4.5) and (4.6) into (4.4), and then put the resulting equation into (4.3). This leads to the following expression for \( \tau \) as a function of \( V_D \) and \( L \):

\[
\tau = 4.31205 \times 10^{-5} \times \{ \exp[0.25501 + 0.8421 \times \ln(L - 0.06585) - \frac{36.54878 \times (L - 0.09393)^{0.190813}}{V_D}] \}^{-1.91898} 
\]

\( (4.7) \)

The above equation is for MOS devices operated in the linear region. Using the same approach, we can also develop an empirical model for MOS devices in the saturation region (MOS devices stressed under the worst-case and measured at a drain voltage of 0.9 V):

\[
\tau = 22.36215 \times \{ \exp[0.25501 + 0.8421 \times \ln(L - 0.06585) - \frac{36.54878 \times (L - 0.09393)^{0.190813}}{V_D}] \}^{-0.94396} 
\]

\( (4.8) \)

Figure 20 and 21 show the measured and simulated \( \tau \) versus \( 1/V_D \) as a function of \( L \) for MOSFETs operated in the linear and saturation regions, respectively. Note that while the majority of lifetimes (open symbols) were obtained from the projection of the power law based
on short-term stress data, a few lifetimes (closed symbols) were actually long-term stress data measured all the way to the 10% $G_m$ degradation. Very good agreement between the model and measurements is obtained.

The model developed is highly useful to provide MOS design guide concerning reliability issues. For example, for a given MOS device and a specific lifetime time, one can determine the maximum $V_D$ allowed to apply to the device, or one can determine the minimum channel length for a known $V_D$ and lifetime. Tables 3 and 4 give the specifics of such information.

Table 3  Maximum drain voltage (in V) allowed for the specific lifetime and channel length

<table>
<thead>
<tr>
<th>$V_D$</th>
<th>Lifetime/Length</th>
<th>0.18μm</th>
<th>0.25μm</th>
<th>0.35μm</th>
<th>0.5μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Region</td>
<td>3 Yrs</td>
<td>1.729</td>
<td>1.880</td>
<td>2.013</td>
<td>2.143</td>
</tr>
<tr>
<td>5 Yrs</td>
<td>1.695</td>
<td>1.844</td>
<td>1.975</td>
<td>2.104</td>
<td></td>
</tr>
<tr>
<td>10 Yrs</td>
<td>1.651</td>
<td>1.797</td>
<td>1.926</td>
<td>2.053</td>
<td></td>
</tr>
<tr>
<td>Saturation Region</td>
<td>3 Yrs</td>
<td>1.569</td>
<td>1.710</td>
<td>1.835</td>
<td>1.958</td>
</tr>
<tr>
<td>5 Yrs</td>
<td>1.513</td>
<td>1.651</td>
<td>1.772</td>
<td>1.893</td>
<td></td>
</tr>
<tr>
<td>10 Yrs</td>
<td>1.443</td>
<td>1.576</td>
<td>1.694</td>
<td>1.811</td>
<td></td>
</tr>
</tbody>
</table>

Table 4  Minimum channel length (in μm) allowed for the specific lifetime and drain voltage

<table>
<thead>
<tr>
<th>Channel length</th>
<th>Lifetime/$V_D$</th>
<th>0.9V</th>
<th>1.2V</th>
<th>1.5V</th>
<th>1.8V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Region</td>
<td>3 Yrs</td>
<td>0.096</td>
<td>0.102</td>
<td>0.127</td>
<td>0.208</td>
</tr>
<tr>
<td>5 Yrs</td>
<td>0.096</td>
<td>0.104</td>
<td>0.132</td>
<td>0.225</td>
<td></td>
</tr>
<tr>
<td>10 Yrs</td>
<td>0.096</td>
<td>0.105</td>
<td>0.139</td>
<td>0.252</td>
<td></td>
</tr>
<tr>
<td>Saturation Region</td>
<td>3 Yrs</td>
<td>0.097</td>
<td>0.110</td>
<td>0.158</td>
<td>0.318</td>
</tr>
<tr>
<td>5 Yrs</td>
<td>0.098</td>
<td>0.114</td>
<td>0.175</td>
<td>0.379</td>
<td></td>
</tr>
<tr>
<td>10 Yrs</td>
<td>0.099</td>
<td>0.121</td>
<td>0.206</td>
<td>0.483</td>
<td></td>
</tr>
</tbody>
</table>
Figure 16 Electric field contours obtained from device simulation for MOS devices having three different channel length of 0.5, 0.25, and 0.18 μm but the same substrate current of $4.4 \times 10^{-6}$ A. The maximum fields in the three devices are also indicated.

Figure 17 Lifetime versus substrate current obtained from measurements and fitting.
Figure 18 Substrate current versus $1/V_D$ for three different channel lengths obtained from measurements and fitting.
Figure 19  Measured and fitting data of (a) parameter A and (b) parameter B.

Figure 20  Lifetime versus $1/V_D$ in the linear region obtained from measurements and empirical model. Open symbols are lifetimes obtained from power law projection based on short-term stress data, and close symbols are lifetimes obtained from the long-term stress measured all the way to the 10% transconductance degradation.
4.4 Conclusion

Reliability is a major concern for modern deep-submicron MOS devices. In this study, n-channel MOSFETs fabricated from the 0.18-μm CMOS technology and subjected to different bias conditions were considered. Short-term stress data were first measured, and the MOS’s long-term transconductance degradation and lifetimes were projected from the power law. Fitting to these data, an empirical model for predicting the MOS lifetime as a function of the channel length and drain voltage has been developed. This study provides useful design guides concerning MOS reliability issues, and the approach developed can be readily extended to the empirical modeling of other semiconductor devices.
5. SUBSTRATE CURRENT, GATE CURRENT, GATE CURRENT AND LIFETIME PREDICTION OF DEEP-SUBMICRON nMOS DEVICES

5.1 Introduction

Being scaled down to the deep-submicron range, the MOS transistors have suffered from various large leakage currents and significant reliability degradation [35-37]. The long-term reliability of MOS devices is governed by the hot carrier irradiation effects, which are often characterized with the substrate current or gate current [38-40]. The device reliability parameters, e.g. threshold voltage shift and transconductance degradations, are often found to be power functions of the stressing duration. The power time dependence is extrapolated to estimate the device lifetime [38-39]. However, there are many reports suggesting that the device degradation does not follow the power law and the lifetime prediction based on the extrapolation of the power law can be questionable [40-43].

Besides the lifetime model, the MOS degradation characterization has become more difficult because of the presence of large gate leakage currents. In deep-submicron devices, the thickness of silicon gate oxide has been scaled down to the direct-tunneling limit (<3 nm) [37]; as a result, the measured gate current may not represent the actual amount of the hot-carrier current involved in the device degradation. In addition, this tunneling process has pronounced effects on the mechanism of charge trapping in the oxide which is a main origin of the threshold voltage shift in short-channel devices. Hence, the relationships amongst the threshold voltage shift, the gate current, and the substrate current are more complicated and less straightforward. This work aims at the investigation of physical mechanisms underlying the hot-carrier stressing induced
characteristic degradation in deep-submicron devices based on the observation of the gate and substrate currents. With a better understanding of substrate and gate currents, a more precise MOS device lifetime fitting model will be developed. Experimental details will be given in Sec. 5.2. Sec 5.3.1 demonstrates the inaccuracy of the MOS lifetime prediction based on the existing methods, and a new prediction method will be proposed in Sec. 5.3.2. Further comments on the power-law model and the newly proposed model will be given in Sec. 5.4. Finally, major results of this work will be summarized in Sec. 5.5.

5.2 Experiments

N-channel deep-submicron MOS devices fabricated using the 0.18-μm CMOS technology are considered. The channel width of the devices is 10 μm and the gate oxide thickness is 3.2 nm. Three different channel lengths of 0.18, 0.25, and 0.5 μm were used to study the effect of channel length on the device degradation characteristics. Substrate current stressing and device characteristic measurements were carried out with an HP 4156 Precision Semiconductor Parameter Analyzer. In the experiments, the devices were biased at the worst-case stress condition, i.e., at maximum substrate current (I_{Sub}). The gate currents (I_{G}) were also measured under the same stress condition. Unless noted otherwise, MOS lifetimes were determined using the criteria of 10% shift in the threshold voltage (V_T), which was measured based on extrapolating the point where the slope of drain current vs. gate voltage curve is maximum. Figure 22(a) shows I_{Sub} vs. gate voltage V_g characteristics as a function of the drain voltage V_d for the MOS devices considered, and Figure 22(b) shows the drain current I_D , substrate current I_{Sub} and gate current I_{G} vs. V_d characteristics under the worst-case stress condition (i.e., V_g is
varied until the maximum substrate current is reached). Note that the ranges of $V_d$ used are 2.0-2.3 V and 2.5-2.8 V for 0.18-μm and 0.25-μm devices, respectively.

5.3 **Substrate current, gate current, and lifetime estimation**

5.3.1 **Substrate current and gate current in deep-submicron devices**

The main degradation mechanism and the lifetime ($\tau$) of MOS devices are believed to be strongly related to the impact ionization in the high electric-field region near the drain junction [44-45]. In nMOS transistors, the generated hot holes will flow to the substrate and constitute the substrate current ($I_{\text{Sub}}$). Hence $I_{\text{Sub}}$ has been widely used as an indicator of the number of electron-hole pairs generated by impact ionization, and the MOS device lifetime ($\tau$) could be correlated with $I_{\text{sub}}$ quite well from the following power-law expression [46-48]

$$\tau = A(I_{\text{Sub}})^{-n} \quad (5.1)$$

where $A$ and $n$ are empirical parameters. This widely used empirical relationship, however, is only valid for large-size MOS transistors or relatively small $I_{\text{Sub}}$. As shown in Figure 23, the power law fits very well with the measured data at small substrate currents, but considerable deviations are observed at large substrate currents, especially for the 0.18 μm MOS devices. That is, (5.1) underestimates the lifetime of MOS devices having a large substrate current and/or small channel length. This observation agrees with a recent study which reported that thinner gate oxide nMOS transistors have better reliability than that predicted by (5.1) over a wide range of
bias conditions and gate lengths [36]. This observation further indicates that in deep-submicron devices either the power law is invalid in large substrate current case or not all “substrate hot carriers” produce the same degradation as those of small substrate current case. Note that the substrate currents of the two MOS devices at normal operation condition ($V_d = 1.8$ V and $V_g = 0.5$ V for 0.18-$\mu$m and $V_d = 2.2$ V and $V_g = 1.0$ V for 0.25 $\mu$m MOS) are also indicated in Figure 23.

While the above-mentioned power law is widely used, a more recently developed expression

$$I_D = A (I_{Sub} / I_D)^{-n}$$

Where $I_D$ is the drain current is also quite common [49]. Figure 23 shows the fitting of such a power law. A very similar trend as that in Figure 22 is found. That is, the fitting becomes worsen as $I_{Sub}/I_D$ is increased and/or the channel length is decreased.
Figure 22  (a) Substrate current vs. gate voltage characteristics (b) drain current, substrate current and gate current vs. drain voltage characteristics under the worst-case stress condition (i.e., maximum substrate current)

Figure 23  Power-law fitting of 0.18 µm and 0.25 µm MOS devices. Markers are the experimental data and lines are the curve fittings using the power law of $I_D = A(I_{Sub}/I_D)^n$. 
Figure 24  Power-law fitting of 0.18 μm and 0.25 μm MOS devices. Markers are the experimental data and lines are the curve fittings using the power law of $I_D = A(I_{Sub}/I_D)^n$.

Figure 25 shows an alternative power-law fitting based on the gate current, i.e.

$$\tau = A(I_G)^{-n}$$  \hspace{1cm} (5.3)

Better results are produced. However, the values of both fitting parameters (included in the figure) vary too much even for the devices with the same fabrication processes. As listed in the table in Figure 25, the power index ($n$) varies from 2.5 to 14.47 and the proportional coefficient ($A$) changes from 10-18 to 10-149 for channel length ranging from 0.5 μm to 0.18 μm. Thus this model cannot be a good model for practical applications. It seems that the physics of hot carrier-induced degradation of deep-submicron devices are quite different from that of submicron devices. With these observations, a more precise lifetime model for deep-submicron
MOS devices has to be developed and is urgently needed.

Figure 25  Plot of lifetime as a function of gate current for devices with channel length of 0.18, 0.25 and 0.5 μm. Markers are the experimental data and lines are curve fittings. The values of fitting parameters for each device are listed in the table. Good power law fittings are obtained but large variations of the model parameters suggested the fittings are impractical.

A few words about how the gate currents and lifetimes were obtained in Figure 25 are needed. The bias conditions used in obtaining the gate currents in Figure 25 are as follows. Typical ranges of the drain voltages for the different devices were used (1.8-2.2 V for 0.18 μm, 2.2-2.6 V for 0.25 μm, and 2.6-3.0 V for 0.5 μm). Then for a specific drain voltage, the gate voltage was adjusted such that the substrate current is maximum (i.e., worst-case stress). This bias condition was then used to measure the gate current, and the MOS lifetime for this particular gate current was extracted from the time-dependent MOS characteristics (in this case, the threshold voltage
shift versus time) subject to this particular bias condition. Changing the drain voltage within the range and repeating this process will thus yield several different gate currents and the corresponding MOS lifetimes. The same approach applies to the substrate currents and lifetimes in Figure 23.

Before a more effective MOS lifetime model could be developed, a better understanding of the substrate current and gate current generation mechanisms is indispensable. The generation of substrate current in long-channel device is mainly due to the flow of hot holes (generated by impact ionization in the high field region near the drain [44-45]) to the substrate ($I_{hh}$ in Figure 25). The amount of hot electrons involves in degrading the device (via charge trapping and interface trap generation [42]) can be approximated quite well with the substrate current. However, in deep-submicron devices, the base width of the parasitic $n^+\text{-p-n}^+$ transistor (formed by source, substrate and drain) is so narrow that the base current can be a significant component of the substrate current (see Figure 27) [50]. In other words, the substrate current in the deep-submicron devices is larger than that involved only the flow of hot holes generated by impact ionization. With this connection, the substrate current does not reflect very well the amount of hot electrons involved in the threshold voltage degradation. This substrate current can result in the overestimated threshold voltage degradation as evidenced in Figure 23.
Figure 26  Generation of substrate and gate currents in long-channel MOS devices. Solid lines indicate the major current or charge transport and dash lines indicate charge transport may exist but are negligible. Modified based on Ref. [49].
Figure 27  Generation of substrate and gate currents in deep submicron MOS devices. Solid lines indicate the major current or charge transport and dash lines indicate charge transport may exist but are negligible. Modified based on Ref. [49].

On the other hand, the gate current is also not a good variable for modeling the threshold voltage degradation in deep-submicron devices because of the increasing direct tunneling in the gate oxide. In a thick oxide, the gate current is mainly contributed by the trapping, de-trapping and interface trap generation. These processes give rise to the threshold voltage degradation [42].
However, in a very thin gate oxide, a large part of the gate current comes from the direct tunneling of hot electrons in the impact ionization region or electrons in the channel, and the oxide trapping and de-trapping effect will also become less significant because the oxide is so thin that the rate of tunneling from the trap is high (see Figure 27). This tunneling current does not cause electron trapping in the gate oxide and thus does not produce threshold voltage shift. When the gate current is increased (i.e., stress is increased), a portion of the gate current produces trapped oxide charges, whereas the other portion of the gate current actually reduces such charges. As a result, a smaller number of trapping charges takes place in the thinner gate oxide [41]. Hence, the lifetime of deep-submicron MOS devices can be underestimated if the characterization is based either on the substrate current or the gate current.

5.3.2 New lifetime estimation model

As shown in Figure 27, the substrate current and gate current in deep-submicron device consist of “non-degrading” current components. Hence, neither the substrate nor gate current is a good measure of the amount of hot electrons involved in the threshold voltage degradation. A precise way to quantify this degradation will be too difficult, as the non-degrading currents cannot be separated from the total current using any known experimental methods. Since the measured substrate and gate currents are the only readily accessible data for characterization purposes, any approach based on these currents but can suppress the “non-degrading” (does not lead to device degradation) part and make the degrading part more relevant would be highly attractive and lead to a better estimation of the MOS device lifetime.

Since the non-degrading gate current is strongly related to the non-degrading substrate
current, a simple and effective way to gauge the significance of the “degradation” variable for
inducing threshold voltage and transconductance degradation is using the ratio \( I_G/I_{Sub} \). In other
words, this ratio is a measure of the significance of the degrading component. Using this ratio,
the non-degrading current components (\( I_B \) and \( I_{DT} \)) will become less noteworthy because these
components exist in both the gate and substrate currents and the ratio could somewhat eliminate
their effect in the gate and substrate currents. With this approach, we found that the device
lifetime can be plotted as an exponential function of \( I_G/I_{Sub} \) instead of the power law; namely, the
lifetime can be expressed as

\[
\tau = \tau_0 \exp(\alpha I_G / I_{Sub}) 
\]

where the fitting parameters \( \tau_0 \) is in the dimension of \([s]\) and \( \alpha \) is dimensionless. Expression (5.2)
indicates that the device lifetime can be improved with increasing \( I_G/I_{Sub} \) ratio. Figure 27 plots
the lifetime versus \( I_G/I_{Sub} \) based on the empirical relationship suggested in (5.2) for MOS devices
with channel lengths of 0.18 and 0.25 \( \mu \)m. Very good fittings are obtained. The values of the
fitting parameters are also showed in the figure. When compared to the power-law models (using
either substrate current or gate current as the variable), the present fittings yield a more
reasonable range for the values of the fitting parameters. In addition, we can assign the model
parameters with unambiguous dimensions.
Figure 28  Plot of lifetime as a function of gate/substrate current ratio for MOS transistor with 0.18 μm gate length. Markers are experimental data and lines are exponential fitting using Eq. (5.2). Table inserted lists the values of fitting parameters.

Figure 29  Relationship between threshold voltage shift and transconductance degradation measured for MOS devices having three different channel lengths.
Figure 30  Exponential fit of transconductance lifetime with the gate current/substrate current ratio for deep submicron devices. The lifetime represents the duration for making 10% transconductance degradation at the substrate current. Markers are experimental data and lines are exponential fitting using Eq. (5.2).

Comparison between the post-stressed transconductance ($G_m$) degradation and $V_T$ shift can also provide useful insights. Unlike the threshold voltage degradation, the origins of $G_m$ degradation are twofold. The transconductance can be degraded due to the threshold voltage shift and mobility degradation resulting from charge trapping and interface trap generation [40]. Thus $G_m$ will be degraded more severely than the threshold voltage for the same hot-carrier stressing. Moreover, as indicated in Figure 29, the transconductance degradation rate tends to slow down or saturate for large threshold voltage degradation. This trend suggests that the degradation rate of mobility is much slower than that of threshold voltage degradation. Nevertheless, the
transconductance degradation can still be fitted very well with the exponential function in (5.2) using \( I_G/I_{Sub} \) as the degradation variable, as shown in Figure 30. In this figure, the MOS lifetime is defined as the time when \( G_m \) degrades 10% from its initial value. This result again demonstrates that \( I_G/I_{Sub} \) is a good measure of the physical mechanisms underlying the deep-submicron MOS transistor degradation.

5.4 Discussions

Although the power-law degradation models are often used in fitting the experimental data of hot-carrier induced degradation, non-power law relationships have also been reported [40-43]. A disadvantage of the power law fitting is that its fitting parameters have arbitrary dimensions (and thus it is impossible to establish the physics and relationship with the device parameters) [42]. In the present model, the model parameters have unambiguous dimensions. In addition, the range of the parameters’ values is more reasonable and well behaved than that of the power-law models (see Figure 27).

Meanwhile, the extrapolation of the conventional power-law methods is also questionable. It implies that the VT shift can be increased without limit as the stressing goes on. The degradable quantities, e.g. Si-Si bonds or hydrogen bonds, will finally consume up and the degradation will reach a maximum value [42, 51-53]. It has long been suspected that the power-law fitting cannot represent well the stress-induced degradation of the MOS devices for all cases [42]. Depending on different trapping and generation rates, the degradation behavior in fact can be modeled in exponential law, power law, or exponential law with a quasi-saturation region [42]. An exponential law with the ratio \( I_G/I_{Sub} \) has been proposed in this work and it is encouraging that
such an empirical model fits very well both the threshold voltage and transconductance degradation behavior in advanced MOS devices.

In summary, although the present model is still an empirical one, the correct device physics is indeed imbedded in the ratio $I_G/I_{Sub}$, thereby making the proposed method more effective. In addition, the fitting parameters are well behaved and vary within a reasonable range. Note that expression (5.2) is also valid in extreme cases. When there is no substrate current (no hot carriers generated), the lifetime will be infinite. When the substrate current is extremely large, the lower bound of the lifetime is $\tau_0$, which indicates that the device degradation reaches a maximum value. When the gate current approaches zero, severe degradation occurs because most of charges are trapped in the oxide and produces large threshold voltage shift and transconductance degradation. The lifetime is improved when the gate current is large (e.g. with direct tunneling in the oxide) because the amount of charge trapping in the oxide is reduced. Of course, further experimental validation and investigation on the relationship between model parameters and devices will help to make the present model with stronger physical justification.

5.5 Conclusion

In summary, we have shown clearly that the conventional power-law empirical models for MOS lifetime versus substrate/gate current characteristics are valid only for the cases of relatively long channel devices and/or relatively small stress conditions. These models underestimate the lifetime for deep-submicron MOS devices. This effect can be attributed to the “non-degrading” components of the substrate and gate currents. A simple and accurate empirical expression correlating the MOS lifetime with the ratio of gate to substrate current has been
proposed, and it can serve as an effective alternative to the power-law models for the lifetime prediction of modern and future MOS devices.
6. A SPICE-LIKE RELIABILITY MODEL FOR DEEP-SUBMICRON CMOS TECHNOLOGY

6.1 Introduction

Due to continue down scaling, the channel electric field increases and the hot-carrier (HC) effect becomes more significant [54]. When the oxide thickness is scaled down to 3 nm, deep-submicron nMOS transistors have different reliability mechanism compare with the long-channel devices [55-56]. As a result, the conventional modeling for hot-carrier aging is questionable for deep-submicron devices, and a systematic method is needed for predicting the lifetime of the devices and circuits.

In this paper, we develop a Spice-like reliability model for advanced radio frequency RF MOS devices and implement the model into SpectreRF circuit simulator via Verilog-A HDL (Hardware Description Language).

6.2 Methodology

While many studies have been devoted to the field of MOSFET reliability, most of the works were focused on the device-level modeling [57-60] and not much attention has been paid to develop a model which is suitable for reliability simulation of MOS circuits. There is no new systemic and transplantable methodology to study MOS circuit performance degradations due to the hot-carrier effects. A widely used reliability simulation tool called the BERT (Berkeley Reliability Tool) was introduced in 1993.
We propose a new and improved methodology to model MOS reliability, and the flowchart is shown in Figure 31.

![Flowchart of RF circuits performance degradation](image)

**Figure 31** A methodology of RF circuits performance degradation making use of reliability simulation

First of all, 0.18-micron nMOS devices having different channel lengths are stressed in different dc bias conditions and the degraded MOS parameters are extracted. Most conventional methods apply the measured fresh and degraded device model files to Cadence SpectreRF simulation and then obtain the degraded RF circuit performance. Other methods combine Berkeley Reliability Tools (BERT) with Cadence SpectreRF to simulate the RF MOS circuit performance degradation. The first method ignores the fact that the degradation would depend
on the stress conditions, and each transistor in the circuit should experience different stress during operation. The second method can give a more accurate circuit degradation prediction but it completely depends on the BERT model, which assume all Spice model parameters degradation will obey the equations

\[
\Delta D = f(A GE) \quad (6.1)
\]

\[
A GE = \int_0^\tau \frac{I_{DS}}{W \cdot H_S} \left[ \frac{I_{SUB}}{I_{DS}} \right]^{m_S} dt \quad (6.2)
\]

where \( \Delta D \) is the amount of degradation suffered by any MOSFET device parameters, \( W \) refers to the device width, \( H_S \) and \( m_S \) are determined experimentally from a given technology, \( I_{SUB} \) is the substrate current, \( I_{DS} \) the drain current, and \( \tau \) is the stress time.

As a matter of fact, thinner gate oxide nMOS transistors have better reliability than that predicted by (6.1) over a wide range of bias conditions and gate lengths [61]. It is obviously that new degradation mechanism is needed in evaluating submicron nMOS with an ultra-thin gate oxide.

6.3 Lifetime determination

The devices under study are n-channel MOSFETs fabricated using the 0.18 \( \mu \)m CMOS technology, and the following channel lengths are considered: 0.5, 0.25, and 0.18 \( \mu \)m. The channel width is 10 \( \mu \)m, and device make-ups include P-well, N-well, threshold-adjust implant, and retrograde doping profiles. These devices are stressed over a relatively short period of time
at different bias conditions, and the degradation of transconductance $G_m$ and threshold voltage $V_{TH}$ are measured in the linear regions. Based on these short-term stress data, the long-term degradation and lifetime are then projected based on a time-dependent degradation law. The lifetime is defined as the time when $G_m$ and $V_{TH}$ degrades 10% from its initial value. To predict the long-term $G_m$ and $V_{TH}$ degradation and thus the MOS lifetime, we use the well-known power law, which has the form of

$$\frac{\Delta D}{D} = A \cdot t^n$$  \hspace{1cm} (6.3)

An extraction method is needed to determine the values of the two parameters ($C$ and $n$) associated with the power law. The conventional way to do this is to arrange the short-term stress data on the log-log scale and conduct the fitting scheme. Recently, we have developed an improved extraction method that arranges the short-term stress data on the exponential-exponential scale [62]. The improved method leads to a much better accuracy than the conventional method. Based on this new method, we have extrapolated the lifetimes of nMOS devices at different stress conditions. It has been observed experimentally that lifetime $\tau$ versus $I_{SUB}$ characteristics are not a function of $L$ [62]. The results are given in Figure 32 and can be fitted using the following expression:

$$\tau = K \cdot \left(\frac{I_{SUB}}{W}\right)^{-B}$$  \hspace{1cm} (6.4)
Figure 32  Transconductance lifetime versus substrate current obtained from measurements and fitting.

Figure 33  Threshold voltage lifetime versus substrate current obtained from measurements and fitting.

Similar trend for the lifetime based on the threshold voltage shift can be seen in Figure 33.
6.4 Reliability model development

As it is well known that CADENCE SPECTRE supports all Berkeley MOS models including BSIM3v3 model, which can be thought of as an improved Berkeley SPICE that address several numerical problems and the inadequacies in simulation for RF circuits [63].

In BSIM3v3 model, two parameters, threshold voltage $V_{TH}$ and mobility $\mu_{eff}$, influence most significantly the MOSFET DC and RF performance. The influence of BSM3vs parameter change on single MOS circuit DC and RF performance are showed in Table 5 and 6. In DC performance, we choose $I_{DS}$ degradation at $V_G = 1.6$ v and $V_D = 0.1$ v and 1.8 v seperatly. The S21 magnitude degradations are also simulated at $V_G = 0.9$ v, $V_D = 1.8$ v as monitor of AC performance.

Table 5 The influence of BSIM DC parameters on single MOS circuit performance

<table>
<thead>
<tr>
<th>BSIM Parameters</th>
<th>BSIM Parameter 10% change</th>
<th>BSIM Parameter 30% change</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DC performance</td>
<td>AC performance</td>
</tr>
<tr>
<td></td>
<td>0.1 v 1.8 v 1G 3G</td>
<td>0.1 v 1.8 v 1G 3G</td>
</tr>
<tr>
<td>$V_{TH0}$</td>
<td>4.08% 5.64% 0.65% 0.64%</td>
<td>12.35% 16.73% 2.52% 2.41%</td>
</tr>
<tr>
<td>$U_0$</td>
<td>4.83% 2.42% 1.36% 1.23%</td>
<td>15.46% 8.48% 5.14% 4.62%</td>
</tr>
<tr>
<td>$U_A$</td>
<td>2.00% 0.98% 0.69% 0.67%</td>
<td>5.66% 2.88% 2.09% 2.00%</td>
</tr>
<tr>
<td>$U_B$</td>
<td>3.16% 1.55% 1.43% 1.40%</td>
<td>8.72% 4.51% 3.87% 3.74%</td>
</tr>
<tr>
<td>$E_{TAB}$</td>
<td>&lt;0.1% &lt;0.1% &lt;0.1% &lt;0.1%</td>
<td>&lt;0.1% 0.19% &lt;0.1% &lt;0.1%</td>
</tr>
<tr>
<td>$P_{DIBLC2}$</td>
<td>&lt;0.1% &lt;0.1% 1.42% 1.12%</td>
<td>&lt;0.1% &lt;0.1% 4.10% 5.33%</td>
</tr>
<tr>
<td>$J_{SW}$</td>
<td>&lt;0.1% &lt;0.1% &lt;0.1% &lt;0.1%</td>
<td>&lt;0.1% &lt;0.1% &lt;0.1% &lt;0.1%</td>
</tr>
<tr>
<td>$J_S$</td>
<td>&lt;0.1% &lt;0.1% &lt;0.1% &lt;0.1%</td>
<td>&lt;0.1% &lt;0.1% &lt;0.1% &lt;0.1%</td>
</tr>
<tr>
<td>$P_B$</td>
<td>&lt;0.1% &lt;0.1% &lt;0.1% 0.17%</td>
<td>&lt;0.1% &lt;0.1% 0.19% 0.47%</td>
</tr>
</tbody>
</table>

63
Table 6 The influence of BSIM RF parameters on single MOS circuit performance

<table>
<thead>
<tr>
<th>BSIM Parameters</th>
<th>BSIM Parameter 10% change</th>
<th>BSIM Parameter 30% change</th>
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<tr>
<td></td>
<td>AC performance</td>
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<td>1G</td>
<td>3G</td>
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<tr>
<td>Cit</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
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<tr>
<td>CGSO</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>CGDO</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>CGBO</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>MJ</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>PBSW</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>MJSWG</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>PBSWG</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>MJJSWG</td>
<td>&lt;0.1%</td>
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</tr>
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</table>

It is obviously that only $V_{TH}$ and $\mu_{eff}$ have the most significant influence on circuit performance.

The threshold voltage $V_{TH}$ in BSIM3 can be expressed as

$$V_{TH} = V_{th0} + \delta_{NF}(\Delta V_{T, body\_effect} - \Delta V_{T, charge\_sharing} - \Delta V_{T, DIBL}$$

$$+ \Delta V_{T, reverse\_short\_channel} + \Delta V_{T, narrow\_width} + \Delta V_{T, small\_size}) \quad (6.5)$$

It can also be expressed empirically as
Here, $V_{GS\_max}$ and $I_{DS\_max}$ are $V_{GS}$ and $I_{DS}$ at maximum transconductance $G_m$. As shown in Figure 34, simulated and extracted $V_T$ is agreeing with each other.

Figure 34  Comparison of threshold voltage $V_T$ extracted from $I_{DS}$ vs $V_{DS}$ using equation 6.6 with simulation $V_T$ from BSIM 3v3 model

At a fixed stress condition, the degradation of $V_T$ will obey the power law [64].

$$\frac{dV_T}{V_T(0)} = A \cdot t^n$$

(6.7)
Where $V_T(0)$ is the threshold voltage of fresh device, and $A$ and $n$ are parameters to be extracted. Different stress conditions (different substrate current $I_{SUB}$) will give rise to different $A$ and $n$. Figure 35 compares the measured and modeled threshold voltage shift, and Figure 36 and 37 show the extracted values of $A$ and $n$.

![Graph showing threshold voltage shift over time](image)

For a fixed $I_{sub}$

$\Delta V_{TH, extracted} = A t^n$

For a fixed $I_{sub}$

Figure 35 Extraction of coefficient $A$ and $n$ from time dependent $V_T$ shift.
Figure 36  Fitting data of $V_T$ coefficient A at different substrate current $I_{SUB}$.

Figure 37  Fitting data of $V_T$ coefficient n at different substrate current $I_{SUB}$.
Based on above results, we obtain the following equation, which can be implemented in CADENCE SPECTRE via Verilog-A language,

\[
V_{TH_{deg}} = V_{TH_{fres}} \left[ 1 + (1191.78184 \times I_{SUB}^{1.43805}) \times t^{0.58747} \right] \quad (6.8)
\]

As mentioned before, mobility is another important parameter that can affect MOSFET device DC and RF performances. In BSIM3v3 model, effective mobility \( \mu_{eff} \) can be calculated from three different models:

- **Model 1**
  \[
  \mu_{eff} = \frac{U_0}{1 + (U + U_C \cdot V_{BS}) \left( \frac{V_{GS} + V_T}{TOX} \right) + U_B \left( \frac{V_{GS} + V_T}{TOX} \right)^2}
  \]

- **Model 2**
  \[
  \mu_{eff} = \frac{U_0}{1 + (U + U_C \cdot V_{BS}) \left( \frac{V_{GS} - V_T}{TOX} \right) + U_B \left( \frac{V_{GS} - V_T}{TOX} \right)^2}
  \]

- **Model 3**
  \[
  \mu_{eff} = \frac{U_0}{1 + U_A \left[ \left( \frac{V_{GS} + V_T}{TOX} \right) + U_B \left( \frac{V_{GS} + V_T}{TOX} \right)^2 \right] (1 + U_C \cdot V_{BS})}
  \]

\( U_0 \) is a key parameter for \( \mu_{eff} \) and can be modeled as

\[
U_0 = \frac{G_m \cdot L}{C_{ox} \cdot W \cdot V_{DS}} \quad (6.9)
\]
As shown in Figure 38, we can use equation 6.9 to extract $U_0$ from transconductance experiment data and implement it into $\mu_{\text{eff}}$ in BSIM 3v3 model equation. Figure 39 shows the calculated mobility degradation and Figure 40 and 41 show the extracted $A$ and $n$ coefficients.

![Comparison of mobility $U_0$ extracted from $G_m$ vs $V_G$ using equation 6.9 with simulation $U_0$ from BSIM 3v3 model.](image)

Figure 38   Comparison of mobility $U_0$ extracted from $G_m$ vs $V_G$ using equation 6.9 with simulation $U_0$ from BSIM 3v3 model.
Figure 39  Extraction of coefficient $A$ and $n$ from time dependent $U_0$ shift.

Figure 40  Fitting data of $U_0$ coefficient $A$ at different substrate current $I_{SUB}$. 
Finally, $U_0$ can be expressed as

$$U_{0_{deg}} = U_{0_{fresh}} (1 - (35.85177 \times I_{SUB}^{0.99024}) \times t^{0.469913}) \quad (6.10)$$

We can easily implement the above equations into BSIM3 model [65]. Figure 42 (a) and (b) are our Verilog-A codes and the schematic in CADENCE.
DBU_CSAF макс = T3 + theta(0/64);
DBU_CSAF = aDBU_CSAF_0 + Wds;

after stress Vth

Vth = \((1 + 1191.76194^{pow(SUBCURR, 1.43805) + pow(TIMEZDH, 0.66740, 0.615774)}) \times (T1 + T2) \times (1 - T1 - DBU_CSAF)\);

// end of Vth calculation

// Calculate n */
tmp2 = nfactor * DSSS / Xdes;
tmp3 = cosx - cosch + Vbseff + cosx * Wds;
tmp4 = (tmp2 + tmp3 + Theta0 + c12) / cos;
if (tmp4 >= 0.5)
  n = 1.0 + tmp4;
else
  if (n >= (a11))
    Lambda = a2;
    if (Lambda = a2)
      begin
        T0 = \(1 + a2\);
        T1 = T0 + a11 * Vbseff - 0.0001;
        Lambda = a2 + T0 - 0.5 * (T1 + T2);
      end
    else
      begin
        T1 = a2 + a11 * Vbseff - 0.0001;
        T2 = \(sqrt(T1) \times T1 \times 0.0001 \times a2\);
        Lambda = a2 + T1 + T2;
      end
      end

// after stress mobility

ueff = \((1 - 35.6637^{pow(SUBCURR, -2.99244) + pow(TIMEZDH, 0.469913)}) \times (usamp / Dens1)\);

/* Saturation Drain Voltage Vdsat */
Vdsat = ueff * vsextmp \times cos;
Vdsatds = Vdsat \times Rds;
Exst = 2.0 \times vsextmp / ueff;
ExstL = Exst \times Lef;

/* sqrt() */
if (a1 == 0.0)
  Lambda = a2;
else if (a11 > 0.0)
  /* Added to avoid the discontinuity problem caused by a1 and a2 (Lambda) */
  begin
    T0 = 1.0 + a2;
    T1 = T0 + a11 * Vbseff - 0.0001;
    Lambda = a2 + T0 - 0.5 * (T1 + T2);
  end
else
  begin
    T1 = a2 + a11 * Vbseff - 0.0001;
    T2 = \(sqrt(T1) \times T1 \times 0.0001 \times a2\);
    Lambda = 0.5 \times (T1 + T2);
  end

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6.5 Prediction of DC and RF performance degradation

Figure 43 (a) and (b) are results simulated and measured from the reliability model developed in the preceding section. Here, nMOS devices have been stressed at $V_D = 2.4 \, \text{V}$ and $V_G = 1.5 \, \text{V}$ for 3000 S and 10000 S. The drain current was measured at gate voltages of 1.1 V and 1.6 V, and the magnitude of $S_{21}$ was measured at $V_D = 1.8 \, \text{V}$ and $V_G = 1.1 \, \text{V}$. It is obvious that the reliability model developed can evaluate the DC and RF performance degradation accurately.
Figure 43  Comparison simulation results and measured data for fresh device and stressed after 3000s and 10000s.

Figure 44  Comparison simulation results and measured data for fresh device and stressed after 3000s and 10000s.
6.6 Conclusion

Having the ability to predict the time- and stress-dependent degradation is very critical to the device and circuit design engineers. An accurate, simple, and BSIM-based MOS reliability model has been developed in this paper. The model was developed based on the characterization of two important BSIM parameters: mobility and threshold voltage. Very good agreement between the measured and simulated DC and RF performance has been demonstrated.
/*****************************************************************
/* Berkeley BSIM3v3.2.0 & BSIM3v3.2.4 (default) Verilog-A model */
*******************************************************************/

// UPDATED March 19 2004
// Contributed By:
// Geoffrey Coram, Ph.D Senior CAD Engineer Analog Devices, Inc.
// Edited By
// Zhi Cui, Ph.D University of Central Florida

`define VOLTAGE_MAXDELTA 0.3
`include "discipline.h"

// Following line must be uncomment for using NQS charge model (NQSMOD=1)
`ifdef NQSMOD

****** Physical constants *****
`define EPSOX 3.453133e-11
`define KboQ 8.617087e-5
`define EPSSI 1.03594e-10
`define Charge_q 1.60219e-19
`define CONSTvt0 0.02586419
`define CONSTroot2 1.41421356

****** Mathematical constants and constants of limitation *****
`define PI 3.141592654
`define EXP_THRESHOLD 34.0
`define MIN_EXP 1.713908431e-15
`define MAX_EXP 5.834617425e14

****** Constants for the model *****
`define DELTA_1 0.02
`define DELTA_3 0.02
`define DELTA_4 0.02

module a_mos_18_10(drain, gate, source, bulk);
  inout drain, gate, source, bulk;
  electrical drain, gate, source, bulk;
  electrical drainp, sourcep; // internal nodes
`ifdef NQSMOD
electrical q;               // NQS charge model node
`endif

// degradation parameters
`include "/export/home/zhicui/verilogalib/after_stress_18_10.h"
`include "/export/home/zhicui/verilogalib/time_zhi.h"

****** Device Parameters ******
parameter real L       =  1.8e-7;
parameter real W       =  1.6e-4;

****** Model Selectors/Controllers ******
parameter real MOBMOD    =  1;   // Mobility model selector

*** Length dependance model parameters ***
parameter real LCDSC     =  0.0;  // Length dependence of cdsc

// stress time
integer   Fatal_Flag;
integer   stressfile;

// Parameter define
real      tox, cox, vth0, nch, ngate, uc, uc1, u0, tnom;

// Depletion capacitance related variables

// Charge model related variables

// extrinsic capacitance related variables

// NQS model
`ifdef NQSMOD
real sxpart, dxpart;
real qcheq , qdump, qdef, gtau_drift, gtau_diff, ScalingFactor, gtau;
real cqcheq, cqdef;
`endif
real cqgate, cqdrn, cqbulk;

analog
begin

I(drain, drainp) <=+ NRD*RSH * V(drain, drainp);
I(source, sourcep) <=+ NRS*RSH * V(source, sourcep);

@((initial_step("dc","ac","tran","sp") )
begin
tox = TOX;
cox = 3.453133e-11 / tox;
//Paramter replacement
`ifdef NQSMOD
   ScalingFactor = 1.0e-9;
`endif
...
// calculating ungiven parameters
...
// Channel length dependance parameters
...
// Cross-term dependence parameters
...
Tempr = Stemperature;
Tnom = tnom;
TRatio = Tempr / Tnom;

factor1 = sqrt(`EPSSI / `EPSOX * tox);

Vtm0 = `KboQ * Tnom;
Eg0 = 1.16 - 7.02e-4 * Tnom * Tnom / (Tnom + 1108.0);
   ni = 1.45e10 * (Tnom / 300.15) * sqrt(Tnom / 300.15) * exp(21.5565981 - Eg0 / (2.0 * Vtm0));

vtm = `KboQ * Tempr;
\[ \text{Eg} = 1.16 - 7.02e^{-4} \times \text{Tempr} \times \text{Tempr} / (\text{Tempr} + 1108.0); \]

if (Tempr != Tnom)
begin
\[ T0 = \text{Eg0} / \text{Vtm0} - \text{Eg} / \text{vtm} + \text{jctTempExponent} \times \ln(\text{Tempr} / \text{Tnom}); \]
\[ T1 = \exp(T0 / \text{jctEmissionCoeff}); \]
\[ \text{jctTempSatCurDensity} = \text{jctSatCurDensity} \times T1; \]
\[ \text{jctSidewallTempSatCurDensity} = \text{jctSidewallSatCurDensity} \times T1; \]
d
dend
else
begin
\[ \text{jctTempSatCurDensity} = \text{jctSatCurDensity}; \]
\[ \text{jctSidewallTempSatCurDensity} = \text{jctSidewallSatCurDensity}; \]
d
dend

if (jctTempSatCurDensity < 0.0)
\[ \text{jctTempSatCurDensity} = 0.0; \]
if (jctSidewallTempSatCurDensity < 0.0)
\[ \text{jctSidewallTempSatCurDensity} = 0.0; \]

\/* Temperature dependence of D/B and S/B diode capacitance */
\[ \text{delTemp} = \text{Stemperature} - \text{tnom}; \]
\[ T0 = \text{TCJ} \times \text{delTemp}; \]

if (T0 >= -1.0)
begin
if (VERSION == 3.24)
\[ \text{unitAreaTempJctCap} = \text{unitAreaJctCap} \times (1.0 + T0); \]
else
\[ \text{unitAreaJctCap} = \text{unitAreaJctCap} \times (1.0 + T0); \]
don
else if (unitAreaJctCap > 0.0)
begin

if (VERSION == 3.24)
    unitAreaTempJctCap = 0.0;
else
    unitAreaJctCap = 0.0;
$strobe ("Temperature effect has caused cj to be negative. Cj is clamped to zero.");
end

T0 = TCJSW * delTemp;
if (T0 >= -1.0)
    begin
    if (VERSION == 3.24)
        unitLengthSidewallTempJctCap = unitLengthSidewallJctCap * (1.0 + T0);
    else
        unitLengthSidewallJctCap = unitLengthSidewallJctCap * (1.0 + T0);
    end
else if (unitLengthSidewallJctCap > 0.0)
    begin
    if (VERSION == 3.24)
        unitLengthSidewallTempJctCap = 0.0;
    else
        unitLengthSidewallJctCap = 0.0;
    end
$strobe ("Temperature effect has caused cjsw to be negative. Cjsw is clamped to zero.");
end

T0 = TCJSWG * delTemp;
if (T0 >= -1.0)
    begin
    if (VERSION == 3.24)
        unitLengthGateSidewallTempJctCap = unitLengthGateSidewallJctCap * (1.0 + T0);
    else
        unitLengthGateSidewallJctCap = unitLengthGateSidewallJctCap * (1.0 + T0);
    end
else if (unitLengthGateSidewallJctCap > 0.0)
    begin
if (VERSION == 3.24)
    unitLengthGateSidewallTempJctCap = 0.0;
else
    unitLengthGateSidewallJctCap = 0.0;
$strobe ("Temperature effect has caused cjswg to be negative. Cjswg is clamped to zero.");
end

PhiB = bulkJctPotential - TPB * delTemp;
    if (PhiB < 0.01)
        begin
            PhiB = 0.01;
        $strobe ("Temperature effect has caused pb to be less than 0.01. Pb is clamped to 0.01.");
        end

    PhiBSW = sidewallJctPotential - TPBSW * delTemp;
        if (PhiBSW <= 0.01)
            begin
                PhiBSW = 0.01;
            $strobe ("Temperature effect has caused pbsw to be less than 0.01. Pbsw is clamped to 0.01.");
            end

    PhiBSWG = GatesidewallJctPotential - TPBSWG * delTemp;
        if (PhiBSWG <= 0.01)
            begin
                PhiBSWG = 0.01;
            $strobe ("Temperature effect has caused pbswg to be less than 0.01. Pbswg is clamped to 0.01.");
            end

/* End of junction capacitance */

/**** Effective channel length and width calculation ****/
Ldrm = L;
Wdrm = W;
T0 = pow(Ldrn, LLN);
    T1 = pow(Wdrn, LWN);

tmp1 = LL / T0 + LW / T1 + LWL / (T0 * T1);
    dl    = LINT + tmp1;

tmp2 = LLC / T0 + LWC / T1 + LWC / (T0 * T1);
    dlc   = dlc + tmp2;

T2 = pow(Ldrn, WLN);
    T3 = pow(Wdrn, WWN);

tmp1 = WL / T2 + WW / T3 + WWL / (T2 * T3);
    dw    = WINT + tmp1;

tmp2 = WLC / T2 + WWC / T3 + WWLC / (T2 * T3);
    dwc   = DWC + tmp2;

leff = L - 2.0 * dl;

    if (leff <= 0.0)
    begin
        $strobe("BSIM3: device %m: Effective channel length <= 0");
        $finish(1);
    end

weff = W - 2.0 * dw;
    if (weff <= 0.0)
    begin
        $strobe("BSIM3: device %m: Effective channel width <= 0");
        $finish(1);
    end

leffCV = L - 2.0 * dlc;
    if (leffCV <= 0.0)
begin
$strobe ("BSIM3: device %m: Effective channel length for C-V <= 0");
$finish(1);
end

weffCV = W - 2.0 * dwc;
if (weffCV <= 0.0)
begin
$strobe ("BSIM3: device %m: Effective channel width for C-V <= 0");
$finish(1);
end

if (BINUNIT == 1)
begin
Inv_L  = 1.0e-6 / leff;
Inv_W  = 1.0e-6 / weff;
Inv_LW = 1.0e-12 / (leff * weff);
end
else
begin
Inv_L  = 1.0 / leff;
Inv_W  = 1.0 / weff;
Inv_LW = 1.0 / (leff * weff);
end

cdsc  = CDSC + LCDSC * Inv_L + WCDSC * Inv_W + PCDSC * Inv_LW;
...

abulkCVfactor = 1.0 + pow((clc / leffCV), cle);
T0 = (TRatio - 1.0);
ua = ua + ua1 * T0;
ub = ub + ub1 * T0;
uc = uc + uc1 * T0;
if (u0 > 1.0)
    u0 = u0 / 1.0e4;
\[ u\text{temp} = u0 \times \text{pow}(\text{TRatio}, \text{ute}); \]
\[ v\text{sat}\text{temp} = \text{vsat} - at \times T0; \]
\[ \text{rds}0 = (\text{rdsw} + \text{prt} \times T0) / \text{pow(weff} \times 1E6, \text{wr}); \]

// *** check model and instance parameters ***

```
Fatal_Flag = 0;
if (nlx < -leff)
    begin
        $\text{strobe ("Fatal: Nlx = %g is less than -Leff.", nlx);}
        Fatal_Flag = 1;
    end
if (tox <= 0.0)
    begin
        $\text{strobe ("Fatal: Tox = %g is not positive.", tox);}
        Fatal_Flag = 1;
    end
    if (TOXM <= 0.0)
        begin
            $\text{strobe ("Fatal: Toxm = %g is not positive.", TOXM);}
            Fatal_Flag = 1;
        end
    if (npeak <= 0.0)
        begin
            $\text{strobe ("Fatal: Nch = %g is not positive.", npeak);}
            Fatal_Flag = 1;
        end
    if (nsub <= 0.0)
        begin
            $\text{strobe ("Fatal: Nsub = %g is not positive.", nsub);}
            Fatal_Flag = 1;
        end
    if (ngate < 0.0)
        begin
            $\text{strobe ("Fatal: Ngate = %g Ngate is not positive.", ngate);}
            Fatal_Flag = 1;
        end
```

```
end
if (ngate > 1.0e25)
begin
$strobe("Fatal: Ngate = %g Ngate is too high", ngate);
Fatal_Flag = 1;
end
if (xj <= 0.0)
begin
$strobe("Fatal: Xj = %g is not positive.", xj);
Fatal_Flag = 1;
end
if (dvt1 < 0.0)
begin
$strobe("Fatal: Dvt1 = %g is negative.", dvt1);
Fatal_Flag = 1;
end
if (dvt1w < 0.0)
begin
$strobe("Fatal: Dvt1w = %g is negative.", dvt1w);
Fatal_Flag = 1;
end
if (w0 == -weff)
begin
$strobe("Fatal: (W0 + Weff) = 0 causing divided-by-zero.");
Fatal_Flag = 1;
end
if (dsub < 0.0)
begin
$strobe("Fatal: Dsub = %g is negative.", dsub);
Fatal_Flag = 1;
end
if (b1 == -weff)
begin
$strobe("Fatal: (B1 + Weff) = 0 causing divided-by-zero.");
Fatal_Flag = 1;
    end
if (u0temp <= 0.0)
begin
$strobe("Fatal: u0 at current temperature = %g is not positive.", u0temp);
Fatal_Flag = 1;
end

/* Check delta parameter */
if (delta < 0.0)
begin
$strobe("Fatal: Delta = %g is less than zero.", delta);
Fatal_Flag = 1;
end

if (vsattemp <= 0.0)
begin
$strobe("Fatal: Vsat at current temperature = %g is not positive.", vsattemp);
Fatal_Flag = 1;
end

/* Check Rout parameters */
if (pclm <= 0.0)
begin
$strobe("Fatal: Pclm = %g is not positive.", pclm);
Fatal_Flag = 1;
end
if (drout < 0.0)
begin
$strobe("Fatal: Drout = %g is negative.", drout);
Fatal_Flag = 1;
end
if (pscb2 <= 0.0)
begin
$strobe("Warning: Pscbe2 = %g is not positive.", pscb2);
end
if (unitLengthSidewallJctCap > 0.0 || unitLengthGateSidewallJctCap > 0.0)
if (drainPerimeter < weff)
    begin
        $strobe ("Warning: Pd = %g is less than W.", drainPerimeter);
    end
if (sourcePerimeter < weff)
    begin
        $strobe ("Warning: Ps = %g is less than W.", sourcePerimeter);
    end
if (noff_param < 0.1)
    $strobe ("Warning: Noff = %g is too small.", noff_param);
if (noff_param > 4.0)
    $strobe ("Warning: Noff = %g is too large.", noff_param);
if (voffcv_param < -0.5)
    $strobe ("Warning: Voffcv = %g is too small.", voffcv_param);
if (voffcv_param > 0.5)
    $strobe ("Warning: Voffcv = %g is too large.", voffcv_param);
if (IJTH < 0.0)
    begin
        $strobe ("Fatal: Ijth = %g cannot be negative.", IJTH);
        Fatal_Flag = 1;
    end
/* Check capacitance parameters */
if (clc < 0.0)
    begin
        $strobe ("Fatal: Clc = %g is negative.", clc);
        Fatal_Flag = 1;
    end
if (moin < 5.0)
    $strobe ("Warning: Moin = %g is too small.", moin);
if (moin > 25.0)
    $strobe ("Warning: Moin = %g is too large.", moin);
if ((acde < 0.4) && !(VERSION == 3.24)) ||
((acde < 0.4) && (VERSION == 3.24) && (CAPMOD == 3.0)))
    $strobe ("Warning: Acde = %g is too small.", acde);
    if (((acde > 1.6) && !(VERSION == 3.24)) ||
    ((acde > 1.6) && (VERSION == 3.24) && (CAPMOD == 3.0)))
    $strobe ("Warning: Acde = %g is too large.", acde);
    // *** end of parameters checking ***
if (PARAMCHK ==1)
    begin
    /* Check L and W parameters */
    if (leff <= 5.0e-8)
        $strobe ("Warning: Leff = %g may be too small.", leff);
    if (leffCV <= 5.0e-8)
        $strobe ("Warning: Leff for CV = %g may be too small.", leffCV);
    if (weff <= 1.0e-7)
        $strobe ("Warning: Weff = %g may be too small.", weff);
    if (weffCV <= 1.0e-7)
        $strobe ("Warning: Weff for CV = %g may be too small.", weffCV);
    /* Check threshold voltage parameters */
    if (nlx < 0.0)
        $strobe ("Warning: Nlx = %g is negative.", nlx);
    if (tox < 1.0e-9)
        $strobe ("Warning: Tox = %g is less than 10A.", tox);
    if (npeak <= 1.0e15)
        $strobe ("Warning: Nch = %g may be too small.", npeak);
    else if (npeak >= 1.0e21)
        $strobe ("Warning: Nch = %g may be too large.", npeak);
    if (nsub <= 1.0e14)
        $strobe ("Warning: Nsub = %g may be too small.", nsub);
    else if (nsub >= 1.0e21)
        $strobe ("Warning: Nsub = %g may be too large.", nsub);
    if ((ngate > 0.0) && (ngate <= 1.0e18))
        $strobe ("Warning: Ngate = %g is less than 1.E18cm^-3.", ngate);
    if (dvt0 < 0.0)
        $strobe ("Warning: Dvt0 = %g is negative.", dvt0);
if (abs(1.0e-6 / (w0 + weff)) > 10.0)
    $strobe ("Warning: (W0 + Weff) may be too small.");
/* Check subthreshold parameters */
if (nfactor < 0.0)
    $strobe ("Warning: Nfactor = %g is negative.", nfactor);
if (cdsc < 0.0)
    $strobe ("Warning: Cdsc = %g is negative.", cdsc);
if (cdscd < 0.0)
    $strobe ("Warning: Cdscd = %g is negative.", cdscd);
/* Check DIBL parameters */
if (eta0 < 0.0)
    $strobe ("Warning: Eta0 = %g is negative.", eta0);
/* Check Abulk parameters */
if (abs(1.0e-6 / (b1 + weff)) > 10.0)
    $strobe ("Warning: (B1 + Weff) may be too small.");
/* Check Saturation parameters */
if (a2 < 0.01)
begin
    $strobe ("Warning: A2 = %g is too small. Set to 0.01.", a2);
    a2 = 0.01;
end
else if (a2 > 1.0)
begin
    $strobe ("Warning: A2 = %g is larger than 1. A2 is set to 1 and A1 is set to 0.", a2);
    a2 = 1.0;
    a1 = 0.0;
end
if (rdsw < 0.0)
begin
    $strobe ("Warning: Rdsw = %g is negative. Set to zero.", rdsw);
    rdsw = 0.0;
    rds0 = 0.0;
end
else if ((rds0 > 0.0) && (rds0 < 0.001))
    begin
      $strobe ("Warning: Rds at current temperature = %g is less than 0.001 ohm. Set to zero.", rds0);
      rds0 = 0.0;
    end
if (vsattemp < 1.0e3)
  $strobe ("Warning: Vsat at current temperature = %g may be too small.", vsattemp);
if (pdibl1 < 0.0)
  $strobe ("Warning: Pdibl1 = %g is negative.", pdibl1);
if (pdibl2 < 0.0)
  $strobe ("Warning: Pdibl2 = %g is negative.", pdibl2);
/* Check overlap capacitance parameters */
if (cgdo_param < 0.0)
    begin
      $strobe ("Warning: cgdo = %g is negative. Set to zero.", cgdo_param);
      cgdo_param = 0.0;
    end
if (cgso_param < 0.0)
    begin
      $strobe ("Warning: cgso = %g is negative. Set to zero.", cgso_param);
      cgso_param = 0.0;
    end
if (cgbo_param < 0.0)
    begin
      $strobe ("Warning: cgbo = %g is negative. Set to zero.", cgbo_param);
      cgbo_param = 0.0;
    end
end/* loop for the parameter check for warning messages */
if (Fatal_Flag)
  $finish(1);
cgdo_param = (cgdo_param + cf) * weffCV;
  cgso_param = (cgso_param + cf) * weffCV;
  cgbo_param = cgbo_param       * leffCV;
T0      = leffCV * leffCV;
tconst = u0temp * elm / (cox * weffCV * leffCV * T0);
if ( !npeakGiven && gamma1Given )
begin
T0 = gamma1 * cox;
npeak = 3.021E22 * T0 * T0;
end
phi = 2.0 * Vtm0 * ln(npeak / ni);
sqrtPhi = sqrt(phi);
phis3 = sqrtPhi * phi;
Xdep0 = sqrt(2.0 * `EPSSI / (`Charge_q * npeak * 1.0e6)) * sqrtPhi;
li = sqrt(3.0 * xj * tox);
vbi = Vtm0 * ln(1.0e20 * npeak / (ni * ni));
cdep0 = sqrt( `Charge_q * `EPSSI * npeak * 1.0e6 / 2.0 / phi);
ldeb = sqrt( `EPSSI * Vtm0 / ( `Charge_q * npeak * 1.0e6)) / 3.0;
acde = acde * pow((npeak / 2.0e16), -0.25);
if ( k1Given || k2Given )
begin
if (!k1Given)
begin
$strobe("Warning: k1 should be specified with k2.");
k1 = 0.53;
end
if (!k2Given)
begin
$strobe("Warning: k2 should be specified with k1.");
k2 = -0.0186;
end
if (nsubGiven)
$strobe("Warning: nsub is ignored because k1 or k2 is given.");
if (xtGiven)
$strobe("Warning: xt is ignored because k1 or k2 is given.");
if (vbxGiven)
$strobe("Warning: vbx is ignored because k1 or k2 is given.");
if (gamma1Given)
Sstrobe ("Warning: gamma1 is ignored because k1 or k2 is given.");

if (gamma2Given)
    Sstrobe ("Warning: gamma2 is ignored because k1 or k2 is given.");
else
begin
if (!vbxGiven)
    vbx = phi - 7.7348e-4 * npeak * xt * xt;
    if (vbx > 0.0)
        vbx = -vbx;
    if (vbm > 0.0)
        vbm = -vbm;
    if (!gamma1Given)
        gamma1 = 5.753e-12 * sqrt(npeak) / cox;
    if (!gamma2Given)
        gamma2 = 5.753e-12 * sqrt(nsub) / cox;
    T0 = gamma1 - gamma2;
    T1 = sqrt(phi - vbx) - sqrtPhi;
    T2 = sqrt(phi * (phi - vbm)) - phi;
    k2 = T0 * T1 / (2.0 * T2 + vbm);
    k1 = gamma2 - 2.0 * k2 * sqrt(phi - vbm);
end
if (k2 < 0.0)
begin
    T0 = 0.5 * k1 / k2;
    vbsc = 0.9 * (phi - T0 * T0);
    if (vbsc > -3.0)
        vbsc = -3.0;
    else if (vbsc < -30.0)
        vbsc = -30.0;
end
else
vbsc = -30.0;
if (vbsc > vbm)
    vbsc = vbm;
if (!vfbGiven)
    begin
if (!vth0Given)
    vfb = TYPE * vth0 - phi - k1 * sqrtPhi;
else
    vfb = -1.0;
end
if (!vth0Given)
    vth0 = TYPE * (vfb + phi + k1 * sqrtPhi);
k1ox = k1 * tox / TOXM;
k2ox = k2 * tox / TOXM;
T1 = sqrt('EPSSI / EPSOX * tox * Xdep0);
T0 = exp(-0.5 * dsup * leff / T1);
theta0vb0 = (T0 + 2.0 * T0 * T0);
T0 = exp(-0.5 * drout * leff / T1);
T2 = (T0 + 2.0 * T0 * T0);
thetaRout = pdibl1 * T2 + pdibl2;
/* vfbzb for capMod 1, 2 & 3 */
tmp  = sqrt(Xdep0);
tmp1 = vbi - phi;
tmp2 = factor1 * tmp;
T0 = -0.5 * dvt1w * weff * leff / tmp2;
if (T0 > -'EXP_THRESHOLD)
    begin
    T1 = exp(T0);
    T2 = T1 * (1.0 + 2.0 * T1);
    end
else
    begin
    T1 = 'MIN_EXP;
    T2 = T1 * (1.0 + 2.0 * T1);
    end
T0 = dvto * T2;
T2 = T0 * tmp1;
T0 = -0.5 * dvto * leff / tmp2;
if (T0 > -'EXP_THRESHOLD)
  begin
  T1 = exp(T0);
  T3 = T1 * (1.0 + 2.0 * T1);
  end
else
  begin
  T1 = 'MIN_EXP;
  T3 = T1 * (1.0 + 2.0 * T1);
  end
T3 = dvto + T3 + tmp1;
T4 = tox * phi / (weff + w0);
T0 = sqrt(1.0 + nlx / leff);
T5 = k1ox * (T0 - 1.0) * sqrtPhi + (kt1 + kt1l / leff) * (TRatio - 1.0);
tmp3 = TYPE * vth0 - T2 - T3 + k3 * T4 + T5;
vfbzb = tmp3 - phi - k1 * sqrtPhi;
// End of vfbzb calculation
// process source/drain series resistance
drainConductance = sheetResistance * drainSquares;
  if (drainConductance > 0.0)
    drainConductance = 1.0 / drainConductance;
else
  drainConductance = 0.0;

sourceConductance = sheetResistance * sourceSquares;
  if (sourceConductance > 0.0)
    sourceConductance = 1.0 / sourceConductance;
else
  sourceConductance = 0.0;
Nvtm = vtm * jctEmissionCoeff;
  if ((sourceArea <= 0.0) && (sourcePerimeter <= 0.0))
\text{SourceSatCurrent} = 1.0e-14;

\text{else}

\text{SourceSatCurrent} = \text{sourceArea} * \text{jctTempSatCurDensity}
+ \text{sourcePerimeter} * \text{jctSidewallTempSatCurDensity};

\text{if} ((\text{SourceSatCurrent} > 0.0) \&\& (\text{IJTH} > 0.0))
\text{begin}

\text{vjsm} = \text{Nvtm} * \ln(\text{IJTH} / \text{SourceSatCurrent} + 1.0);

\text{if} (\text{VERSION} == 3.24)

\text{IsEvjsm} = \text{SourceSatCurrent} * \exp(\text{vjsm} / \text{Nvtm});

\text{end}

\text{if} ((\text{drainArea} <= 0.0) \&\& (\text{drainPerimeter} <= 0.0))

\text{DrainSatCurrent} = 1.0e-14;

\text{else}

\text{DrainSatCurrent} = \text{drainArea} * \text{jctTempSatCurDensity}
+ \text{drainPerimeter} * \text{jctSidewallTempSatCurDensity};

\text{if} ((\text{DrainSatCurrent} > 0.0) \&\& (\text{IJTH} > 0.0))
\text{begin}

\text{vjdm} = \text{Nvtm} * \ln(\text{IJTH} / \text{DrainSatCurrent} + 1.0);

\text{if} (\text{VERSION} == 3.24)

\text{IsEvjdmd} = \text{DrainSatCurrent} * \exp(\text{vjdm} / \text{Nvtm});

\text{end}
\text{end}

\text{//*********************************//}
\text{//****** End of initial_step ******//}
\text{//*********************************//}

\text{vbs} = \text{TYPE} * \text{V(bulk, sourcep)};
\text{vgs} = \text{TYPE} * \text{V(gate, sourcep)};
\text{vds} = \text{TYPE} * \text{V(drainp, sourcep)};

\text{`ifdef NQSMOD}
\text{qdef} = \text{TYPE} * \text{V(q)};
\text{`endif}

\text{vbd} = \text{vbs} - \text{vds};
vgd = vgs - vds;
vgb = vgs - vbs;

temp = $temperature;

// Source/drain junction diode DC model begins
if (SourceSatCurrent <= 0.0)
begin
    gbs = GMIN;
    cbs = gbs * vbs;
end
else
begin
    if (IJTH == 0.0)
    begin
        evbs = exp(vbs / Nvtm);
        gbs = SourceSatCurrent * evbs / Nvtm + GMIN;
        cbs = SourceSatCurrent * (evbs - 1.0) + GMIN * vbs;
    end
else
    begin
        if (vbs < vjsm)
        begin
            evbs = exp(vbs / Nvtm);
            gbs = SourceSatCurrent * evbs / Nvtm + GMIN;
            cbs = SourceSatCurrent * (evbs - 1.0) + GMIN * vbs;
        end
else
        begin
            if (VERSION == 3.24)
            begin
                T0 = IsEvjsm / Nvtm;
                cbs = IsEvjsm - SourceSatCurrent
                    + GMIN * vbs + T0 * (vbs - vjsm);
\begin{verbatim}
if (DrainSatCurrent <= 0.0)
  begin
    gbd = GMIN;
    cbd = gbd * vbd;
  end
else
  begin
    if (IJWT == 0.0)
      begin
        evbd = exp(vbd / Nvm);
        gbd = DrainSatCurrent * evbd / Nvm + GMIN;
        cbd = DrainSatCurrent * (evbd - 1.0) + GMIN * vbd;
      end
    else
      begin
        if (vbd < vjdm)
          begin
            evbd = exp(vbd / Nvm);
            gbd = DrainSatCurrent * evbd / Nvm + GMIN;
            cbd = DrainSatCurrent * (evbd - 1.0) + GMIN * vbd;
          end
        else
          begin

end
end
end
end
end
end
end
end
\end{verbatim}
begin
if (VERSION == 3.24)
begin
    T0 = IsEvjdm / Nvtm;
    cbd = IsEvjdm - DrainSatCurrent
        + GMIN * vbd + T0 * (vbd - vjdm);
end
else
begin
    T0 = (DrainSatCurrent + IJTH) / Nvtm;
    cbd = IJTH + GMIN * vbd + T0 * (vbd - vjdm);
end
gbd = T0 + GMIN;
end
// End of diode DC model

if (vds >= 0.0)
begin /* normal mode */
    mode = 1;
    Vds = vds;
    Vgs = vgs;
    Vbs = vbs;
end
else
begin /* inverse mode */
    mode = -1;
    Vds = -vds;
    Vgs = vgd;
    Vbs = vbd;
end
\[
\begin{align*}
T0 &= Vbs - \text{vbsc} - 0.001; \\
T1 &= \sqrt{T0 \times T0 - 0.004 \times \text{vbsc}}; \\
\text{Vbseff} &= \text{vbsc} + 0.5 \times (T0 + T1); \\
\end{align*}
\]

// Added to avoid the possible numerical problems due to computer accuracy.
// (See comments for diffVds)
if (Vbseff < Vbs)
    Vbseff = Vbs;
if (Vbseff > 0.0)
begin
    T0 = \phi \div (\phi + \text{Vbseff});
    \text{Phis} = \phi \times T0;
    \text{sqrtPhis} = \text{phis3} \div (\phi + 0.5 \times \text{Vbseff});
end
else
begin
    \text{Phis} = \phi - \text{Vbseff};
    \text{sqrtPhis} = \sqrt{\text{Phis}};
end

\text{Xdep} = \text{Xdep0} \times \text{sqrtPhis} \div \sqrt{\phi};

\text{Leff} = \text{leff};
\text{Vtm} = \text{vtm};

/*** Vth Calculation ***/
T3 = \sqrt{\text{Xdep}};
\text{V0} = \text{vbi} - \phi;

\text{T0} = \text{dvt2} \times \text{Vbseff};

if (T0 >= -0.5)
begin
\[ T1 = 1.0 + T0; \]
\[ T2 = dvt2; \]
end

else /* Added to avoid any discontinuity problems caused by dvt2 */
begin
\[ T4 = 1.0 / (3.0 + 8.0 * T0); \]
\[ T1 = (1.0 + 3.0 * T0) * T4; \]
\[ T2 = dvt2 * T4 * T4; \]
end

lt1 = factor1 * T3 * T1;

T0 = dvt2w * Vbseff;

if (T0 >= -0.5)
begin
\[ T1 = 1.0 + T0; \]
\[ T2 = dvt2w; \]
end
else /* Added to avoid any discontinuity problems caused by dvt2w */
begin
\[ T4 = 1.0 / (3.0 + 8.0 * T0); \]
\[ T1 = (1.0 + 3.0 * T0) * T4; \]
\[ T2 = dvt2w * T4 * T4; \]
end

ltw = factor1 * T3 * T1;

T0 = -0.5 * dvt1 * Leff / lt1;

if (T0 > -'EXP_THRESHOLD)
begin
\[ T1 = \exp(T0); \]
\[ \Theta_0 = T1 * (1.0 + 2.0 * T1); \]
```plaintext
end
else
begin
  T1 = `MIN_EXP;
  Theta0 = T1 * (1.0 + 2.0 * T1);
end

thetavth = dvt0 * Theta0;
Delt_vth = thetavth * V0;

T0 = -0.5 * dvt1w * weff * Leff / ltw;

if (T0 > `-EXP_THRESHOLD)
begin
  T1 = exp(T0);
  T2 = T1 * (1.0 + 2.0 * T1);
end
else
begin
  T1 = `MIN_EXP;
  T2 = T1 * (1.0 + 2.0 * T1);
end

T0 = dvt0w * T2;
T2 = T0 * V0;

TempRatio = temp / tnom - 1.0;
T0 = sqrt(1.0 + nlx / Leff);
T1 = k1ox * (T0 - 1.0) * sqrtPhi
  + (kt1 + kt1l / Leff + kt2 * Vbseff) * TempRatio;

tmp2 = tox *phi / (weff + w0);

T3 = etato + etab * Vbseff;
```
if (T3 < 1.0e-4) /* avoid discontinuity problems caused by etab */
begin
    T9 = 1.0 / (3.0 - 2.0e4 * T3);
    T3 = (2.0e-4 - T3) * T9;
    T4 = T9 * T9;
end
else
    T4 = 1.0;

ddIBL_Sft_dVd = T3 * theta0vb0;
DIBL_Sft = dDIBL_Sft_dVd * Vds;

//**after stress Vth**/

Vth = (1+(1191.78184*pow(SUBCURRENT,1.43805)*pow(TIMEZHI*86400,0.58747)))
    *(TYPE * vth0 - k1 * sqrtPhi
         + k1ox * sqrtPhis
         - k2ox * Vbseff
         - Delta_vth - T2
         + (k3 + k3b * Vbseff) * tmp2 + T1 - DIBL_Sft);

/*** end of Vth calculation ***/

/* Calculate n */
tmp2 = nfactor * EPSSI / Xdep;
    tmp3 = cdsc + cdscb * Vbseff + cdscd * Vds;
    tmp4 = (tmp2 + tmp3 * Theta0 + cit) / cox;

if (tmp4 >= -0.5)
    n = 1.0 + tmp4;
else
    begin /* avoid discontinuity problems caused by tmp4 */
        T0 = 1.0 / (3.0 + 8.0 * tmp4);
        n = (1.0 + 3.0 * tmp4) * T0;
    end
/* Poly Gate Si Depletion Effect */

\[
T_0 = v_{fb} + \phi;
\]

\[
\text{if } ((\text{ngate} > 1.0e18) \&\& (\text{ngate} < 1.0e25) \&\& (V_{gs} > T_0)) \text{ begin } /* \text{added to avoid the problem caused by ngate } */
\]

\[
T_1 = 1.0e6 \times \text{Charge}_q \times \text{EPSSI} \times \text{ngate} / (\text{cox} \times \text{cox});
\]

\[
T_4 = \sqrt{(1.0 + 2.0 \times (V_{gs} - T_0) / T_1)};
\]

\[
T_2 = T_1 \times (T_4 - 1.0);
\]

\[
T_3 = 0.5 \times T_2 \times T_2 / T_1; /* T_3 = V_{poly} */
\]

\[
T_7 = 1.12 - T_3 - 0.05;
\]

\[
T_6 = \sqrt{T_7 \times T_7 + 0.224};
\]

\[
T_5 = 1.12 - 0.5 \times (T_7 + T_6);
\]

\[
V_{gs\_eff} = V_{gs} - T_5;
\]

\[
\text{end}
\]

else

\[
V_{gs\_eff} = V_{gs};
\]

\[
V_{gst} = V_{gs\_eff} - V_{th};
\]

/* Effective Vgst (Vgsteff) Calculation */

\[
T_{10} = 2.0 \times n \times V_{tm};
\]

\[
V_{gstNVt} = V_{gst} / T_{10};
\]

\[
\text{ExpArg} = (2.0 \times \text{voff} - V_{gst}) / T_{10};
\]

/* MCJ: Very small Vgst */

\[
\text{if } (V_{gstNVt} > \text{EXP\_THRESHOLD}) \text{ begin}
\]

\[
V_{gsteff} = V_{gst};
\]

\[
\text{end}
\]

else if (\text{ExpArg} > \text{EXP\_THRESHOLD}) \text{ begin}

\[
T_0 = (V_{gst} - \text{voff}) / (n \times V_{tm});
\]

\[
\text{ExpVgst} = \exp(T_0);
\]

end
\[ V_{\text{gsteff}} = \frac{V_{\text{tm}} \cdot \text{cdep0} \cdot \text{cox} \cdot \exp(V_{\text{gst}})}{\text{ExpVgst}}; \]

\[ \text{end} \]

\[ \text{else} \]

\[ \begin{align*}
\expVgst &= \exp(V_{\text{gstNVt}}); \\
T1 &= T10 \cdot \ln(1.0 + \expVgst); \\
T2 &= 1.0 - T10 \cdot (-\text{cox} / (V_{\text{tm}} \cdot \text{cdep0}) \cdot \exp(\text{ExpArg})); \\
V_{\text{gsteff}} &= T1 / T2;
\end{align*} \]

\[ \text{end} \]

\[ /* \text{Calculate Effective Channel Geometry} */ \]

\[ T9 = \sqrt{\phi_i} - \sqrt{\phi}; \]

\[ \text{Weff} = \text{weff} - 2.0 \cdot (\text{dwg} \cdot V_{\text{gsteff}} + \text{dwb} \cdot T9); \]

\[ \text{if (Weff < 2.0e-8) /* to avoid the discontinuity problem due to Weff*/} \]

\[ \begin{align*}
T0 &= 1.0 / (6.0e-8 - 2.0 \cdot \text{Weff}); \\
\text{Weff} &= 2.0e-8 \cdot (4.0e-8 - \text{Weff}) \cdot T0;
\end{align*} \]

\[ \text{end} \]

\[ T0 = \text{prwg} \cdot V_{\text{gsteff}} + \text{prwb} \cdot T9; \]

\[ \text{if (T0 >= -0.9)} \]

\[ \text{Rds} = \text{rds0} \cdot (1.0 + T0); \]

\[ \text{else /* to avoid the discontinuity problem due to prwg and prwb*/} \]

\[ \begin{align*}
T1 &= 1.0 / (17.0 + 20.0 \cdot T0); \\
\text{Rds} &= \text{rds0} \cdot (0.8 + T0) \cdot T1;
\end{align*} \]

\[ \text{end} \]

\[ /* \text{Calculate Abulk */} \]

\[ T1 = 0.5 \cdot k_{1ox} / \sqrt{\phi_i}; \]

\[ T9 = \sqrt{x_j \cdot X_{\text{dep}}}; \]

\[ \text{tmp1} = \text{Leff} + 2.0 \cdot T9; \]
\[ T_5 = \text{Leff} / \text{tmp1}; \]
\[ \text{tmp2} = a_0 \times T_5; \]
\[ \text{tmp3} = \text{weff} + b_1; \]
\[ \text{tmp4} = b_0 / \text{tmp3}; \]
\[ T_2 = \text{tmp2} + \text{tmp4}; \]
\[ T_6 = T_5 \times T_5; \]
\[ T_7 = T_5 \times T_6; \]
\[ \text{Abulk0} = 1.0 + T_1 \times T_2; \]
\[ T_8 = \text{ags} \times a_0 \times T_7; \]
\[ \text{Abulk} = \text{Abulk0} + (-T_1 \times T_8) \times \text{Vgsteff}; \]

\[
\text{if (Abulk0 < 0.1) /* added to avoid the problems caused by Abulk0 */} \\
\text{begin} \\
\quad T_9 = 1.0 / (3.0 - 20.0 \times \text{Abulk0}); \\
\quad \text{Abulk0} = (0.2 - \text{Abulk0}) \times T_9; \\
\text{end} \\
\]

\[
\text{if (Abulk < 0.1) /* added to avoid the problems caused by Abulk */} \\
\text{begin} \\
\quad T_9 = 1.0 / (3.0 - 20.0 \times \text{Abulk}); \\
\quad \text{Abulk} = (0.2 - \text{Abulk}) \times T_9; \\
\text{end} \\
\]

\[ T_2 = \text{keta} \times \text{Vbseff}; \]
\[
\text{if (T2 >= -0.9)} \\
\quad T_0 = 1.0 / (1.0 + T_2); \\
\text{else /* added to avoid the problems caused by Keta */} \\
\text{begin} \\
\quad T_1 = 1.0 / (0.8 + T_2); \\
\quad T_0 = (17.0 + 20.0 \times T_2) \times T_1; \\
\text{end} \\
\]
Abulk = T0 * Abulk;
Abulk0 = T0 * Abulk0;

/* Mobility calculation */
if (MOBMOD == 1)
begin
    T0 = Vgsteff + Vth + Vth;
    T2 = ua + uc * Vbseff;
    T3 = T0 / tox;
    T5 = T3 * (T2 + ub * T3);
end
else if (MOBMOD == 2)
    T5 = Vgsteff / tox * (ua + uc * Vbseff + ub * Vgsteff / tox);
else
begin
    T0 = Vgsteff + Vth + Vth;
    T2 = 1.0 + uc * Vbseff;
    T3 = T0 / tox;
    T4 = T3 * (ua + ub * T3);
    T5 = T4 * T2;
end

if (T5 >= -0.8)
    Denomi = 1.0 + T5;
else /* Added to avoid the discontinuity problem caused by ua and ub*/
    Denomi = (0.6 + T5) * (1.0 / (7.0 + 10.0 * T5));

/***after stress mobility***/
ueff = (1-(35.85176*pow(SUBCURRENT,0.99024)*pow(TIMEZHI*86400,0.469913)))
    *(u0temp / Denomi);

/* Saturation Drain Voltage  Vdsat */
WVCox = Weff * vsattemp * cox;
WVCoxRds = WVCox * Rds;

Esat = 2.0 * vsattemp / ueff;
EsatL = Esat * Left;

/* Sqrt() */
if (a1 == 0.0)
  Lambda = a2;
else if (a1 > 0.0)
  /* Added to avoid the discontinuity problem caused by a1 and a2 (Lambda) */
  begin
    T0 = 1.0 - a2;
    T1 = T0 - a1 * Vgsteff - 0.0001;
    T2 = sqrt(T1 * T1 + 0.0004 * T0);
    Lambda = a2 + T0 - 0.5 * (T1 + T2);
  end
else
  begin
    T1 = a2 + a1 * Vgsteff - 0.0001;
    T2 = sqrt(T1 * T1 + 0.0004 * a2);
    Lambda = 0.5 * (T1 + T2);
  end

Vgst2Vtm = Vgsteff + 2.0 * Vtm;

if ((Rds == 0.0) && (Lambda == 1.0))
  begin
    T0 = 1.0 / (Abulk * EsatL + Vgst2Vtm);
    tmp1 = 0.0;
    T1 = T0 * T0;
    T2 = Vgst2Vtm * T0;
    T3 = EsatL * Vgst2Vtm;
    Vdsat = T3 * T0;
  end
else
    begin
        T9 = Abulk * WVCoxRds;
        T7 = Vgst2Vtm * T9;
        T6 = Vgst2Vtm * WVCoxRds;
        T0 = 2.0 * Abulk * (T9 - 1.0 + 1.0 / Lambda);

        T1 = Vgst2Vtm * (2.0 / Lambda - 1.0) + Abulk * EsatL + 3.0 * T7;
        T2 = Vgst2Vtm * (EsatL + 2.0 * T6);
        T3 = sqrt(T1 * T1 - 2.0 * T0 * T2);

        Vdsat = (T1 - T3) / T0;
    end

    vdsat = Vdsat;

    /* Effective Vds (Vdseff) Calculation */
    T1 = Vdsat - Vds - delta;
    T2 = sqrt(T1 * T1 + 4.0 * delta * Vdsat);
    Vdseff = Vdsat - 0.5 * (T1 + T2);

    if ((Vds == 0.0) && (VERSION == 3.24))
        Vdseff = 0.0;

    /* Calculate VAsat */
    tmp4 = 1.0 - 0.5 * Abulk * Vdsat / Vgst2Vtm;
    T9 = WVCoxRds * Vgstef;
    T0 = EsatL + Vdsat + 2.0 * T9 * tmp4;
    T9 = WVCoxRds * Abulk;
    T1 = 2.0 / Lambda - 1.0 + T9;

    Vasat = T0 / T1;

    if (Vdseff > Vds)
Vdseff = Vds; /* This code is added to fixed the problem
caused by computer precision when
Vds is very close to Vdseff. */
diffVds = Vds - Vdseff;

/* Calculate VAACL */
if ((pclm > 0.0) && (diffVds > 1.0e-10))
begin
    T0 = 1.0 / (pclm * Abulk * litl);
    T2 = Vgsteff / EsatL;
    T1 = Leff * (Abulk + T2);
    T9 = T0 * T1;
    VAACL = T9 * diffVds;
end
else
    VAACL = `MAX_EXP;

/* Calculate VADB */
if (thetaRout > 0.0)
begin
    T0 = Vgst2Vtm * Abulk * Vdsat;
    T1 = Vgst2Vtm + (Abulk * Vdsat);
    VADB = (Vgst2Vtm - T0 / T1) / thetaRout;
    T7 = pdiblb * Vbseff;
    if (T7 >= -0.9)
        begin
            T3 = 1.0 / (1.0 + T7);
            VADB = T3 * VADB;
        end
    else
        /* Added to avoid the discontinuity problem caused by pdibleb */
        begin
            T4 = 1.0 / (0.8 + T7);
        end
end

T3 = (17.0 + 20.0 * T7) * T4;
VADIBL = T3 * VADIBL;

end

end

else
VADIBL = `MAX_EXP;

/* Calculate VA */
T9 = pvag / EsatL * Vgsteff;

if (T9 > -0.9)
    T0 = 1.0 + T9;
else /* Added to avoid the discontinuity problems caused by pvag */
    T0 = (0.8 + T9) * 1.0 / (17.0 + 20.0 * T9);

T1 = VACLML * VADIBL / (VACLML + VADIBL);

V_a = Vasat + T0 * T1;

/* Calculate VASCBE */
if (pscbe2 > 0.0)
begin
    if (diffVds > (pscbe1 * litl / `EXP_THRESHOLD))
        VASCBE = Leff * exp(pscbe1 * litl / diffVds) / pscbe2;
    else
        VASCBE = `MAX_EXP * Leff / pscbe2;
end
else
VASCBE = `MAX_EXP;

/* Calculate Ids */
CoxWovL = cox * Weff / Leff;
beta = ueff * CoxWovL;

fgche1 = Vgsteff * (1.0 - 0.5 * Abulk * Vdseff / Vgst2Vtm);
fgche2 = 1.0 + (Vdseff / EsatL);

gche = beta * fgche1 / fgche2;
Idl   = gche * Vdseff / (1.0 + gche * Rds);

Idsa = Idl   * (1.0 + (diffVds / Va));
Ids   = Idsa * (1.0 + (diffVds / VASCBE));

/* Substrate current begins */
tmp = alpha0 + alpha1 * Leff;

if ((tmp <= 0.0) || (beta0 <= 0.0))
  Isub = 0.0;
else
  begin
    T2 = tmp / Leff;

    if (diffVds > beta0 / `EXP_THRESHOLD)
      T1 = T2 * diffVds * exp(-beta0 / diffVds);
    else
      T1 = T2 * `MIN_EXP * diffVds;

    Isub = T1 * Idsa;
  end

cdrain = Ids;
csub   = Isub;
// End of I-V model

// C-V model

// *** Depletion capacitance calculation ***

/* charge storage elements
* bulk-drain and bulk-source depletion capacitances
* czbd: zero bias drain junction capacitance
* czbs: zero bias source junction capacitance
* czbdsw: zero bias drain junction sidewall capacitance along field oxide
* czbssw: zero bias source junction sidewall capacitance along field oxide
* czbdswg: zero bias drain junction sidewall capacitance along gate side
* czbsswg: zero bias source junction sidewall capacitance along gate side
*/

if (VERSION == 3.24)
  begin
    czbd = unitAreaTempJctCap * drainArea;
    czbs = unitAreaTempJctCap * sourceArea;
  end
else
  begin
    czbd = unitAreaJctCap * drainArea;
    czbs = unitAreaJctCap * sourceArea;
  end

if (drainPerimeter < weff)
  begin
    if (VERSION == 3.24)
      czbdswg = unitLengthGateSidewallTempJctCap * drainPerimeter;
    else
      czbdswg = unitLengthGateSidewallJctCap * drainPerimeter;
    czbdsw = 0.0;
  end
else
  begin
    if (VERSION == 3.24)
begin
  czbdsw  = unitLengthSidewallTempJctCap * (drainPerimeter - weff);
  czbdswg = unitLengthGateSidewallTempJctCap * weff;
end
else
  begin
    czbdsw  = unitLengthSidewallJctCap * (drainPerimeter - weff);
    czbdswg = unitLengthGateSidewallJctCap * weff;
  end
end

if (sourcePerimeter < weff)
begin
  czbssw  = 0.0;
if (VERSION == 3.24)
  czbsswg = unitLengthGateSidewallTempJctCap * sourcePerimeter;
else
  czbsswg = unitLengthGateSidewallJctCap * sourcePerimeter;
end
else
begin
if (VERSION == 3.24)
  begin
    czbssw  = unitLengthSidewallTempJctCap * (sourcePerimeter - weff);
    czbsswg = unitLengthGateSidewallTempJctCap * weff;
  end
else
  begin
    czbssw  = unitLengthSidewallJctCap * (sourcePerimeter - weff);
    czbsswg = unitLengthGateSidewallJctCap * weff;
  end
end
mj     = bulkJctBotGradingCoeff;
mjsw = bulkJctSideGradingCoeff;
mjswg = bulkJctGateSideGradingCoeff;

qbs = 0.0;
qbd = 0.0;

/* Source Bulk Junction */
if (vbs == 0.0)
begin
    qbs = 0.0;
    capbs = czbs + czbssw + czbsswg;
end
else if (vbs < 0.0)
begin
    if (czbs > 0.0)
    begin
        arg = 1.0 - vbs / PhiB;
        if (mj == 0.5)
            sarg = 1.0 / sqrt(arg);
        else
            sarg = exp(-mj * ln(arg));
        qbs = PhiB * czbs * (1.0 - arg * sarg) / (1.0 - mj);
        capbs = czbs * sarg;
    end
else
    begin
        qbs = 0.0;
        capbs = 0.0;
    end
end /* else: !if(czbs > 0.0) */

if (czbssw > 0.0)
begin
arg = 1.0 - vbs / PhiBSW;

if (mjsw == 0.5)
    sarg = 1.0 / sqrt(arg);
else
    sarg = exp(-mjsw * ln(arg));

qbs = qbs + PhiBSW * czbssw * (1.0 - arg * sarg) / (1.0 - mjsw);
capbs = capbs + czbssw * sarg;
end // if (czbssw > 0.0)

if (czbsswg > 0.0)
begin
    arg = 1.0 - vbs / PhiBSWG;

if (mjswg == 0.5)
    sarg = 1.0 / sqrt(arg);
else
    sarg = exp(-mjswg * ln(arg));

qbs = qbs + PhiBSWG * czbsswg * (1.0 - arg * sarg) / (1.0 - mjswg);
capbs = capbs + czbsswg * sarg;
end
end
else
begin
    T0 = czbs + czbssw + czbsswg;
    T1 = vbs * (czbs * mj / PhiB + czbssw * mjsw / PhiBSW + czbsswg * mjswg / PhiBSWG);

    qbs = vbs * (T0 + 0.5 * T1);
capbs = T0 + T1;
end
/* Drain Bulk Junction */

if (vbd == 0.0)
begin
    qbd = 0.0;
    capbd = czbd + czbdsw + czbdswg;
end
else if (vbd < 0.0)
begin
    if (czbd > 0.0)
        begin
            arg = 1.0 - vbd / PhiB;
            if (mj == 0.5)
                sarg = 1.0 / sqrt(arg);
            else
                sarg = exp(-mj * ln(arg));
            qbd = PhiB * czbd * (1.0 - arg * sarg) / (1.0 - mj);
            capbd = czbd * sarg;
        end
    else
        begin
            qbd = 0.0;
            capbd = 0.0;
        end // else: !if(czbd > 0.0)

if (czbdsw > 0.0)
begin
    arg = 1.0 - vbd / PhiBSW;
    if (mjsw == 0.5)
        sarg = 1.0 / sqrt(arg);
    else
        sarg = exp(-mjsw * ln(arg));

qbd   = qbd   + PhiBSW * czbdsw * (1.0 - arg * sarg) / (1.0 - mjsw);
capbd = capbd + czbdsw * sarg;
end // if (czbdsw > 0.0)

if (czbdswg > 0.0)
begin
arg = 1.0 - vbd / PhiBSWG;
if (mjswg == 0.5)
sarg = 1.0 / sqrt(arg);
else
sarg = exp(-mjswg * ln(arg));
qbd   = qbd   + PhiBSWG * czbdswg * (1.0 - arg * sarg) / (1.0 - mjsw);
capbd = capbd + czbdswg * sarg;
end
end
else
begin
T0 = czbd + czbdsw + czbdswg;
T1 = vbd * (czbd * mj / PhiB + czbdsw * mjsw / PhiBSW + czbdswg * mjswg / PhiBSWG);
qbd   = vbd * (T0 + 0.5 * T1);
capbd = T0 + T1;
end

// *** Intrinsic charge calculation ***
// qdrn, qgate, qsrc, qbulk

qgate = 0.0;
qdrn  = 0.0;
qsrc  = 0.0;
qbulk = 0.0;
if (XPART < 0)
begin
  qgate = 0.0;
  qdren = 0.0;
  qsrc  = 0.0;
  qbulk = 0.0;
`ifdef NQSMOD
  gtau  = 0.0;
`endif
end

else if (CAPMOD == 0)
begin
  if (Vbseff < 0.0)
    Vbseff = Vbs;
  else
    Vbseff = phi - Phis;

  Vfb = vfbcv;
  Vth  = Vfb + phi + k1ox * sqrtPhis;

  Vgst = Vgs_eff - Vth;

  CoxWL = cox * weffCV * leffCV;
  Arg1  = Vgs_eff - Vbseff - Vfb;

  if (Arg1 <= 0.0)
    begin
      qgate = CoxWL * Arg1;
      qbulk = -qgate;
      qdren = 0.0;

      qinv  = 0.0;
    end
else if (Vgst <= 0.0)
    begin
        T1 = 0.5 * k1ox;
        T2 = sqrt(T1 * T1 + Arg1);
        qgate = CoxWL * k1ox * (T2 - T1);
        qbulk = -qgate;
        qdrn = 0.0;
        qinv = 0.0;
    end
else
    begin
        One_Third_CoxWL = CoxWL / 3.0;
        Two_Third_CoxWL = 2.0 * One_Third_CoxWL;
        AbulkCV = Abulk0 * abulkCVfactor;
        Vdsat = Vgst / AbulkCV;
        if (XPART > 0.5)
            begin
                /* 0/100 Charge partition model */
                if (Vdsat <= Vds)
                    begin /* saturation region */
                        T1 = Vdsat / 3.0;
                        qgate = CoxWL * (Vgs_eff - Vfb - phi - T1);
                        T2 = Two_Third_CoxWL * Vgst;
                        qbulk = -(qgate + T2);
                        qdrn = 0.0;
                        qinv = -(qgate + qbulk);
                    end
                else
                    begin /* linear region */

    end

120
\[
\text{Alphaz} = \frac{\text{Vgst}}{\text{Vdsat}};
\]
\[
\text{T1} = 2.0 \times \text{Vdsat} - \text{Vds};
\]
\[
\text{T2} = \frac{\text{Vds}}{(3.0 \times \text{T1})};
\]
\[
\text{T3} = \text{T2} \times \text{Vds};
\]
\[
\text{T9} = 0.25 \times \text{CoxWL};
\]
\[
\text{T4} = \text{T9} \times \text{Alphaz};
\]
\[
\text{T7} = 2.0 \times \text{Vds} - \text{T1} - 3.0 \times \text{T3};
\]
\[
\text{T8} = \text{T3} - \text{T1} - 2.0 \times \text{Vds};
\]
\[
\text{qgate} = \text{CoxWL} \times (\text{Vgs-eff} - \text{Vfb} - \text{phi} - 0.5 \times (\text{Vds} - \text{T3}));
\]
\[
\text{T10} = \text{T4} \times \text{T8};
\]
\[
\text{qdrn} = \text{T4} \times \text{T7};
\]
\[
\text{qbulk} = -(\text{qgate} + \text{qdrn} + \text{T10});
\]
\[
\text{qinv} = -(\text{qgate} + \text{qbulk});
\]
\[
end
\]
\[
end // if (\text{XPART} > 0.5)
\]
\[
\text{else if (XPART < 0.5)}
\]
\[
begin /* 40/60 Charge partition model */
\]
\[
\text{if (Vds} \geq \text{Vdsat})
\]
\[
begin /* saturation region */
\]
\[
\text{T1} = \frac{\text{Vdsat}}{3.0};
\]
\[
\text{qgate} = \text{CoxWL} \times (\text{Vgs-eff} - \text{Vfb} - \text{phi} - \text{T1});
\]
\[
\text{T2} = -\frac{\text{Two_Third_CoxWL} \times \text{Vgst}}{2};
\]
\[
\text{qbulk} = -(\text{qgate} + \text{T2});
\]
\[
\text{qdrn} = 0.4 \times \text{T2};
\]
\[
\text{qinv} = -(\text{qgate} + \text{qbulk});
\]
\[
end
\]
\[
else
\]
\[
begin /* linear region */
\]
\[
\text{Alphaz} = \frac{\text{Vgst}}{\text{Vdsat}};
\]
\[
T1 = 2.0 \times V_{\text{dsat}} - V_{\text{ds}}; \\
T2 = V_{\text{ds}} / (3.0 \times T1); \\
T3 = T2 \times V_{\text{ds}}; \\
T9 = 0.25 \times \text{CoxWL}; \\
T4 = T9 \times \text{Alphaz}; \\
q_{\text{gate}} = \text{CoxWL} \times (V_{\text{gs eff}} - V_{\text{fb}} - \phi - 0.5 \times (V_{\text{ds}} - T3)); \\
\]

\[
T6 = 8.0 \times V_{\text{dsat}} \times V_{\text{dsat}} - 6.0 \times V_{\text{dsat}} \times V_{\text{ds}} \\
+ 1.2 \times V_{\text{ds}} \times V_{\text{ds}}; \\
T8 = T2 / T1; \\
T7 = V_{\text{ds}} - T1 - T8 \times T6; \\
q_{\text{drn}} = T4 \times T7; \\
\]

\[
T7 = 2.0 \times (T1 + T3); \\
q_{\text{bulk}} = -(q_{\text{gate}} - T4 \times T7); \\
\]

\[
q_{\text{inv}} = -(q_{\text{gate}} + q_{\text{bulk}}); \\
\]

end // else: !if(V_{\text{ds}} \geq V_{\text{dsat}})

end // if (\text{XPART} < 0.5)

else

begin /* 50/50 partitioning */

if (V_{\text{ds}} \geq V_{\text{dsat}})

begin /* saturation region */

\[
T1 = V_{\text{dsat}} / 3.0; \\
q_{\text{gate}} = \text{CoxWL} \times (V_{\text{gs eff}} - V_{\text{fb}} - \phi - T1); \\
T2 = -\text{Two}_\text{Third}_\text{CoxWL} \times V_{\text{gst}}; \\
q_{\text{bulk}} = -(q_{\text{gate}} + T2); \\
q_{\text{drn}} = 0.5 \times T2; \\
\]

\[
q_{\text{inv}} = -(q_{\text{gate}} + q_{\text{bulk}}); \\
\]

end

else

begin /* linear region */

\[
\text{Alphaz} = V_{\text{gst}} / V_{\text{dsat}}; \\
\]

end

end

else

begin /* linear region */

\[
\text{Alphaz} = V_{\text{gst}} / V_{\text{dsat}}; \\
\]
T1 = 2.0 * Vdsat - Vds;
T2 = Vds / (3.0 * T1);
T3 = T2 * Vds;
T9 = 0.25 * CoxWL;
T4 = T9 * Alphaz;
qgate = CoxWL * (Vgs_eff - Vfb - phi - 0.5 * (Vds - T3));

T7 = T1 + T3;
qdrn = -T4 * T7;
qbulk = - (qgate + qdrn + qdrn);
qinv = -(qgate + qbulk);
end
end
end
else
begin
if (Vbseff < 0.0)
VbseffCV = Vbseff;
else
VbseffCV = phi - Phis;
CoxWL = cox * weffCV * leffCV;

/* Seperate VgsteffCV with noff and voffcv */
Noff2 = n * noff_param;
T0 = Vtm * Noff2;
VgstNVt = (Vgst - voffcv_param) / T0;
if (VgstNVt > EXP_THRESHOLD)
Vgsteff = Vgst - voffcv_param;
ext if (VgstNVt < -EXP_THRESHOLD)
Vgsteff = T0 * ln(1.0 + MIN_EXP);
else
begin
ExpVgst = exp(VgstNVt);
Vgsteff = T0 * ln(1.0 + ExpVgst);
end /* End of VgsteffCV - Weidong 5/1998 */

if (CAPMOD == 1)
begin
if (VERSION < 3.2)
Vfb = Vth - phi - k1ox * sqrtPhis;
else
Vfb = vfbzb;

Arg1 = Vgs_eff - VbseffCV - Vfb - Vgsteff;

if (Arg1 <= 0.0)
qgate = CoxWL * Arg1;
else
begin
T0 = 0.5 * k1ox;
T1 = sqrt(T0 * T0 + Arg1);
qgate = CoxWL * k1ox * (T1 - T0);
end

qbulk = -qgate;

One_Third_CoxWL = CoxWL / 3.0;
Two_Third_CoxWL = 2.0 * One_Third_CoxWL;

AbulkCV = Abulk0 * abulkCVfactor;
VdsatCV = Vgsteff / AbulkCV;

if (VdsatCV < Vds)
begin
\[ T_0 = \frac{V_{gsteff} - V_{dsatCV}}{3.0}; \]
\[ q_{gate} = q_{gate} + CoxWL \times T_0; \]
\[ T_0 = V_{dsatCV} - V_{gsteff}; \]
\[ q_{bulk} = q_{bulk} + One_{Third}\_CoxWL \times T_0; \]

\[ \text{if} \ (X_{PART} > 0.5) \]
\[ T_0 = -\text{Two}_{Third}\_CoxWL; \]
\[ \text{else if} \ (X_{PART} < 0.5) \]
\[ T_0 = -0.4 \times CoxWL; \]
\[ \text{else} \]
\[ T_0 = -\text{One}_{Third}\_CoxWL; \]

\[ q_{src} = T_0 \times V_{gsteff}; \]
\[ \text{end} \]
\[ \text{else} \]
\[ \text{begin} \]
\[ T_0 = \text{AbulkCV} \times V_{ds}; \]
\[ T_1 = 12.0 \times (V_{gsteff} - 0.5 \times T_0 + 1.0e-20); \]
\[ T_2 = \frac{V_{ds}}{T_1}; \]
\[ T_3 = T_0 \times T_2; \]

\[ q_{gate} = q_{gate} + CoxWL \times (V_{gsteff} - 0.5 \times V_{ds} + T_3); \]
\[ q_{bulk} = q_{bulk} + CoxWL \times (1.0 - \text{AbulkCV}) \times (0.5 \times V_{ds} - T_3); \]

\[ \text{if} \ (X_{PART} > 0.5) \]
\[ \text{begin} \] /* 0/100 Charge petition model */
\[ q_{src} = -CoxWL \times (0.5 \times V_{gsteff} + 0.25 \times T_0 - T_0 \times T_0 \times (T_1 + T_1)); \]
\[ \text{end} \]
\[ \text{else if} \ (X_{PART} < 0.5) \]
\[ \text{begin} \] /* 40/60 Charge petition model */
\[ T_2 = 0.5 \times CoxWL \times (T_1 / 12.0 \times T_1 / 12.0); \]
\[ T_3 = V_{gsteff} \times (2.0 \times T_0 \times T_0 / 3.0 + V_{gsteff} \times (V_{gsteff} - 4.0 \times T_0 / 3.0)) \]
\[ - 2.0 \times T_0 \times T_0 / 15.0; \]
\[ q_{src} = -T_2 * T_3; \]
\[
\text{end}
\]
\[
\text{else}
\]
\[
\begin{align*}
&\text{/* 50/50 Charge petition model */} \\
&q_{src} = -0.5 * (q_{gate} + q_{bulk}); \\
&\text{end}
\end{align*}
\]
\[
\text{end}
\]
\[
q_{drn} = -(q_{gate} + q_{bulk} + q_{src}); \\
q_{inv} = -(q_{gate} + q_{bulk}); \\
\text{end} // \text{if (CAPMOD == 1)}
\]
\[
\text{else if (CAPMOD == 2)}
\]
\[
\begin{align*}
&\text{begin} \\
&\text{if (VERSION < 3.2)} \\
&V_{fb} = V_{th} - \phi - k_{1ox} * \text{sqrt}\phi_{is}; \\
&\text{else} \\
&V_{fb} = v_{fzb}; \\
&V_3 = V_{fb} - V_{gs_{eff}} + V_{bseffC} - \Delta_3; \\
&\text{if (V_{fb} <= 0.0)} \\
&\text{begin} \\
&T_0 = \text{sqrt}(V_3 * V_3 - 4.0 * \Delta_3 * V_{fb}); \\
&T_2 = -\Delta_3 / T_0; \\
&\text{end} \\
&\text{else} \\
&\text{begin} \\
&T_0 = \text{sqrt}(V_3 * V_3 + 4.0 * \Delta_3 * V_{fb}); \\
&T_2 = \Delta_3 / T_0; \\
&\text{end} \\
&T_1 = 0.5 * (1.0 + V_3 / T_0); \\
V_{beff} = V_{fb} - 0.5 * (V_3 + T_0); \\
Q_{ac0} = C_{oxW} * (V_{beff} - V_{fb});
\end{align*}
\]
\[ T_0 = 0.5 \cdot k_{1ox}; \]
\[ T_3 = V_{gs_{eff}} - V_{fbeff} - V_{bseffCV} - V_{gsteff}; \]

\[
\text{if (} k_{1ox} == 0.0 \text{)}
\]
\[ \begin{align*}
T_1 &= 0.0; \\
T_2 &= 0.0;
\end{align*} \]
\[ \text{end} \]

\[
\text{else if (} T_3 < 0.0 \text{)}
\]
\[ \begin{align*}
T_1 &= T_0 + \frac{T_3}{k_{1ox}}; \\
T_2 &= C_{ox} W L;
\end{align*} \]
\[ \text{end} \]

\[
\text{else}
\]
\[ \begin{align*}
T_1 &= \sqrt{T_0 \cdot T_0 + T_3}; \\
T_2 &= C_{ox} W L \cdot \frac{T_0}{T_1};
\end{align*} \]
\[ \text{end} \]

\[ Q_{sub0} = C_{ox} W L \cdot k_{1ox} \cdot (T_1 - T_0); \]

\[ A_{bulkCV} = A_{bulk0} \cdot a_{bulkCVfactor}; \]
\[ V_{dsatCV} = V_{gsteff} / A_{bulkCV}; \]

\[ V_4 = V_{dsatCV} - V_{ds} - \text{`DELTA}_4; \]
\[ T_0 = \sqrt{V_4 \cdot V_4 + 4.0 \cdot \text{`DELTA}_4 \cdot V_{dsatCV}}; \]
\[ V_{dseffCV} = V_{dsatCV} - 0.5 \cdot (V_4 + T_0); \]

\[
/\ast \text{ Added to eliminate non-zero } V_{dseffCV} \text{ at } V_{ds}=0.0 /*
\]
\[ \text{if (} (V_{ds} == 0.0) && (\text{VERSION} == 3.24)) \]
\[ V_{dseffCV} = 0.0; \]

\[ T_0 = A_{bulkCV} \cdot V_{dseffCV}; \]
\[ T_1 = 12.0 \times (V_{\text{gsteff}} - 0.5 \times T_0 + 1e-20); \]
\[ T_2 = V_{\text{dseffCV}} / T_1; \]
\[ T_3 = T_0 \times T_2; \]

\[ T_4 = (1.0 - 12.0 \times T_2 \times T_2 \times \text{AbulkCV}); \]
\[ T_5 = (6.0 \times T_0 \times (4.0 \times V_{\text{gsteff}} - T_0) / (T_1 \times T_1) - 0.5); \]
\[ T_6 = 12.0 \times T_2 \times T_2 \times V_{\text{gsteff}}; \]

\[ q_{\text{inoi}} = -\text{CoxWL} \times (V_{\text{gsteff}} - 0.5 \times T_0 + \text{AbulkCV} \times T_3); \]
\[ q_{\text{gate}} = \text{CoxWL} \times (V_{\text{gsteff}} - 0.5 \times V_{\text{dseffCV}} + T_3); \]

\[ T_7 = 1.0 - \text{AbulkCV}; \]
\[ q_{\text{bulk}} = \text{CoxWL} \times T_7 \times (0.5 \times V_{\text{dseffCV}} - T_3); \]

if (XPART > 0.5)
begin /* 0/100 Charge petition model */
\[ q_{\text{src}} = -\text{CoxWL} \times (0.5 \times V_{\text{gsteff}} + 0.25 \times T_0 - T_0 \times T_0 / (T_1 + T_1)); \]
end
else if (XPART < 0.5)
begin /* 40/60 Charge petition model */
\[ T_2 = 0.5 \times \text{CoxWL} / (T_1 / 12.0 \times T_1 / 12.0); \]
\[ T_3 = V_{\text{gsteff}} \times (2.0 \times T_0 \times T_0 / 3.0 + V_{\text{gsteff}} \times (V_{\text{gsteff}} - 4.0 \times T_0 / 3.0)) \]
\[ - 2.0 \times T_0 \times T_0 / 15.0; \]
\[ q_{\text{src}} = -T_2 \times T_3; \]
end
else
begin /* 50/50 Charge petition model */
\[ q_{\text{src}} = -0.5 \times (q_{\text{gate}} + q_{\text{bulk}}); \]
end

\[ q_{\text{gate}} = q_{\text{gate}} + Q_{\text{ac0}} + Q_{\text{sub0}}; \]
\[ q_{\text{bulk}} = q_{\text{bulk}} - (Q_{\text{ac0}} + Q_{\text{sub0}}); \]
\[ q_{\text{drn}} = -(q_{\text{gate}} + q_{\text{bulk}} + q_{\text{src}}); \]
qinv = qino;
end

/* New Charge-Thickness capMod (CTM) begins - Weidong 7/1997 */
else if (CAPMOD == 3)
begin
V3 = vfbzb - Vgs_eff + VbseffCV - `DELTA_3;

if (vfbzb <= 0.0)
begin
T0 = sqrt(V3 * V3 - 4.0 * `DELTA_3 * vfbzb);
    T2 = `-DELTA_3 / T0;
end
else
begin
T0 = sqrt(V3 * V3 + 4.0 * `DELTA_3 * vfbzb);
    T2 = `DELTA_3 / T0;
end

T1 = 0.5 * (1.0 + V3 / T0);
Vfbeff = vfbzb - 0.5 * (V3 + T0);

Cox = cox;
Tox = 1.0e8 * tox;
T0 = (Vgs_eff - VbseffCV - vfbzb) / Tox;

    tmp = T0 * acde;

    if ((-EXP_THRESHOLD < tmp) && (tmp < EXP_THRESHOLD))
Tcen = ldeb * exp(tmp);
else if (tmp <= -EXP_THRESHOLD)
    Tcen = ldeb * `MIN_EXP;
else
    Tcen = ldeb * `MAX_EXP;
LINK = 1.0e-3 * tox;

V3 = ldeb - Tcen - LINK;
V4 = sqrt(V3 * V3 + 4.0 * LINK * ldeb);
Tcen = ldeb - 0.5 * (V3 + V4);
T1 = 0.5 * (1.0 + V3 / V4);

Ccen = `EPSSI / Tcen;
T2 = Cox / (Cox + Ccen);
Coxeff = T2 * Ccen;
T3 = -Ccen / Tcen;
CoxWLcen = CoxWL * Coxeff / Cox;

Qac0 = CoxWLcen * (Vb eff - vfbz b);

T0 = 0.5 * k1ox;
T3 = Vgs _eff - Vb eff - VbseffCV - Vgsteff;

if (k1ox == 0.0)
begin
T1 = 0.0;
T2 = 0.0;
end
else if (T3 < 0.0)
begin
T1 = T0 + T3 / k1ox;
T2 = CoxWLcen;
end
else
begin
T1 = sqrt(T0 * T0 + T3);
T2 = CoxWLcen * T0 / T1;
end

Qsub0 = CoxWLcen * k1ox * (T1 - T0);
/* Gate-bias dependent delta Phis begins */
if (k1ox <= 0.0)
begin
Denomi = 0.25 * moin * Vtm;
T0 = 0.5 * sqrtPhi;
end
else
begin
Denomi = moin * Vtm * k1ox * k1ox;
T0 = k1ox * sqrtPhi;
end
T1 = 2.0 * T0 + Vgsteff;

DeltaPhi = Vtm * ln(1.0 + T1 * Vgsteff / Denomi);
/* End of delta Phis */

T3 = 4.0 * (Vth - vfbzb - phi);
Tox2 = Tox + Tox;

if (T3 >= 0.0)
T0 = (Vgsteff + T3) / Tox2;
else
T0 = (Vgsteff + 1.0e-20) / Tox2;

tmp = exp(0.7 * ln(T0));
T1 = 1.0 + tmp;
T2 = 0.7 * tmp / (T0 * Tox2);
Tcen = 1.9e-9 / T1;

Ccen = `EPSSI / Tcen;
T0 = Cox / (Cox + Ccen);
Coxeff = T0 * Ccen;
T1 = -Ceen / Tcen;
CoxWLcen = CoxWL * Coxeff / Cox;

AbulkCV = Abulk0 * abulkCVfactor;
VdsatCV = (Vgsteff - DeltaPhi) / AbulkCV;
V4 = VdsatCV - Vds - 'DELTA_4;
T0 = sqrt(V4 * V4 + 4.0 * 'DELTA_4 * VdsatCV);
VdseffCV = VdsatCV - 0.5 * (V4 + T0);
T1 = 0.5 * (1.0 + V4 / T0);
T2 = 'DELTA_4 / T0;
T3 = (1.0 - T1 - T2) / AbulkCV;

if ((Vds == 0.0) && (VERSION == 3.24))
    VdseffCV = 0.0;

T0 = AbulkCV * VdseffCV;
T1 = Vgsteff - DeltaPhi;
    T2 = 12.0 * (T1 - 0.5 * T0 + 1.0e-20);
    T3 = T0 / T2;
    T4 = 1.0 - 12.0 * T3 * T3;
    T5 = AbulkCV * (6.0 * T0 * (4.0 * T1 - T0) / (T2 * T2) - 0.5);
T6 = T5 * VdseffCV / AbulkCV;

qinoi = CoxWLcen * (T1 - T0 * (0.5 - T3));
qgate = qinoi;

T7 = 1.0 - AbulkCV;

qbulk = CoxWLcen * T7 * (0.5 * VdseffCV - T0 * VdseffCV / T2);

if (XPART > 0.5)
    begin /* 0/100 partition */
        qsrc = -CoxWLcen * (T1 / 2.0 + T0 / 4.0 - 0.5 * T0 * T0 / T2);
    end
else if (XPART < 0.5)
begin /* 40/60 partition */
  T2 = T2 / 12.0;
  T3 = 0.5 * CoxWLcen / (T2 * T2);
  T4 = T1 * (2.0 * T0 * T0 / 3.0 + T1
             * (T1 - 4.0 * T0 / 3.0)) - 2.0 * T0 * T0 * T0 / 15.0;
  qsrc = -T3 * T4;
end
else
begin /* 50/50 partition */
  qsrc = -0.5 * qgate;
end

qgate = qgate + Qac0 + Qsub0 - qbulk;
qbulk = qbulk - (Qac0 + Qsub0);
qdm = -(qgate + qbulk + qsrc);
qinv = -qinoi;
end /* End of CTM */

// *** end of intrinsic charge calculation ***

`ifdef NQSMOD
if (NQSMOD)
begin
  qcheq = -(qbulk + qgate);

  gtau_drift = abs(tconst * qcheq) * ScalingFactor;
  gtau_diff = 16.0 * u0temp * vtm / (leffCV * leffCV) * ScalingFactor;

  gtau = gtau_drift + gtau_diff;
end
`endif

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qgdo = 0.0;
qgso = 0.0;

// *** overlap capacitance charge calculation ***
if (CAPMOD == 0.0)
begin
  qgdo = cgdo_param * vgd;
  qgso = cgso_param * vgs;
end
else if (CAPMOD == 1.0)
begin
  if (vgd < 0.0)
  begin
    T1 = sqrt(1.0 - 4.0 * vgd / ckappa);
    qgdo = cgdo_param * vgd - weffCV * 0.5 * cgdl * ckappa * (T1 - 1.0);
  end
  else
  begin
    qgdo = (weffCV * cgdl + cgdo_param) * vgd;
  end
  if (vgs < 0.0)
  begin
    T1 = sqrt(1.0 - 4.0 * vgs / ckappa);
    qgso = cgso_param * vgs - weffCV * 0.5 * cgsl * ckappa * (T1 - 1.0);
  end
  else
  begin
    qgso = (weffCV * cgsl + cgso_param) * vgs;
  end
end
else
begin
\[
T_0 = vgd + \Delta_1;
\]
\[
T_1 = \sqrt{T_0 \times T_0 + 4.0 \times \Delta_1};
\]
\[
T_2 = 0.5 \times (T_0 - T_1);
\]
\[
T_3 = \text{weffCV} \times \text{cgdl};
\]
\[
T_4 = \sqrt{1.0 - 4.0 \times T_2 / \kappa};
\]
\[
q_{gd0} = (\text{cgdo_param} + T_3) \times vgd - T_3 \times (T_2 + 0.5 \times \kappa \times (T_4 - 1.0));
\]
\[
T_0 = vgs + \Delta_1;
\]
\[
T_1 = \sqrt{T_0 \times T_0 + 4.0 \times \Delta_1};
\]
\[
T_2 = 0.5 \times (T_0 - T_1);
\]
\[
T_3 = \text{weffCV} \times \text{cgs};
\]
\[
T_4 = \sqrt{1.0 - 4.0 \times T_2 / \kappa};
\]
\[
q_{gso} = (\text{cgso_param} + T_3) \times vgs - T_3 \times (T_2 + 0.5 \times \kappa \times (T_4 - 1.0));
\]

// Add Overlap capacitance charges contribution to total node charge
// according to mode and NQS model
if (mode > 0)
begin
if (NQS == 0)
begin
qgd = qgd0;
qgs = qgs0;
qgb = cgbo_param * vgb;
qgate = qgate + qgd + qgs + qgb;
bulk = qbulk - qgb;
qdrn = qdrn - qgd;
qsrc = -(qgate + qbulk + qdrn);
end
\ifdef NQS
sxpart = 0.6;
dxpart = 0.4;
`endif
   end // if (NQSMOD == 0)
else
   begin
      CoxWL = cox * weffCV * leffCV;

ifdef NQSMOD
   if ( abs(qcheq) <= 1.0e-5 * CoxWL )
      begin
         if ( XPART < 0.5)
            dxpart = 0.4;
         else if ( XPART > 0.5)
            dxpart = 0.0;
         else
            dxpart = 0.5;
      end
   else
      dxpart = qdrn / qcheq;
   end
   sxpart = 1.0 - dxpart;
`endif

qg   = qgdo;
   qgs  = qgso;
   qgb  = cgbo_param * vgb;

   qgate = qg   + qgs + qgb;
   qbulk = -qgb;
   qdrn  = -qg;
   qsrc  = -(qgate + qbulk + qdrn);
end
end // if (mode > 0)
else
   begin
      if (NQSMOD == 0)
begin
    qgd = qgdo;
    qgs = qgs;
    qgb = cgbo_param * vgb;

    qgate = qgate + qgd + qgs + qgb;
    qbulk = qbulk - qgb;
    qsrc = qdrn - qgs;
    qdrn = -(qgate + qbulk + qsrc);

    `ifdef NQSMOD
        sxpart = 0.4;
        dxpart = 0.6;
    `endif

    end // if (NQSMOD == 0)
else
    begin
        CoxWL = cox * weffCV * leffCV;
    `ifdef NQSMOD
        if ( abs(qcheq) <= 1.0e-5 * CoxWL )
            begin
                if ( XPART < 0.5 )
                    sxpart = 0.4;
                else if ( XPART > 0.5 )
                    sxpart = 0.0;
                else
                    sxpart = 0.5;
            end
        else
            sxpart = qdrn / qcheq;
        `endif
        dxpart = 1.0 - sxpart;
    `endif

    qgd = qgdo;
qs = qgs;
qgb = cgbo_param * vgb;
qgate = qgd + qgs + qgb;
qbulk = -qgb;
qsrc = -qgs;
qdrn = -(qgate + qbulk + qsrc);

`ifdef NQSMOD
   if (NQSMOD)
     begin
       qcdump = qdef * ScalingFactor;
       cqdef = ddt(qcdump);
       cqcheq = ddt(qcheq);
     end

   if (analysis("static"))
     begin
       dxpart = (mode > 0) ? 0.4 : 0.6;
       sxpart = 1.0 - dxpart;

       if (NQSMOD)
         gtau = 16.0 * u0temp * vtm / leffCV / leffCV * ScalingFactor;
       else
         gtau = 0.0;
     end
   `endif

// Add depletion capacitance charge contribution
Qdrn = qdrn - qbd;
Qsrc = qsrc - qbs;
Qbulk = qbulk + qbd + qbs;
Qgate = qgate;
if (mode > 0)

begin

  I(drain, sourcep) <+ TYPE * cdrai;
  I(bulk,   drainp)  <+ TYPE * (cbd - csub);
  I(bulk,   sourcep) <+ TYPE * cbs;

end

else

begin

  I(drain, sourcep) <+ TYPE * (-cdrai);
  I(bulk,   drainp)  <+ TYPE * cbd;
  I(bulk,   sourcep) <+ TYPE * (cbs - csub);

end

// Process drain/source resistance

//if ( drainConductance > 0.0 )
//  I(drain, drainp) <+ drainConductance * V(drain, drainp);
//else
//  V(drain, drainp) <+ 0.0;
//if ( sourceConductance > 0.0 )
//  I(source, sourcep) <+ sourceConductance * V(source, sourcep);
//else
//  V(source, sourcep) <+ 0.0;

// Charge current including overlap and depletion capacitance contribution

cqgate = TYPE * ddt(Qgate);
cqdrn  = TYPE * ddt(Qdrn);
cqbulk = TYPE * ddt(Qbulk);

I(gate)    <+ cqgate;
I(drainp)  <+ cqdrn;
I(bulk)    <+ cqbulk;
I(sourcep) <+ -(cqgate + cqdrn + cqbulk);

`ifdef NQSMOD

if (NQSMOD)

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begin
    I(gate) <+ TYPE * (-1) * qdef * gtau;
    I(drainp) <+ TYPE * dxpart * qdef * gtau;
    I(sourcep) <+ TYPE * sxpart * qdef * gtau;

    I(q) <+ -TYPE * ( cqdef - cqcheq );
    I(q) <+ -V(q) * gtau;
end
else
    begin
        I(q) <+ GMIN * qdef;
    end
'endif

end // analog begin

endmodule
REFERENCES


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