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UV-Ozone Oxide Treatments for High-Efficiency Silicon Photovoltaic Devices

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UV-OZONE OXIDE TREATMENTS FOR HIGH-EFFICIENCY SILICON PHOTOVOLTAIC DEVICES

by

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ABSTRACT

Fabrication of solar cells with higher efficiency, simpler processes and lower cost is largely perceived as the ultimate goal for photovoltaic research. To reach such a goal each step needs to be refined and optimized. In this dissertation, a UV-ozone treatment is proposed as a simple and versatile process that can be applied to multiple fabrication steps for improvement. The UV-ozone cleaning method provides comparable surface cleaning quality to more expensive and hazardous industrial standard RCA clean with less chemical used. A good passivation quality was achieved on both *n*-type and *p*-type silicon wafer by a silicon oxide/aluminum oxide passivation stack, formed by UV-ozone treatment and ALD. Creating a thin layer of silicon oxide on the silicon wafer surface before depositing the aluminum contact form a metal-insulator-semiconductor (MIS) contact structure, showing low contact resistance for both *n*-type and *p*-type wafers. Device performance simulation was performed by Quokka and Sunsolve using experimental results. The simulation results shown promising power conversion efficiency and indicated contact resistance as the key factor in reaching higher efficiency.

ACKNOWLEDGMENTS

Looking back on my 6 years Ph.D. time in CREOL, it is truly a long and amazing trip. One can achieve nothing without helps and supports from others, and I want to express my sincere thanks to all of them.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

1.1. Background

Photovoltaic energy relies on the process of converting sunlight directly into electricity by solar cells. An early observation of the photovoltaic effect and attempt to make use of it can go back to 19 centuries. But even the best effort at that time was less than 1 percent efficient at converting light to electricity. The first practical silicon solar cell was demonstrated by Bell Laboratories on April 25, 1954[1]. It had about 6% efficiency. Since then the solar cell growth quickly. In the 1960s due to the space race solar cell was selected as the power supply for satellites, attract a lot of intention and funds in this area of research. And the oil crisis in the 1970s forced people to look for alternative energy sources, the solar cell being a strong candidate. The efficiency of solar cells has increased steadily over time. It reached a milestone of 20% in 1985[2] and now is more than 40%[3]. More and more materials are used to build a solar cell. Aside from the well-known silicon wafer, there are cadmium telluride (CdTe)[4], gallium arsenide (GaAs)[5], germanium (Ge)[6] and so on. The industry of solar cell is also growing stable and fast, experienced more than 10% per year growth rate in decades. In one sentence, solar cell is a strong and active area for both research and work.

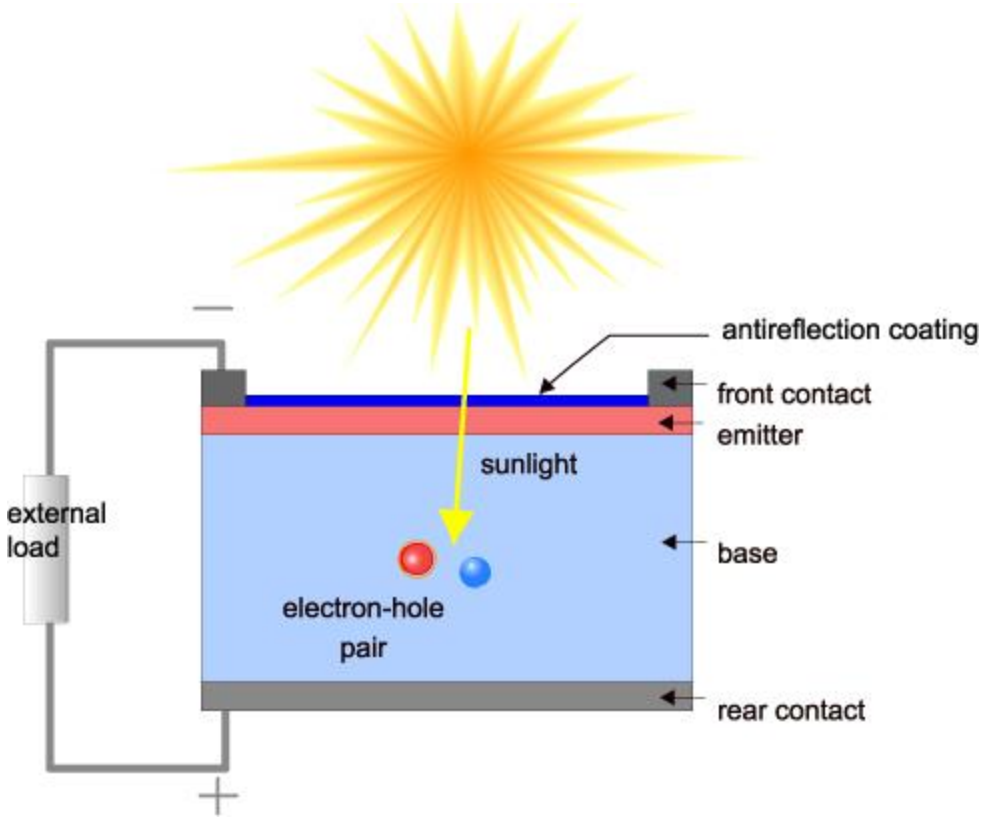


Figure 1: Cross-section of a solar cell.[7]

Figure 1 shows the structure of a typical solar cell. The light was absorbed by the semiconductor material and raised the electron to a higher energy state to generate electron-hole pair. These carriers were collected by the contact on semiconductor surface and moved to external circuit. A variety of materials and structures were studied for solar cell, the most common one is the silicon solar cell with p-n junction form.

Building a silicon solar cell begins from growing the ingot of silicon. It doesn't require extremely pure silicon as the integrated circuit industry, so the material price is much less. Then to saw the

ingot into bricks, and further sliced into the wafer. The wafer will be cleaned and textured. The next step is emitter diffusion to create emitter layer and p-n junction. Edge isolation is needed to isolate this front emitter from the cell rear. The anti-reflection layer was coated to help absorb light. Finally, the front and rear contact were deposited.

Making solar cells with higher efficiency, simpler process and lower cost is an endless path of pursuing. To reach that goal, each step during the fabrication needs to be optimized. Surface cleaning is a key factor to device performance, only effective cleaning can lead to high-quality performance. Over the years, various approach of cleaning method has been applied. The well-known RCA clean is considered as the primary method of wet chemical cleaning in the microelectronic industry[8]. And a potential replacement named “IMEC-Clean” due to its simpler process but near-perfect removal of metallic particles was introduced later[9]. On the other hand, dry cleaning like plasma etch[10] and cryogenic cleaning[11] was considered as a valuable complement to reach optimized results in certain process sequence. Ozone involved cleaning was also discussed[12-15] due to its strong oxidizing ability and easy to generate by dielectric barrier discharge[16].

Surface passivation is another important process for pursuing high conversion efficiency. The passivation helps to prevent unwanted recombination of photogenerated electron-hole pairs in two ways[17]. It completes the dangling bonds by a surface dielectric coating or chemical species, usually referred as the chemical passivation. It also reduces the minority carrier density on the

surface to lower recombination rate, referred as electrical passivation. Multiple materials are studied as passivation layer for silicon solar cells such as silicon oxide[18], silicon nitride[19], amorphous silicon[20], aluminum oxide[13, 21, 22], titanium oxide[23] and so on.

Contact resistance is also important to power conversion efficiency. the intimate metal-silicon contact leads to recombination losses due to a high density of states at the metal-silicon interface[24]. Using high-temperature functional-impurity doping beneath the metal terminal is a way to drastically lowering the contact resistance. But absorber doping induces its own fundamental energy losses like Auger recombination, bandgap narrowing and free-carrier absorption to limit the device performance[25-28]. Metal-insulator-semiconductor (MIS) contact is another approach to reduce contact recombination losses. A thin film of inserted between the silicon wafer and the metal terminal, physically separate them to prevent the recombination loss of direct contact but thin enough to allow current flows. A range of different structures and materials are discussed[29-32].

1.2. Dissertation Outline

This dissertation is organized as follows: CHAPTER 2: Methods and Materials. This chapter introduces all the equipment and methods were used in this dissertation. CHAPTER 3: Surface Preparation: Reason and Process. This chapter discusses how the defect of the wafer surface happens and various methods to remove them. The UV-Ozone method is experimentally proved to be a candidate with high quality, low cost, and simple process for surface cleaning. CHAPTER 4: Passivating the Surface. This chapter introduces reasons for surface passivation and several methods to achieve it. The UV-Ozone treatment is proved to be able to improve the passivation quality. CHAPTER 5: Contact Resistance and How to Decrease it. This chapter explaines methods to lower the contact resistance. UV-Ozone generated interlayer shown promising low resistance results. CHAPTER 6: Simulation of the Cells. This chapter shows the simulation results of cells using experimental parameters from previous chapters. We also discuss how different factors affect cell simulation results, respectively. CHAPTER 7: Summary and Conclusion summarizes the concept studied and conclude all the works presented above.

CHAPTER 2: METHODS AND MATERIALS

In this chapter, the key pieces of equipment, general experiment process applied, and standard measurements to define the quality of these processes is presented.

2.1 UV Ozone Treatment

The majority of the work contained in this dissertation involved applying UV ozone treatment to different fabrication processes of the sloar cell. Such treatment was done using a Jelight 42 UV-ozone generator.

Figure 2: Picture of a Jelight 42 UV-ozone generator.

The generator uses the low-pressure mercury vapor grid lamp as the UV source. The molecular oxygen will absorb 184.9nm UV and generate atomic oxygen to create ozone. The ozone will also absorb 253.7nm UV and dissociated. Therefore, the sample under UV exposure will experience continuous generation of atomic oxygen and ozone formed. The sample surface gets oxidized within several minutes.

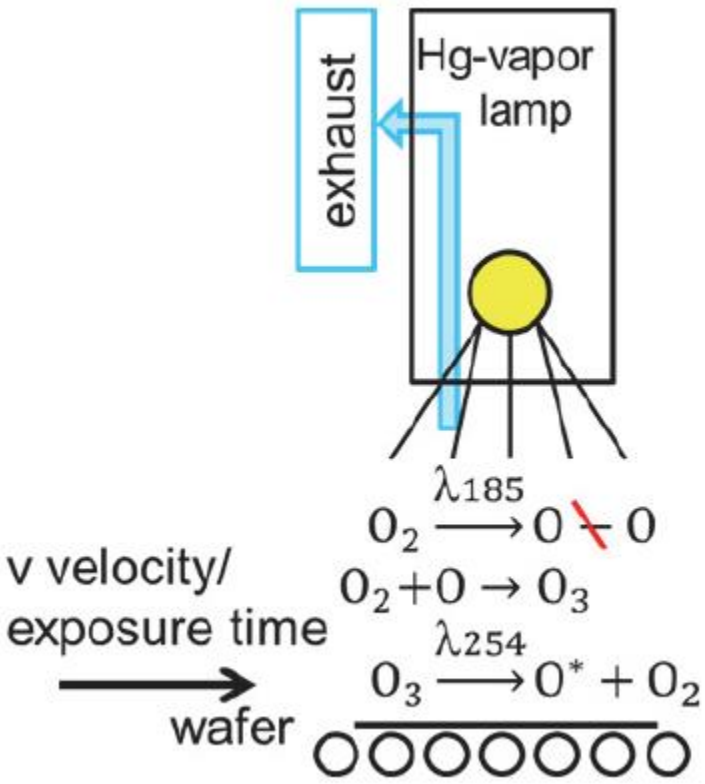


Figure 3: Schematic picture of the mercury vapor lamp and reaction process[33].

2.2 AlO_x ALD

Aluminum oxide(AlO_x) deposition by atomic layer deposition(ALD) is a standard process in our experiment. It was performed on all the samples before measuring its electric properties like the effective lifetime. The deposition was realized by an ALD Cambridge Nanotech Savannah S100 as shown in Figure 4.

Figure 4: Photo of ALD Cambridge Nanotech Savannah S100.

The materials used for AlO_x deposition are trimethylamine(TMA) and water vapor. The reaction chamber was heated to 200°C. Materials were pulse on samples surface for reaction and purged by the carrier gas(nitrogen for our experiment). The purge time for water and TMA were 8s and 12s, respectively. The deposition rate is about 0.88nm/cycle.

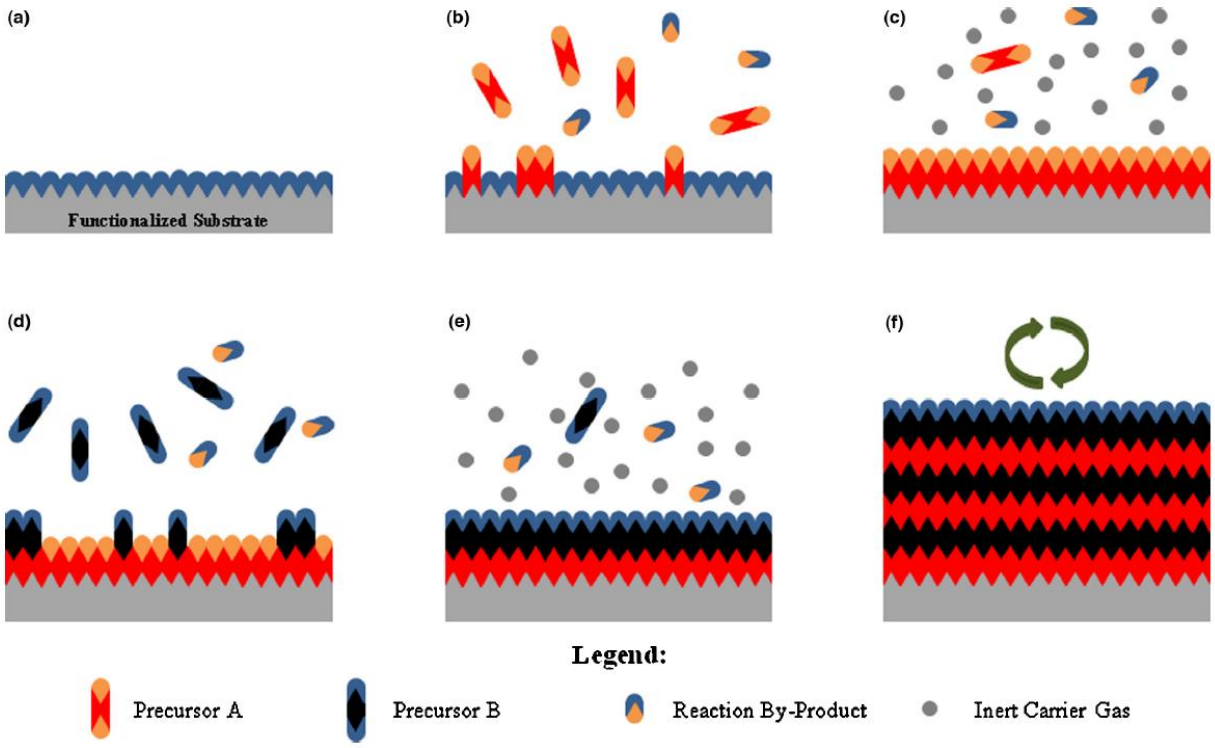


Figure 5: Schematic of ALD process[34]. For our experiment, precursor A is water vapor, precursor B is TMA and the inert carrier gas is nitrogen.

The detail process is the following steps as shown in Figure 5: a) the sample was heated and prepared for reaction, b) precursor A was pulsed and reacts with sample surface, c) extra precursor and reaction by-products were purged by carrier gas, d) precursor B was pulsed and reacts, and e)

extra precursor and reaction by-products were purged by carrier gas. Steps b) to e) are considered as one cycle of deposition. As shown by f), the cycle is repeated until the sample reached the designed thickness.

2.3 Minority Carrier Lifetime Measurement

We are using effective carrier lifetime τ_{eff} and surface recombination current density J_0 as the figure of merit for sample surface quality. Because all the surface preparation process is purposed to make surface recombination less happening and reach a longer carrier lifetime from that.

We are using the method of photoconductance measurements to measure these numbers. A very short light pulse was shined on the sample and the photoconductivity can be sensed without contacting the sample by microwave reflectance, capacitive coupling or the use of a coil to couple the sample conductivity[35]. The effective lifetime is obtained directly from the slope of the photoconductance transient decay curve.

$$\tau_{eff}(\Delta n) = -\frac{\Delta n(t)}{d\Delta n(t)/dt} \tag{2.1}$$

Where Δn(t) is the time-dependent average excess carrier density. The effective lifetime is contributed by two parts: bulk lifetime and surface recombination[36]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + 2\frac{J_0}{qWn_i^2}(\Delta n + N_d) \tag{2.2}$$

Where J_0, q, W, n_i, N_d, and τ_{bulk} represent the surface recombination current density, electronic charge, sample thickness, intrinsic carrier concentration, bulk dopant concentration and intrinsic bulk lifetime of crystalline silicon respectively[25]. In the case of high injection, $\Delta n >> N_d$ so we can ignore N_d to get

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + 2\frac{J_0}{qWn_i^2}\Delta n \tag{2.3}$$

With τ_{eff} measured with different Δn, we can then derive J_0. J_0 is considered a better indicator of the surface property as it purely reflected surface recombination velocity without considering bulk lifetime. While the effective lifetime is more useful for defining the quality of a solar cell as one integrity as it directly related to the power conversion efficiency of the cell.

Typically, in nowadays high-quality commercial wafer for solar cells have bulk lifetime about several milliseconds. That means when surface recombination current density J_0 reaches the order of 10fA/cm^2, the contribution of surface recombination to the effective lifetime will be comparable to the bulk lifetime. Thus, in general we can say J_0<10fA/cm2 is considered as a good quality of the surface property. J_0 lower than that will still result in a longer effective lifetime, but it won't be the dominance parameter of it.

Figure 6: Sinton Instruments WCT-120 wafer-lifetime tool

2.4 Four-Point Probe Measurement of Sheet Resistance

We are using the method of four-point probe measurement to measure the sheet resistance of the wafer sample. The basic concept of the four-point probe measurement is shown in Figure 7.

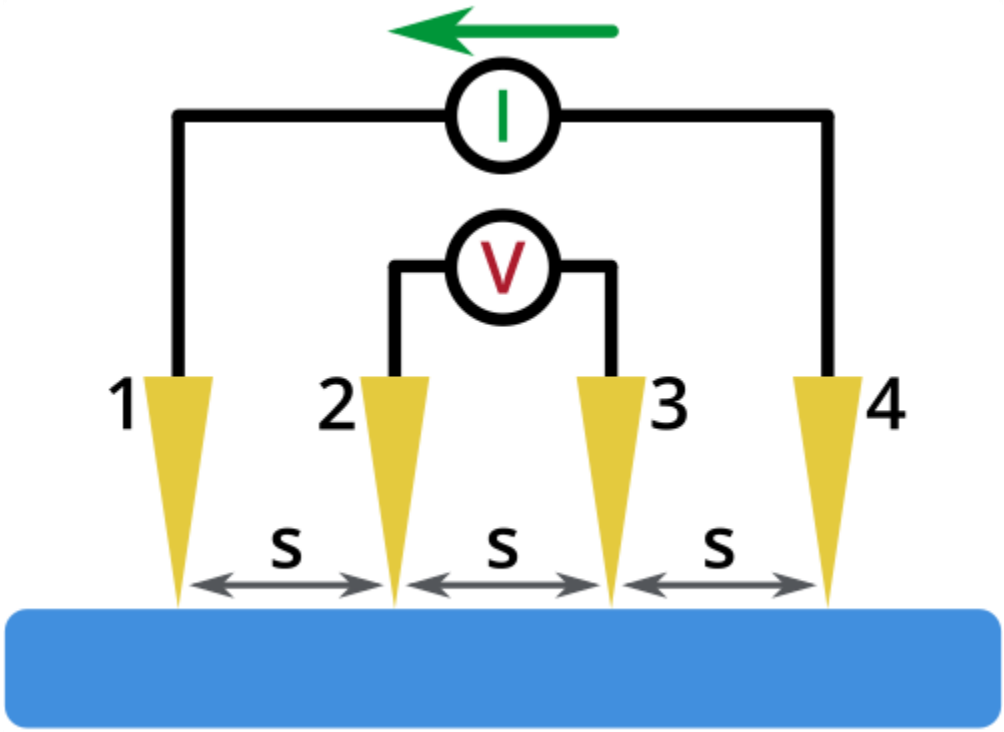


Figure 7: Schematic diagram of a four-point probe.

The current was injected through the outer probe (1 and 4) while the voltage was measured by the inner probe (2 and 3). In such a way we avoided the effect of contact resistance of the probe and only focusing on the resistance of the sample itself. Sheet resistance is commonly defined as the resistivity of the material divided by its thickness:

$$R_s = \frac{\rho}{t} \tag{2.4}$$

The unit of it is Ω. However, this number actually represents the resistance between two sides of a material. So, the more commonly used unit is Ω/□ (ohm per square). We are using a four-point probe system from Ossila to achieve the measurements.

Figure 8: picture of an Ossila four-point probe system

The sheet resistance we measured is considered as an indicator of the wafer sample's doping concentration. As the heavier doped sample will have more carriers, which results in lower sheet resistance. We also experimentally probed the validity of this indicator.

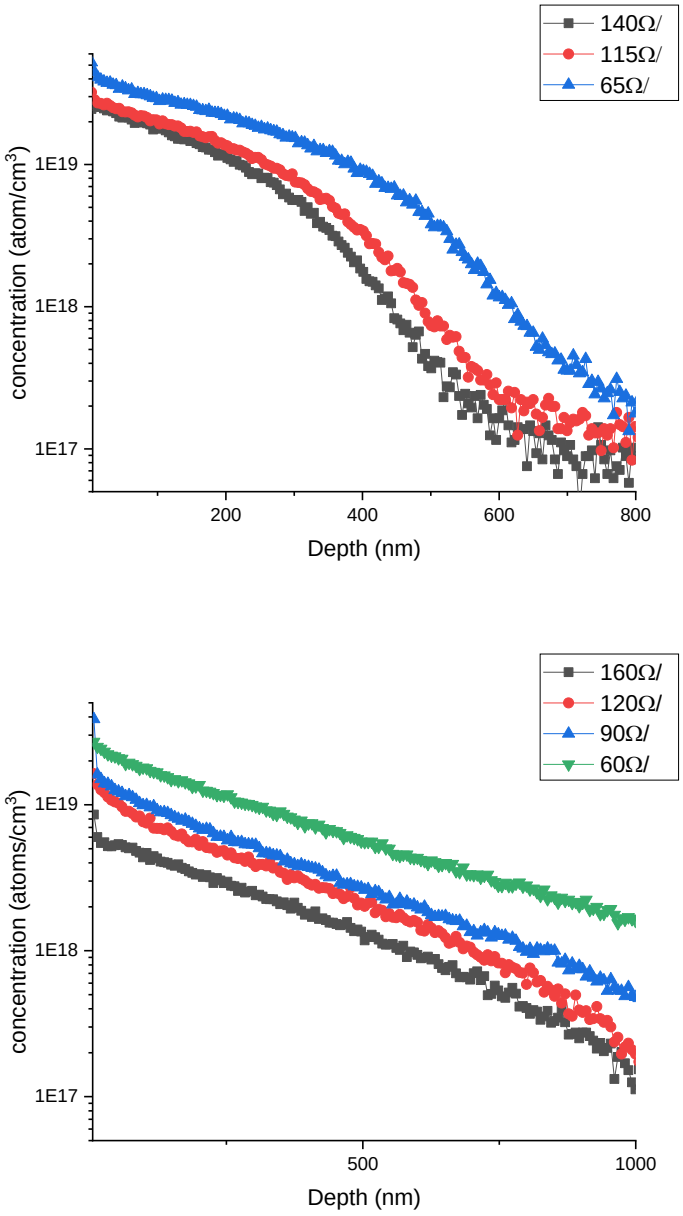


Figure 9: SIMS measurement result of boron (upper) and phosphorus (bottom) doped silicon wafer sample.

2.5 Metal Contact Deposition and Measurement of Contact Resistance

To measure the contact resistance, we need to build contact for silicon wafer sample first. We choose aluminum as the contact material for our experiment. Aluminum is considered as the standard contact material for the solar cell industry. In the lab experiment level, we can use silver contact to get lower contact resistance, however in real life silver is too expensive to be a commercially available contact material.

We used an e-beam evaporator (Temescal FC2000) for our Aluminum contact deposition. The machine uses a strong electron beam to evaporate the metal material in a graphene crucible at the bottom of the vacuum chamber. The sample was placed on top of the chamber to get metal ion deposited. For a typical deposition process, the crucible was slowly heated at the speed of around 0.1% of the power of e-beam every 30 seconds. The aluminum begins evaporated at around 4% of the power. Keep increasing the power until it reaches the deposition rate of 0.1nm/s. Stable the e-beam power at there during all the deposition process. The contact layer to be deposited should be at least 800nm thick. After the required thickness achieved, slowly decrease the e-beam power at the same speed of increasing it. The whole process typically takes about 3~4 hours in total. The slow increase and decrease of the e-beam power are to prevent the temperature of crucible and metal to change drastically, which would otherwise crack the crucible.

Figure 10: Picture of Temescal FC2000 e-beam evaporator

In the deposition process, we are depositing the TLM pattern on the wafer for contact resistance measurement. The transmission line method(TLM) is a commonly used way to measure the contact resistance of a metal-semiconductor junction. The pattern is a series of contact with different gap spaces in between. With current applied on the contacts and voltage measured, we

can derive the resistance between the contacts. This resistance is considered to be the combination of contact resistance and sheet resistance of semiconductor itself:

$$R_T = \frac{R_S}{W} L + 2R_c \tag{2.5}$$

Where the R_T is the total resistance between the contacts, R_s is the sheet resistance of the semiconductor, W is the width of the contact pad, L is the gap distance between contacts, R_c is the contact resistance. By fitting resistance of different contact gap sizes, we can eliminate the effect of semiconductor resistance and derive the contact resistance.

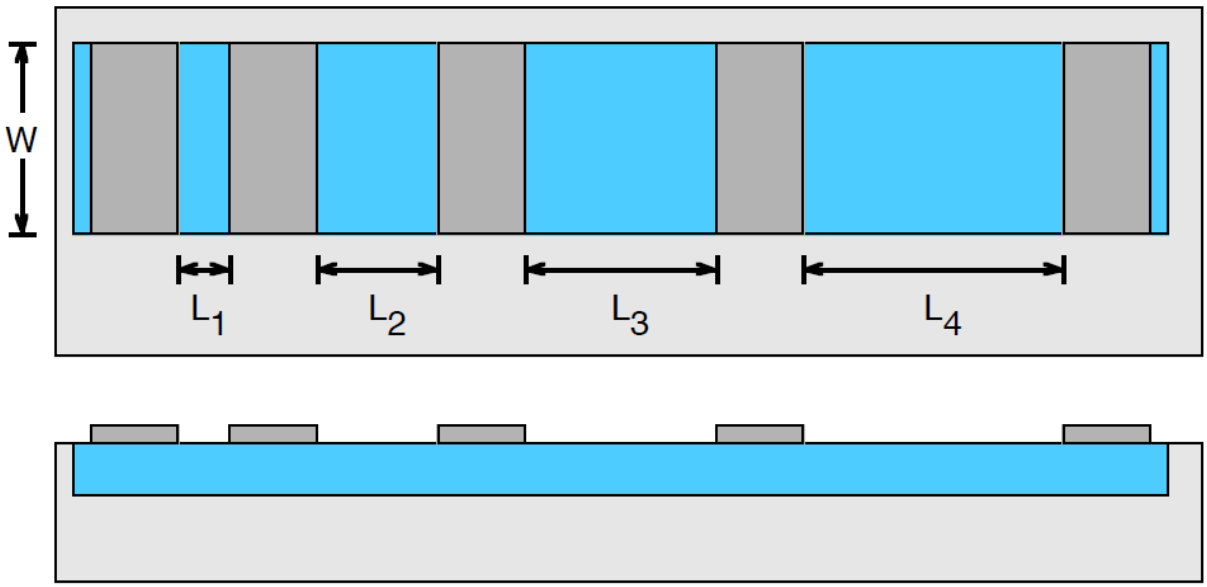


Figure 11: schematic plot of TLM pattern

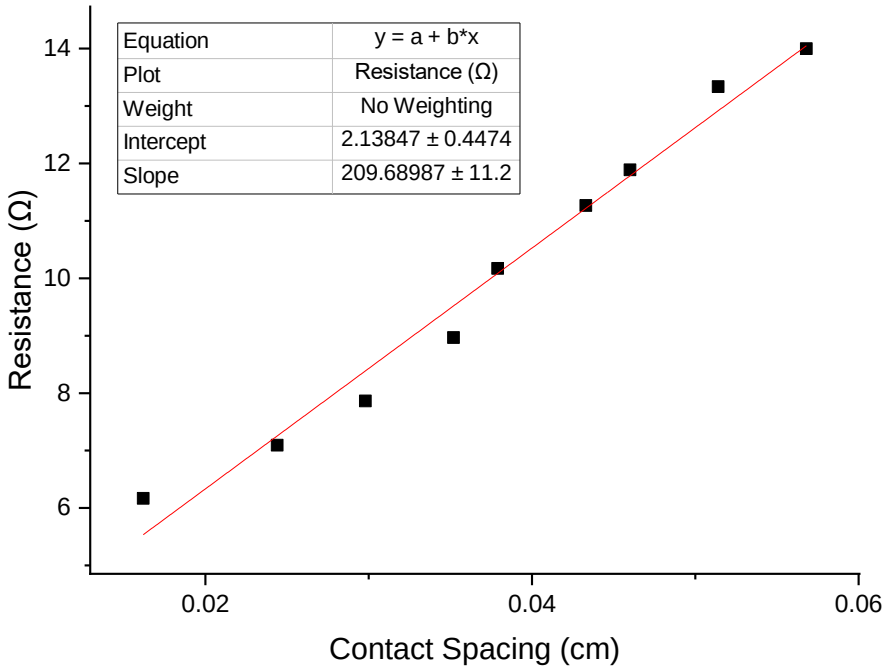


Figure 12: fitting plot for contact resistance

Figure 12 is an example of TLM fitting plot. The fitted intercept is $2R_c$ so we can derive R_c=1.07Ω. The slope is R_s/W while W=0.475cm in this case. The fitted sheet resistance Rs=99Ω/□, comparable to the measured result 90Ω/□.

CHAPTER 3: SURFACE PREPARATION: REASON AND PROCESS

Usually, the source material of silicon is in the form of big ingots. We need to saw it into bricks and then slice to wafer pieces as our initial sample. After all these processes the silicon wafer in our hand won't be perfect. There will be saw damage, contaminant, dust and eventually oxide surface. To acquire good results, we must remove saw damage and clean the sample surface before fabrication into a PV cell.

3.1. Saw Damage Etching

Saw damage etching is the process to remove the damage on the sample surface, penetrating roughly 4 μm into the wafer[37]. A wet alkaline etch is commonly used for such a purpose[38]. The most common solutions utilize sodium hydroxide (NaOH), potassium hydroxide (KOH), or tetramethylammonium hydroxide (TMAH) diluted in de-ionized water as the etch solution. The reaction process is essentially similar for all solutions, where OH– and water (H_2O) plays a key role in the reaction:

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2 \quad (3.1)$$

The etch rate depends on the [OH^-] and [H_2O] concentrations. The etch rate increases with increasing [OH^-] concentration until some maximum point is reached. With further [OH^-] increases, the etch rate decreases due to decreasing [H_2O]. Over-etching leads to thinner wafers

that could lower production yield due to breakage. Under-etching can lead to shunting and degradation of the minority carrier lifetimes because of residual surface micro-damage.

3.2. Surface Cleaning Methods

Surface cleaning in the process intended to remove all the dust, contaminant, particle, organic/inorganic impurities and native oxide from the wafer surface. It's a key factor to device performance, only effective cleaning can lead to high-quality performance. Over the years, various approach of cleaning method has been applied. The well-known RCA clean is considered as the primary method of wet chemical cleaning in the microelectronic industry[8]. The process includes a mixed solution of $NH_4OH/H_2O_2/H_2O$ naming SC-1 to remove the organic contaminants, mixed solution of $HCl/H_2O_2/H_2O$ naming SC-2 to remove inorganic contaminants and ultraclean deionized water for rinsing. A potential replacement of RCA named "IMEC-Clean" was introduced later[9]. It has a simpler process that includes a mixture of H_2SO_4/H_2O_2 and diluted HF while reaching near-perfect removal of metallic particles. Ozone is another good candidate chemical for the cleaning process due to its strong oxidizing ability and easy to generate by dielectric barrier discharge[16]. The benefits and applications of ozonated deionized water (DI-O_3) for wafer surface preparation was first discussed in detail by Chen[39] and reported by several groups[40-42]. Bakhshi et al. also represented using DI-O_3 for surface preparation before dielectric layer passivation can achieve outstanding surface passivation quality as the saturation current density J_0 down to 8 fA/cm^2(per side)[43]. Aside from wet chemical cleaning, dry cleaning like plasma etch[10] and cryogenic cleaning[11] was considered as a valuable complement to reach optimized results in certain process sequence. In general, dry cleaning consumes fewer chemicals and reduces the possibility of impurity contamination[9, 44-46]. Ozone involved cleaning also has a dry process version, which is ultraviolet radiation assisted photosensitized oxidation process

(UV-ozone process). It was first reported in 1972 by Bolon[47] of able to remove organic residue. The UV-ozone process was reported to be able to produce a clean surface in less than a minute[48] and significantly reduce contaminations on chemical cleaned silicon surfaces[49]. The UV-ozone process also proved to be beneficial to organic photovoltaics. It is reported capable of improving electron extraction[50], stability in polymer solar cells[51], surface morphology, transmittance and film quality[52]. It is also used for fluorine-doped tin oxide glass substrate cleaning[53].

3.2.1. RCA Cleaning

Among all these methods, one of the well-known and widely used way is the so-called RCA cleaning. The basic procedure was developed by Werner Kern in 1965 while working for the Radio Corporation of America (RCA)[8]. The first step (SC-1) is to prepare a solution with deionized water, ammonia and hydrogen peroxide as the ratio 5:1:1. Dip wafer in it for 10 minutes at 75 °C to remove organic residues. Then prepare another solution with deionized water, hydrochloric acid, and hydrogen peroxide as ratio 6:1:1. Again, dip the wafer in it for 10 minutes at 75 °C to remove the metallic contaminant. Finally, rinsing with ultrapure deionized water and dry to get a clean wafer surface.

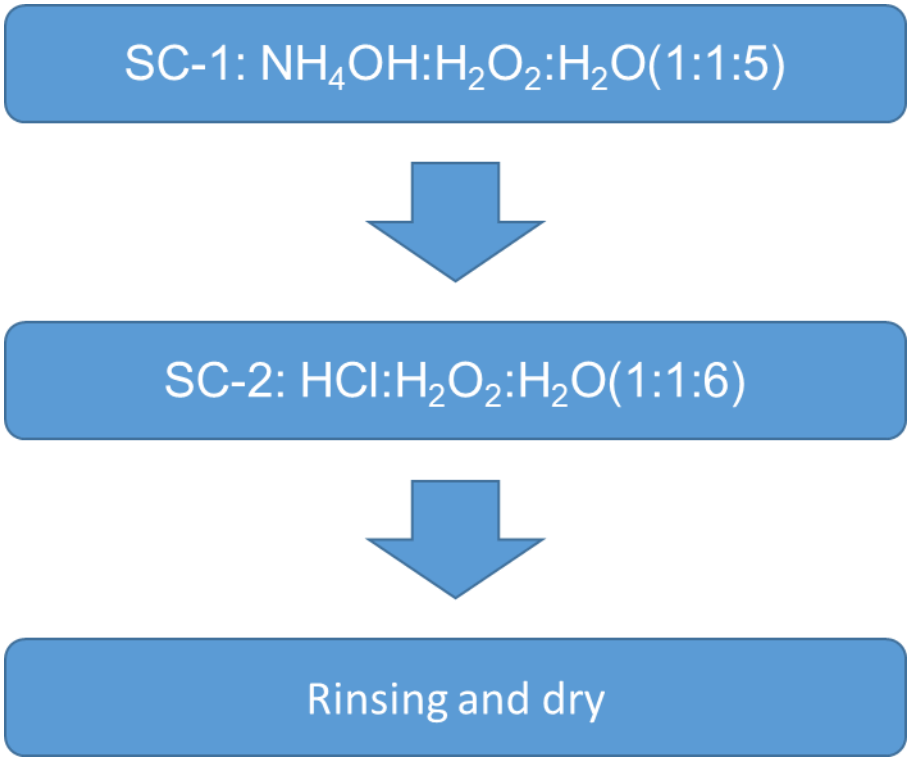


Figure 13: process plot of RCA cleaning

3.2.2. Ozone Involved Cleaning

Another method for surface preparation is involved with ozone. The reliable ozone generation based on dielectric barrier discharge was first developed by Werner Siemens in 1857[16, 54, 55]. It has been the standard ozone generation technique since then.

A process using ozonated deionized water (DI-O_3) for wafer surface preparation was discussed in detail by different groups[39-42]. Basically, such a process is a sequential treatment DI-O_3+HF. The contaminations are oxidized by ozone and either dissolved or incorporated into the oxide layer on the wafer surface. And such a layer will be removed by HF dip afterward.

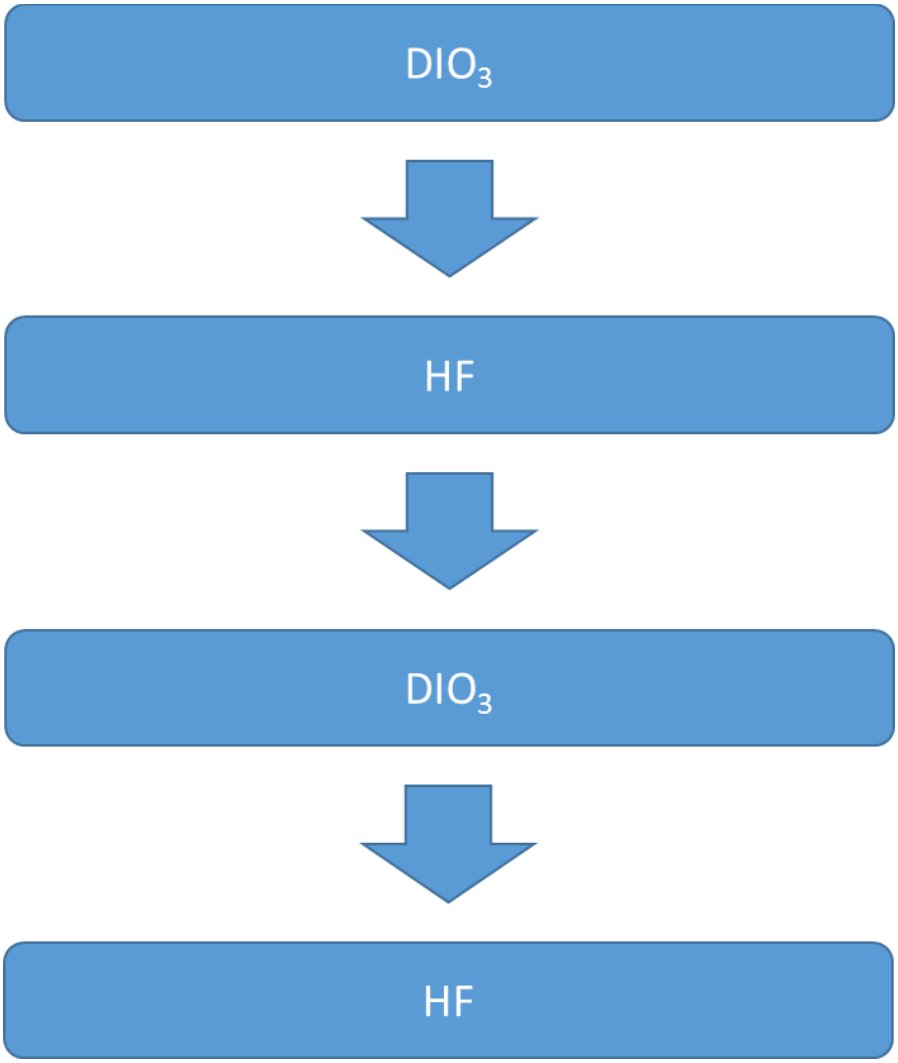


Figure 14: process plot of DI-O_3 cleaning

In addition to wet ozone cleaning, dry ozone cleaning based on exposing wafer under ultraviolet radiation can also remove a wide variety of contaminants and is less complicated than the DI-O_3 process. The first report of UV ozone can remove organic layer such as photoresist polymer was back to 1972[47]. Later, Sowell presented UV cleaning of adsorbed hydrocarbons from glass and gold surface in air and vacuum environments [56]. As for the wafer cleaning process, it is a sequential UV-grow + HF. Instead of dip sample in DI-O_3 as wet ozone cleaning did, we only need to expose it under UV lamp for several minutes.

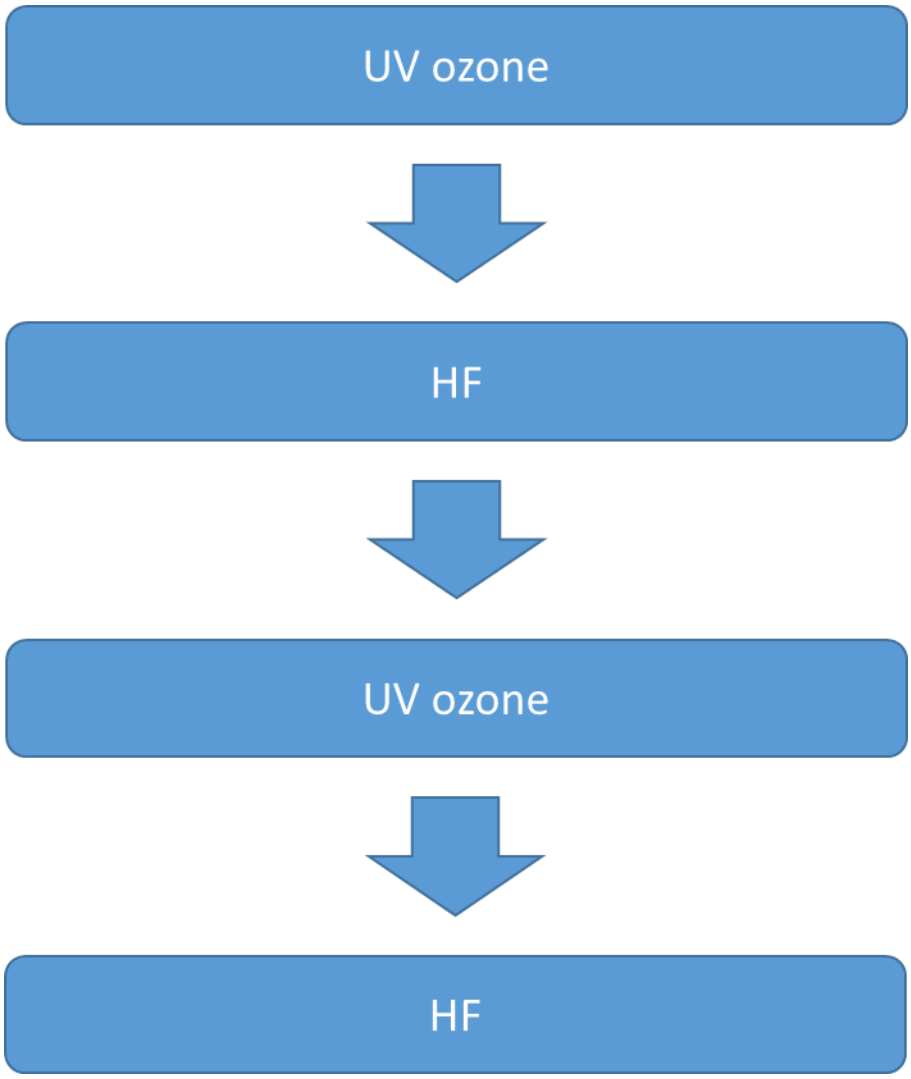


Figure 15: process plot of UV-Ozone cleaning

3.3 Experimental Process

Textured 2.5Ω.cm n-type Cz silicon wafers were used to compare different surface cleaning methods. Saw damage etching was performed in a 25% TMAH solution at 90 ℃ before the cleaning process. RCA cleaning used solution of NH_3:H_2O_2:H_2O 1:1:5 as SC-1 and HCl: H_2O_2:H_2O 1:1:5 as SC-2. The samples were dipped in SC-1 for 10 minutes at 75°C, followed by dipping in SC-2 for 10mintues at 75°C and rinsing with ultrapure deionized water and dry by nitrogen flow afterward. UV-ozone oxide was formed by a Jelight 42 UV-ozone generator for the UV-ozone cleaning process. The samples were exposed under the ozone generator for 5 minutes each side. Followed by dipping into diluted 5% HF to remove the oxide layer formed on the sample surface. DI-O_3 cleaned samples were soaked in deionized water at near saturation with dissolved ozone having about 40 ppm at ambient temperature for 10 minutes, then rinsing in deionized water for 5 minutes and drying in an N_2/IPA-based dryer. A comparison group of sample goes through the same saw damage etch process but no cleaning method applied.

Aluminum oxide (AlO_x) deposition was performed in a thermal ALD system (Cambridge NanoTech Savannah 100 ALD) after cleaning with a deposition rate at 0.088 nm/cycle at 200°C. Deposited samples were annealed in a thermal furnace at 450 ℃ for 30min in nitrogen ambient to activate the passivation.

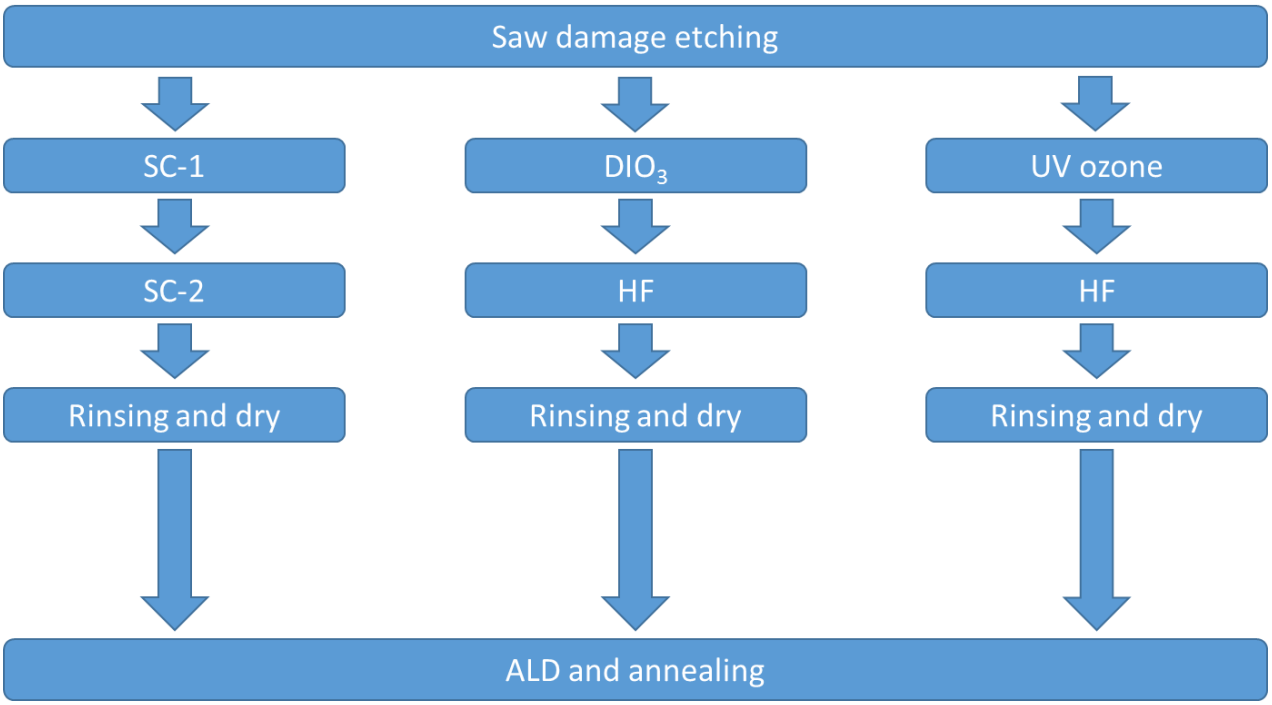


Figure 16: experiment process plot

A Sinton Instruments WCT-120 was used to measure effective carrier lifetime τ_{eff} and surface recombination current density J_0 of annealed samples. J_0 is derived from

$$J_0 = qWn_i^2\,(\Delta n + N_d)/2 \cdot \left(1/\tau_{eff} - 1/\tau_{bulk}\right) \tag{2.1}$$

where q, W, n_i, N_d, and τ_{bulk} represent the electronic charge, sample thickness, intrinsic carrier concentration, bulk dopant concentration and intrinsic bulk lifetime of crystalline silicon respectively[25]. The τ_{eff} and J_0 were considered as criteria of surface cleaning quality, with higher τ_{eff} and lower J_0 indicating improved performance.

M-2000 J.A. Woollam spectral ellipsometer was used to measure the thickness of the oxide layer created by ozone.

3.4 Results and Discussion

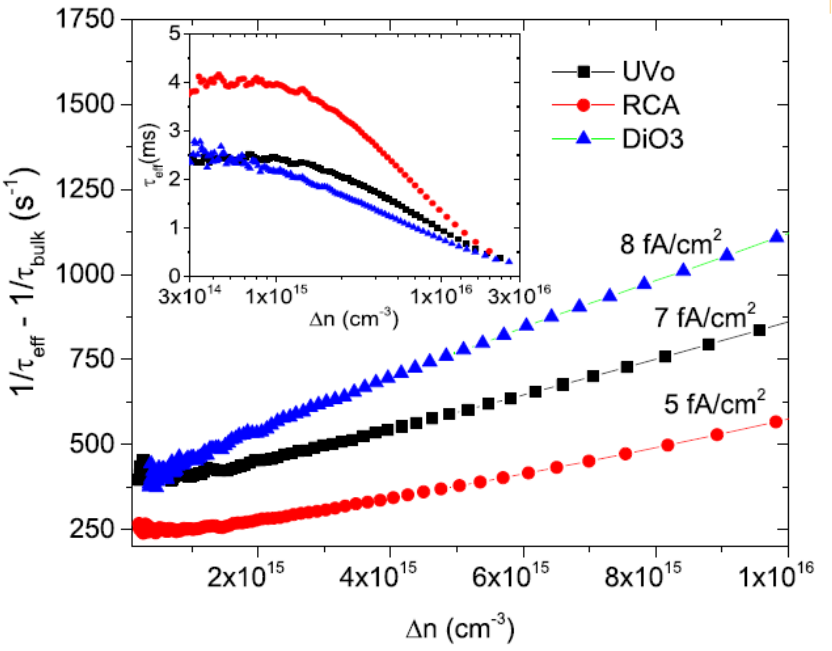


Figure 17: Auger-corrected inverse τ_{eff} and effective lifetime (inset figure) of samples following UV ozone clean twice, RCA clean and DI-O_3 clean have iV_{oc} of 721,713 and 710 mV respectively. High τ_{bulk} (>10ms) coupled with very low J_0(5 fA/cm^2) have enabled τ_{eff} low to high injection) of RCA cleaned sample to be significantly higher than the samples cleaned by UV ozone and DI-O_3.[15]

Figure 17 shows the results of silicon samples cleaned by three methods. They achieved comparable surface clean as the J_0 of RCA, DI-O_3 and UV ozone clean is 5 fA/cm^2, 8 fA/cm^2, and 7 fA/cm^2. τ_{eff} also follows the same trend. The slightly better result from UV ozone than DI-O_3

might come from a thicker oxide layer generated by UV. As the mechanism of ozone clean is to grow oxide of silicon surface and subsequently remove organic and inorganic impurities by etching such an oxide layer in HF. The thickness of the UV ozone oxide layer is 1.6 nm. While DI-O_3 oxide layer thickness is around 1.3 nm. But in general, as we mentioned before, all three methods can achieve the surface quality of J_0 less than 10fA/cm^2, which considered a good enough result for surface cleaning.

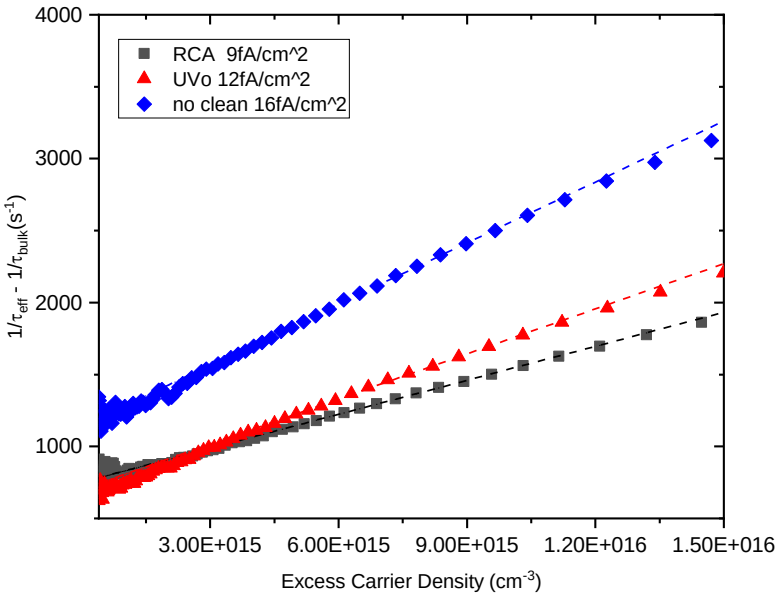


Figure 18: Auger-corrected inverse τ_{eff} of samples applied RCA clean, UV-ozone clean and no clean.

Figure 18 proves the necessity of the cleaning process, as the cleaning methods clearly improved τ_{eff} and J_0. With cleaning methods applied, the J_0 drops 25-50% and τ_{eff} almost doubled. It also proves our previous claim about "good enough" J_0 as the RCA cleaned sample has almost identical τ_{eff} but 25% less J_0 of the UV-ozone cleaned sample. But the uncleaned sample gets only half of the τ_{eff} with 33% more J_0 than UV-ozone cleaned sample. In another word, the J_0 will greatly affect the τ_{eff} when its number above a specific threshold but the effect will greatly drop when the number is under the threshold.

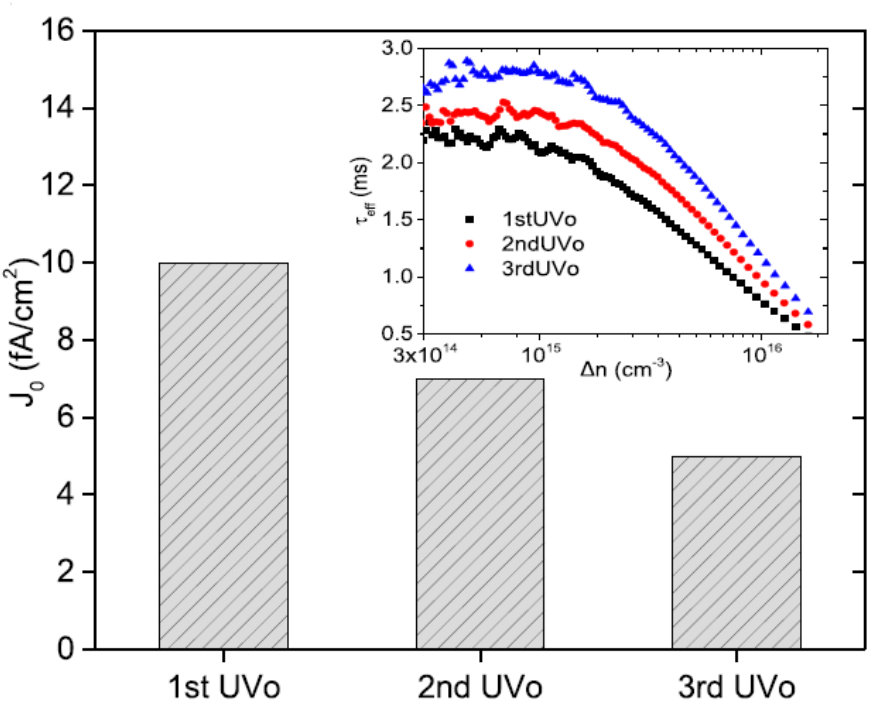


Figure 19: J_0 and τ_{eff}(inset figure) of samples that went through once, twice, and three times UV ozone clean. iV_{oc} of the sample cleaned with UV ozone three times was increased to 718mV.[15]

Figure 19 proves further sequences of UV ozone treatment can provide an even better clean effect. 1st UVo means the sample only goes through UV exposure and HF dip cycle once. 2nd and 3rd UVo refer to samples take such cycle twice and three times. As shown in the figure, more cycles resulted in a longer lifetime and lower J_0. Typically, the J_0 decreased about 2 fA/cm^2 for each extra cycle of the UVo process. After three times UV ozone process the J_0 is already close to RCA cleaned samples. Again, because the J_0 is already "good enough" for even one cycle of UV-ozone treated sample, the τ_{eff} didn't change much as the cycles increase. But the decrease of J_0 shows UV-ozone cleaning can reach the exact surface quality as RCA cleaning, no matter what the bulk property is.

Furthermore, since UVo clean is a dry process, it consumes less chemical and the possibilities of impurities contaminating samples that typically reduce the performance and yield of semiconductor devices are less than the wet clean process[44-46].

To further simplify the clean process, we reduced UV exposure time to 5 minutes. All the other processes are the same as the previous experiment. As shown in Figure 20, such reduced time UV exposure still gives a comparable result. Ellipsometer measurement shows the thickness of the oxide layer grown by 5 minutes of UV exposure is around 1.4nm. It indicates that such thickness of UVo is already sufficient to react with organic and inorganic contaminants. The two sample results of A and B show the good surface quality of the reduced UV exposure time process is reproducible.

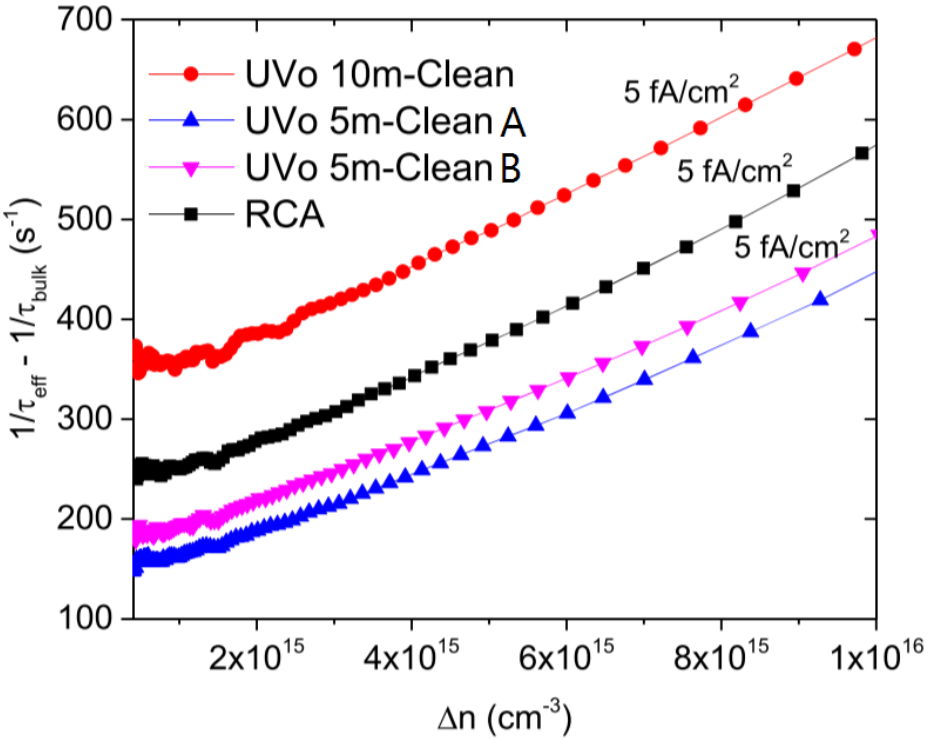


Figure 20: Auger-corrected inverse τ_{eff} of samples processed for RCA and UV ozone clean with a varying exposure time of 10 and 5 minutes. Samples with 5 minutes UV ozone clean have iV_{oc} of 721 and 720mV, respectively.[15]

3.5 Summary

We have experimentally proved UV-ozone treatment as a successful method of silicon wafer surface cleaning. The treatment can be repeated multiple times, each time can prove about 20% improvement of the cleaning quality. After three times of UV-ozone treatment, the cleaning quality is close to the industrial standard RCA cleaning result. We also experimentally proved 5 minutes of exposure time under a UV source is long enough for the UV-ozone cleaning process.

CHAPTER 4: PASSIVATING THE SURFACE

Passivation, originally a chemistry process, refers to a material become “passive”, which means less affected by the environment. While in the semiconductor area, surface passivation especially refers to the process that creates a thin layer on the semiconductor surface to improve the performance of the device. Surface passivation is another important process for pursuing high conversion efficiency. The passivation helps to prevent unwanted recombination of photogenerated electron-hole pairs in two ways[17]. It completes the dangling bonds by a surface dielectric coating or chemical species, usually referred as the chemical passivation. It also reduces the minority carrier density on the surface to lower the recombination rate, referred as electrical passivation[57].

4.1 Materials of The Passivation Layer

Multiple materials are studied as a passivation layer for silicon solar cells. The thermally grown silicon dioxide is one of the most common dielectric films in the semiconductor area. Its passivation quality for silicon solar cell application has been well studied[18, 58]. A so-called *alneal* process[59] was introduced to achieve good passivation quality. The thermal SiO_2 layer was deposited with aluminum and then annealed at 400-450°C in a forming gas atmosphere. The process generates hydrogen and diffused it to the Si-SiO_2 interface to improve passivation quality, the aluminum was stripped by acid later. Silicon nitride (SiN_x) is another well-studied passivation

material[19, 60-62] and currently the standard film for commercial production of silicon solar cells[63]. It has several advantages to be such successful. First, the deposition of SiN_x is achieved by the low-temperature method (comparing to SiO_2) like PECVD, which is more favorable to mass production. Second, the deposition and post-deposition anneal release a large amount of hydrogen to passivates defects on the surface and in bulk. Third, the refractive index of SiN_x makes it be an excellent antireflection coating as well. The combined stack of SiO_2/SiN_x was also studied and reported[64, 65]. Introducing aluminum oxide (AlO_x) surface layer became one of the main breakthroughs in surface passivation in the recent two decades. It was first proved to be a capable passivation layer in the 1980s[66] and attracts research interests until now[21, 22, 67]. The main advantage of AlO_x is its concentration of negative charge[67] rather than the positive charge from SiO_2 and SiN_x, which makes it especially suitable for the p-type surface as it won't induce inversion layers that lead to shunting loss[57].

4.2 Applying UV-Ozone Treatment for Passivation

The benefit of UV-Ozone treatment in organic photovoltaics has been well-studied. It was reported to be used to treat the ultrathin aluminum and form an alumina interlayer between the active layer and indium tin oxide (ITO) to improve electron extraction[50]. The UV-Ozone treatment was also reported to improve the charge collections in dithienogermole–thienopyrrolodione-based polymer solar cells while treating the zinc oxide–polyvinyl pyrrolidone (ZnO-PVP) nanocomposite film used as an electron tunneling layer[68]. Aside from electron tunneling layers, UV-Ozone treatment on the hole collection layer like molybdenum trioxide (MoO_3) was reported to improve the surface morphology, transmittance, and film quality[52]. In addition, UV-Ozone treatment was demonstrated to change the highest occupied molecular orbital level of Phenyl-C61-butyric acid methyl ester ($PC_{61}BM$)[14].

In this chapter, we will discuss in detail how the UV ozone treatment improves the passivation quality of AlO_x.

4.3 Experiment Process

Planar 2.5 Ω.cm p-type silicon wafer and textured 2.5 Ω.cm n-type Cz silicon wafer was used in this experiment. All the samples go through TMAH saw damage etch at 90 °C and UV-ozone cleaning process before passivation. Samples were exposed under UV light with different time duration to generate a layer of silicon oxide of different thicknesses. All the samples were deposited aluminum oxide by thermal ALD and annealed in nitrogen ambient later.

PV2000 Semilab SDI instrument was used to measure effective carrier lifetime τ_{eff} and surface recombination current density J_0 of annealed samples. Btimaging LIS-R1 system was used to obtain the PL image of samples[69]. The images were taken under the quasi-steady-state photoluminescence (QSS-PL) mode. Cross-sectional TEM specimens were prepared using an FEI 200TEM FIB to obtain the nano-scale interface characterization. HRTEM images were obtained in the conventional TEM model (FEI Tecnai F30 TEM) at an operating voltage of 300kV.

4.4 Results and Discussion

Figure 21 shows a comparison of samples with or without UV ozone treatment. Clearly, the UV ozone treated sample has a longer lifetime τ_{eff} and lower J_0, meaning better passivation quality. Again, the results show the great effect of J_0 on τ_{eff} around the threshold value. The passivation without UV-ozone treatment has J_0 of 11fA/cm^2 which at the edge of the good spot while UV-ozone treatment can help to decrease the J_0 down to 7fA/cm^2. The lifetime of the UV-ozone treated sample is 50% longer than the sample without treatment. The decreased J_0 also makes a buffer zone for the sample by sample variation that may get a J_0 out of the "good enough" zone.

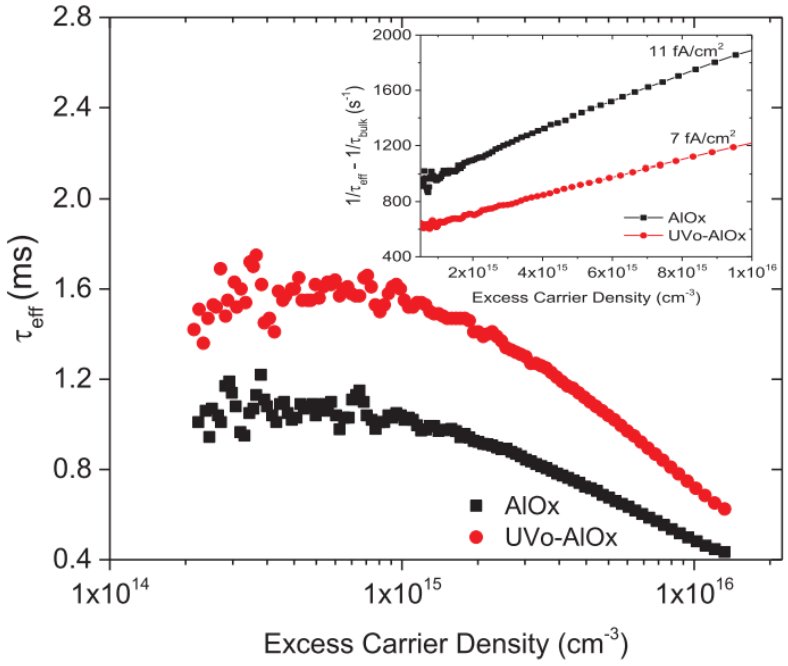


Figure 21: Comparison of τ_{eff} and J_0 (inset figure) between samples passivated by AlO_x and UVo/AlO_x stack.[22]

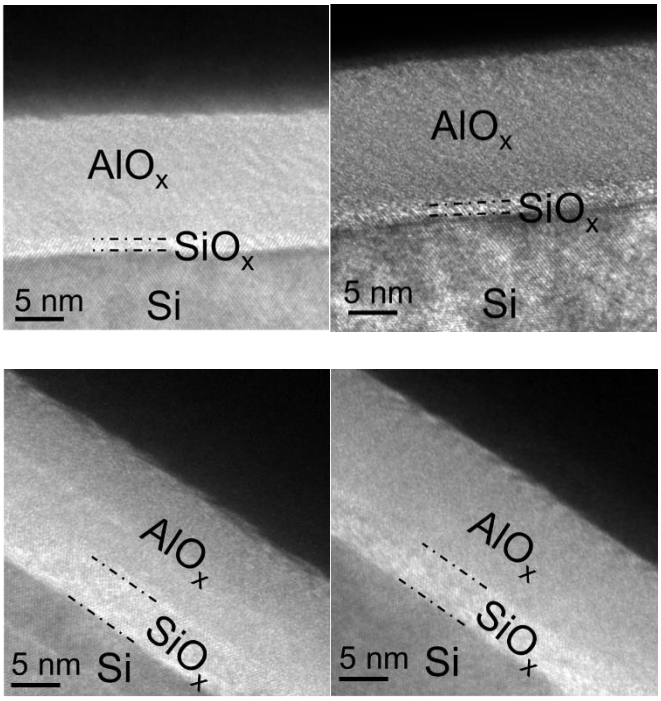


Figure 22: HRTEM images of c-Si/AlOx: as-deposited (top left), after annealing (top right); c-Si/UVo (15 min)/AlOx: as-deposited (bottom left), after annealing (bottom right).

It can be seen in Figure 22 that a 1-2nm of SiO_x interlayer is present at the c-Si/AlO_x interface even in the as-deposited state for samples not subjected to UVo treatment. This indicates that SiO_x was formed during the ALD of AlO_x. On the other hand, a 4-5nm of SiO_x interlayer is observed at the c-Si/AlO_x interface in the as-deposited state for samples subjected to 15 min UVo treatment. This indicates that possibly a 3-4nm SiO_x layer is formed at Si surface when subjected to UVo treatment for 15 min which grows further to 4-5nm during subsequent AlO_x deposition. In both cases, HRTEM images reveal no apparent structural change during annealing. In a nutshell, HRTEM images revealed the presence of a 4-5nm of SiO_x layer at the c-Si surface when subjected

to 15 min of UVo treatment followed by AlO_x deposition. This 4-5nm SiO_x layer results in improved surface passivation as evidenced by the lower J_0 value of 7fA/cm^2.

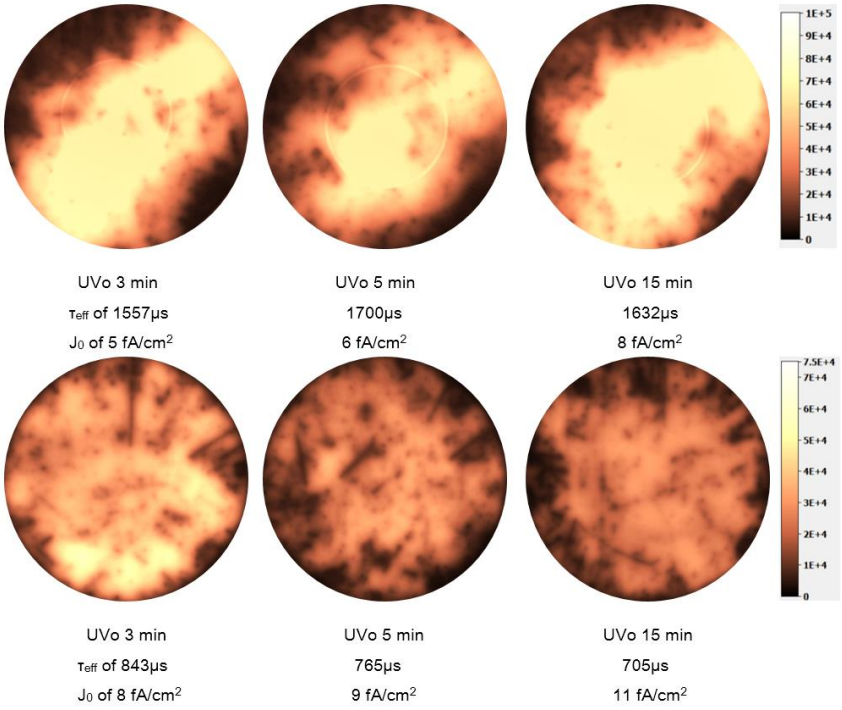


Figure 23: uncalibrated PL lifetime images of planar (top row) and textured (bottom row) samples go through different UV-ozone grow time before passivated by AlO_x. τ_{eff} and J_0 values from PCD measurements are listed for each.

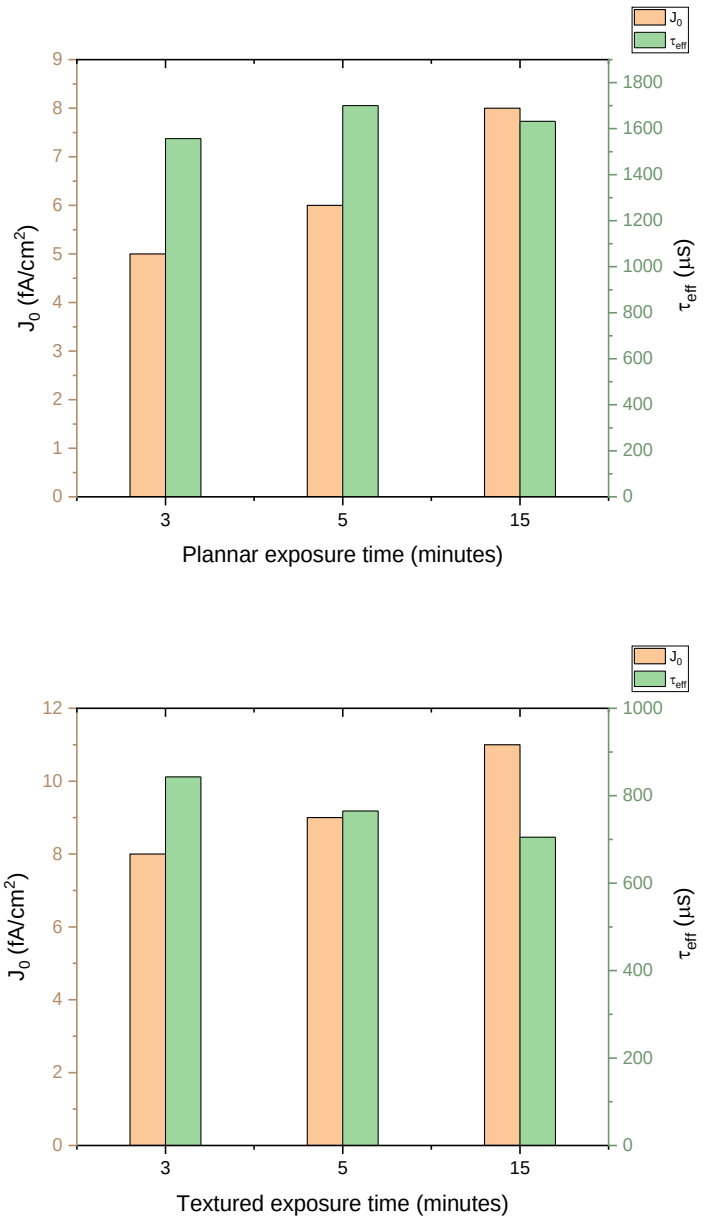


Figure 24: PCD measurement results of planar and textured samples with different UV exposure time before ALD passivation.

Similar to the previous chapter, we explored the effect of different UV exposure time on the passivation stack. Figure 23 shows uncalibrated PL lifetime images of both planar and textured samples. Figure 24 shows the J_0 and τ_{eff} of the same samples acquired by PCD measurement. The planar samples are *p*-type 2.5Ω-cm silicon wafer and the textured samples are *n*-type 1.5Ω-cm silicon wafer, All samples were processed with a UV ozone clean (5 minutes of UV exposure, followed by HF dip) three times, passivated with a UVo/AlO_x stack (different UV exposure time followed by 10-15 nm AlO_x by ALD), and then annealed in N_2 at 450 °C for 30 minutes. Such a process was proved to be the optimized procedure for UV-ozone cleaning and UV-ozone treated ALD passivation experimentally. Both planar and textured samples show good uniformity. The τ_{eff} and J_0 values are extracted by PCD measurement. The τ_{eff} of planar samples ranges from 1557 to 1700μs and J_0 5 to 8 fA/cm^2. The textured samples have a shorter lifetime τ_{eff} 705 to 843μs and higher J_0 8 to 11 fA/cm^2. The uniformity of textured samples is also worse than the planar sample as shown in the figure. Slightly poorer passivation on textured samples relative to planar samples could be attributed to two major reasons. Firstly, since we chose the AlO_x as the passivation layer material, the *p*-type wafer is supposed to have better passivation quality than the *n*-type wafer. Secondly, it may due to an increased surface area of textured pyramids and non-conformal coating of pyramid peaks by the thin UV ozone passivation layer. But overall, with the reduced UV ozone oxide layer thickness, samples in this work still get good passivation quality and uniformity.

We further discovered how the passivation quality changes depending on wafer doping concentration. Both *n*-type and *p*-type heavily doped silicon wafers were treated with TMAH etch.

Doping concentration was controlled by different etching times. Sheet resistance R_{sh} were measured after etching as the indicator of doping concentration, the higher R_{sh} means the lighter doped. All the samples go through the 5min UV-ozone grow followed by AlO_x passivation. Figure 25 shows the J_0 from the PCD measurement of passivated samples. Both *n*-type and *p*-type results show better passivation quality with the lighter diffused sample, as the electrical passivation has more effect on less dopant. The general better result from *p*-type samples could due to the negative charge generated during AlO_x passivation[57]. It also worth to mention for lightly diffused samples, both *n*-type and *p*-type surface get good passivation quality, while the heavily diffused *p*-type surface get much better passivation quality than *n*-type. Because for *p*-type surface, the negative charges from AlO_x passivation is enhancing the potential barrier but for *n*-type, it is reducing the existing potential barrier. So, for heavier diffused sample maybe it actually let the carrier move easier, makes the passivation quality worse. And for lighter diffused samples it overcomes the existing barrier and builds its own potential barrier, so it also has a good passivation quality.

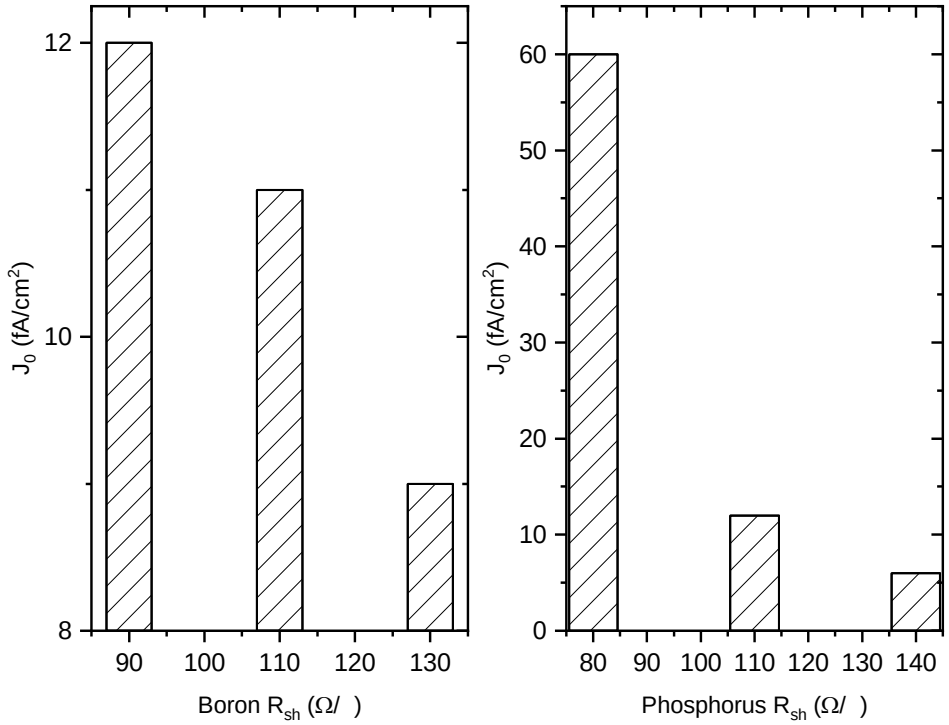


Figure 25: J_0 of AlO_x passivated silicon wafers. The different doping concentration of n-type and p-type samples are shown, respectively.

4.5 Summary

We have experimentally proved UV ozone treatment can improve AlO_x passivation quality when applied before the ALD process. The effective lifetime is 50% longer with UV ozone treatment applied. The improvement happened on both planar and textured sample, *n*-type and *p*-type, lightly and heavily doped. The planar sample gets better passivation quality than the textured sample due to the bigger surface area and less uniformity of the surface of the textured sample. *P*-type sample gets better passivation quality than *n*-type sample due to AlO_x as the passivation material generates extra negative charges that contribute to the electric passivation of the *p*-type sample. Lightly doped sample gets better passivation quality than heavily doped sample due to the less dopant of the lightly doped sample, makes electric passivation relatively more effective.

CHAPTER 5: CONTACT RESISTANCE AND HOW TO DECREASE IT

The concept of contact resistance refers to the resistance attributed to the contacting interface, rather than the intrinsic resistance which is an inherent property of the material itself. In solar cells, the contact resistance specifically referred to the resistance due to the interface between contacting metal and the light-absorbing silicon wafer. It is a crucial parameter to the power conversion efficiency of the cell. Typically, the contact resistivity at the order of 1~10 $m\Omega.cm^2$ is considered as an acceptable good number. The most common way to measure it is by applying the transmission line model (TLM).

5.1 Methods of Reducing Contact Resistance

the intimate metal-silicon contact leads to recombination losses due to a high density of states at the metal-silicon interface[24]. The selective emitter is a commonly used way to drastically lowering contact resistance. The design uses high-temperature functional-impurity doping beneath the metal terminal to achieve it. But this absorber doping induces its own fundamental energy losses like Auger recombination, bandgap narrowing, and free-carrier absorption to limit the device performance[25-28]. Due to these inherent limitations, the concept of passivating contacts was introduced[24]. A passivation thin film inserted between the silicon wafer and the metal terminal, physically separate them to prevent the recombination loss of direct contact but thin enough to allow current flows. The early approach of passivating contact took the form of metal-

insulator-semiconductor(MIS) contacts[29]. A specific structure of metal-insulator-semiconductor-insulator-metal(MISIM) was realized[70] with good performance. It used two different metals for electron and hole collection and a film of silicon oxide as the insulator layer. The lack of choice for affordable, high-work-function metals limits the application of such structure. The MIS inversion layer(MIS-IL)structure solves the issue by forming a front MIS contact on a p-type cell with an Al-BSF hole contact. The MIS contact was formed by thermally evaporated Al and thin film of thermally grown SiO_2[71]. Another design is the metal-insulator-NP junction (MINP) concept. It formed MIS contact on a dopant-diffused surface, looking for the benefits of reduced recombination velocity[72]. Different metals and insulators are studied using the MINP structure for both n-type and p-type silicon cells[31, 32].

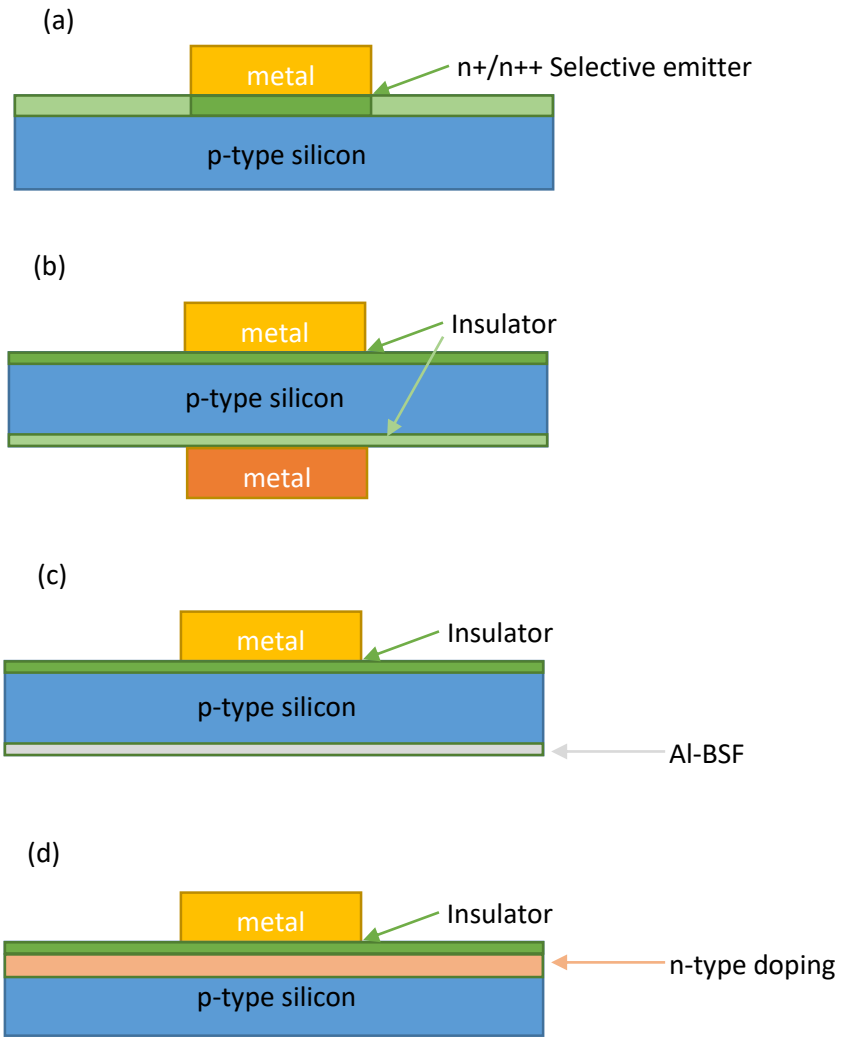


Figure 26: schematic pictures of different designs for reducing contact resistance. (a) selective emitter, (b) MISSM, (c) MIS-IL, (d) MINP

5.2 Experiment Process

Heavily diffused samples were performed in 25% TMAH solution at 70°C with varied time to obtain different doping concentrations. Sheet resistance was measured (Ossila Four-Point Probe System) after TMAH etch as the indicator of doping concentration. SIMS measurement (PHI Adept 1010 Dynamic SIMS System) was performed later to prove the indicator is trustworthy.

UV-ozone treated samples(UV-ozone clean and thin oxide layer grown on the surface) were deposited with Aluminum for contact resistance measurement by the TLM method[73, 74]. The TLM pattern was made by covering a shadow mask on the sample while depositing Aluminum. The shadow mask was cut from a thin silicon wafer by a laser marking system (TYKMA Electrox Minilase Manual). The mask design was made by related software of the marking system(Minilase PRO SE). The Aluminum deposition was performed by e-beam evaporator (Temescal FC2000), the depositing speed is 0.1nm/s and the final thickness is 900 nm. Samples were annealed in a nitrogen ambient at 450°C for 30 min after metal deposition. The TLM measurement was performed by a semi-auto tool, the Contactspot from BrightSpot Automation.

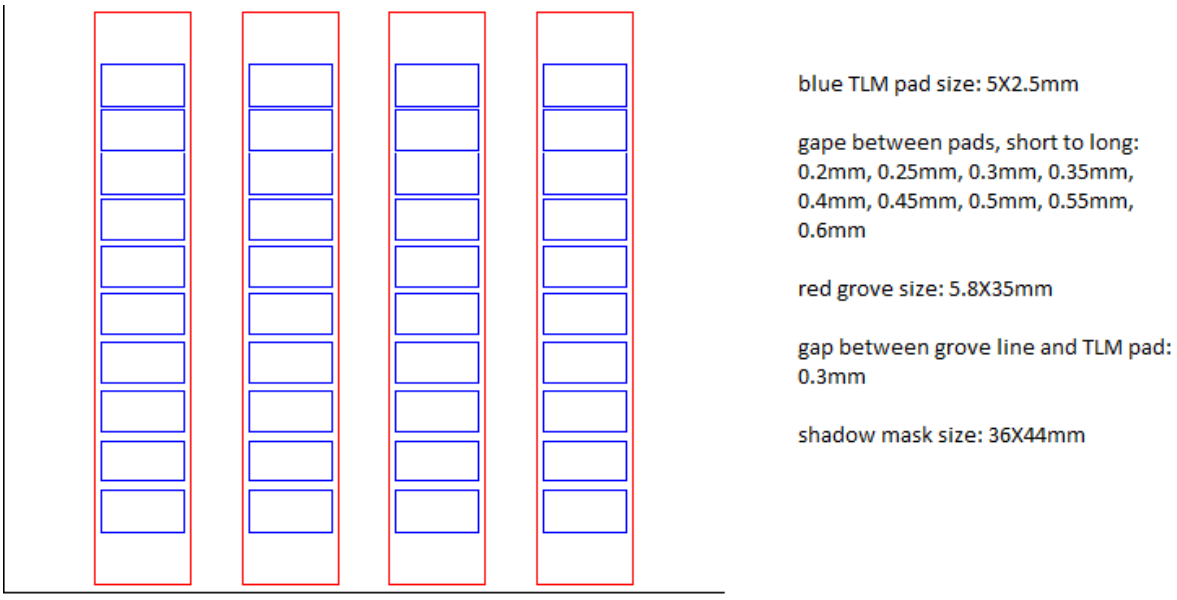


Figure 27: TLM mask design

The nitrogen ambient annealing after the metal contact deposition is to active the conductance of this MINP structure. The annealing temperature is critical to the contact resistance. We varied annealing temperature from 350 to 550°C to see how it affects the measured contact resistance. For the cases of annealing temperature less than 400°C, the total resistance between contacts is extremely high. When the applied voltage reaches 1.15V which is the system's higher limit, the measured current is only 2 to 4 mA. We believe this situation means the UV generated oxide layer completely separated metal contact and the silicon wafer, build an open circuit. Annealing temperature between 400 and 450°C is the best shot for most of the samples, we will discuss these experiment results later in detail. Further increase the annealing temperature up to 550°C shows contact resistance increased again and the fitting curve of TLM shows a different shape than previous. We assume it means the oxide layer has been dissipated during the high-temperature

annealing, turned the contact structure into a simple metal-semiconductor interface. We did not try higher annealing temperature as the melting point of aluminum is 660°C. Based on these experiments, we decided 450°C as the optimized annealing temperature and keep using it in all the experiments.

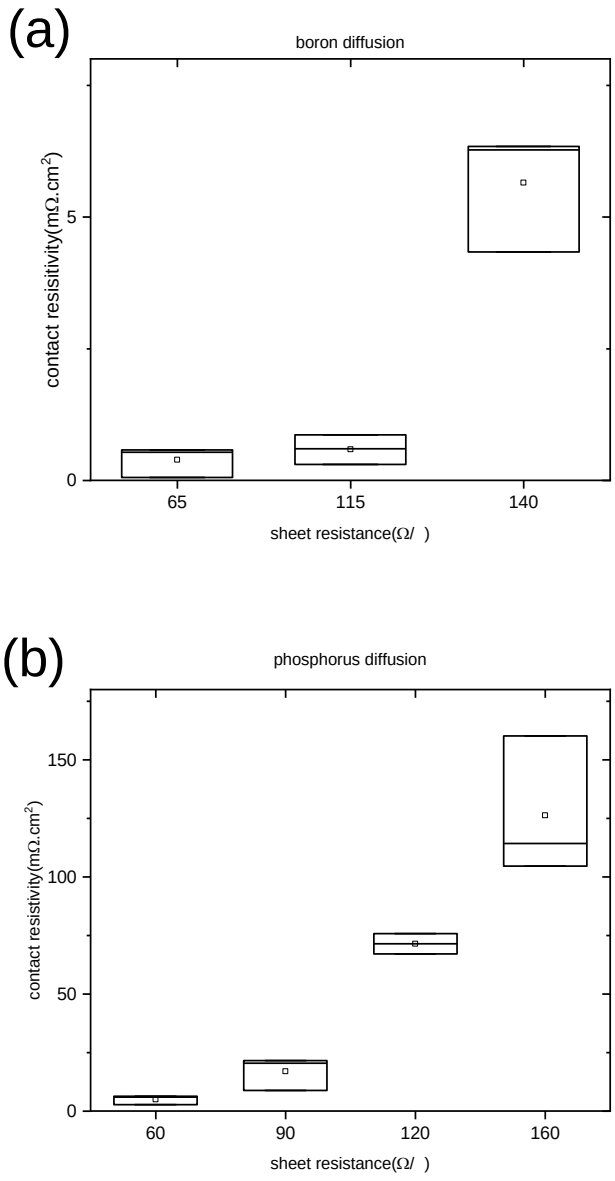


Figure 28: contact resistivity of (a) *p*-type and (b) *n*-type samples following different TMAH etching time to create diffusion situation from light to heavy.

Figure 28 shows the contact resistivity of both boron and phosphorus diffused silicon samples with different doping concentrations. The box plot included data of every TLM pattern on the samples. As shown in Figure 27, each sample with different R_{sh} was covered by a TLM mask with four separate stripes of TLM patterns. So, each box takes these four fitted results to show the average and variation range. The box plot shows for high R_{sh} case(lightly diffused) the measured contact resistivity gets a bigger variation range. It may because for these samples the dopant is etched a lot, makes the surface less uniformity. So, the different stripes on the same sample actually see different material properties, which results in the bigger variation of contact resistivity between them.

As for the quantitative analysis of the contact resistivity. The boron diffused samples provide lower resistance in general. The heavy diffused samples (R_{sh}=65Ω/□) get the lowest resistivity as 0.4mΩ.cm^2 on average, even light diffused samples (R_{sh}=140Ω/□) have an average resistivity of 5.6mΩ.cm^2. Heavy phosphorus diffused samples (R_{sh}=60Ω/□) have comparable low average resistivity of 5mΩ.cm^2, but it increases drastically with sheet resistance. The normal diffused samples have an average resistivity of 17mΩ.cm^2 and the light phosphorus diffused samples (R_{sh}=160Ω/□) reach 126mΩ.cm^2. In general, a higher doping concentration is needed for lower contact resistivity.

But higher doping concentration not always means better. As we have already proved in the previous chapter, higher doping concentration means more carriers on the wafer surface and will result in a shorter lifetime. On the other hand, a lightly diffused wafer sacrifices contact resistivity and surface uniformity for a longer carrier lifetime. Clearly, there is a trade-off between these parameters for the good performance of the cell. In practice, the R_{sh} around 100Ω/□ is considered a moderate diffused case with balanced and good performance.

5.4 Investigation of Contact on AlO_x Passivation

As we have shown in previous chapters, the SiO_x/AlO_x stack provides high-quality surface passivation, and the SiO_x/Al stack provides low contact resistance. It would introduce more complexity to the fabrication for different layer structures of contacted and not contacted surfaces. So we are trying to discover the conductivity of a SiO_x/AlO_x/Al stack, figuring out if we can form good contact by applying contact on top of the high-quality passivation layer, thus simplify the overall fabrication process.

5.4.1 Experiment setup and methods

The sample design was shown in Figure 29. The bulk silicon is a 1.5 Ω.cm p-type silicon wafer. The back contact is rapid-fired Al-BSF, a separated TLM measurement shows the contact resistivity of 6.5 $m\Omega.cm^2$. The SiO_x layer was formed by UV-Ozone treatment as described in the previous chapter. The thin AlO_x layer for about 1.5nm was deposited by the ALD process. The front contact node is 800nm Aluminum deposited by an e-beam evaporator.

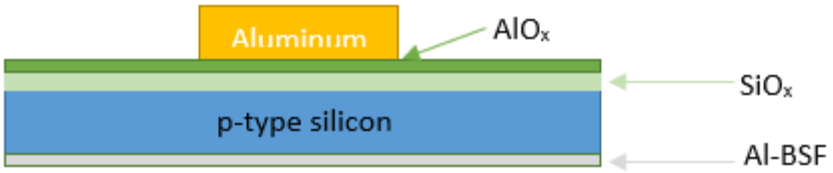


Figure 29: structure scheme of the experiment sample

The possible carrier transport in the sample can be cataloged as several types. Tunneling is one of the major effects that might happen under a high field. The tunnel emission is a result of the quantum mechanic that allows electron wave function to penetrate a potential barrier. It can happen for direct tunneling that penetrates the whole width of the potential barrier or Fowler-Nordheim tunneling that tunnel through a partial width of the barrier.[75] For both cases, the process is highly dependent on the applied voltage and independent of temperature.

Thermionic emission is another process of carrier transport. The electron gets enough kinetic energy from heating to overcome the potential barrier. As the name indicated, the process is highly dependent on temperature.

The Frenkel-Poole emission is also a possible type of carrier transport.[76] The trapped electrons were emitted into the conduction band due to thermal excitation. For trap states with Coulomb potentials, the expression is similar to thermionic emission while the barrier height is replaced by the depth of trap potential well.

With low voltage and high temperature, the carrier transport can be the form of electrons hopping from one isolated state to another. This mechanism will result in an ohmic characteristic behavior.

The space-charge-limited current occurs when carriers injected into a material with no compensating charge presented, such as lightly doped semiconductor or insulator. For this unipolar trap-free case the current is proportional to the square of the applied voltage.

For a given structure, these processes may not exactly independent from each other, and different processes may dominate the carrier transport at a certain temperature and voltage range. Table 1 listed the basic types of carrier transport processes and their dependence on voltage and temperature. The experiment sample was measured I-V curve at different temperatures. By fitting the I-V curve and I-T curve with different dependence expressions, we can get an understanding of which process is the most possible dominant process.

Table 1: Basic carrier transport types

Process	Voltage and temperature dependence
Tunneling	$J \propto V^2 e^{-\frac{b}{V}}$
Thermionic emission	$J \propto T^2 e^{\frac{q}{kT}(a\sqrt{V}-\phi_B)}$
Frenkel-Poole emission	$J \propto V e^{\frac{q}{kT}(2a\sqrt{V}-\phi_B)}$
Ohmic	$J \propto V e^{-\frac{c}{T}}$
Space-charge-limited	$J \propto V^2$

5.4.2 Experiment Results and Discussion

The sample's I-V curve was measured by a MDC CSM/Win Semiconductor Measurement System. The temperature was controlled by a Instec mK2000 precision temperature controller. Figure 30 shows the measured I-V curve of the as-deposited sample at different temperatures. As the figure shows, the sample does not have a good conductance. The maximum current is less than 0.2mA. Further fitting shows the curves match thermionic emission type and space-limited-charge type well. We believe both mechanics contribute to carrier transport as the curve varies along with the temperature but not as the thermionic emission type predicted. Either way, the carrier does not transport through direct contact, makes conductivity high.

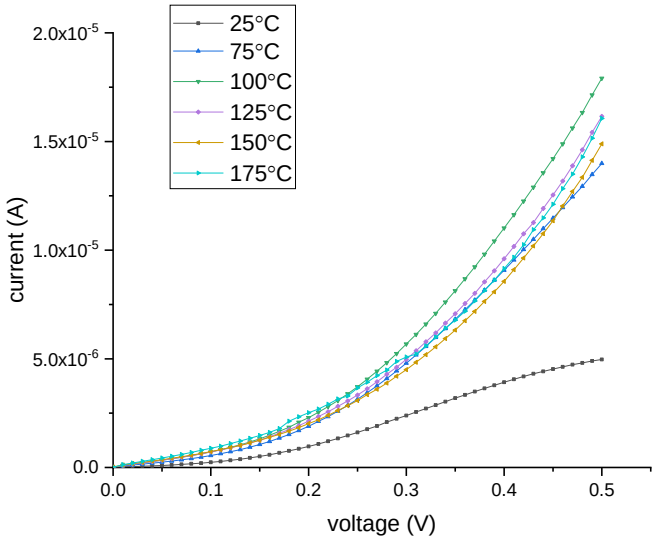


Figure 30: I-V curve of the sample measured at different temperature

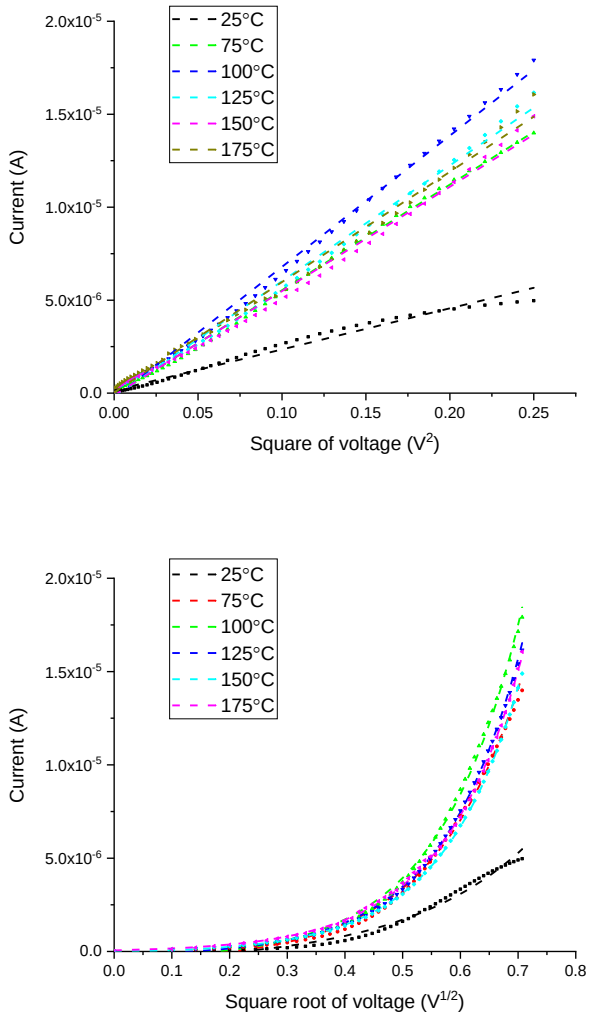


Figure 31: the fitting curve of space-limited-charge relation(upper) and thermionic emission relation(lower)

We also investigate the sample after annealing. The sample was annealed in a nitrogen ambient at 450°C for 30 minutes. We chose this anneal process because it is the standard annealing situation to activate the AlO_x passivation in our previous experiment.

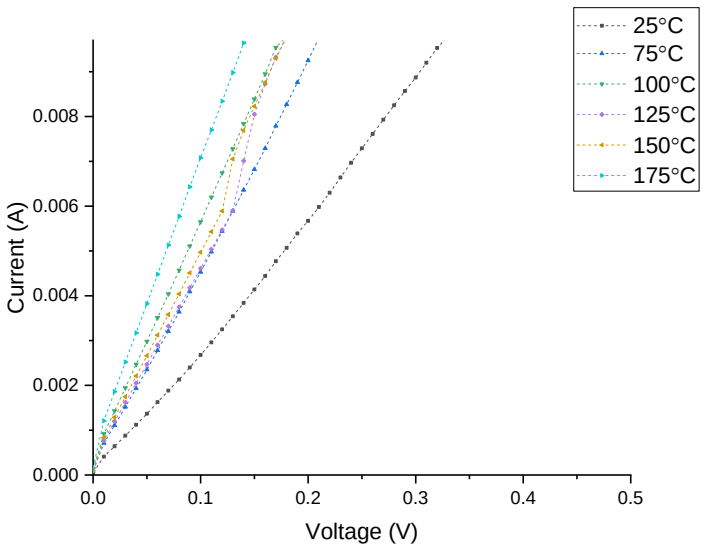


Figure 32: I-V curve of the annealed sample measured at different temperature

Figure 32 shows the I-V curve of the sample after annealing. Comparing to the result before annealing, the conductance improved significantly. The measured current easily reached the higher limit of the measurement system which is 0.01A. It also worth mention that the type of carrier transport also changes, as the annealed I-V curve shows a linear relationship between current and voltage, attributed to the ohmic type transport. It remains further investigation to figure out the structural mechanic behind the low conductivity ohmic contact.

5.5 Summary

We built a MINP structure for both *n*-type(MIPN for *n*-type in fact) and *p*-type silicon wafer substrate. The experiment results show Boron doped sample has less contact resistivity than Phosphorus doped one in general. Higher doping concentration will generate lower contact resistivity for both doping situations. But there are trade-offs between other properties to improve cell performance in the end. A combination of passivating contact and AlO_x passivation shows a low conductance without annealing but greatly improved after annealed in a nitrogen ambient at 450°C for 30 minutes. The detailed carrier mechanic behind it remains unclear and needs further investigation.

CHAPTER 6: SIMULATION OF THE CELLS

In the above chapters, we applied UV-Ozone treatment for different processes of fabricating the solar cell. The results proved such treatment made contributions to higher quality in each step. But for the solar cell as a device, all the processes are aiming for one goal at last: higher power conversion efficiency. we would like to make real cells with UV-Ozone treatment involved but the project and time schedule limited our ability. In this chapter, we will simulate the solar cell with experimental parameters, and discuss how these different parameters affect the final efficiency of the cell.

6.1 Simulation Methods and Setup

The optical simulation was done by Sunsolve, which combines ray tracing with thin-film wave optics. The program sets a number of rays, each assigned a wavelength, intensity, and direction. They are traced as a straight line until hit an interface between different materials. The interaction was calculated as thin-film wave optics to determine absorptance, reflectance, and transmittance. Thus, decided the intensity and direction of the next step ray trace. Such loop of calculation repeated until 1) the ray either reflected from the front surface or transmitted through the rear surface of the simulated module, or 2) the ray's intensity decreased lower than a threshold, or 3) the ray has reached the maximum interaction count. In the end, the gains and losses are recorded for each ray and averaged to give the result used in the further simulation. The simulation's

accuracy can be improved by applying more rays, lower intensity threshold, and higher interaction count cap. Through optical simulation, we discussed how to optimize the interface stack on a silicon wafer to maximize the electron generation.

The 3D device simulation of solar cells was performed with Quokka[77], based on the conductive boundary approach[78]. The program numerically solves 3D steady-state charge carrier transport in a quasi-neutral silicon device to figure out parameters of the device's performance. The near-surface regions are modeled by several decisive parameters like sheet resistance and effective recombination characteristics rather than detailed doping profile and surface recombination. Thus the simulation can be performed quickly without losing accuracy. All input simulation parameters are determined experimentally, PCD measurement for J_0 values, four-point probe measurement for R_{sh} values, and TLM measurement for R_c values. The generation file was acquired from the Sunsolve simulation as described above.

6.2 Optical Simulation Results and Discussion

We are simulating the cell based on the structure so-called bifacial passivated emitter and rear contact(bifi PERC). The simulation is on the cell level, so the contact grid was not considered. The first and foremost is the front surface design, to collect incident light as much as possible.

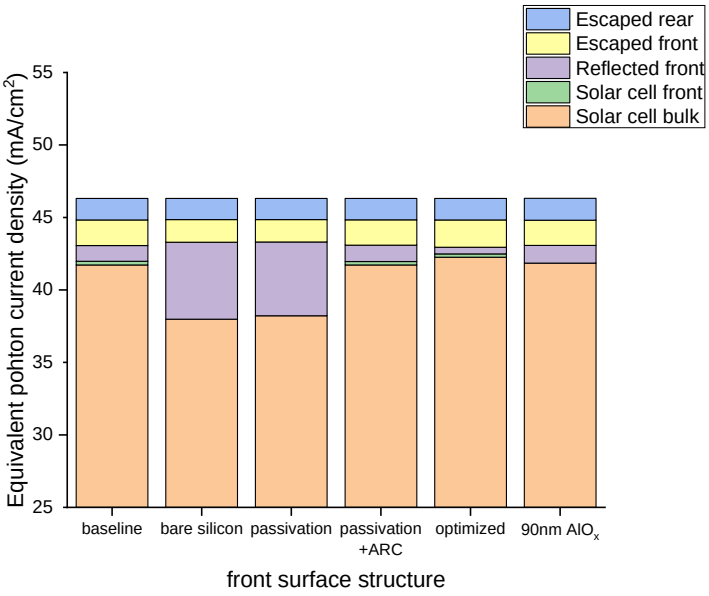


Figure 33: equivalent photon current density by different simulation setting

Figure 33 shows the simulation results of different front surface setup. We are using the default setting of Sunsolve as a baseline setting. The sample has 125μm thick bulk silicon. The front surface is textured by the upright pyramid and the back surface is planar. The back surface was coated by a stack of 10nm Al_2O_3 and 100nm SiN_x. We are varying the front surface structure to achieve the optimized light collection. The equivalent current density of incident light is

46.32mA/cm^2. The baseline setting has a 75nm thick layer of SiN_x as the anti-reflection coating. The bulk silicon absorbed current density is 41.72mA/cm^2.

Our first try of the front surface design is just using the passivation layer as the experiments shown in previous chapters. The layer is a stack of 5nm SiO_x and 10nm AlO_x. As shown in the figure, this structure is almost the same as the bare silicon surface, which has more than 10% of the incident light reflected on the front surface. The bulk absorbed current density is only 38.22mA/cm^2. This is because the anti-reflection effect required a specific thickness of the film depends on the incident wavelength and refractive index. Thus, the extra anti-reflection layer is needed for the front surface film structure.

with the help of an online calculator OPAL2[79], we determined the optimized anti-reflection coating is a 53nm thick SiN_x film on top of the passivation layer. With this anti-reflection layer, the bulk absorbed current density is the same as the baseline setting.

It is also worth mention that even without the extra SiN_x anti-reflection coating, a well-designed AlO_x layer can also be a good anti-reflection layer. As shown in the figure, the bulk absorbed current density of a single layer of 90nm AlO_x(41.85 mA/cm^2) is even slightly higher than the optimized AlO_x/SiN_x stack(41.72 mA/cm^2). This is due to AlO_x has a very large bandgap that makes it transparent to the whole sunlight spectrum while the SiN_x has some absorption in both UV and IR region(labeled as solar cell front in the figure). But in reality, it is not worth creating

such a thick layer of AlO_x for merely less than 1% improvement of the bulk absorption so we won't consider this structure in the future simulation.

We can further improve the bulk absorption by applying a more complex structure.[80] Adding another SiO_x film on top of SiNx will further decrease the front surface reflection. The optimized design is 5nm SiO_x/10nm AlO_x/39nm SiN_x/98nm SiO_x. The simulation of this structure shows only 1% of the incident light was reflected and the bulk absorption achieved 42.26 mA/cm^2. That is why we labeled it as optimized and will use the generation file from this design in future simulations.

6.3 Cell Simulation Results of Quokka

The unit cell geometry was shown in Figure 34, all simulation parameters were listed in Table 2.

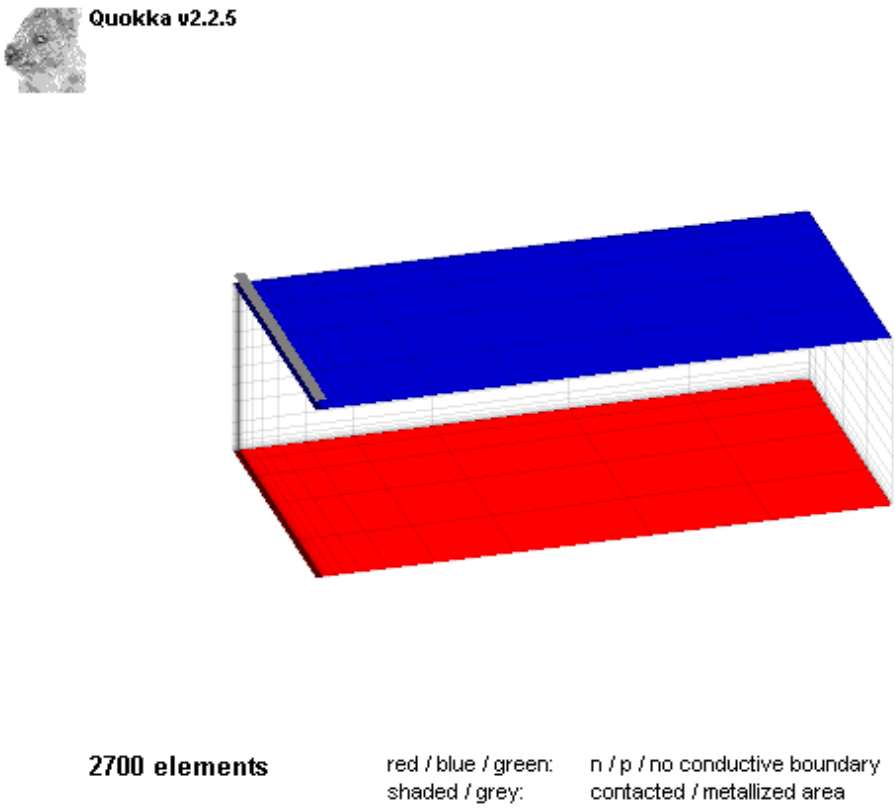


Figure 34: simulation cell geometry generated by Quokka.

Table 2: Parameters used in the simulation.

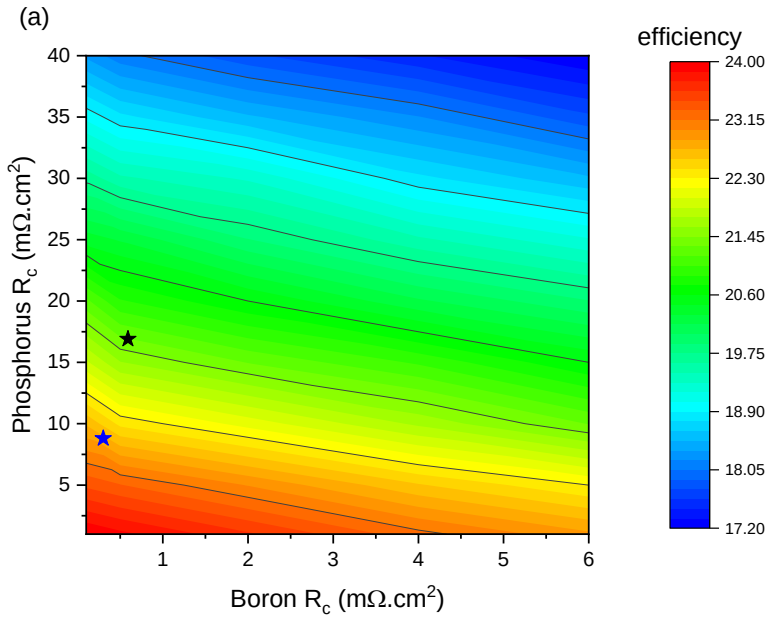
Name	Value
Cell thickness	125 μm
Surface length	399 μm
Surface width	50 μm
Contact length	4 μm
Contact width	50 μm
n-type bulk resistivity	1.5 Ω.cm
SRH electron lifetime	2.5 ms
SRH hole lifetime	2.5 ms
Diffusion sheet resistance	Variable
Diffusion J_0 - passivated	Variable
Contact resistivity	Variable
Front surface J_0 – contacted	150 fA/cm^2
Back surface J_0 – contacted	300 fA/cm^2

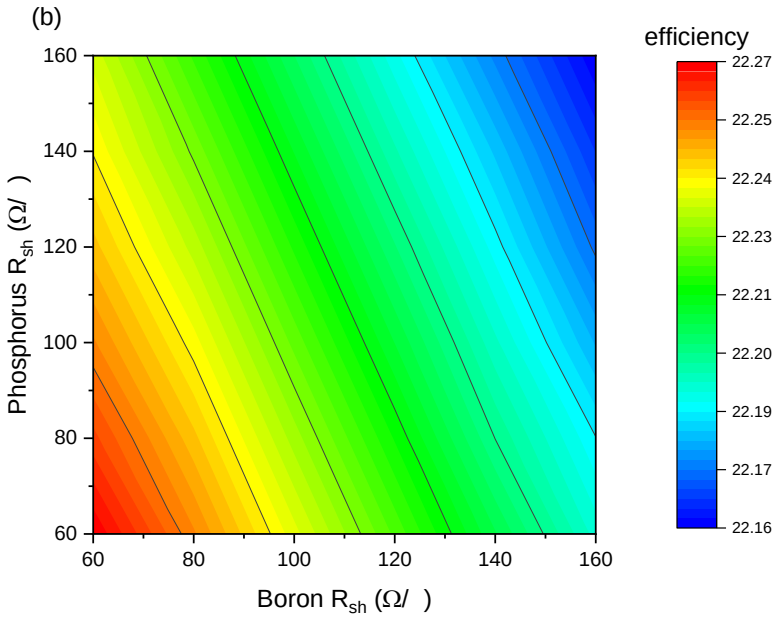
Among the table, parameters of cell size like thickness and length are set as the program default number. Bulk properties(bulk lifetime, SRH electron, and hole lifetime) are real numbers of wafers we used for the experiment. We did not measure them as they are already labeled when we get the wafer. Diffusion R_{sh}, diffusion $J_{0,}$ and contact resistivity are the variable for our simulation. We are going to change these parameters to see how they will affect the power conversion efficiency

of the simulated cell. But the varying range of these variables is determined by the experiments in previous chapters, meaning the lower and upper limit of the variable will not be far away from experiment results. In this way, the simulation will not come up with an unrealistic result that is impossible to achieve in practice. The contacted J_0 is set to an arbitrarily large number to represent its conductance compared to the semiconductor part.

In the simulation, we fixed two of the variable parameters to experimental results and varied one according to the experimental reasonable range. The simulation results are shown in Figure 35, it shows contact resistance is the key factor to the cell efficiency. With fixed sheet resistance and J_0 of both boron and phosphorus diffusion, varying boron contact resistivity from 0.1 to 6 $m\Omega.cm^2$ and phosphorus contact resistivity 1 to 40 $m\Omega.cm^2$ results in a significant efficiency change from 24% to 17.2%. This demonstrates that lower contact resistivity will provide higher efficiency. But with fixed contact resistivity and J_0/sheet resistance, varying sheet resistance/J_0 respectively covering all the experimental results presented in previous sections will only change efficiency less than 0.3%. The stars in Figure 35(a) are referred to the simulation results using the experimental parameters presented in the report. The black star represented simulation result (efficiency 21.5%, V_{oc}=713 mV, J_{sc}=40.6 mA/cm^2 and FF=74.4%) using average parameters of normal diffusion situation (boron contact resistivity 0.6 $m\Omega.cm^2$, J_0=10 fA/cm^2, sheet resistance 115Ω/□. Phosphorus contact resistivity 16.9 $m\Omega.cm^2$, J_0=15 fA/cm^2, sheet resistance 90Ω/□). The blue star represented the best simulation result we got (efficiency 22.8%, V_{oc}=713 mV, J_{sc}=40.6 mA/cm^2 and FF=78.7%) using the parameter of a specific sample (boron contact resistivity 0.3 $m\Omega.cm^2$, J_0=10 fA/cm^2, sheet resistance 115Ω/□. Phosphorus contact resistivity 8.8 $m\Omega.cm^2$,

J_0=15 fA/cm^2, sheet resistance 90Ω/□) in our experiment within the reasonable normal diffusion situation.


(a)
efficiency
24.00
23.15
22.30
21.45
20.60
19.75
18.90
18.05
17.20
Phosphorus R_c (mΩ.cm^2)
40
35
30
25
20
15
10
5
Boron R_c (mΩ.cm^2)
1
2
3
4
5
6


(b)
efficiency
22.27
22.25
22.24
22.23
22.21
22.20
22.19
22.17
22.16
Phosphorus R_{sh} (Ω/)
160
140
120
100
80
60
Boron R_{sh} (Ω/)
60
80
100
120
140
160

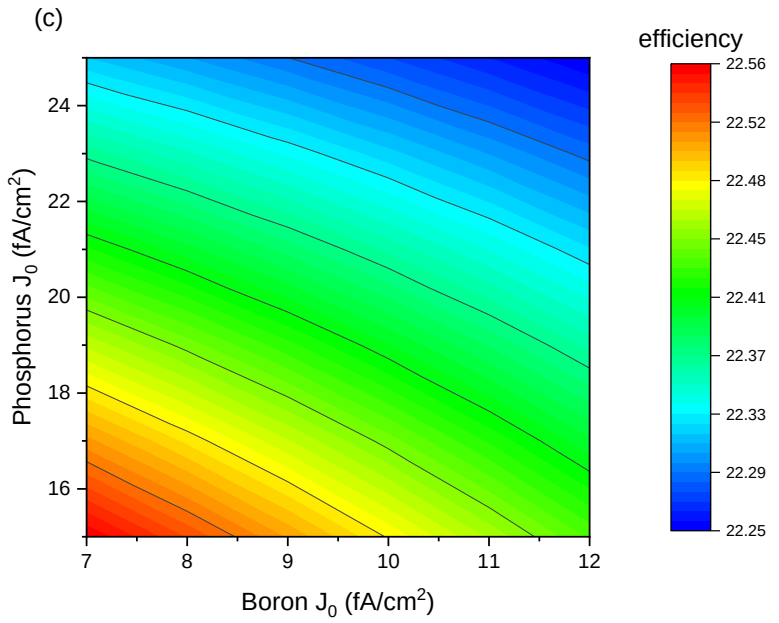


Figure 35: Contour plot of simulated cell efficiency vs sample parameters variable. (a)the sheet resistance and J_0 were fixed as boron J_0=10fA/cm^2, sheet resistance 115Ω/□. Phosphorus J_0=15fA/cm^2, sheet resistance 90Ω/□. (b)the contact resistivity and J_0 were fixed as boron contact resistivity 1mΩ.cm^2, J_0=12fA/cm^2. Phosphorus contact resistivity 10mΩ.cm^2, J_0=25fA/cm^2. (c)the contact resistivity and sheet resistance were fixed as boron contact resistivity 1 mΩ.cm^2, sheet resistance 115Ω/□. Phosphorus contact resistivity 10 mΩ.cm^2, sheet resistance 90Ω/□.

Table 3: Efficiency change based on different variable

Variable (unit)	Range	Efficiency change (%)
R_c ($m\Omega.cm^2$)	Boron 0.1→6	24→17.2
	Phosphorus 1→40	
J_0 (fA/cm^2)	Boron 7→12	22.56→22.25
	Phosphorus 15→25	
R_{sh} ($\Omega/\square$)	Boron 60→160	22.27→22.16
	Phosphorus 60→160	

6.4 Summary

We have simulated the performance of a solar cell based on the experimentally acquired parameters. The simulation results showed a trade-off between parameters as we expected. Lower contact resistivity leads to higher cell efficiency, which can be achieved by increasing doping concentration. Lower J_0 also leads to higher cell efficiency, which can be achieved by decreasing doping concentration. Increasing doping concentration itself for a lower R_{sh} can increase efficiency, too. Within the range of moderate doping situation, contact resistivity shows a dominating effect on power conversion efficiency comparing to J_0 and R_{sh}. The simulation results suggest aiming for a heavier doped design to achieve higher efficiency of solar cells.

CHAPTER 7: SUMMARY AND CONCLUSION

We have demonstrated the effective use of UV-ozone treatment in multiple silicon solar cell fabrication processes:

1) a surface cleaning method providing comparable cleaning quality to the industrial standard RCA clean. Both methods can reduce the surface recombination current density J_0 down to less than 10fA/cm^2. Repeating treatment can further improve the cleaning quality by 15-20% each time.
2) in combination with ALD aluminum oxide, a passivation stack providing high passivation quality for both *n*-type and *p*-type silicon. The thicker oxide layer made by UV-ozone treatment can reduce J_0 up to 25% and nearly double the effective lifetime.
3) an MIS contact structure with low contact resistivity on both *n*-type and *p*-type silicon. The *p*-type samples get a generally better result for contact resistivity as low as 0.6mΩ.cm^2 while *n*-type samples get the lowest contact resistivity of 16.9mΩ.cm^2. The contact on AlO_x also shows good conductance after the annealing process.

Combining experimental results in the processes mentioned above, Quokka simulation predicted promising high cell efficiency and indicated reducing contact resistivity is a key factor for reaching higher efficiency.

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