Chemical Vapor Deposition Growth of Transition Metal Dichalcogenides and Their Heterostructure Integration

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CHEMICAL VAPOR DEPOSITION GROWTH OF TRANSITION METAL DICHALCOGENIDES AND THEIR HETEROSTRUCTURE INTEGRATION

by

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ABSTRACT

Two-dimensional transition metal dichalcogenides (TMDs) are of great interest for the discovery of many novel physics owing to their extraordinary electrical, optical, mechanical properties as well as many promising applications including heterojunctions. To realize the overreaching goals of these materials, it is important to develop scalable growth techniques and investigate the role of different growth parameters on the resulting material properties. In this dissertation, I study, (i) controllable and reproducible growth of monolayer molybdenum disulfide (MoS₂) via chemical vapor deposition (CVD), (ii) the role of growth temperature on the properties of large area MoS₂ thin films grown via thermal vapor sulfurization route, and (iii) low temperature growth of palladium diselenide (PdSe₂) thin films, their doping and integration into heterojunctions. In particular, for the growth of MoS₂ monolayer crystals, I modified the CVD process by using molybdenum trioxide thin films as a precursor addressing the difficulty of controlling the local variations of the precursor concentrations in the conventional method resulting in highly reproducible MoS₂ crystal growth. For large area MoS₂ thin films, I show that the electrical properties of the samples change significantly with growth temperature and discuss the challenges in using Si/SiO₂ substrates for the direct growth of these films, specially at high temperature. For PdSe₂ thin films, I studied the changes in electrical, chemical, and crystalline quality of the PdSe₂ films grown under low pressure CVD conditions below 400 °C and showed its integration with molybdenum diselenide to fabricate a vertical heterojunction diode with a high rectification ratio. I have also investigated the surface charge transfer doping of PdSe₂ devices and used it toward fabrication of lateral heterojunction diode by selective area doping. The TMD
synthesis, doping, and heterojunction integrations shown in this study is a significant step forward for the scalable fabrication of photodetectors, sensors, logic circuits, and other high-performance electronic devices.
To my family
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CHAPTER 1: INTRODUCTION

1.1 Motivation

Transition metal dichalcogenides (TMDs) is a new class of 2D materials which has a wide range of applications owing to their unique optical, electrical, and mechanical properties.[1-6] The most fascinating fact about the TMDs is that many of them compose intrinsic bandgaps unlike zero bandgap graphene which attracted interest in semiconductor electronic applications such as field effect transistors (FETs)[7,8] and memory devices.[9-12] TMDs consist of a layered structure with the monolayers only 3-atom thick. Weak inter-layer Van der Waal bonds allow exfoliating down to a monolayer via simple micromechanical exfoliation and numerous exciting device prototypes have demonstrated in recent years including sensors[9], photodetectors[13], and logic devices[9]. Molybdenum disulfide (MoS$_2$), the most studied material among all TMDs has a direct band gap of 1.8 eV in monolayer[4] with theoretically predicted room temperature mobility of 410 cm$^2$/Vs [14] and on/off ratio of $10^8$[7] showing a great potential to be influential in next-generation electronics. In recent years, substantial amount of research is devoted on developing controllable and reproducible synthesis methods for batch production of MoS$_2$ and other TMDs which would enable their integration into modern semiconductor industry.[15,16]

Over the years since the discovery of graphene, the family of 2D materials is continuously growing; there are closer to 6000 layered materials[17] that can be exfoliated down to a monolayer. In semiconductor electronics, applicability of a 2D material for a specific device depends on whether the bandgap of the material falls into a desired range. Graphene has a zero bandgap; hence its optoelectronic applications fall into far IR wavelengths while most applications of TMDs are in small range of NIR or visible wavelengths.[18] To bridge the gap between these materials,
narrow band gap semiconductors such as black phosphorus (BP) have attracted significant interest in recent years[18,19] since the NIR, mid-IR detection is very important in thermal imaging for medical and military applications. The problem with BP however is that it is very unstable in air, so the devices need additional layer of protective coating which may cause difficulties in practical device integrations. Very recently, noble metal dichalcogenides such as PtSe2, PtS2, and PdSe2 attracted attention with their narrow and variable layer dependent band gaps similar to BP and high air stability.

Figure 1: Comparison of bandgaps of 2D semiconductors and their applications. Figure is reprinted with the permission form reference [18]
High quality, wafer-scale synthesis beyond low yield mechanical exfoliation is an essential step toward realizing industrial applications of these materials.[15,16] Chemical vapor deposition (CVD) is undoubtedly the most promising method for such synthesis, commercialization of graphene became a reality with the development of such CVD methods. CVD is achieving milestones in TMD material growth, defect engineering, heterostructures, and device applications as shown in Figure 2.[20] TMD crystal growth via co-evaporation CVD route is studied extensively due to its ability to produce highly crystalline materials with large lateral dimensions.[21-24] Achieving a good control in partial pressure of vapor phase precursors is the key for successful growth, deposition of intermediate oxide or oxysulfide/selenide species is reported under less ideal conditions. Therefore, comprehensive understanding in growth mechanism and alternate methods to achieve precursor vapor control is desirable for high quality material growth via this route. Large area synthesis of TMDs have also realized via annealing of metal thin films in chalcogen vapor which enable easy, wafer scale synthesis with good film thickness control.[25-27] However, large variation in film properties is observed among the reported literature [25,26,28-32] encouraging a closer investigation on the effect of growth conditions on the film properties.
In addition to the inherent band gaps of the materials, band-structure engineering plays an important role in modern semiconductor applications. New materials design such as Heterostructures/superlattices are important for this aspect since stacking of different bandgap materials allow tuning of the band structure at the interfaces by design for prospective applications.[33-36] Semiconductor heterojunction grown in conventional method require pristine interface between two dissimilar semiconductors which require high precision growth techniques such as molecular beam epitaxy [37] and the material choice is greatly limited due to mismatches in their thermal expansion coefficients, lattice parameters, and crystal structures.[38] In contrast, 2D layered materials allow heterostructure integration with atomic precision owing to weak
interlayer bonds. Wide variety of 2D materials with different band gaps and work functions can be stacked simply as Lego blocks (Figure 3)[33] to study exciting physics emerging at the interfaces and could lead to new technologies in next generation electronics.

Figure 3: The atomic layers of 2D materials are analogous to Lego blocks since they are weakly bonded by Van der Waals interactions. One can construct multiple different heterostructures by simply stacking alternate layers of 2D materials without the lattice mismatch issues in the conventional semiconductor heterojunction fabrication. Reprinted with the permission form reference [33]

Doping is another popular method for electrical property tailoring of semiconductors.[39] Selective area doping allows making local changes of the materials electronic configuration which enable fabrication of devices such as p-n junctions and transistors in the same wafer.[40,41] Beyond conventional substitutional doping which implant foreign atoms in host semiconductor lattice to change its carrier concentration, the ultra-thin nature of 2D semiconductors allow successful doping via electrostatic[42] or surface transfer[43,44] methods. In recent years, surface transfer doping has attracted significant interest owing to its easy implementation to effectively modulate carrier concentration in 2D semiconductors without introducing defects to the materials
lattice.[44] Application of this method toward scalable device applications is however rarely shown, especially in novel members in TMD family such as PdSe$_2$.

1.2 Thesis Organization

In chapter 2: background, I discuss the structure, properties, and applications of the 2D TMDs studied in this dissertation: MoS$_2$ and PdSe$_2$. I also discuss the concept of CVD and main parameters drive the growth kinetics in CVD growth, the mechanisms of MoS$_2$ crystal growth via co-evaporation-based CVD, and edge terminations of MoS$_2$ crystal domains grown with the CVD methods. Other topics including doping of TMDs, 2D heterostructures are also discussed in this chapter.

Chapter 3 presents the experimental methods. The chapter starts by introducing the CVD setup used for all 2D material growths followed by the device fabrication and the characterization techniques used in this study. In characterization methods, I provide a detail discussion on the operating principles of characterization techniques used for topography and composition analysis of the TMDs in this study including AFM, Raman and PL spectroscopy, SEM, and XPS. Also, the techniques used for electrical characterizations are discussed including 2-probe transport measurements and KPFM.

Chapter 4 presents the controllable, reproducible CVD method to grow large MoS$_2$ crystals on amorphous Si/SiO$_2$ substrates by using MoO$_3$ thin film as a precursor. This chapter contain a comprehensive discussion on the vapor phase control achieved by the new precursor design contrasting to the conventional methods, the growth mechanism, and effect of CVD parameters
including the temperature and precursor film thickness along with a study of crystalline, electrical, and optical quality of as-grown MoS$_2$ crystals.

In chapter 5, I present the effect of CVD growth temperature in the electrical properties of large area MoS$_2$ films grown via thermal vapor sulfurization. I found that the device resistance continuously increased with increasing growth temperature for the MoS$_2$ films grown on Si/SiO$_2$ substrates despite of their improved structural quality indicated in Raman characterizations. A SiO$_2$ surface layer formation and its increased thickness at high temperature was shown via XPS measurements which played the major role in observed resistance variation.

The low-pressure CVD growth of large area PdSe$_2$ films is comprehensively studied in chapter 6. The thickness, composition, crystallinity, and electrical property variations of the PdSe$_2$ films grown in 250 °C – 375 °C were analyzed and discussed. Direct, contamination free vertical Van der Waal heterostructure assembly of PdSe$_2$ with pre-grown MoSe$_2$ which showed good current rectifying characteristics is also presented in this chapter.

In Chapter 7, electrical property modulation of PdSe$_2$ films via surface charge transfer doping by benzyl viologen (BV) molecules is presented. The doping mechanism, changes in carrier concentration, and work function modulation were studied and applied toward fabrication of lateral heterojunction diode.

Chapter 8 conclude the dissertation and suggest directions for future research.

1.3 References


CHAPTER 2: BACKGROUND

2.1 MoS$_2$

2.1.1 Crystal structure

MoS$_2$ is a hexagonal crystal similar to graphene. Monolayer MoS$_2$ consists of a molybdenum (Mo) atomic layer sandwiched between two atomic layers of sulfur (S). The top and side views monolayer MoS$_2$ lattice are shown in Figure 4 (a) and (b), respectively. Each Mo atom coordinate with six S atoms via covalent bonds with bond length ~ 2.4 Å and bond angle of ~ 80.8°.[1] These monolayers are held together by weak Van der Waal bonds with inter-layer separation of 6.5 Å[3] to form the layered structure of MoS$_2$. The arrangement of the six S atoms with respect to the associated Mo atom defines two main phases of MoS$_2$, the trigonal prismatic (2H) and octahedral (1T) as shown in Figure 4 (c). 2H phase is thermodynamically stable and
semiconducting while the metallic 1T phase is metastable with higher formation energy; therefore, show high electrochemical activity.[4]

2.1.2 Optical and electrical properties

Semiconducting 2H-MoS$_2$ (MoS$_2$ hereafter) consists of a unique band structure which varies with layer number up to few layers and with direct band gap in monolayer. Figure 5 summarizes the calculated electronic band structure of MoS$_2$.[5] Bulk MoS$_2$ has an indirect bandgap of $\sim 1.29$ eV where the valence band maximum and conduction band minimum located at $\Gamma$ point and at a point on $\Gamma$- $K$ line, respectively.[6] As the layer number decreases, the indirect bandgap increases while the direct excitonic path exists at the K point remain unchanged. In the monolayer, the material become a direct bandgap semiconductor with the band gap of 1.87 eV as the energy of the indirect transitions become higher than the direct transitions.

![Figure 5: (a) An optical image of an exfoliated few-layer MoS$_2$ flake. (b) Calculated band structures of bulk (left-most) to monolayer (right-most) MoS$_2$. Smallest energy transitions are indicated by arrows. In monolayer, direct transitions occur at the K point giving rise to photoluminescence. Figures are reprinted with the permission from reference [5]](image-url)
Owing to the direct band gap, monolayer MoS\textsubscript{2} showed more than 1000 times increase in photo luminescence quantum efficiency compared to the bulk material.[7] With gate electrode engineering, monolayer MoS\textsubscript{2} transistors showed room temperature mobilities up to 200 cm\textsuperscript{2}V\textsuperscript{-1}s\textsuperscript{-1} with on/off ratio of $10^8$, and ultralow power dissipation.[3] In addition to the intrinsic bandgap, MoS\textsubscript{2} bandgap can also be modulated by applied strain, external electrical fields, and doping. Hui et al.[8] showed that ~300 meV blue shift in the bandgap of few-layer MoS\textsubscript{2} can be obtained for each 1\% increase in strain. Continuous decrease of MoS\textsubscript{2} bandgap with the applied electric field perpendicular to the layers was shown by Ramasubramaniam et al.[9] Over 10 \% modulation in the band gap is reported with the selenium (Se) doping of MoS\textsubscript{2} monolayers.[10]

### 2.1.3 Mechanical properties

Ultrathin MoS\textsubscript{2} layers have shown high stiffness compared to steel. The breaking strength of the monolayer MoS\textsubscript{2} is superior to commonly used flexible substrates such as polydimethylsiloxane (PDMS) and polyimide (PI) which make them promising candidates for flexible electronics applications.[11] It was also shown that, the electrical quality of the MoS\textsubscript{2} FET devices remain unchanged under a bent of 0.75 mm radius of curvature.[12]

### 2.2 PdSe\textsubscript{2}

PdSe\textsubscript{2} is a recently discovered member of the TMD family with a layer tunable narrow bandgap of 0 (bulk) to 1.3 eV (monolayer). Unlike most TMDs, PdSe\textsubscript{2} has a puckered pentagonal structure as shown in Figure 6. The basic tetragonal backbone is formed with a Pd atom bonded to four Se atoms and neighboring Se atoms form covalent Se-Se bonds due to which pentagonal rings and the puckering of the layers originate. PdSe\textsubscript{2} is the first isolated 2D material with such structure.
with the vertical puckering distance of 1.6 Å.[13] PdSe$_2$ monolayer has a thickness of ~ 4 Å[14,15], the layers are held together by weak Van der Waal bonds in few-layer PdSe$_2$.

![Figure 6](image_url)

Figure 6: (a) crystallographic structure of pentagonal puckered PdSe$_2$ monolayer. (b) top and side view of the monolayer lattice. (c) atomic structure of few layer PdSe$_2$ revealed by STEM. Figures are reprinted with the permission from reference [13]

The electronic band structures obtained from the first principle calculations for bulk and monolayer PdSe$_2$ are shown in Figure 7 (a) and (b). Bulk PdSe$_2$ shows no band gap while monolayer PdSe$_2$ shows an indirect bandgap of 1.3 eV with the valence band maximum (VBM) and conduction band minimum (CBM) located close to X and M points, respectively. Both Pd 4d and Se 4p electronic levels make strong contribution to the band structure (VBM and CBM edges) of PdSe$_2$; therefore, the electronic structure is very sensitive to the interlayer coupling.[13,16] Compared to other TMDs like MoS$_2$ where the bandgap reaches its bulk value within few layers, the bandgap of PdSe$_2$ shows a large tunability with the layer number. Figure 7 (c) and (d) show experimentally measured and theoretically calculated band gaps of PdSe$_2$ with number of layers. Interestingly, the experimental values obtained via optical absorption measurements showed much larger variation compared to the theoretically predicted bandgaps which could have originated from the high defect sensitivity of the material.
Figure 7: Theoretically calculated electronic band structures of (a) monolayer and (b) bulk PdSe$_2$. The lowest energy transitions are shown with dashed arrows. Bandgap variation with number of layers derived from (c) optical absorption spectra and (d) first principle calculations. Figure is reprinted with the permission from reference [13].

The narrow and widely tunable bandgap of PdSe$_2$ facilitates high performance optoelectronic devices such as photodetectors operating in the infrared region.[17-19] Recently, facile wafer scale growth of PdSe$_2$ was reported by Zeng et al.[14] by using pre-deposited Pd layers with excellent band-gap control enabling the mass production of PdSe$_2$ electronic devices. The heterojunction integration enabled by this synthesis is receiving much interest recently. PdSe$_2$/Si heterojunction device shown to function as a self-driven and broadband photodetector, with a high on/off ratio ($\sim 10^5$), specific detectivity ($\approx 10^{13}$ Jones), and responsivity up to 300.2 mA W$^{-1}$ which are higher than other 2D TMDs based devices.[20] In another recent application, as-assembled PdSe$_2$/perovskite Schottky junction shown sensitive to light illumination ranging from 200 to 1550
nm with a high responsivity of 313 mA W\(^{-1}\) and a rapid response speed of 3.5/4 \(\mu\)s.[19] Similar heterojunction with PdSe\(_2\) multilayer on germanium nanocones showed superior responsivity of 530.2 mA W\(^{-1}\) and external quantum efficiency of 42.4\%.[17]

### 2.3 Chemical Vapor Deposition

Thin film coating on a substrate is often carried out by placing the substrate in a vapor of the material need to be coated which is called vapor deposition. Depending on whether the vapor of the coating material is obtained by physical evaporation of the material or through a chemical reaction, the deposition method is called physical vapor deposition (PVD) or chemical vapor deposition (CVD). In CVD, the volatile species of the chemical components (precursors) of the coating material is brought together to react at desired temperature and pressure conditions. A carrier gas (e.g. Argon, hydrogen) is used to dilute the precursors and to bring the vapors to the desired reaction zone. Through a series of chemical reactions occur in the gas and/or at the substrate surface results in thin film coating of the substrate. Figure 8 shows a schematic representation of the main reactions involved in the CVD thin film coating.[21] As shown in the figure, a boundary layer is formed due to the unique fluid dynamics closer to the substrate surface which is different from the main gas stream. Therefore, controlling the chemistry in this boundary layer is the main factor regarding successful thin film deposition via CVD.
In the next section, the main factors that drive the CVD growth kinetics are briefly discussed.

2.3.1 Temperature and Reaction Rate

The rate of a chemical reaction exponentially increases with the temperature according to the Arrhenius equation:

\[ k = A e^{-\frac{E_a}{RT}} \]  \hspace{1cm} (1)

where,

\( k \) = Rate constant of the reaction

\( A \) = Arrhenius Constant

\( E_a \) = Activation Energy for the reaction (in Joules mol\(^{-1}\))

\( R \) = Universal Gas Constant

\( T \) = Temperature in absolute scale (in kelvins)
2.3.2 Vapor pressure and volatility

Since CVD is driven by a series of complex chemical reaction which may produce more reactive species at intermediate steps, the volatility of these species is another factor to be carefully considered when choosing the precursors. The volatility of a species depends on its vapor pressure (P) which is related to the temperature (T) in following manner.

\[ P \propto e^{-\frac{\Delta H_{\text{evp}}}{RT}} \]  \hspace{1cm} (2)

Where \( \Delta H_{\text{evp}} \) is the Enthalpy of vaporization (characteristic to the material) and R is the gas constant (8.3145 J mol\(^{-1}\) K\(^{-1}\))

2.3.3 Diffusion

Diffusion is the process that gas molecules move from higher to lower concentration regions. The rate of diffusion (R) is defined as,

\[ R = \frac{\text{volume of diffusion}}{\text{time of diffusion}} \]  \hspace{1cm} (3)

\[ R = \frac{\text{cross section area} \cdot \text{distance of diffusion}}{\text{time of diffusion}} \]  \hspace{1cm} (4)

The main factors affect R are temperature (T), viscosity of the medium (n), and the molecular mass of the particles (M). R, T, and n are related to each other in the following form[22],

\[ R = \frac{3nK_d}{8T} \]  \hspace{1cm} (5)

Where \( K_d \) is the diffusion rate constant

At same temperature and pressure conditions, R is inversely proportional to the square root of M which is known as the Graham's law of diffusion.[22]
Under the given temperature conditions in CVD where activation energy barrier is overcome with the thermal energy, the rates of reactions are mostly diffusion controlled.

**2.4 MoS₂ crystal growth mechanism via CVD**

CVD growth of MoS₂ crystals by using molybdenum trioxide (MoO₃) and S as precursors is a two-step process.[23]

\[
MoO_3 + \frac{x}{2} S \rightarrow MoO_{3-x} + \frac{x}{2} SO_2 \tag{7}
\]

\[
MoO_{3-x} + \frac{7-x}{2} S \rightarrow MoS_2 + \frac{3-x}{2} SO_2 \tag{8}
\]

First, the MoO₃ reduces to volatile MoO₃-x species at low S vapor concentration.[24-27] This reaction occurs at the early stages of growth where small amount of S vapor enters the reaction zone with its sublimation at low temperatures. As temperature increases, melting of S occurs creating sufficient S environment to reduce the MoO₃-x to MoS₂.[24,26] Figure 9 (a) show the Mo-O-S phase diagram for possible reaction pathways of growing MoS₂ from MoO₃ and S precursors. According to the phase diagram, sub-oxide or oxysulfide (MoO₃-x, MoO₂-xSₓ) nanoparticle formation is resulted in a sulfur poor conditions preventing MoS₂ formation. At high S concentration, rapid sulfurization of MoO₃-x species can occur which could create MoO₃-x nanoparticles coated in MoS₂[28] or MoS₂ fullerene.[29] Therefore, successful deposition of MoS₂ on a substrate highly depend on the S vapor concentration with respect to Mo vapor.
Figure 9: (a) Mo–O–S ternary phase diagram showing the possible reaction pathways for MoS₂ growth in CVD with MoO₃ and S precursors. Figure reprinted with the permission from reference [26]. (b) Flow chart of MoO₃ and chalcogen reaction pathways with respect to the chalcogen concentration. Figure reprinted with the permission from reference [29].

Growth dynamics of MoS₂ in CVD is not fully understood yet since it is a combination of many factors including precursor partial pressures, reaction rates, growth geometry and substrate type. However, two possible mechanisms are elucidated based on the experimental observations throughout multiple studies in the literature as shown in Figure 10. Mechanism I is a complete gas phase reaction where both steps of the reaction between MoO₃ and S only occur in the vapor phase, and MoS₂ deposits directly onto the substrate. In Mechanism II, MoO₃−ₓ species diffuse and condense onto the growth substrate, reacting with S and forming MoS₂.[20,30] Some reports discussed the growth as a combination of these two mechanisms where most MoS₂ is created in the vapor phase (mechanism I) and some MoO₂−ₓSₓ nanoparticles adsorbed on the substrate surface (mechanism II) act as heterogeneous nucleation sites to support MoS₂ adsorption on the substrate surface.[29]
Figure 10: Possible pathways of MoS$_2$ growth during co evaporation of MoO$_3$ and S precursors. The complete vapor phase reaction pathway is shown as I and the vapor-solid reaction pathway is shown as II. Figure reprinted with the permission from reference [26]

2.5 Edge terminations of MoS$_2$ crystal domains

In CVD grown MoS$_2$ crystals, different shapes are observed based on the growth rate of different crystal faces[31,32]. Wang et al.[31] associated this shape evolution to the changes in Mo:S ratio. According to their hypothesis, the slow growing face which associate with low edge free energy dominate the final shape of the crystal since the fast-growing faces become small or disappear. Mo zigzag (Mo-zz) and S zigzag (S-zz) are the commonly observed edge terminations in MoS$_2$ crystals. Figure 11 show the shape and edge terminations of the crystals starting from a hexagonal nucleus under different Mo:S ratios. When this ratio is $>1:2$ ($<1:2$) which is a Mo (S) rich condition, S-zz (Mo-zz) terminations grow faster than Mo-zz (S-zz) because existence of free S (Mo) in a Mo (S) rich environment is highly unstable. Therefore, the final shape of the crystal become triangular with three Mo-zz (S-zz) terminated edges. Under the exact stoichiometric ratio of Mo and S, the initial shape of the nucleation which is hexagonal will remain intact due to the equal growth rates of Mo-zz and S-zz terminations. In TEM studies, Zande et al.[32] showed a clear contrast between Mo-zz terminated and S-zz terminated edges of triangular MoS$_2$ crystals as
shown in Figure 12. The Mo-zz crystals (Figure 12 (a)) have sharper edges while the S-zz (Figure 12 (b)) consists of curved edges. This morphological difference can be used as a facile optical identification of two types of crystals and therefore relates to the Mo:S ratio in the growth environment.[31]

Figure 11: A schematic illustration showing the relationship between Mo:S atomic ratio and the shape of the grown MoS$_2$ crystals. Figure reprinted with the permission from reference [31]

Figure 12: Bright field TEM images of MoS$_2$ crystals with (a) Mo-zz terminated, and (b) S-zz terminated edges. Figure reprinted with the permission from reference [32]
2.6 Doping of TMDs

Doping engineering of semiconductors play an important role in controllable tuning of their electrical properties for desired applications. This section summarizes different doping methods utilized for the doping of 2D materials.

2.6.1 Substitutional Doping

In silicon (Si) based electronics, substitutional doping is a popular technique where acceptor or donor atoms are incorporated to the Si lattice to increase carrier concentration.[33] Analog to that, substitutional doping is used in 2D materials for both n- and p-type doping. Suh et al. [34] showed stable p-doping of MoS$_2$ by niobium (Nb) substitution and achieved degenerate hole concentration of $3 \times 10^{19}$ cm$^{-3}$. In another study, high energy (10 keV) ion implantation of phosphorus (P) dopants in to MoS$_2$ flakes was shown by Xu et al.[35] achieving p-doping. They used a PMMA protective layer to slow down the dopant atoms but still significant kinetic damage to thin MoS$_2$ flakes occurred as high energy atoms knocked off S atoms creating more S vacancies in the lattice in addition to the P implantation. In-situ Nb doping of CVD grown WS$_2$ and MoS$_2$ was shown by Gao et al.[36] Non-degenerate doping was achieved, but controlling the doping level and impurity concentration was difficult with this method. Near-degenerate n-doping of MoS$_2$ was achieved by incorporation of ReO$_2$ in the CVD co-evaporation process with ~ 1% Re substitution to the lattice.[37] Following the doping, 400% quenching of the PL signal was observed. Similar PL quenching was reported in a study performed by Zhang et al. [38] using Mn as an n-dopant for monolayer MoS$_2$ due to the foreign atom incorporation in to the lattice and the strain caused by the dopants which shows the detrimental effects of substitutional doping in optoelectronic properties of 2D materials.
2.6.2 Electrostatic Doping

Since 2D materials are more sensitive for external fields due to their ultra-thin nature, electrostatic doping is gained interest in 2D material doping.[39] Electrostatic doping utilizes induction of charge carriers in the metal-oxide-semiconductor (MOS) system. The gate metal and the semiconductor channel are separated by a dielectric; when a voltage is applied to the gate, charges are induced in the semiconductor channel modulating its carrier concentration. The electrostatic doping is implemented in many diode applications by fabricating two separate gates to the same semiconductor channel so the carrier concentrations in these two regions can be independently controlled to create a virtual junction.[40] An MoS$_2$ p-n junction with good rectification and photovoltaic effect was shown by Sutar et al. [41] by configuring two buried bottom gates to the MoS$_2$ channel. The concept of electrostatic doping is applied toward advanced device architectures in 2D materials such as memory device by using floating gate configurations.[42,43] In this device configuration, when large electrical bias is applied through the control gate, the electrons tunnel through the dielectric separating the control gate and floating gate and trap in the floating gate. Then the carrier concentration of the TMD channel is modulated and maintained due to the capacitive configuration between the floating gate and the channel material.[42] Electrostatic doping of MoTe$_2$ by ionic liquid gating was shown by Wang et al. [44] and Zakhidov et al. [45] and achieved phase transitions in the material.

2.6.3 Surface charge transfer doping

In charge transfer doping, physical or chemical interaction between the dopant atoms adsorbed at the host surface allow exchange of charge carriers with the host material. Charge transfer direction is determined by the Fermi level difference of the two materials.[46] This surface
transfer doping model was initially put forward to explain the intriguingly high surface conductivity of intrinsic diamond, which in principle should be a bona fide insulator.[47] Surface transfer doping is recently developed as an effective way to dope 2D semiconductors and other nanomaterials since with a suitable surface dopant, it can easily implement on any material surface in a reversible way without making permanent damage to the materials lattice. Figure 13 show a summary of n and p type dopant that are successfully employed in charge transfer doping of typical TMDs.[46]

Figure 13: A summary of n and p type surface charge transfer dopants used for STCD of TMDs. Figure reprinted with the permission from reference[46]

As one can observe from the figure, there are different types of surface dopants available for TMDs including gasses, metallic nanoparticles (Pt, Au, etc.), metal oxides (WO₃, MoO₃, etc.), and organic molecules (F4-TCNQ, BV). Dopants with high work function or high electronegativity are used as acceptors for p-doping while low work function/electronegative dopants are used as donors. Molecules such as BV works as n-dopants since their low ionization potential allow them to donate charges to the host material easily. The dopants can be incorporated.
on the semiconductor surface by vapor deposition methods, spin coating or drop casting which is very convenient and low cost for mass production unlike any other doping method.

2.7 2D Heterojunctions

The interface between two semiconductors with different band gaps is called a heterojunction. In 2000, the Noble prize was awarded to Dr. Herbert Kroemer “for developing semiconductor heterostructures used in high-speed- and opto-electronics”[48] showing the high importance and impact of the semiconductor heterojunction research in the field. Heterojunctions are important in modifying the electronic band alignment and have utilized toward many device applications such as lasers[49,50], tunneling transistors[51-54], negative differential resistance (NDR) devices[55,56], etc. Based on the band alignment of the two materials at the interface, the heterojunctions are divided into three main categories as shown in Figure 14. When the conduction band edge of one material is at a higher energy and the valence band edge is at a lower energy with respect to the other material, the interface is called a type I heterojunction. At a type II heterojunction, both band edges of one material are at lower energy than those of the other material. With the similar conditions and additionally if the conduction band edge of one material stays below the valence band edge of the other material, type III junction is formed.[57]
Figure 14: Conduction and valence band alignments of two materials forming heterointerfaces of type I, II, and III.

Heterojunction assembly of 2D semiconductors is a promising way to tailor the band structures and electrical properties for specific applications such as phototransistors[58], photoelectronic memory[59], and excitonic devices.[60] Lack of dangling bonds and weak interlayer bonding allow fabrication of vertical heterostructures by stacking of different 2D layers without any lattice mismatch issues. These heterostructures have shown exciting physics at the interface. For an example, efficient and ultrafast charge transfer down to femtosecond level was shown for many TMD heterointerfaces including WS$_2$/WSe$_2$ [61] and MoS$_2$/WSe$_2$.[62] Vertical tunneling transistor was realized by using an WS$_2$ layer as the atomically thin barrier between two graphene layers.[52]

Different from vertical stacking, the lateral heterojunctions are also attempted and shown superior device performance owing to the atomically precise stitching at the interface.[63] The WS$_2$/WSe$_2$ lateral heterojunction grown via in situ modulation of the vapor-phase reactants in CVD was shown application as a high voltage gain complementary inverter.[64] Doping or passivation is also used to create lateral heterojunctions. Choudhary et al.[65] showed gate tunable
rectification behavior at the pristine and oxygen plasma exposed MoS₂ interface with a rectification ratio up to $10^3$. Other methods such as dielectric and strain modulation are also used for the lateral heterojunction formation of 2D semiconductors.[66]

### 2.8 References


CHAPTER 3: EXPERIMENTAL METHODS

3.1 CVD setup

All the single crystal and polycrystalline thin film TMD materials were grown in a home-built CVD system composed with a single zone horizontal tube furnace which can reach the temperatures up to ~ 1200 °C, a carrier gas supply with precise flow rate control, two-way control for low pressure (LPCVD) or atmospheric pressure (APCVD) conditions configured by Kenneth Dumas in Khondaker Group. The main components of the CVD setup are shown in Figure 15. In a typical growth trial, the substrate and the transition metal/metal oxide compounds are loaded at the center of the furnace and the chalcogen (S, Se) powder is kept upstream at a low temperature region. The heating profile of the central zone is adjusted from the input parameters including temperature set point (C), ramp rate (C/min) and dwell time (min). The positioning of the chalcogen powder was determined based on its malting point, desired vapor introduction time and the temperature gradient of the furnace at the upstream region closer to the edge. APCVD conditions were used for the monolayer crystal growth while LPCVD conditions were used for thin film TMD growth via thermal conversion of transition metal films in chalcogen vapors.
Figure 15: A photograph of the CVD setup used for the growth of 2D materials used in this study. Acknowledgements goes to Kenneth Dumas who built this setup.

3.2 Device Fabrication

For the device fabrication, materials directly grown on Si/SiO₂ substrates were used. The fabrication steps are shown in Figure 16. First, a metal seed layer was deposited through a shadow mask with channel dimensions of 750 µm x 250 µm via e-beam evaporation (Figure 16 (a)) and subsequently selenized in the CVD chamber (Figure 16 (b)). For the vertical heterostructure integration, the second seed metal layer was deposited in a crossbar manner by aligning the same shadow mask perpendicular to the first channel and selenized under appropriate CVD conditions (Figure 16 (c)). For the devices with single 2D material channels, this step was skipped. By properly aligning another shadow mask designed for the metal contacts, 40 nm gold was deposited via e-beam deposition as source and drain electrodes. For the small devices shown in chapter 7,
similar shadow masking procedure was followed, and the devices were configured with channel dimensions of 100 µm x 30 µm.

Figure 16: Device fabrication steps. (a) an optical image of the first metal seed layer deposited with the shadow mask. (b) an optical image of the channels after CVD selenization step. (c) an image showing the crossbar alignment of the second TMD layer. (d) final device configuration after the deposition of contact electrodes.

3.3 Characterization Techniques

3.3.1 Topography and composition

3.3.1.1 Atomic force microscopy (AFM)

AFM is a powerful technique to acquire nanoscale topographical information. A schematic diagram of the AFM operating procedure is shown in Figure 17 (a). The AFM operating principle simply based on the forces between the atoms of a sharp AFM tip and the atoms of the scan sample surface. The tip is attached to a cantilever and depending on these forces, a deflection of the cantilever occurs. The photodetector captures the laser beam reflected off from the cantilever and generate an image which is related to the changes in the atomic forces caused by the topography of the sample. According to the Van der Waal force curve shown in Figure 17 (b), the force between the atoms in the AFM tip and surface of the scan sample can be either attractive or repulsive depending on the distance between them. Accordingly, AFM can operate in either contact, non-contact or intermittent contact (tapping) mode for desired applications. In contact mode, the AFM tip scans the sample in close contact and the deflection is kept constant through a
feedback loop. Contact mode is commonly used in force microscopy and conductive AFM. Non-contact mode is used when the sample surface can be altered upon the tip contact. In this mode, the tip is located around 5-15 nm above the sample surface where the atomic forces are attractive, but relatively weaker compared to the contact mode. Tapping mode is one of the key advances in the AFM and commonly used method for topographical scan of soft samples such as polymers and samples that are loosely held on substrates such as 2D materials. In tapping mode, a cantilever oscillating at its resonance frequency is brought close to the scan until it lightly taps the surface. The cantilever vertically vibrates at a high frequency where it intermittently contacts and lift off the surface and the amplitude are lost as the repulsive contact forces increase closer to the surface. This amplitude changes are then translated to a topographical image of the sample surface. Taping mode AFM is employed to evaluate the thickness of the grown TMD samples, the changes of the thin film topography after growth steps and to visualize the crystalline/polycrystalline nature of the samples in this study.

Figure 17: (a) The basic components and operating concept of AFM. (b) The Van der Waal force curve showing the nature of forces between AFM tip and the scan sample surface as a function of their separation distance
3.3.1.2 Raman Spectroscopy

Raman spectroscopy is a contactless, non-destructive characterization technique developed based on the concept of inelastic scattering from the molecules. Most photons are elastically scattered when they interact with a molecule, therefore have the same wavelength as the incident photon. This is called Rayleigh scattering. A small percentage of photons is scattered inelastically with different frequencies than the incident photon due to the interference of photon energy with the vibrational energy of the molecule, called Raman scattering. Figure 18 shows a schematic diagram of this scattering process that led to Raman spectroscopy. 2D materials compose some Raman active modes due to their lattice vibrations. Not only the frequency of the modes can be used as a material characterization technique, it also sensitive to the thickness, stress/strain, and doping level of the material hence a powerful tool to obtain such information in 2D materials.

![Schematic Diagram of Raman Scattering](image)

Figure 18: A schematic representation of different scattering processes occurs when a photon interacts with a vibrating molecule.

*Layer number evaluation with Raman spectroscopy*

Raman spectra of 2D materials is sensitive to layer number since the strength of Van der Waal forces and long-range coulombic forces change with the layer stacking. As the layer number increases, the atomic vibrations are suppressed due to the inter-layer Van der Waal forces; hence,
a blue shift in the Raman modes is expected.[1] While this is true for some modes (e.g. A\textsubscript{1g} mode in MoS\textsubscript{2}), opposite shifts are also observed in some Raman active modes. It was found that in such cases, the stacking induced structural changes and long-range coulomb forces dominate over the effect of Van der Waal forces. For an example, the E\textsubscript{2g} mode of MoS\textsubscript{2} that is caused by the in-plane vibrations of the S atoms in the lattice experience a red shift increasing layer number. Similar shift is seen in all the major Raman modes of PdSe\textsubscript{2}. The main differentiation here is whether the vibrational modes are in-plane or out-of-plane since the out-of-plane modes are affected more by the coulombic repulsion from the chalcogen atoms in adjacent layers. In the case of MoS\textsubscript{2}, where the two Raman peaks show opposite shifts with the layer number, the difference of the wavenumbers (\(\Delta\)) is used to characterize the thickness of the material up to 4-5 layers.[1,2]

Figure 19: Evolution of Raman spectra of MoS\textsubscript{2} with Layer number. (a) Raman single spectra taken at regions with different thicknesses of MoS\textsubscript{2} flake shown in the inset. (b), (c) Frequency maps of E\textsubscript{1g} and A\textsubscript{1g} peaks of the flake, respectively which showing the opposite shift of the peak frequencies. Figures are reprinted with the permission from reference [1]
Doping related changes in Raman spectra

Doping of a material can affect its Raman spectra due to following reasons.

changes to the bond length:

When bond length increases (e.g., Substitutional n-doping), the vibrations are weakened, red-shift in Raman modes is expected and vice versa.

Stress/strain in the lattice:

Raman modes red shift with tensile stress and blue shift with compressive stress which is a similar effect as the bond length changes.

Changes in electron-phonon interactions:

This is the more dominant effect in spectral changes in the case of electrostatic and charge transfer doping. With the free carrier accumulation, the strength of electron-phonon coupling increases resulting in phonon softening which can be seen as a red shift in the out of plane modes.[3-5] With combined theoretical and experimental investigations in multiple 2D TMDs including MoS$_2$, WS$_2$ and WSe$_2$, it was shown that the phonon softening occurs when multiple inequivalent valleys are populated simultaneously. Much larger energy separation between valleys in the valence band compared to the conduction band in these TMDs prevent the population of multiple valleys upon hole accumulation. Therefore, this effect is more prominent in electron doping than in hole doping.[5]
3.3.1.3 Photoluminescence (PL) spectroscopy

Figure 20: A schematic representation of the photoexcitation and emission process in a semiconductor that utilized in PL spectroscopy.

Photoluminescence spectroscopy is another non-destructive analytical technique useful in determining the electronic structure of a material. A schematic representation of the photoexcitation and emission process in a semiconductor is shown in Figure 20. When light is directed onto a sample, the electrons absorb the photon energy and move to excited states. When the excited electrons come down to their equilibrium states (relaxation), the energy is dissipated through the emission of light, called photoluminescence. This is a powerful technique to distinguish the monolayer TMDs since the direct bandgap give rise to strong PL intensity compared to multilayers.

The photoexcitation process in MoS$_2$ is as follows. With the absorption of energy from the incident photons, the electrons excite to the conduction band and positively charged holes are left in the valence band. Due to the strong Coulombic forces, the electrons and holes are bound together to form a neutral exciton.[6] MoS$_2$ PL spectra consist of two exciton peaks due to valence band splitting at the K point[7], A exciton peak at $\sim$ 1.87 eV and B exciton peak at $\sim$ 2.05 eV. The A
exciton peak with the largest intensity is resulted from the recombination of an electron at conduction band minimum with a hole at the valance band maximum and B peak is due to recombination of an electron with a hole at the lower branch of the VBM.[6]

The positively charged hole in the exciton can also be attracted by another electron via coulombic forces forming a trion (electron-hole-electron). Trion formation is energetically favorable in the presence of excess free charges.[8] Therefore, the A exciton peak of MoS$_2$ is further divided into two; the neutral exciton (X) peak at ~ 1.9 eV and trion peak (X$^-$) at ~ 1.85 eV.[8] The shift in A peak is related to relative contribution of X and X$^-$ intensities which can reveal important information on the doping level in the monolayer material.

3.3.1.4 Scanning Electron Microscopy (SEM)

Electron microscopies use the products of electro-matter interactions to investigate material properties such as topography, morphology, composition, and crystallinity. When an energetic electron beam is directed to sample, multiple transmission, emission and scattering phenomena could occur as shown in Figure 21 (a) depending on the energy of the incident electrons and the penetration depth.[9] SEM uses the secondary electrons generated upon the exposure to reveal topographical information of the sample. Some SEM setups also contain detectors that can detect the emitted characteristic x-rays which provide the information on materials composition (EDX). The main components of a SEM setup are shown in Figure 21 (b). An electron beam generated at the source is attracted and accelerated toward the positive anode. The condenser lens converges the electron beam and directed to the aperture where the beam size is controlled to an exact diameter. The beam is converged once again at the objective lens before hitting the scan sample. The scanning motion of the beam is controlled by the scan coils located between aperture
and objective lens. The lateral resolution in SEM is typically 2-5 nm and mainly depend on the working distance and the acceleration voltage (5-30 kV).

Figure 21: (a) The transmission, emission and scattering phenomena occur in a sample with upon electron beam exposure. Figure reprinted with the permission from reference[9] (b) Main components of a SEM setup.

3.3.1.5 X-ray photoelectron spectroscopy (XPS)

XPS which is also known as electron spectroscopy for chemical analysis (ESCA) uses the photoelectric effect to analyze chemical composition at a sample surface. When the material surface is irradiated by an X-ray beam, the electrons of the surface atoms absorb energy from the photons and emitted with some kinetic energy. In XPS, the photoelectron count is recorded in a range of kinetic energies of the emitted electrons. The peaks appear in the spectrum are related to the characteristic energies of the atoms’ core electronic levels in the material. These energies and their intensities allow identification of all the surface elements and quantification of their binding state. Figure 22 show a schematic representation of the photoemission process used in XPS.
Figure 22: A schematic diagram representing the operating principle of XPS.

From Einstein equation,

Photon energy = kinetic energy + binding energy of the photoelectron \[ (9) \]

In XPS instrumentation, a common Fermi level is established between the sample and spectrometer and the energies are measured with respect to the Fermi level.\[10\] Therefore, the equation takes the following form:

\[ E_k = h\nu - E_B - \phi_s \] \[ (10) \]

Where, \( E_k \) is the measured kinetic energy at the spectrometer,

\( h\nu \) is the photon energy (6.1486 eV for Al K\(\alpha\) radiation),

\( E_B \) is the binding energy, and

\( \phi_s \) is the spectrometer work function (constant)

Since the binding energy of an electron in a core level is influenced by the electron density of the material due to the Coulombic interactions, the shifts in core level binding energies can be used to analyze the doping level of the material. For an example, when a material accumulates free
electrons, the core energy levels shrink and shift toward the nucleus due to the influence of strengthened Coulombic repulsion between the electrons. This increases the measured binding energies, and blue shift the XPS spectra is observed as a result.

The atomic percentage of each element in the XPS spectra can be calculated by the following equation:

$$C_i = \frac{A_i}{\sum_{j=1}^{N} A_j}$$  \hspace{1cm} (11)

Where, $C_i$ is the atomic percentage of element $i$,

$A_i$ is the normalized area of the XPS peak for element $i$, and

$\sum_{j=1}^{N} A_j$ is the total normalized area of all peaks.

The normalized area is calculated by dividing peak area by the sensitivity factor. The atomic percentages quantify the bonding state of the atoms and often used to calculate the stoichiometry of the material.

3.3.2 Electrical Characterizations

3.3.2.1 Electrical transport measurements

To investigate the electrical properties of grown materials, 2-probe transport measurements were employed. The devices were configured in a bottom gate, top contact FET setup with heavily doped Si substrate as the gate material, SiO$_2$ (250 nm) as the gate dielectric, 2D semiconducting materials directly grown on SiO$_2$ as the channel material. Drain/source electrodes for the channel are defined by either e-beam lithography or direct deposition through shadow masks as shown in section 3.2. The choice of metal for the source and drain electrodes is done based on the work function compatibility with the channel material for effective charge injection. The gate and the
channel separated by the dielectric to form a capacitor which enables charge accumulation or depletion in the semiconducting channel based on the voltage applied to the gate. Under a positive gate bias, charge accumulation occurs in n-type channels while charge depletion occurs in p-type materials.

![Diagram](image.png)

**Figure 23**: A schematic representation of 2-probe electrical measurement setup.

Current-voltage characteristics ($I_D-V_{DS}$) measured with varying gate voltage is called output characteristics of the transistor (Figure 24 (a)) and the current-gate voltage curve is called the transfer characteristics (Figure 24 (b)). Following section briefly discuss the commonly used terms in FET characterizations.

**Field effect mobility**

The drift velocity of a charge carrier per unit electric field is defined as its mobility. When mobility is measured through field effect measurements is called field-effect mobility ($\mu_{FE}$). In the linear regime where the drain current ($I_D$) of the device is directly proportional to the gate voltage, $\mu_{FE}$ can be calculated using the equation:

$$\mu_{FE} = \left( \frac{L}{W C_G V_{DS}} \right) \left( \frac{d I_D}{d V_G} \right)$$

(12)
where \(L, W\) and \(C_G\) are the channel length, channel width, and the capacitance per unit area of gate dielectric, respectively.

*On-off ratio of the device \((I_{on}/I_{off})\)*

On- and off-currents can be extracted from output current at on and off states as shown in Figure 24 (b). State in the \(I_D-V_G\) curve. The ratio between these two is expressed as the on/off ratio of the device.

*Threshold voltage \((V_{th})\)*

The minimum gate voltage required to create a conduction path between source and drain electrodes is called Threshold voltage. This can be extracted from the \(x\)-intercept of the transfer curve.

*Subthreshold swing \((SS)\)*

The gate voltage needed to be applied to make a decade change in drain current is defined as the subthreshold swing of the device. This is calculated from the inverse slope of the transfer curve in the depletion region.
Figure 24: (a) Output and (b) transfer characteristics of a bottom gated MoS$_2$ FET. The linear region of the output curve is highlighted in orange. The on off regions of the transfer curve are shown in green and red, respectively. Figure is reprinted with the permission from reference [11].

3.3.2.2 Kelvin Probe Force Microscopy (KPFM)

KPFM is an AFM based technique to measure the work function of samples. A schematic diagram of a typical KPFM setup is shown in Figure 25 (a). When a conducting AFM tip is brought closer to a sample, a potential difference (CPD) occurs due to difference in work functions of the tip and the sample. If tip-sample distance is small enough, an electrical connection between the tip and the sample is established by a tunneling current as shown in Figure 25 (b). With this electrical connection, the Fermi levels will align, and the system reaches its equilibrium. Since the surfaces are charged, there is a force between the sample and the tip which will be nulled by providing an external bias with equal magnitude to the contact potential difference ($V_{CPD}$) but with opposite sign. $V_{CPD}$ is related to the work functions of the materials in the following manner.[12]

$$V_{CPD} = \frac{\Phi_{tip} - \Phi_{sample}}{e}$$  \hspace{1cm} (13)

Where, $V_{CPD}$ is the CPD in volts,

$\phi_{tip}$ is the work function of the tip,
\( \phi_{\text{sample}} \) is the work function of the sample, and 

\( e \) is the electronic charge.

To find \( \phi_{\text{tip}} \), a reference sample with known work function is used. Highly oriented pyrolytic graphite (HOPG) with the work function of 4.6 eV is often used for this purpose.

![Diagram of a typical KPFM setup and energy levels](image)

Figure 25: (a) Main components of a typical KPFM setup. (b) The energy level configuration of the sample and the tip when separated by a distance \( d \) with no electrical contact (left) and when tip and the sample are in electrical contact (right). Figure is reprinted with the permission from reference[12]

### 3.4 References


CHAPTER 4: MONOLAYER MoS$_2$ CRYSTAL GROWTH WITH MoO$_3$ THIN FILM PRECURSOR


4.1 Introduction

2D MoS$_2$ has been studied extensively in recent years owing to its extraordinary properties [1-5] and making expedited progress in its applications in the fields of electronics and optoelectronics with photodetectors[6], light emitting devices[7], solar cells[8], and bio sensors[9-11]. Most of these studies were performed in exfoliated samples, which limits their practical application due to the low yield, small lateral size, and uncontrolled layer number. For scalable device fabrication, large scale synthesis of MoS$_2$ is highly desirable.[12,13] Various CVD based bottom-up synthesis methods are employed for this aspect including thermal vapor sulfurization (TVS) of Mo/MoO$_3$ films[14-16], thermal decomposition of thiosalts in sulfur vapor[17], atomic layer diffusion[13,18], and co-evaporation of Mo and S precursors. The TVS method was first developed by Zhan et al. [14] to grow large area MoS$_2$ films by selenization of Mo films and many research have followed to improve the material quality of these films.[16] The main advantages of the TVS methods are that the process is highly scalable and the thickness control of the MoS$_2$ film can be easily achieved by controlling the initial thickness of Mo/MoO$_3$.[15,16] However, These films contain only nanocrystalline grains of MoS$_2$ with sizes ~ 10-30 nm [12], therefore showed poor electrical transport properties.[14,19] The thermolysis method proposed by Liu et al [20]
produced MoS$_2$ films with both polycrystalline and amorphous regions and additional high temperature annealing steps were needed to improve the film quality. Due to this, functional FETs were only obtained by transferring MoS$_2$ films grown on sapphire on to Si/SiO$_2$ substrates. Even though the ALD method utilized by Kalanyan et al.[13] was highly scalable, growing stoichiometric MoS$_2$ was difficult due to the intermediate oxysulfide layers.

The co-evaporation of Mo and S precursors has received much attention for the past few years due to its ability to produce high quality MoS$_2$ single crystals with excellent electrical and optical properties[21-24] in large scale. In the co-evaporation technique MoO$_3$ powder and S powder are commonly used to produce Mo and S vapor which then reacts to produce MoS$_2$ crystals. Since most of the growth-related reactions occur in the vapor phase, the uniform melting/sublimation of the precursors and maintaining uniform partial pressure of the gas phase precursors is highly desirable for clean and reproducible growth of MoS$_2$. However, such a control of precursor vapors turned out to be very challenging resulting in a growth of oxide/oxysulfide (MoO$_2$/MoOS$_2$) species along with MoS$_2$.[25,26] The importance of controlling S partial pressure in order to achieve monolayer MoS$_2$ growth is discussed in detail in many studies.[27,28] For an example, Najmei et al.[29] showed that in their experimental setup, when initial S loading is $< 0.5$ g only rectangle domains are grown which are oxysulfides. At 0.5-0.7 g loading of S, thick hexagonal MoS$_2$ domains were grown and triangular MoS$_2$ monolayers were grown at initial S loading greater than 1 g. S vapor control by adjusting carrier gas flow rate was discussed by Liu et al.[30] However, we find that the importance of controlling partial pressure of Mo vapor is rarely discussed in the literature. Having a uniform partial pressure of Mo in the reaction region when S enters the zone can help to maintain proper Mo:S ratio for the successful, uniform growth of MoS$_2$. 
However, when small amount of MoO$_3$ powder is used, due to the different particle sizes in the powder, MoO$_3$ cannot be uniformly distributed in the crucible which might hinder clean growth of MoS$_2$. As a result of these local variations in Mo:S ratio, crystals with different shapes and compositions are observed.[25,31]

In this chapter, I show that by replacing MoO$_3$ powder with a MoO$_3$ thin film for Mo precursors, clean and reproducible growth of monolayer MoS$_2$ can be obtained. MoO$_3$ thin film of 5 – 20 nm was thermally evaporated from MoO$_3$ powder which was then used as the Mo precursor for co-evaporation. Uniform evaporation rate of our thin film precursor facilitates better control of Mo vapor in the vapor phase resulting in clean triangular crystals of monolayer MoS$_2$ on amorphous Si/SiO$_2$ substrates as well as on sapphire substrates with high crystal quality and uniformity proved by scanning electron microscopy (SEM), Raman spectroscopy, photoluminescence (PL) spectroscopy, atomic force microscopy (AFM) and transmission electron microscopy (TEM). Electric characterization of these pristine crystals with bottom gated field effect transistors (FETs) showed n type transistor behavior with a good on/off ratio of $10^6$ under ambient conditions verifying the ability of these materials in modern semiconductor electronics.

4.2 Experimental Procedures

4.2.1 Growth process

Si substrates with 250 nm thick oxide layer were used as the growth substrates as well as the substrates to deposit the MoO$_3$ thin films which was used as precursor for co-evaporation. The substrate was cleaned via sonication in acetone for 5 min followed by sonication in IPA for 5 min, DI water rinse and 10 min mild oxygen plasma treatment. MoO$_3$ thin films with thickness 5-20 nm
were deposited using thermal evaporation of MoO$_3$ powder (99.5%, Sigma Aldrich) in a vacuum chamber at low evaporation rates of 0.2-0.5 A/s. The thickness of these thin films was confirmed via AFM. A schematic representation of the CVD setup with the precursor positioning is shown in Figure 26 (a). The thin film deposited substrates were cut into 1cm x 1cm size and placed in a ceramic boat, bare target substrates were placed on the same boat facing down with the separation (Figure 26 (b)) of 3-4 mm toward the source and placed at the center of the furnace. While the front end of the boat left open for S vapor to enter the reaction zone easily, the rear end was covered by the substrate to trap the vapor phase precursors near the substrate, but a small spacing (less than a mm) left at the end to ensure S vapor pressure does not overstep the balance between precursors. Ceramic crucible containing 600 mg of S powder (99.5%, Sigma Aldrich) was loaded in to a 1-inch quartz tube placed at the edge of the tube furnace (Barnstead International F79300 Tube Furnace) upstream. For different temperature setpoints, the MoO$_3$ and S precursor distance (r) is adjusted accordingly in such a way that S starts melting below 100 degrees from the setpoint value. Argon gas (99.995% purity) was used as the carrier gas. Temperature of the furnace was raised to the growth temperature of 750 - 850 °C at the rate of 20 C/min and hold for 10 min (dwell time). After the dwell time the furnace could cool down naturally until the temperature dropped to 500 °C at which point, the furnace hood was opened for rapid cooling. 200sccm Ar flow was passed initially before heating up the furnace for 10 min to saturate the environment with argon, after which the flow rate was kept constant at 10 sccm. For the parameters used in this process, we found that 10 sccm gas flow with 10 min dwell time is optimum for our growth. When temperature of the furnace dropped to 350 °C, it was purged with 200 sccm Ar again to flush off the excess reactants.
Figure 26: Experimental setup. (a) schematic representation of the atmospheric pressure CVD setup and the relative S, MoO$_3$ and substrate positioning. (b) Cross sectional view of the substrate boat: target substrate was placed face down toward the film at a small distance $d$. (c) The temperature profile of MoO$_3$ and S at setpoint value of 750 $^\circ$C.

4.2.2 Characterization of the materials

The surface imaging and the grain size measurements were carried out by Olympus BX51M microscope equipped with Jenoptic Progres Gryphax camera) and The SEM images were taken with a Zeiss ULTRA-55 FEG SEM. A tapping mode AFM (Veeco instruments, Dimension 3100) topography was used to determine the height of MoS$_2$ crystals. The samples were scanned at slow rates in small scan areas at the edge of MoS$_2$ crystal to achieve more accurate height profile.

Raman and PL spectroscopy measurements were carried out with confocal Raman microscope (Witec alpha 300 RA) at an excitation wavelength of 532 nm and with laser power of 0.293 mW at ambient conditions. For TEM characterizations, a droplet of buffered oxide etchant (BOE) was placed on the Si/SiO$_2$ substrate where MoS$_2$ crystals were grown. After a few minutes the oxide layer was etched, and the crystals were transferred to the liquid. The liquid was then picked up by
a clean syringe and released on a TEM grid with a carbon mesh. All TEM/STEM measurements were performed with a JEOL ARM200F FEG-TEM/STEM with a Cs-corrector.

4.2.3 Device fabrication and transport measurements:

The bottom gated FETs for the transport measurements were fabricated using standard electron beam lithography (EBL) using a Nabity Pattern Generator System connected to a Zeiss ultra 55 SEM for selected single crystals. Poly (methyl methacrylate) (PMMA) was spin coated on to the substrate containing MoS$_2$ samples and baked at 130 °C for 3 mins. The source and drain electrodes were then defined using EBL and developed in a solution of methyl isobutyl ketone and isopropyl alcohol. A 30 nm thick Ni film were deposited for the metal contacts using E-beam evaporation. The electron transport measurements of the final MoS$_2$ devices were carried out in a room temperature probe station using a Keysight Semiconductor Device Analyzer.
4.3 Results and Discussions

4.3.1 Growth Results

Figure 27: Growth Results. (a) Contrast between bare Si/SiO\(_2\) substrate and substrate after the growth of MoS\(_2\). (b) A sketch of the sample with the corresponding image positions. The blue regions marked here are outside of the boat. (c) The grain size histogram with the surface coverage. (d) the optical images of the source at the positions specified in (b). Scale bar is 100 \(\mu\)m in each image.

Figure 27 shows a representative result of our optimized CVD growth of MoS\(_2\). For this, we used 20 nm thin film of MoO\(_3\) as a precursor for Mo vapor. S was placed at the edge of the furnace, 23.5 cm upstream from the center of the furnace and the growth temperature was 750 °C. Figure 27 (a) show an optical image of the whole Si/SiO\(_2\) substrate after MoS\(_2\) growth as well as a
picture of bare substrate for comparison. The darker region of the growth substrate is where the crystals are grown. This region of the substrate is directly facing toward the thin film MoO$_3$ source. To show the growth on this substrate in detail, we divided this region into nine sections as shown in Figure 27 (b) and present optical micrographs of each of these region (labelled 1 - 9) in Figure 27 (d). Form here, we see that dense crystal grains of self-seeded MoS$_2$ are grown throughout the growth substrate without any traces of MoO$_2$/MoOS$_2$. This is in clear contrast to what we have observed when we used a small amount of (~1 mg) MoO$_3$ powder as a Mo precursor where we saw isolated regions of MoS$_2$ growth along with rhomboidal MoO$_2$/MoOS$_2$ on MoS$_2$ in other regions as seen in Figure 28. At spot 1, the Raman spectra is a combination of MoS$_2$/MoOS$_2$[25] and the reduced intensity of Si peak is an indication that these plates are very thick. Also, the high intensity of MoS$_2$ peaks implies that a thick layer of MoS$_2$ is grown on top of the oxysulfide plates. The spot 2 shows a $\Delta=18.92$ cm$^{-1}$ between $E_{2g}^1$ and $A_{1g}$ peaks which corresponds to monolayer MoS$_2$. Increasing amount of MoO$_3$ powder only increased the regions of MoO$_2$/MoOS$_2$. Since the difference between the two scenarios is the constant evaporation surface maintained by MoO$_3$ thin film which produced uniform vapor pressure in the growth region, we conclude that uniform evaporation of Mo has an important role in dense single crystal growth of MoS$_2$. We repeated the MoO$_3$ thin film growth over 50 times and we always obtained clean MoS$_2$ growth without any oxysulfides. This was not the case when we used MoO$_3$ powder, where clean and reproducible MoS$_2$ crystals were hard to achieve.
Figure 28: Growth results for co-evaporation of MoO$_3$ and S powders. (a) Optical micrographs for the crystals grown with 1mg of MoO$_3$ powder and 600mg of S with the same setup. (b) The Raman single spectra taken at spot 1 (blue) and spot 2 (red) shown in the inset of (a)

Another important observation is that all the single crystals grown are triangular shaped. Given the conditions of the growth and the rough edges of these triangular crystals (Figure 29 (b) which are S- zz terminations, we conclude that they are grown at a S sufficient environment.[32,33] Wang et al.[34] observed variations in the MoS$_2$ crystal shape from triangular to hexagonal geometries with respect to the distance from MoO$_3$ powdered precursor location. This variation in crystal shape was attributed to the variation of Mo vapor concentration along the growth substrate. In our growth, we observe same triangular crystal shape throughout the growth region which may related to the ability of maintaining uniform Mo concentration in the gas phase by replacing the powdered precursor by the thin film precursor. In some regions, the triangular domains are merged to form polycrystalline aggregates[35] can be seen due to the random orientations of the crystals and higher density.[35-37]

Figure 27 (d) also show a size and density variation of the MoS$_2$ grains in different regions. A statistical view to the grain size variation is provided in Figure 27 (c). We observed crystal sizes
up to 95 µm which is the largest we measured for this growth and most crystals favored to grow in 20-40 µm size that covered around 40% of the growth region. The variation in size can be explained due to a local variations of vapor phase precursors.[38] Slight variations of spatial distribution of Mo vapor can occur as a result of diffusion patterns within the gas. More importantly, variations in chalcogen vapor plays a major role here since the growth substrate is facedown and we closed the rear end of the boat with the substrate to trap the S to create S rich environment. S density is expected to be higher in regions 3, 6, 9 which also causes increased nucleation density resulting in merging of MoS₂ crystals.[38,39]

4.3.2 Topography, Composition and Crystallinity of the grown crystals

Figure 29: Characterization of the MoS₂ single crystals. (a) optical image of one of the largest monolayer crystals observed. (b) SEM image of a single crystal. (c) The AFM topography and height profile (inset) taken at an edge of a monolayer domain. (d) E₁₂g and A₁g vibrational modes of atoms and Raman single spectra for a single crystal.
Figure 29 (a) shows an optical micrograph of a single crystal grown with the size ~95 µm. These big crystals are mostly composed of monolayer regions along with some isolated dendritic bilayers[40-42] region which can be clearly seen in the SEM image as well (Figure 29 (b)). We only observe this bi-layer formation in large size crystals which could be due to the added nucleation sites by the defects in the first layer.[42] Self-seeded nucleation center with thicker layers is also visible in the SEM image. The tapping mode AFM image (Figure 29 (c)) taken at a single crystal edge was analyzed to identify the number of layers of the grown crystals. The step height at this edge was measured to be 0.78 nm which corresponds to the monolayer MoS$_2$ thickness and the topography of the crystal shows a highly uniform layer. Raman single spectra (Figure 29 (d)) was acquired to confirm the chemical composition of the material grown as well as the layer number. As shown in Figure 29 (d), Raman spectrum has the two prominent peaks, E$^{12g}$ and A$_{1g}$ which corresponds to in plane and out of plane vibrations of Mo and S atoms with respective wave numbers of 390.76 cm$^{-1}$ and 410.76 cm$^{-1}$. Spacing between these two peaks (Δ) is 19.82 cm$^{-1}$ consistent with monolayer MoS$_2$.[43,44]

Figure 30: PL characterization. (a) PL single spectra of a MoS$_2$ crystal grown with the optimized growth recipe. (b) PL intensity mapping of A peak for the same crystal. Inset shows mapping of B peak)
Figure 30 (a) show a PL spectrum from a representative single crystal with two signature peaks at 1.85 eV and 1.99 eV which corresponds to A (direct band gap excitations) and B (excitations resulted from valence band splitting due to strong spin-orbit coupling[45]) direct excitronic transitions.[43,46,47] The full width at half-maximum (FWHM) of the A peak is measured to be ~80 meV which is narrower than the exfoliated monolayer MoS$_2$ samples on Si/SiO$_2$ substrates[45,48] showing better optical quality of our samples. PL mapping was performed with the spectral center at 1.85 eV for the same crystal. The even color contrast of the maps near A and B (inset) excitation peaks shown in Figure 30 (b) confirms the uniform layer thickness of the crystal.

Figure 31: TEM characterization. (a) low magnification DF-STEM image of the transferred thin film on the copper grid. (b) HRSTEM image of the monolayer MoS$_2$ showing hexagonal atom arrangement. (c) DF-STEM image for the folded edge of the monolayer.

Scanning transmission electron microscopy (STEM) was employed to further varify the crystal quality of the MoS$_2$ crystals (acknowledgements to Dr. Hee-Suk Chung and Dr. Yeonwoong Jung for TEM data). As grown MoS$_2$ crystals were transferred to a TEM grid with a carbon mesh using buffered oxide etchant. Figure 31 shows dark-field STEM micrographs for the monolayer MoS$_2$ grown using the thin film based co-evaporation. High resolution STEM (HRSTEM) image (Figure 31 (b)) clearly shows the high crystalline quality of the of the monolayers with periodic
hexagonal atomic arrangement. The lattice constant is measured as 0.27 nm well agrees with previously reported results.[36,38] The monolayer can also be identified from the folding edge of the transferred film (Figure 31 (c)).

4.3.3 Effect of growth temperature and MoO$_3$ film thickness

We also experimented this growth at higher temperatures. Figure 32 shows the optical micrographs of the crystals grown at 750 °C, 800 °C and 850 °C by using 20 nm MoO$_3$ thin films. We observe triangular shaped crystals at all growth temperature suggesting that uniform Mo vapor pressure can be maintained at elevated temperature. We also found that the coverage density generally decreases at higher growth temperatures. This could be linked to the reduced nucleation at higher temperatures. The sticking coefficient which defines the nucleation ability of the surface significantly reduces due to the enhanced desorption rate at the higher temperatures[49]. This phenomenon also explains the multilayer growth at the nucleation center at higher temperatures. Since there are less nucleation sites to facilitate the gas phase MoS$_2$ to adsorbed on to the substrate surface which results in growth of multiple MoS$_2$ layers at the same nucleation site. The multilayer growth at high temperatures is discussed as an effect of high precursor supply in the previous reports[39,50,51] when MoO$_3$ powdered precursor is used which is not applicable for our thin film-based growth. In our experiments even at 750 °C, MoO$_3$ thin film precursor is completely evaporated and reacted to grow MoS$_2$, therefore more MoO$_3$ supply is not possible. The AFM, Raman and PL characterizations for the crystals grown at higher temperature are shown in Figure 33. The AFM topography shows a clear stepwise height variation and each step height measured is similar to monolayer MoS$_2$ thickness. Raman single spectra taken near the center of nucleation shows the E$_{1}^{1g}$ and A$_{1g}$ signature peaks for MoS$_2$ with the spacing of $\Delta = 23.43$ cm$^{-1}$ which
corresponds to a few layer MoS$_2$. [43,51] PL mapping of the crystals grown at 850 °C shows a clear PL intensity drop at these multilayers and very thick layers at the center shows no PL response.

Figure 32: Growth at different temperatures. (a) – (c) Optical images of growth at 850 °C, 800 °C, and 750 °C, respectively taken at 20x magnification. (d) – (f) corresponding images at 50x magnification.
Figure 33: Multilayer growth around the nucleation center at 850 °C. (a), (b) Optical images taken at 20x and 100x magnifications, respectively. (c) AFM topography and (d) height profile showing step-like height variation which corresponds to individual MoS$_2$ layers. (e) Raman spectra for the multilayers at the nucleation center. (f) PL mapping centered at 1.8 eV shows the PL intensity drop at the center due to the thick layers and uniform outer region consists of monolayer MoS$_2$.

The effect of MoO$_3$ precursor amount is tested by varying the thickness of the film from 5 nm to 20 nm with the same amount of S (Figure 34). All the crystals grown have the similar shape.
suggesting that the uniform Mo pressure control is possible even with 5 nm thin film. However, the crystal sizes are reduced at lower thickness of MoO₃ due to the low precursor supply.

Figure 34: Effect of MoO₃ film thickness. Optical micrographs of crystals grown with (a) 5 nm, (b) 10 nm, (c) 20 nm MoO₃ precursor thickness with 600 mg of S. Scale bar is 40 µm in each image.

4.3.4 Electrical characterizations of the monolayer MoS₂ crystals

(Acknowledgements to Hirokjyoti Kalita and Dr. Tania Roy for device fabrication and electrical characterizations)

We have measured electrical transport properties of MoS₂ samples in a bottom gated FET geometry. FET devices were fabricated on as grown MoS₂ single crystals by using standard electron beam lithography. The nucleation center was excluded at the device fabrication to minimize the reflection of multiple layers in the transport measurements. We used nickel for source and drain electrodes. Linear I_D-V_D confirm Ohmic contacts are formed at the two electrodes and all the measurements were performed under ambient for as grown samples. Figure 35 shows electrical characteristics of a sample device (optical image is shown in the inset of Figure 35 (b)). The field-effect mobility was extracted based on the slope dI_D / dV_G fitted to the linear region of the I_D-V_G using the equation \( \mu = \frac{(L/WC_GV_D)}{(dI_D/ dV_G)} \), where L, W and C_G are the channel length, channel width and the gate capacitance. For the sample device shown in the figure, 5
μm channel length and 6 μm and channel width is used in mobility calculations. This device shows an n-type conduction with on/off ratio of 10^6 and peak mobility ~4.5 cm^2/Vs which is comparable with the mobilities for pristine devices fabricated on CVD grown monolayers in previous reports.[35]

Figure 35: Electrical characteristics of as-grown MoS₂ single crystals. (a) Output characteristics of the transistor device by sweeping the gate voltage (V_G) from -10 V to 80 V. (b) Transfer characteristics. Plots are provided for the device shown in inset of (b)

### 4.3.5 MoS₂ crystal growth on sapphire substrates

The contents of this section have been published in: Withanage, S. S.; Khondaker, S. I., CVD Growth of Monolayer MoS₂ on Sapphire Substrates by using MoO₃ Thin Films as a Precursor for Co-Evaporation. MRS Advances 2019, 4 (10), 587-592. Reproduced with permission.

To investigate the versatility of our growth method, we conducted MoS₂ growth on sapphire substrates with similar CVD conditions. Sapphire has many advantages as a growth substrate for MoS₂ over Si/SiO₂ substrates including less strain due to smaller mismatch between thermal expansion coefficients[52] and less oxygen doping.[20] The SEM micrograph of the growth substrate shown in Figure 36 (a) shows very clean growth of MoS₂ crystals. Similar
triangular shape of the crystals throughout the substrate suggests the ability of maintaining uniform Mo vapor throughout the growth region with the MoO₃ thin film precursor since shape variation is attributed to Mo concentration gradient[34] as discussed before. Higher magnification image of a single crystal shown in Figure 36 (b) represents a highly uniform growth of MoS₂ with self-seeded nucleation. Compared to Si/SiO₂ substrates, we observe very high density of nucleation on sapphire substrate as exposed from Figure 36 (c). This also associated with the reduced grain sizes reported for the MoS₂ growth on sapphire.[21,36,53,54] Raman and PL spectroscopic analysis results for the MoS₂ crystals is shown in Figure 36 (d) and Figure 36 (e), respectively. Raman single spectra shows MoS₂ signature peaks of E₂g and A₁g which corresponds to in plane and out of plane vibrations of Mo and S atoms with respective wave numbers of 390.76 cm⁻¹ and 409.26 cm⁻¹ with Δ = 18.5 cm⁻¹ confirm monolayer nature of these MoS₂ crystals.[44,55] High PL response of the as grown crystals was observed with the signature A nad B peaks located at 1.85 eV and 1.99 eV, respectively. The narrower FWHM of A peak ~85 meV is an indication of greater optical quality of this CVD grown material.
Figure 36: (a) SEM image of the MoS$_2$ crystals grown on sapphire substrate. (b) Enlarged image of a single domain. (c) High magnification SEM image showing high nucleation density on the substrate. (d) Raman and (e) PL spectra for a MoS$_2$ crystal taken at the position specified by the red circle in the optical image shown in inset of (e)

4.4 Conclusion

In conclusion, a new CVD based method is introduced to synthesize monolayer MoS$_2$ crystals by using MoO$_3$ thin films as a precursor for co-evaporation. This new method facilitates uniform partial pressure of Mo vapor resulting in clean single crystal growth of MoS$_2$ throughout the substrate and is highly reproducible. As grown MoS$_2$ crystals show excellent PL response corresponding to high quality single crystal. TEM characterization further confirms crystalline quality of the sample. The effect of growth temperature and the MoO$_3$ precursor film thickness was also studied. Room temperature electrical transport measurements show a mobility of ~5
cm²/Vs with a current on/off ratio of 10⁶. The growth is tested on sapphire substrates as well. We believe this new CVD process can be used for the synthesis of other TMD materials and the growth can be extended to wide range of substrate types.

4.5 References


CHAPTER 5: EFFECT OF GROWTH TEMPERATURE ON THE ELECTRICAL PROPERTIES OF LARGE AREA CVD GROWN MoS$_2$ THIN FILMS AND EFFECT OF GROWTH SUBSTRATES

5.1 Introduction

Atomically thin 2D MoS$_2$ has attracted a great deal of attention for electronics and optoelectronics device applications owing to its exotic optical, electrical, and mechanical properties.[1-5] Recently, a substantial amount of research is devoted on CVD growth of large area MoS$_2$ and other TMDs which would enable their integration into modern semiconductor industry allowing batch production of these materials.[6,7] Sulfurization of Mo or molybdenum oxide (MoO$_3$, MoO$_2$) thin films, known as thermal vapor sulfurization (TVS), is widely used for direct, wafer scale MoS$_2$ growth on Si/SiO$_2$ substrates [8-15]; however, a significant knowledge gap exists in terms of correlating the growth conditions with their electronic transport properties which is of great importance for their realization of the overreaching goals in electronic device applications.

Since the first realization of MoS$_2$ growth via sulfurization of Mo films by Zhan et al in 2012 [8], many research have followed and focused on improving the quality of these films owing to the high scalability, low production cost, and the great thickness control achieved by this method.[11,16] High temperature growth/annealing is proposed by many groups in order to improve crystallinity since increased grain sizes and good layer orientation is seen in high temperature grown films.[9,17] Also, it was reported that the stoichiometric MoS$_2$ is grown only at high temperatures (> 750 °C) while low temperature grown films are heavy in S vacancies.[9,18] The TVS growth technique is widely used to grow MoS$_2$ films directly on Si/SiO$_2$ substrates for electronics applications and projecting from better structural/crystalline/chemical quality, high
temperature grown films are expected to give better electrical quality. However, a direct correlation between the growth temperature and the electrical quality of the films is not reported for these films to our best knowledge. We collected information on how the device resistance varied among the reported literature where the as-grown MoS\textsubscript{2} films on Si/SiO\textsubscript{2} substrates are used for device fabrication. The results are shown in Table 1, and Figure 37 show the reported device resistance values as a function of growth temperature. As one can observe, there is a six orders of magnitude variation in these resistance values, yet no direct relation to the growth temperature is present. In addition, atomic diffusion of SiO\textsubscript{2} to the grown MoS\textsubscript{2} in the TVS grown films at the high temperature was observed by Liu et al.[16,19] In another recent study which showed passivation of Si/SiO\textsubscript{2} substrates with S prior to the MoS\textsubscript{2} crystal growth via co-evaporation, the S bonding with Si at the Si/SiO\textsubscript{2} substrate surface was seen at temperatures as low as 500 °C.[20] The effect of such substrate changes are not studied in correlation with the device properties. Therefore, understanding the effect of growth temperature on the electrical properties of these films and detailed evaluation of the influence of underlying growth substrate is necessary to improve their electrical quality for future scalable device applications.
Table 1: A summary of resistance values reported for the devices on MoS$_2$ films directly grown on Si/SiO$_2$ substrates via TVS methods. *The resistance values shown here are either directly reported values or approximated using I-V curves provided in the reports.

<table>
<thead>
<tr>
<th>Resistance*</th>
<th>Growth Temperature</th>
<th>MoS$_2$ thickness</th>
<th>Notes on growth method/Precedurs</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 kΩ</td>
<td>750 °C</td>
<td>1-2 L</td>
<td>Sulfurization of e-beam deposited Mo film. S vapor provided by independent heating of S powder</td>
<td>[8]</td>
</tr>
<tr>
<td>~1 GΩ</td>
<td>1050 °C</td>
<td>3 L</td>
<td>Sulfurization of e-beam deposited 1 nm Mo film. S vapor by independent heating of S powder at 160 °C</td>
<td>[9]</td>
</tr>
<tr>
<td>~10 MΩ</td>
<td>750 °C</td>
<td>4 L</td>
<td>Sulfurization of e-beam deposited 0.5-3 nm Mo film. Annealing in H$_2$S/H$_2$/Ar (1: 5: 50)</td>
<td>[10]</td>
</tr>
<tr>
<td>~50 MΩ</td>
<td>800 °C</td>
<td>10 nm</td>
<td>Sulfurization of sputtering deposited 3 nm Mo film. S vapor provided by heating of S powder upstream side of single zone furnace</td>
<td>[11]</td>
</tr>
<tr>
<td>~80 MΩ</td>
<td>850 °C</td>
<td>5.1 nm</td>
<td>Sulfurization of thermally evaporated 1.3 nm Mo film. S vapor by independent heating of S powder at 160 °C</td>
<td>[12]</td>
</tr>
<tr>
<td>~130 MΩ</td>
<td>600 °C</td>
<td>4-5 L</td>
<td>Sulfurization of e-beam deposited 1-2 nm Mo film. S vapor provided by heating of S powder upstream side of single zone furnace</td>
<td>[13]</td>
</tr>
<tr>
<td>~160 GΩ</td>
<td>830 °C</td>
<td>3.95 nm</td>
<td>Sulfurization of e-beam deposited 2.5 nm Mo film. S vapor provided by independent heating of MoS$_2$ powder at 900 °C</td>
<td>[14]</td>
</tr>
<tr>
<td>~2 GΩ</td>
<td>950 °C</td>
<td>3-4 L</td>
<td>RF magnetron sputtering using MoS$_2$ target, followed by electron beam irradiation and 1 h annealing in H$_2$S</td>
<td>[15]</td>
</tr>
</tbody>
</table>

Figure 37: A plot of MoS$_2$ device resistances reported in the literature for large area CVD grown films on Si/SiO$_2$ substrates as a function of growth temperature.

In this chapter, I study the effect of growth temperature on the electrical properties of large area MoS$_2$ films grown via TVS method. The electrical characterizations show a continuous
increase in device resistance with growth temperature and a 258x increase in average device resistance was observed when the growth temperature increased from 650 °C to 800 °C. The Raman characterizations showed peak narrowing as the growth temperature increases illustrating the improved structural quality of the films as expected which indicated that the unexpected high-resistive behavior has a different origin than the structural quality of the films. In a control experiment, it was found that the roughness of SiO₂ surface increased by ~24 times after S annealing indicating a reaction between the amorphous SiO₂ and S at elevated temperatures. Via XPS characterizations, we found evidence for the presence of SiO₂ surface layer on grown films with increased thickness at high temperature that led to the increased device resistance by affecting both channel and contact resistances. Similar growth performed on sapphire showed absence of these substrate related contaminations and the device properties were mainly attributed to the composition and structural quality of the MoS₂ films. The results shown here reveals a large resistance variation of CVD grown MoS₂ films on Si/SiO₂ substrates with growth temperature and the significance of growth substrate in such variation which are essential information for improving the quality these large area MoS₂ films for device applications.

5.2 Experimental procedures

5.2.1 MoS₂ film growth

Si/SiO₂ (SiO₂ thickness 250 nm) and sapphire substrates were cleaned by sonicating in an acetone bath for 5 min followed by 5 min sonication in isopropanol and DI water rinse. Samples were then treated with mild oxygen plasma for 10 min to remove any organic residue. 6 nm thick Mo films were deposited on the substrates via e-beam evaporation at a rate of 0.05 A/s. Mo deposited substrates were then placed at the center of a 1-inch quartz tube in a single zone tube
furnace (Barnstead International F79300 Tube Furnace). 2g of S powder (99.5%, Sigma Aldrich) was loaded to the tube and placed at the upstream side of the tube at a 10 cm distance from the center. With this positioning, the melting and evaporation of the S powder occurs when the temperature of the central zone reach 550 °C. The system was then pumped down to a base pressure of 60 mTorr, a 140 sccm flow of argon (Ar) gas (99.995% purity) was continuously flowed in the tube throughout the growth time to transport the S vapor to the reaction zone. The temperature was then raised to the growth temperature (650 °C - 800 °C) at a rate of 15 °C/min and held for 1 hour (dwell time). After the dwell time, the furnace could cool down naturally to the room temperature.

5.2.2 Material and Device Characterizations

For resistance measurements, 40 nm thick gold pads with 300 μm x 300 μm dimensions separated by 100 μm were deposited through a shadow mask via thermal evaporation. The electrical measurements of the devices were performed in a probe station using a current preamplifier (DL instruments 1211) interfaced with Lab View program under ambient conditions. A tapping mode AFM (Veeco instruments, Dimension 3100) topography was used to obtain the topography of sulfurized Mo films. Raman spectroscopy measurements were carried out with confocal Raman microscope (Witec alpha 300 RA) at an excitation wavelength of 532 nm and with laser power < 1 mW in ambient conditions. XPS measurements were carried out using a Thermo Scientific (Escalab Xi) system with a monochromatic Al Kα source in a scan area of 300 x 300 μm².
5.3 Results and Discussions

5.3.1 Electrical characterizations of the films grown at 650 °C - 800 °C.

We electrically characterized as-grown MoS₂ films by 2-probe I-V measurements with top gold (Au) contacts. The channel length of all the devices measured in this study is 100 µm and the channel width is 300 µm. Figure 38 shows the electrical characterizations of the films grown on Si/SiO₂ substrates at the growth temperatures of 650 °C, 700 °C, 750 °C, and 800 °C. The I-V curves of representative devices (Figure 38 (a)) shows the drain currents at 1V to be 17.9 nA, 9.1 nA, 0.9 nA, and 0.1 nA at 650 °C, 700 °C, 750 °C, and 800 °C, respectively which is a clear decrease with the growth temperature. A boxplot of resistance of multiple devices with same dimensions is shown in Figure 38 (c). The average values for the resistance are calculated to be 55.7 MΩ, 111.9 MΩ, 1.15 GΩ, 14.4 GΩ. There is 258 times increase in device resistance when the growth temperature increased from 650 °C to 800 °C. At 800 °C, we observe non-linear I-V characteristics for the device and large hysteresis as shown in Figure 38 (b). Many reports have shown that 2D materials show this hysteresis behavior due to intrinsic/extrinsic defects.[21-23] Therefore, this is an indication that charge traps are created on the MoS₂ films at high growth temperature which could also be responsible for the increased resistance of the films.
Figure 38: (a) I-V curves of representative MoS$_2$ devices on films grown at 650 – 800 ºC. (b) An I-V curve of a device on 800 ºC grown film with forward and reverse voltage sweeps. (c) A boxplots of device resistance in log scale as a function of growth temperature.

5.3.2 Raman characterizations

In order to characterize the grown films and to find the origin of the resistance variation discussed in the previous section, we performed a detailed analysis of the Raman spectra of grown MoS$_2$ films. Figure 39 (a) show the Raman single spectra of the films grown at 650 ºC - 800 ºC. At all the temperatures, we observed two prominent peaks in the Raman spectra at ~ 387 cm$^{-1}$ and 413 cm$^{-1}$ which corresponds to the Raman active E$_{1g}^1$ and A$_{1g}$ vibrational modes of MoS$_2$ lattice. The peak positions plotted against the growth temperature is shown in Figure 39 (c). There is no significant shift in E$_{1g}^1$, however the shift in A$_{1g}$ was measured to be 0.8 cm$^{-1}$ from 650 ºC to 800 ºC. This suppression in out of plane A$_{1g}$ vibrational modes also indicate that the high temperature
grown films are richer in extrinsic defects.[24,25] The FWHM values of both peaks fitted with Gaussian functions are shown in Figure 39 (b). The FWHM of E\textsubscript{12g} were measured as 10.0 cm\textsuperscript{-1}, 9.3 cm\textsuperscript{-1}, 9.0 cm\textsuperscript{-1}, 8.4 cm\textsuperscript{-1} and A\textsubscript{1g} peaks showed the FHHMs of 10.8 cm\textsuperscript{-1}, 9.3 cm\textsuperscript{-1}, 8.2 cm\textsuperscript{-1}, 7.7 cm\textsuperscript{-1} with the increasing growth temperature. The difference between the FWHM values for 650 °C and 800 °C grown films are 1.6 cm\textsuperscript{-1} and 3.1 cm\textsuperscript{-1} for E\textsubscript{12g}, and A\textsubscript{1g} peaks, respectively. The FWHM of both peaks decreased with the increasing growth temperature, which is an indication of improved structural quality of the material grown at high temperature.[9,26] Increased resistance of the films with growth temperature is in disagreement with this conclusion derived from Raman results since improved crystallinity should result in better electrical quality of the films.[17] Therefore, we presume that there is another major factor affecting the electrical properties of the MoS\textsubscript{2} films grown on Si/SiO\textsubscript{2} substrates.
Figure 39: (a) Raman single spectra for the films grown at 650 °C – 800 °C on Si/SiO₂ substrates. The raw data is shown with hollow circles and the Gaussian fittings for E₁²g, A₁g peaks are shown in red and blue, respectively. (b) The FWHM of E₁²g (red) and A₁g (blue) peaks as a function of growth temperature. (c) The peak positions of E₁²g (red) and A₁g (blue) as a function of growth temperature.

5.3.3 Topography of the films.

We acquired the topography of films using tapping mode AFM. Figure 40 summarizes the results of AFM analysis. As shown in Figure 40 (a), there is a clear change in topography of the films with growth temperature. We measured the average grain sizes to be 18 nm, 35 nm, 48 nm, and 79 nm and for the films grown at 650 °C, 700 °C, 750 °C, and 800 °C, respectively. The film roughness was measured to be 0.7 nm, 0.8 nm, 1.2 nm, and 5.0 nm at 650 °C, 700 °C, 750 °C, and 800 °C, respectively as shown in Figure 40 (b). Large film roughness was observed in 800 °C film compared to the 650 °C as visualized from the 3D image shown in Figure 40 (c).
Figure 40: (a) Tapping mode AFM topography of MoS$_2$ films grown at 650 °C – 800 °C on Si/SiO$_2$ substrates. (b) The RMS roughness of the films as a function of growth temperature. (c) The 3D images of film topography at 650 °C (top) and 800 °C (bottom)

We conducted a control experiment by annealing bare Si/SiO$_2$ and sapphire substrates under the same CVD conditions to see if the roughness variation is originated from any changes at the substrate surface. Figure 41 show the AFM topography of the substrate surfaces after this annealing step. The topography of the substrate surfaces before annealing are shown in the insets. The change in Si/SiO$_2$ substrate after sulfur annealing is clearly seen in Figure 41 (a) while the change in sapphire substrate is insignificant. We measured the RMS roughness of Si/SiO$_2$ substrate before annealing to be 0.15 nm and after annealing it changed to 3.61 nm which is ~ 24x increase in surface roughness. Sapphire roughness was measured to be ~ 0.13 nm before annealing, after annealing it only changed to 0.28 nm which is only a 2x increase. Therefore, our AFM data suggest
that there could be some reaction occur between SiO\(_2\) and S at high temperature which completely alters the topography of the SiO\(_2\) layer.

![AFM images of (a)Si/SiO\(_2\) and (b) sapphire substrates after annealing in S vapor. Scale bar is 200 nm in each image. The insets show the AFM images of surfaces before annealing. Scale bars are 100 nm for the insets.](image)

Figure 41: AFM images of (a)Si/SiO\(_2\) and (b) sapphire substrates after annealing in S vapor. Scale bar is 200 nm in each image. The insets show the AFM images of surfaces before annealing. Scale bars are 100 nm for the insets.

### 5.3.4 XPS studies

*(Acknowledgements to Kirk Scammon and UCF Material Characterization Facility for XPS data)*

We characterized the 650 °C and 800 °C grown films via XPS to determine their chemical composition. Figure 42 show the XPS survey spectra of the films on Si/SiO\(_2\) substrates grown at 650 °C, and 800 °C. In 650 °C film, we observe Mo 3d and S 2d peaks located at 226 eV and 162 eV, respectively. With their atomic percentages, the Mo:S ratio was calculated to be 1:1.8 which is below expected stoichiometry of 1:2 for the MoS\(_2\) film. This is in agreement with the previous reports and show the S vacancy rich nature of low temperature grown films.[9,18] In addition to MoS\(_2\) related peaks, the O 1s (531 eV) and Si 2p (102 eV) peaks with high intensity are present in the spectra indicating that a surface layer of SiO\(_2\) is present on the MoS\(_2\) films. Due to the limited penetration depth of electrons (~ 5 nm)[16], the SiO\(_2\) layer underneath the MoS\(_2\) cannot give such high intensity peaks in the XPS spectra since our MoS\(_2\) films are ~ 23 nm thick.[12,27] In 800 °C
grown film, only Si, and O peaks are seen. The atomic percentages of Si and O was calculated to be 34% and 66%, respectively with Si:O ratio of 1:1.94 which in fact confirm that the surface layer is SiO₂. Absence of Mo 3d and S 2p peaks suggest that the SiO₂ surface layer grown thicker at higher temperature. It should be noted that films were characterized via Raman spectroscopy before XPS measurements and confirmed the presence of MoS₂ for all the temperatures. Unlike the XPS, the probing depth of photons used in Raman spectroscopy is ~ 700 nm in SiO₂ with the green laser.[28] This observation is in line with the interfacial reactions and SiO₂ diffusion through the MoS₂ film observed by Li et al. in their TEM and XPS measurements.[19]

![XPS survey spectra for the films grown at 650 °C (blue) and 800 °C (red) on Si/SiO₂ substrates. Mo 3d and S 2p core level spectra are shown in insets.](image)

The total resistance measured in our devices is a combination of channel resistance and contact resistance ($R_{\text{total}}=R_{\text{channel}}+R_{\text{contact}}$). The diffusion of SiO₂ through the MoS₂ grains can cause increase in MoS₂ channel resistance. We suggest that some SiO₂ can be trapped between the MoS₂ grains causing additional defect scattering of electrons at the grain boundaries. In many 2D
devices, it was shown that the contact resistance is major limiting factor of achieving good device performance since the contacts are not heavily doped as in typical semiconductors [9,29,30] and known to depend on the interfacial layer between the metal and semiconductor.[31] Therefore, the formation of SiO$_2$ surface layer and its increasing thickness with growth temperature can severely affect and change the contact resistance of the devices as well.

**5.3.5 Control Experiments: MoS$_2$ growth on sapphire substrates**

To confirm that the resistance variation of the devices on Si/SiO$_2$ substrates is mainly due to the SiO$_2$ contamination in the MoS$_2$ films, we grew the films on high temperature tolerant and chemically inert sapphire substrates under identical CVD conditions and electrically characterized. The I-V curves and the boxplot of resistance for the devices are shown in Figure 43. We measured the drain currents for the MoS$_2$ devices on sapphire substrates to be 16.7 nA, 8.9 nA, 9.0 nA, and 9.0 nA. Unlike in Si/SiO$_2$, we did not observe a significant change in drain current after 700 °C. The average values for the resistance are calculated to be 60.8 MΩ, 109.1 MΩ, 108.5 MΩ, and 106.4 MΩ for 650 °C, 700 °C, 750 °C, and 800 °C grown films, respectively. The resistances of the devices are in the same range as the devices on Si/SiO$_2$ substrates until 700 °C, then decreased slightly by 0.6 MΩ at 750 °C, and decreased further by 2.1 MΩ at 800 °C as expected from the improved structural/crystalline quality of MoS$_2$ with increased growth temperature.[17]
Figure 43: (a) I-V curves of representative MoS\textsubscript{2} devices on films grown at 650 – 800 °C on sapphire substrates. (b) A boxplots of device resistance of multiple devices measured as a function of growth temperature.

Figure 44 show the full deconvolution of the Mo 3d and S 2p core-levels in XPS. The atomic percentage of Mo was calculated to be 35.62\% and atomic percentage of S was 64.39\% which gives Mo:S ratio of 1:1.8. The lower resistance of the MoS\textsubscript{2} films observed at 650 °C on both Si/SiO\textsubscript{2} and sapphire substrates can be related to this lower stoichiometry of the films. Commonly observes n-type conductance of MoS\textsubscript{2} is attributed to the S vacancies.\cite{32,33} Low percentage of S implies that the films have more S vacancies, therefore more n doped.\cite{34,35} This higher level of doping could result in higher conductance and lower resistance of the MoS\textsubscript{2} films grown at 650 °C in our experiments.
Figure 44: (a) Mo 3d, and (b) Se 2p XPS core level spectra and their deconvolution for films grown on sapphire at 650 °C.

Figure 45 compare the XPS spectra of films grown on Si/SiO$_2$ and sapphire substrates at 800 °C. Unlike in Si/SiO$_2$, the films grown on sapphire substrates clearly show Mo and S peaks even at this high temperature. Importantly, Al 2p peak (74.6 eV) for the sapphire substrate is absent in the spectra. This validate that the underlying growth substrate cannot be seen in XPS data; therefore, the Si and O peaks observed for the films grown on Si/SiO$_2$ substrates are clearly due to their presence at the surface. The Mo:S ratio at 800 °C was calculated to be 1:2.03 showing stoichiometric MoS$_2$ is grown at high temperature.[9]
Figure 45: Comparison of XPS spectra for the films grown on Si/SiO$_2$ substrates (red) and sapphire substrates (green) at 800 °C. The relevant core-level spectra of Mo 3d, S 2p, and Al 2p are shown in the insets.

5.4 Conclusions

In conclusion, this chapter discuss the experimental evidence of resistance variation with growth temperature in MoS$_2$ thin films grown via sulfurization of Mo films. We found that the device resistance continuously increased with increasing growth temperature for the MoS$_2$ films grown on Si/SiO$_2$ substrates. Raman studies showed continuous narrowing of E$_{12g}$ and A$_{1g}$ peaks indicating improved structural quality with increasing growth temperature in which case improved electrical quality is expected for the films, yet opposite effect was observed. AFM characterizations showed that the roughness of the Si/SiO$_2$ is increased by 24x after annealing in S vapor indicating a reaction between S and SiO$_2$ at elevated temperatures. A SiO$_2$ surface layer formation and its increased thickness at high temperature was shown via XPS measurements for the MoS$_2$ films grown on Si/SiO$_2$ substrates which caused large increase in device resistance by
affecting MoS$_2$ channel resistance as well as the contact resistance while such contamination is not present in the films grown on sapphire substrates. The results presented here show that the MoS$_2$ film quality improves with high temperature growth; however, the substrate-related contamination should be seriously addressed when films are grown directly on Si/SiO$_2$ substrates.

5.5 References


CHAPTER 6: LOW PRESSURE CVD GROWTH OF LARGE AREA PdSe$_2$
AND DIRECT ASSEMBLY OF HETEROSTRUCTURES

6.1 Introduction

Semiconducting MoS$_2$ and similar TMDs compose bandgaps in visible to short-wave near-infrared (SW-NIR) wavelengths. Applications such as thermal imaging require detection of wide range of IR wavelengths (1-14 um). Black phosphorus (BP) is a widely studied layered material for such applications compose a layer tunable band-gap from 0.3 to 1.5 eV[1]; however, this material is highly unstable in air causing challenges in practical electronics applications. In recent years, group-X noble TMDs (PtSe$_2$, PdSe$_2$, PtS$_2$, etc.) with similar narrow bandgaps and high air stability have gained much interest. In particular, PdSe$_2$ shows 0 (bulk) to 1.3 eV (monolayer) variation in band gap which facilitates high performance optoelectronic devices such as photodetectors operating in the infrared region.[2-4] PdSe$_2$ crystals are synthesized by self-flux methods[5] and exfoliated down to mono-few layers for device applications which suffer from low yield and small domain sizes. CVD co-evaporation synthesis methods are adapted for PdSe$_2$ single crystal growth by using Pd/PdCl$_2$ and Se powder precursors.[6,7] These methods still produce localized small crystals which require transfer and/or multi-step lithography processes for device fabrication. Recently, facile wafer scale growth of PdSe$_2$ was reported by Zeng et al.[8] by using pre-deposited Pd films with excellent thickness and band-gap control. The growth temperature reported for these materials are much lower (450 - 480 °C) than most TMDs.[9] Successful modifications for the growth method which can further lower the growth temperature of these films would enable their direct growth on plastic substrates for flexible electronics applications.
Previous studies have shown that low pressure CVD (LPCVD) conditions allow lowering the growth temperature and also improve the homogeneity of the 2D films. [14-16]

Beyond the individual 2D layers, the heterostructures of these materials can show tunable, broad band photovoltaic applications. The large area PdSe$_2$ films were adapted for heterojunction fabrication with Si[8] by directly growing PdSe$_2$ films on a Si wafer which is a 2D-3D semiconductor junction. PdSe$_2$ films transferred on to Si nanowire arrays have shown thermal imaging and humidity sensing applications.[17] Also, PdSe$_2$/perovskite[4] Schottky diode was realized by spin coating perovskite on PdSe$_2$ and showed broadband photodetection with polarization sensitivity.[4] Fabrication of 2D-2D Van der Waal heterojunctions with these large area PdSe$_2$ films have not explored yet.

In this chapter, I show centimeter scale patterned growth of PdSe$_2$ via low pressure selenization of Pd films and its integration in 2D-2D heterojunction integration. In contrast to the previous reports, the method discussed here enabled lowering the growth temperature needed for PdSe$_2$ film growth down to 250 °C. Grown films were first analyzed via AFM, Raman, XPS, and electrical transport measurements in bottom gated FET configuration to comprehensively study the effect of the growth temperature on the topography, composition, and electrical quality of the grown films in the range of temperatures from 250 °C - 375 °C. PdSe$_2$ structural quality improvement at high temperature is evidenced through Raman peak narrowing. Complete conversion of Pd metal layer was supported by the XPS characterizations for the entire range of growth temperatures with evidence of excess Se presence on the surface which resulted in p-type conductance of the films. The I-V measurements conducted on these films showed that the resistance of the films decreased by ~ 40% with increasing growth temperature from 250 °C to 375
°C which is in line with the improved film quality suggested by the Raman data. We have used this PdSe\textsubscript{2} films to fabricate a MoSe\textsubscript{2}/PdSe\textsubscript{2} vertical Van der Waal heterojunction for the first time by directly growing PdSe\textsubscript{2} on pre-grown MoSe\textsubscript{2} which showed a good current rectification behavior with rectification ratio up to 232.

6.2 Experimental Procedure

6.2.1 PdSe\textsubscript{2} film growth

2nm thick Pd films were deposited on Si/SiO\textsubscript{2} substrates via e-beam deposition at a rate of ∼0.05 A/s. The substrates were cleaned by sonicating in an acetone bath for 5 min followed by 5 min sonication in isopropanol and DI water rinse. To further remove the organic residues, samples were treated with mild oxygen plasma for 10 min. The film thickness was confirmed via AFM. The Pd deposited substrate then placed at the center of a 1-inch quartz tube in a single zone tube furnace (Barnstead International F79300 Tube Furnace). 2g of Se powder (99.5\%, Sigma Aldrich) was loaded to the tube and placed at the upstream side of the tube at a 4 cm distance from the center. For each growth temperature, the Se boat position was slightly adjusted in a way that Se starts vaporizing when the center of the furnace reached 250 °C and the vapor remained in the chamber until it reached the growth temperature. The system was then pumped down to a base pressure of 60 mTorr, a 250 sccm flow of argon (Ar) gas (99.995\% purity) was continuously flowed in the tube throughout the growth time to transport the Se vapor to the reaction zone. The temperature was then raised to the growth temperature (250 - 400 °C) at a rate of 7 C/min and held for 1 hour (dwell time). After the dwell time, the furnace was allowed to cool down naturally to the room temperature.
6.2.2 MoSe₂ growth and heterostructure assembly

For heterostructures, molybdenum (Mo) channel with the size of 250 µm x 750 µm was deposited on Si/SiO₂ substrate through a shadow mask using e-beam deposition. Then the patterned Mo film was selenized in a similar LPCVD setup explained above. Following parameters were used for this selenization: 2g Se powder, growth temperature 750 °C, temperature ramp rate 15 °C/min, dwell time 50 min with 250 sccm Ar flow as the carrier gas for Se vapor. The selenized film was characterized via Raman to confirm that MoSe₂ is produced prior to the heterostructure assembly step. After, the shadow mask was aligned orthogonally to the MoSe₂ channel and 2 nm Pd was deposited. The selenization process for the Pd was performed as mentioned above at 300 °C. Au contacts were deposited through another shadow mask for both MoSe₂ and PdSe₂ channels.

6.2.3 Material and Device Characterizations

For I-V measurements for the PdSe₂ devices, a shadow mask was aligned with the grown PdSe₂ channels with the aid of an optical microscope (Olympus BX51M microscope equipped with Jenoptic Progres Gryphax camera). 40 nm thick gold pads were deposited via thermal evaporation. The electrical measurements of the devices were performed in a probe station using a current preamplifier (DL instruments 1211) interfaced with Lab View program under ambient conditions. A tapping mode AFM (Veeco instruments, Dimension 3100) topography was used to determine Pd and PdSe₂ film thickness measurements. Raman spectroscopy measurements were carried out with confocal Raman microscope (Witec alpha 300 RA) at an excitation wavelength of 532 nm and with laser power < 1 mW in ambient conditions. XPS measurements were carried out using a Thermo Scientific (Escalab Xi) system with a monochromatic Al Kα source in a scan area of 300 x 300 µm². Charging effect was calibrated by using standard carbon (C) 1s peak at 284.8
eV. The KPFM measurements were performed in a Horiba LabRAM HR Evolution Nano system with frequency modulation mode (FM-KPFM). Au coated Si cantilever calibrated with a freshly cleaved HOPG surface was used for all measurements.

6.3 Results and Discussions

6.3.1 Growth of PdSe₂ with LPCVD

2D PdSe₂ has unique puckered pentagonal structure unlike most 2D materials with hexagonal lattices. The crystallographic structure few-layer PdSe₂ is shown in Figure 46 (b). In PdSe₂ lattice, the basic tetragonal backbone is formed with a Pd atom bonded to four Se atoms. In addition, neighboring Se atoms form covalent Se-Se bonds due to which pentagonal rings and the puckering of the layers originate. PdSe₂ is the first isolated 2D material with such structure with the vertical puckering distance of 1.6 Å.[1] PdSe₂ monolayer has a thickness of ~ 4 Å[5,8], the layers are held together by weak Van der Waal bonds in few-layer PdSe₂. Figure 46 (a) show a schematic illustration of the experimental setup where the selenization of pre-deposited Pd films was done under low pressure conditions in a range of temperatures of 250 – 400 °C. Figure 46 (c) shows a digital photograph of a 2 nm Pd film deposited via e-beam evaporation of a Pd source along with the selenized films in the range of temperatures mentioned above. After selenization, the color of Pd film changed from deep pink to blue-gray up to 375 °C. Beyond that temperature, the film color changed slightly from its initial color and cracks on the film was observed suggesting the thermal decomposition of the film occurred > 400 °C. We tested the growth with the methods as discussed in previous reports and observed that PdSe₂ films can be grown even at 450 °C under APCVD conditions. These results will be further discussed in section 6.3.3 along with their Raman characterizations. Figure 46 (d) shows the topography of the PdSe₂ films taken via tapping mode
AFM in the range of selenization temperatures. RMS roughness was measured to 0.48±0.08 nm showing the high uniformity of the films. PdSe\textsubscript{2} thickness can be tuned by the adjusting the thickness of Pd metal seed layer.[8] All the samples used in this study are grown from 2 nm thick Pd which converted to 8 nm PdSe\textsubscript{2} after selenization for the whole range of temperatures. Considering each layer is 0.4 nm, this thickness corresponds to 20L PdSe\textsubscript{2}. Despite the small variation in surface roughness, the thickness variation with the selenization temperature is negligible which is an important observation since the bandgap of PdSe\textsubscript{2} is very sensitive to its thickness[1,8]. The thickness uniformity implies that the resistance variation discussed in later sections is not due to any changes in bandgap of the material.
Figure 46: (a) A schematic illustration of LPCVD setup used for the selenization of Pd films. (b) The crystallographic structure of few-layer PdSe$_2$. (c) A digital photograph of the patterned Pd film before and after selenization. (d) AFM topography of the PdSe$_2$ films grown at 250 °C – 375 °C. Scale bar is 100 nm in each image. (e) Corresponding AFM height measurements of the films. Scale bar is 500 nm each image.

6.3.2 Raman Analysis

We utilized Raman spectroscopy for chemical characterization of the films grown. Figure 47 (a) show the Raman single spectra of the films selenized in the range of 250 °C - 400 °C. Up to 375 °C, Raman spectra of the films showed four prominent peaks at ~ 146 cm$^{-1}$, 208 cm$^{-1}$, 224 cm$^{-1}$ and 259 cm$^{-1}$ which are corresponds to the $A_{1g}$, $A_{2g}$, $B_{21g}$ and $A_{3g}$ vibrational modes of PdSe$_2$ lattice, respectively. At 400 °C and above, we do not see any of these vibrational modes appear in the spectra which is an indication of termination of PdSe$_2$ growth above 375 °C. This is an
interesting observation since in APCVD methods, the temperatures as high as 480 °C is used for PdSe₂ growth.[4,8,17] In a control experiment, we also observed that the films can be grown even at 450 °C under APCVD conditions. This difference could have originated from the vapor pressure differences at atmospheric vs low pressure setups which will be discussed in section 6.3.3. Figure 47 (b) shows the position of A₁\text{g} and A₃\text{g} as a function of selenization temperature. We noted that there was no significant variation in the Raman peak positions of PdSe₂ films grown at different temperatures. However, the FWHM of the two high intensity peaks clearly decreased at high temperature as shown in Figure 47 (c). In previous reports, it was observed that the Raman spectra of PdSe₂ and similar noble metal TMDs red shift with the increasing thickness due to the stacking induced structural changes and/or the effect of long-range coulombic interactions.[8,18] In our growth, no significant change in the peak positions is an indication of thickness uniformity in all range selenization temperatures which also agree with the AFM thickness measurements. This signify that the Pd films are completely selenized up to the bottom-most Pd atomic layers even at temperature as low as 250 °C which is the lowest PdSe₂ growth temperature reported so far to our knowledge. We also measured the full width at half maximum values of A₁\text{g} and A₃\text{g} peaks, the results are shown in Figure 47 (c). FWHM of A₁\text{g} peak changed from 7.6 cm⁻¹ for the film selenized at 250 °C to 6.7 cm⁻¹ for the 375 °C selenized film which is a decrease of 0.9 cm⁻¹. Similarly, FWHM of A₃\text{g} decreased by 0.8 cm⁻¹ (6.7 cm⁻¹ at 250 °C to 5.8 cm⁻¹ at 375 °C). The FWHM of both peaks decreased with the increasing temperature, which is an indication of improved structural quality of the material.[19]
Figure 47: Raman Characterizations of the Pd films selenized at 250 °C – 400 °C. (a) Raman single spectra of the films. PdSe\(_2\) signature peaks are observed along with Si peak up to 375 °C, only the Si related peak is seen in the film selenized at 400 °C. (b) Position of the \(A^1_g\) and \(A^3_g\) peaks as a function of selenization temperature. (c) FWHM of the \(A^1_g\) and \(A^3_g\) peaks as a function of selenization temperature.

6.3.3 LPCVD vs APCVD growth

We observe a major difference in terms of the growth temperature needed for the PdSe\(_2\) growth via LPCVD setup used for our growth vs the APCVD setups discussed in the previous reports. As observed from the optical image shown in Figure 48 (a), the film was almost completely etched away at 400 °C when the low-pressure conditions are used. As a result, the Raman spectra does not show any PdSe\(_2\) signature for the film (Figure 48 (b)). In contrast, PdSe\(_2\) growth was successful even at 450 °C under atmospheric pressure conditions and confirmed via Raman measurements (Figure 48 (d)). However, the film grown in APCVD setup is highly non-uniform.
and rough as one can observe from the optical microscope image as well as the AFM image shown in Figure 48 (c). In atmospheric growth, the energy of precursor molecules is lost due to their interactions with the other atoms/molecules may present in the chamber such as O, H₂O, N, etc. Therefore, more energy needs to be supplied via thermal energy to overcome activation energy barrier for Pd-Se reaction. By pumping down the chamber to a low base pressure, the presence of other molecules can be greatly reduced which enable the PdSe₂ growth at lower temperatures and improve film uniformity.

Figure 48: Differences in film growth via LPCVD and APCVD methods. (a) An optical image of Pd film selenized under LPCVD conditions at 400 °C, and (b) its Raman spectra. No PdSe₂ related peaks were observed for this film. (c) An optical microscope image for the PdSe₂ film grown at 450 °C in an APCVD setup. AFM image is shown in the inset which shows the high roughness and nonuniformity of the film. (d) Raman spectra of the film shown in (c).
6.3.4 Composition of the films via XPS

(Acknowledgements to Kirk Scammon and UCF Material Characterization Facility for XPS data)

To verify the chemical composition, we performed XPS analysis for the films grown at the temperature range of 250 °C - 375 °C. The full deconvolution of Pd 3d and Se 3d core level spectra is shown in Figure 49. In Pd 3d spectra (Figure 49 (a)), Pd 3d_{5/2}, Pd 3d_{3/2} peaks (red) are located at ~337.2V, 342.5 eV that are related to the Pd atoms bonded to Se in PdSe₂.[20,21] It is important to note that there is no metallic Pd peak (335.3 eV) present in the spectra even at the lowest selenization temperature, which is an indication of complete selenization of the Pd metal seed layer.[22] The Se 3d spectra (Figure 49 (b)) consists of one main doublet (red) with Se 3d_{5/2}, Se 3d_{3/2} peaks located at ~55.1 eV, 56 eV respectively which is related to the Se atoms bonded to Pd (red) and one additional doublet (blue) located at slightly higher binding energies. A small contribution from selenium oxide (Se_xO_y - green) is observed at ~ 58.5 eV. The peak position of the main Se doublet well coincide with the characteristic peak positions for PdSe₂ reported in the literature.[20,21] The doublet at higher BE which could have caused by the edge/amorphous Se adsorbed on the PdSe₂ surface.[23,24] The contribution of this extra Se is more significant at 250 °C (~ 39%) and considerably reduced (~22%) at 300 °C and higher temperatures. Similar behavior was shown in MoS₂ films grown with similar sulfurization methods at low temperature.[25] It was shown that, at low temperature, the sulfur diffusion rate was slower along the layers than across the layers resulting in crystallization of MoS₂ grains in the out of plane direction. This caused trapping of more sulfur atoms in between MoS₂ nanoscale grains causing the additional sulfur peaks in their XPS measurements. Such possibility needs to be tested with further TEM measurements for our PdSe₂ films. The atomic ratio between Pd and Se was calculated to be 1:3.3.
at 250 °C and 1:2.4 at 300 °C and higher temperatures. We also calculated the Pd:Se ratios of the films based on the atomic percentages of Pd and Se in Pd-Se bond related peaks shown in the deconvolution (peaks shown in red) and were found to be close to 1:2 for all growth temperatures. Therefore, it is possible that even though the Pd metal layer is fully selenized at all selenization temperatures, there is a thin surface layer of amorphous Se/Se$_2^-$ present on the PdSe$_2$ film, more significantly at 250 °C. Presence of this excess Se could be responsible for the p-type conduction of the film observed in the transport measurements discussed in the next section since chalcogen rich TMDs have shown p-type conductance in previous reports.[26]
Figure 49: Core levels XPS spectra of the Pd films selenized at 250 – 375 °C. (a) Pd 3d spectra (b) Se 3d spectra. The circular symbols represent are experimental data. The peaks that are related to Pd-Se bonds are shown in red in both spectra.

### 6.3.5 Electrical properties

For electrical characterizations of the films, Au contacts were deposited by optically aligning a shadow mask for the patterned PdSe$_2$ channels. A schematic diagram of the FET device configuration is shown in Figure 50 (a) and an optical image of a representative device is shown in Figure 50 (b). Current-voltage (I-V) characteristics of representative devices are shown in
Figure 50 (c). Linear I-V characteristics at all selenization temperatures suggest that Au is making Ohmic contacts with PdSe$_2$. We measured the drain currents at 1V to be 0.4 µA, 0.8 µA, 1.3 µA, and 1.5 µA for the films grown at 250 °C, 300 °C, 350 °C, and 375 °C, respectively which is a clear increase with temperature. The total resistance of the devices was calculated to be 2.4 MΩ, 1.2 MΩ, 0.8 MΩ and 0.7 MΩ for these devices. We measured the I-V characteristics for 16 devices for each selenization temperature, the box plot of their resistance variation with growth temperature is shown in Figure 50 (d) along with a digital image of the devices shown in the inset. The average resistances are measured to be 2.4 MΩ (250 °C), 1.2 MΩ (300 °C), 0.7 MΩ (350 °C), and 0.6 MΩ (375 °C) for this set of devices. In PdSe$_2$, decrease in resistance could occur for multiple reasons. Since the bandgap of PdSe$_2$ decrease with increasing layer number, decreased resistance could occur with increasing film thickness. But in our growth, we already ruled out this possibility with AFM and Raman measurements which showed thickness uniformity at all selenization temperatures. Improved structural quality as shown in Raman analysis leads to better conductance and lower resistance of the films. However, this need to be tested further with other characterization methods designated for crystallinity measurements such as XRD since FWHM change seen in Raman is small. Doping of the films due to surface adsorbates could also change the drain current due to doping. As observed from in the XPS measurements, the presence of excess Se could change the doping level of the PdSe$_2$ channels. In the range of temperatures from 300 – 375 °C, where the excess Se amount calculated remained the same, the dominant effect for the decreased resistance with the temperature should be improved structural quality of the films. Much higher resistance observed for the 250 °C grown films could be a combined effect of low crystalline order and the effect of higher percentage of excess Se on the surface.
Figure 50: Electrical characterizations of the PdSe$_2$ films (a) A schematic representation of device configuration used in this study. (b) Optical image of a sample device (c) I-V characteristics of representative devices for the range of selenization temperatures of 250 $^\circ$C – 375 $^\circ$C (d) A boxplot of total resistance of the devices as a function of selenization temperature. 16 devices are measured in each set. The inset shows a digital image of the Si/SiO$_2$ substrate after the device fabrication.

The transfer characteristics of the devices are shown in Figure 51 where the devices show p-type transport behavior with mobilities ranging from 0.4-1 cm$^2$/Vs. Mechanically exfoliated PdSe$_2$ flake have shown ambipolar or n-type conduction in the literature[1,21,27,28]; therefore, the p-type conduction we observe in our CVD grown films could have originated from the presence of excess Se in the films as discussed in the previous section. The mobility of the device is affected by the polycrystalline nature of the films and comparable or better than the reported mobilities of other TMD films grown with similar methods.[29-31] Even though increase in mobility is expected for the devices as the growth temperature increased, we do not see a clear correlation in our data probably because the polycrystallinity effect dominated over the marginal improvement of the structural order with the growth temperature.
Figure 51: (a) Transfer characteristics representative PdSe$_2$ FET device which are synthesized at different selenization temperatures of Pd. (b) A boxplot of mobilities of the devices as a function of selenization temperature.

6.3.6 MoSe$_2$/PdSe$_2$ heterojunction assembly

We directly grew PdSe$_2$ at 300 °C on pre-grown MoSe$_2$ in a crossbar alignment to form a vertical Van der Waal heterojunction. MoSe$_2$ was grown by selenization of a 2 nm Mo film in a similar LPCVD setup at 750 °C. Detailed information can be found in the experimental procedure (section 6.2.2). The Raman spectra of selenized Mo film (Figure 52 (b)-green) consists of two prominent peaks at 240.2 cm$^{-1}$ and 288.5 cm$^{-1}$ which are corresponds to in-plane A$_{1g}$ and out of plane E$_{2g}$ Raman active modes of MoSe$_2$.\[32\] The I-V characteristics for the junction is showed in Figure 52 (a). The current rectification behavior of the junction can be seen in the I-V curve with an off current close to zero and the on current at 4V was measured to be ~ 30 nA with the turn on voltage of ~2V. The rectification ratio of the device was calculated by $I_{\text{forward}}/I_{\text{reverse}}$ and the maximum rectification was found to be ~232 at 3V. An optical image of the vertical heterojunction device along with the I-V curves for the individual PdSe$_2$ and MoSe$_2$ channels are shown in the inset of Figure 52 (a). The I-V curves of both channels are linear confirming that the diode-like behavior is not originated from the metal contacts at the MoSe$_2$ and PdSe$_2$. Via KPFM
measurements (acknowledgements: Ammon Johnston), we found that the work functions of PdSe\textsubscript{2} and MoSe\textsubscript{2} to be 4.58 eV and 3.83 eV, respectively as shown in Figure 53. Therefore, there is a 0.75 eV difference in the work functions of the two materials which leads to the rectifying behavior seen at the heterojunction. Raman spectra of MoSe\textsubscript{2} (taken before the PdSe\textsubscript{2} growth), PdSe\textsubscript{2} and the heterojunction are shown in Figure 52 (b). The Raman modes for the PdSe\textsubscript{2} are located at 147.8 cm\textsuperscript{-1} (A\textsubscript{1g}), 207.6 cm\textsuperscript{-1}(A\textsubscript{2g}), 224.2 cm\textsuperscript{-1} (B\textsubscript{21g}) and 259.2 cm\textsuperscript{-1} (A\textsubscript{3g}). The heterojunction region contains the Raman signature of both MoSe\textsubscript{2} and PdSe\textsubscript{2} with the peaks located at 147.7 cm\textsuperscript{-1}, 207.8 cm\textsuperscript{-1}, 224.4 cm\textsuperscript{-1}, 239.9 cm\textsuperscript{-1}, and 259.1 cm\textsuperscript{-1}. The low intensity E\textsubscript{2g} peak of MoSe\textsubscript{2} in the heterojunction is overlapped A\textsubscript{3g} peak of PdSe\textsubscript{2}, hence hardly observable in the Raman spectra. After the heterojunction assembly, no additional peaks except MoSe\textsubscript{2} and PdSe\textsubscript{2} related peaks present in the spectra confirming that no inter diffusion or hybridization occurred at the interface. The FWHM of MoSe\textsubscript{2} A\textsubscript{1g} peak in the heterojunction region was measured to be 3.7 cm\textsuperscript{-1} which is not significantly different from the pristine sample (3.9 cm\textsuperscript{-1}, with the instrumental uncertainty ~ 0.5 cm\textsuperscript{-1}) and the peak shift is insignificant as well (-0.3 cm\textsuperscript{-1}). This show that no substantial changes to the MoSe\textsubscript{2} structure (strain, doping, etc.) occurred due to the PdSe\textsubscript{2} growth step.
In conclusion, we showed successful patterned growth of PdSe₂ films under low pressure CVD conditions. In contrast to the previous reports, these conditions allowed PdSe₂ growth at temperatures as low as 250 °C. The topography, composition and electrical quality variations of
the films was comprehensively analyzed in the range of growth temperatures from 250 – 375 °C via AFM, Raman, XPS and electrical transport measurements. A vertical heterojunction of MoSe₂/PdSe₂ was implemented by directly growing PdSe₂ on to a pre grown MoSe₂ channel by a simple shadow mask technique at 300 °C. Preserved material quality at the junction was evidenced from Raman characterizations and good current rectification with the rectification ratios up to 232 was shown for the heterojunction device. Future scalable device applications of PdSe₂ can be benefited from the simple, low temperature growth route and direct, location-controlled heterojunction assembly shown in this study.

6.5 References


CHAPTER 7: CHARGE TRANSFER DOPING AND LATERAL HETEROJUNCTION INTEGRATION OF PdSe$_2$


7.1 Introduction

In recent years, there is a growing interest in group-X noble TMDs such as PtSe$_2$, PtS$_2$, and PdSe$_2$ due to their excellent air stability and widely adjustable band gaps similar to BP. The bandgap of PdSe$_2$ can be varied from near zero eV (quasi-metallic) in bulk to 1.3 eV in monolayer. Unlike in MoS$_2$, where the band gap reaches its bulk value within 5-6 layers[1], the band gap of PdSe$_2$ can be controlled more continuously with the layer number up to 40+ layers[2] which makes them very promising for high performance electronic and optoelectronic devices such as photodetectors operating in wide range of IR wavelengths.[3-5] In addition to this inherent layer dependent electrical properties, the ability to further tune the electrical properties of PdSe$_2$ via controlled doping is of fundamental importance for their wide range of electronic and optoelectronic device applications. Although a large number of first principle theoretical studies are initiated in recent years[6,7] due to the evolving interest in the versality of electrical, magnetic and optical properties that could be induced by doping of these materials, practical demonstration of doping engineering of PdSe$_2$ and other group-X TMDS is still at its infancy. Surface charge transfer doping (SCTD) is a simple, reliable and non-destructive method to achieve efficient doping in semiconductor materials.[8,9] In charge transfer doping, dopant molecules adsorb on the
surface of semiconductor material and exchange charges to dope the material. SCTD could be particularly effective in 2D materials owing to their high surface to volume ratio and exposed basal planes which enhances the surface adsorption of dopant molecules.[10] Successful utilization of SCTD to modulate electrical properties in CVD grown PdSe$_2$ could be a significant step towards its integration in practical applications.

In this chapter, we report an effective SCTD of CVD grown PdSe$_2$ thin film samples using BV molecules. PdSe$_2$ channels were grown via low pressure selenization of patterned Pd film at 325 °C. The FET fabricated on pristine PdSe$_2$ showed p-type conduction with a mobility of 0.58 cm$^2$V$^{-1}$s$^{-1}$ and resistance of 2.1 MΩ. Adsorption of BV molecules effectively lowered hole concentration in the PdSe$_2$ channel due to the transfer of electrons from BV via SCTD resulting in a large increase in resistance to 36.2 MΩ and a decrease in mobility to 0.44 cm$^2$V$^{-1}$s$^{-1}$. Raman analysis showed that A$_3^g$ peak red-shifted by 1.2 cm$^{-1}$ and broadened by 2.1 cm$^{-1}$ confirming the n-doping of the PdSe$_2$ film by BV. Electron transfer from BV to PdSe$_2$ was further confirmed by X-ray photoelectron spectroscopy (XPS) where binding energies (BEs) of Pd 3d and Se 3d core levels showed a negative shift with respect to the pristine material. Effective work function (WF) modulation of PdSe$_2$ with BV doping was observed via Kelvin probe force microscopy (KPFM) measurements where the n-doping caused a 0.3 eV decrease in WF of BV doped PdSe$_2$. We successfully applied the carrier density and WF modulation of PdSe$_2$ by SCTD to fabricate lateral heterojunction devices. Excellent current rectifying behavior was observed in the heterojunction devices with a maximum rectification ratio of ~55.
7.2 Experimental Methods

7.2.1 Doping of PdSe$_2$ devices

Patterned PdSe$_2$ films were grown by selenization a patterned Pd film with defined channels of 30 µm x 200 µm and the thickness of 2 nm in a similar CVD setup as described in section 6.2.1. A reduced BV solution was synthesized and extracted from a biphasic solution of toluene and benzyl viologen dichloride (Sigma-Aldrich) dissolved in water as described by Kim et al.[11] The substrate with patterned PdSe$_2$ devices was exposed to BV by either drop-casting or by immersing in BV solution for doping, the amount doping was monitored up to 12 hours. For heterostructure fabrication, doped and undoped regions of the same PdSe$_2$ channel was obtained by covering half of the PdSe$_2$ channel with a PMMA/Au mask and then immersing the substrate in BV solution for 30 min.

7.2.2 Material and device characterizations

For I-V measurements of the PdSe$_2$ devices, electrical contact was made using another shadow mask which was aligned with the grown PdSe$_2$ channels with the aid of an optical microscope (Olympus BX51M microscope equipped with Jenoptic Progres Gryphax camera). 40 nm thick gold pads were deposited via thermal evaporation. The electrical measurements of the devices were performed in a probe station using a current preamplifier (DL instruments 1211) interfaced with Lab View program under ambient conditions. A tapping mode AFM (Veeco instruments, Dimension 3100) topography was used to determine Pd and PdSe$_2$ film thickness measurements. XPS measurements were carried out using a Thermo Scientific (Escalab Xi) system with a monochromatic Al K$_\alpha$ source in a scan area of 300 x 300 µm$^2$. Charging effect was calibrated by using standard carbon (C) 1s peak at 284.8 eV. Confocal Raman measurements were carried out using a Horiba LabRAM HR Evolution Nano system at an excitation wavelength of
532 nm and with laser power < 1 mW in ambient conditions. KPFM measured were performed using the same system in frequency modulation (FM-KPFM) mode with gold coated Si cantilevers. Freshly cleaved HOPG surface was used to calibrate the WF of the cantilever.

7.3 Results and Discussions

7.3.1 Growth and Characterizations of PdSe$_2$ Films

The PdSe$_2$ thin films were grown via selenization of pre-deposited Pd thin films on Si/SiO$_2$ substrates using low pressure chemical vapor deposition (LPCVD) technique as described in the experimental section. After selenization, a noticeable color change of the film from pink to metallic gray was observed (Figure 54 (a)) suggesting the transformation of Pd to PdSe$_2$. The AFM image show initial thickness of Pd to be 2 nm (Figure 54 (b)), which transforms to a uniform PdSe$_2$ film with a thickness of 8 nm (Figure 54 (c)) after selenization corresponding to a 20 layer (L) of PdSe$_2$.[2] This thickness expansion is in good agreement with previously reported data for PdSe$_2$ grown via similar selenization method.[2]

Figure 54: (a) A digital camera image of Pd film before and after selenization. AFM topography and height profile of a Pd film (b) before, and (c) after selenization.
Raman measurement was used to further confirm the formation of PdSe$_2$. The Raman single spectra shown in Figure 55 (a) show four prominent peaks at 146 cm$^{-1}$, 208.4 cm$^{-1}$, 224.1 cm$^{-1}$, and 258.8 cm$^{-1}$ for our sample which corresponds to $A_{1g}$, $A_{2g}$, $B_{21g}$ and $A_{3g}$ vibrational peaks of PdSe$_2$, respectively. Theoretically, PdSe$_2$ Raman spectra is expected to show six prominent peaks due to 3 $A_g$ ($A_{1g}$, $A_{2g}$, $A_{3g}$) and 3 $B_{1g}$ ($B_{11g}$, $B_{21g}$, $B_{31g}$) vibrational modes in the PdSe$_2$ lattice.[12] However, $A_{1g}$/B$_{11g}$ and $A_{3g}$/B$_{31g}$ peaks are located very close together, therefore often observed as single peaks. The observed values of Raman peaks are consistent with previous reports of 2D PdSe$_2$.[2,3] For electrical characterizations, patterned PdSe$_2$ thin films of 200 µm x 30 µm were grown using a shadow mask. Drain and source electrodes were defined by depositing Au contacts through a shadow mask for the pre-defined PdSe$_2$ channel with dimensions of L=100 µm and W=30 µm. FET device properties were measured in ambient conditions by using highly doped silicon as the gate electrode and 250 nm thick SiO$_2$ as the gate dielectric. The linear current - voltage (I – V) characteristics curve shown in Figure 55 (b) suggests that the Au electrodes are making Ohmic contacts with the PdSe$_2$ channel. The gate voltage ($V_g$) was fixed at zero volt. The drain current at 1 V was measured to be 0.48 µA and the device resistance was calculated to be 2.1 MΩ. The I – $V_g$ curve of the same device is shown in the bottom-right inset. The increase of the current with decrease of the gate voltage indicates p-type transport behavior of the PdSe$_2$ FET device. The field effect mobility of the device was calculated to be 0.58±0.02 cm$^2$V$^{-1}$s$^{-1}$ using the equation $\mu = (L/WC_gV_{ds}) \times (dI/dV_g)$, where L, W and $C_g$ are the channel length, width, and the capacitance per unit area of gate dielectric, respectively. The relatively lower mobility of the device compared to the exfoliated sample with similar thickness[12] is possibly caused by the
polycrystalline nature of the film and is consistent with the mobilities reported for similar polycrystalline PdSe$_2$ and other 2D TMD films.[13,14]

Figure 55: Characterizations of a pristine PdSe$_2$ device. (a) Raman spectra of a PdSe$_2$ sample showing characteristics peaks, (b) I - V characteristics of a PdSe$_2$ device (V$_g$ = 0 V). The inset in top-left is an optical image and the bottom-right inset shows the transfer characteristics of the device.

7.3.2 Charge transfer doping of PdSe$_2$ Films with BV molecules

We tested the SCTD effect on the conductivity of the PdSe$_2$ FET device with BV immersion time and the results are shown in Figure 56. First, we drop casted a small amount of BV solution on PdSe$_2$ device and measured the I-V characteristics after drying the solution. The device was then immersed in BV solution for 30 minutes and measured again. The process was repeated by immersing the sample in BV solution for additional 5.5 hrs (total of 6 hrs) followed by another 6 hrs (total of 12 hrs). As illustrated from the I-V curves (Figure 56 (a)), the device conductivity is strongly affected by BV doping. The drain current of the device measured at 1V was decreased to 0.11 µA after drop-casting BV and 0.03 µA after 30 min doping. With longer BV immersion time, the change in the drain current is hardly noticeable in the I-V curve. Figure 57 (c) shows the resistance variation of the device (device 1) as a function of BV immersion time. The PdSe$_2$ devices showed increase of resistance to 7.5 MΩ when BV solution is drop-casted on
the sample. After 30 minutes immersion of the devices in BV solution, the average resistance increased to 36.2 MΩ which is ~1700 percent higher compared to the resistance of pristine device.

The resistance of the device was measured to be 40.6 MΩ and 42 MΩ after 6 hrs and 12 hrs immersion time. Therefore, the sample was close to saturation of doping in 30 min. We also observed relatively smaller drain current variation with gate voltage in the transfer curve shown in Figure 56 (b) after doping as compared to pristine PdSe₂ device. In the pristine device, the average slope of I-V₉ curve was calculated as -7.5 x 10⁻⁴ μA and in the BV doped device it is decreased to -1.8 x 10⁻⁴ μA. The field effect mobility after 30 min doping was calculated to be 0.44±0.02 cm²V⁻¹s⁻¹. We measured the I-V characteristics of a BV doped device after a week (Figure 56 (c)) which showed very small change in current indicating the stability of this doping method. Comparing the 20 L thickness of the pristine PdSe₂ film to the layer dependent band-gap reported in the literature, we anticipate that the valance and conduction bands are located around the energy values of -4.4 eV and -5.1 eV.[2] Accordingly, the conduction band edge of PdSe₂ stays very close to the 0 V vs SHE.[15] Hence, based on the previously reported redox potentials for BV[9,11] (-0.79 V versus standard hydrogen electrode (SHE) for BV⁰/BV⁺ and -0.33 V versus SHE for BV⁺/BV²⁺, respectively) and the conduction band minimum (CBM) and valence band maximum (VBM) for 20 L PdSe₂[2], we can depict energy diagram of the few layer PdSe₂ and BV as shown in Figure 56 (d). According to this diagram, the BV reduction potential is at a higher energy than the VBM and CBM of PdSe₂. Therefore, electron transfer from BV to PdSe₂ is expected. Upon electron transfer, the hole concentration in the valence band decreases resulting in an increase of resistance and decrease in carrier mobility.
Figure 56: BV doping of a PdSe$_2$ device. (a) I-V characteristics of a pristine and BV doped PdSe$_2$ device with different BV exposure time. (b) Transfer characteristics of the pristine and 30 min BV doped device. (c) I-V characteristics for a representative PdSe$_2$ device immediately after doping (red) and a week after doping (green) showing the stability of the doped device. (d) Schematic illustration to show the charge transfer process between PdSe$_2$ and BV.

Based on the charge transfer model depicted in Figure 56 (c), each BV molecule adsorbed on the surface can donate 2 electrons to PdSe$_2$ and these electrons can then diffuse to the inner layers of the sample. For PdSe$_2$ film, which is polycrystalline nature, the molecules can diffuse through the grain boundaries to the bottom layers effectively.[16] The number of electrons transferred to PdSe$_2$ is limited by effective area of exposure to BV molecules. When more BV$^{2+}$ are adsorbed on the PdSe$_2$ surface, further BV molecules cannot be adsorbed on the PdSe$_2$ surface for additional charge transfer. As a result, even after 12 hrs immersion of PdSe$_2$ devices into the BV solution, PdSe$_2$ did not show electron dominant transport. Similar behavior was observed
previously in n-type monolayer WS\textsubscript{2} doped with strong electron accepting molecule F4-TCNQ in which electron concentration gradually decreased and subsequently saturated with doping time while preserving the n-type conduction of the channel.[17]

Figure 57: (a), (b) I-V characteristics of two additional PdSe\textsubscript{2} devices with different BV exposure time. (c) The resistance variation of the three devices as a function of BV exposure time.

The effect of doping in electrical properties was measured for many devices and the same trend was observed. The I-V curves and resistance variation of two additional devices are shown in Figure 57. Device 2 resistance changed from 2.3 MΩ (pristine) to 7.7 MΩ (drop-casting), 30 MΩ (30 min), 32 MΩ (6 h), 34.1 MΩ (12 h) with increasing BV exposure time. Variation in device 3 was from 2.5 MΩ (pristine) to 7.9 MΩ (drop-casting), 31.4 MΩ (30 min), 32.4 MΩ (6 h), 36.1 MΩ (12 h). This is an increase of ~1400 % upon BV doping.

7.3.3 Changes in topography after doping

Figure 58 which show the AFM topography of the PdSe\textsubscript{2} film before and after BV immersion. The polycrystalline nature of the film is clearly seen in Figure 58 (a) with average grain size of ~15 nm and rms roughness of ~0.4 nm. The AFM image of the PdSe\textsubscript{2} film after BV immersion (Figure 58 (b)) show change in topography due to the adsorption of BV molecules on
the PdSe$_2$ surface. The thickness of the BV/toluene layer was measured to be ~ 4 nm which is compatible with the XPS and KPFM measurements discussed in later sections.

Figure 58: AFM image of the PdSe$_2$ film (a) before and (b) after BV immersion. The inset of (b) show the thickness of BV/toluene layer.

7.3.4 Raman investigations of the doping effect

Figure 59: Raman spectrum for pristine and BV doped PdSe$_2$. The inset shows a close-up view of the spectra at $A^3_g$ peak location.

It is known that the Raman peak position and FWHM of the out-of-plane vibrational modes are sensitive to doping. Raman spectra of the pristine and BV doped PdSe$_2$ sample is shown in Figure 59. We observed that all the peaks are red-shifted and broadened upon doping, these changes are more significant in the highest intensity $A^3_g$ peak. The $A^3_g$ peak of the BV doped sample is located at 257.6 cm$^{-1}$ which is a 1.2 cm$^{-1}$ shift toward lower wavenumbers compared to
the pristine sample. The FWHM of the $A^3_g$ peak is also increased from 7.1 cm$^{-1}$ (pristine) to 9.2 cm$^{-1}$ after doping. The electrons transferred to PdSe$_2$ from BV increases the electron-phonon coupling in the lattice causing phonon softening which resulted in red-shift and broadening of the peaks. No additional peaks appeared in the spectra after doping indicates that the chemical composition of the film is not altered by the doping, this non-destructive nature is a main advantage of SCTD of 2D materials.[8]

7.3.5 XPS investigations of the doping effect

(Acknowledgements to Kirk Scammon and UCF Material Characterization Facility for XPS data)

Figure 60: (a) Pd 3d, and (b) Se 3d XPS core level spectra of a pristine (blue) and BV doped (red) PdSe$_2$ films, respectively.

We further characterized the samples via XPS to verify the surface chemical composition and changes to the electronic structure after BV doping. The Pd 3d and Se 3d core level spectra for the pristine and BV doped PdSe$_2$ samples are shown in Figure 60 (a) and Figure 60 (b), respectively. The pristine sample (blue) show Pd 3d$_{5/2}$, Pd 3d$_{3/2}$ peaks at 337.2 eV, 342.5 eV and Se 3d$_{5/2}$, Se 3d$_{3/2}$ peaks at 55.2 eV, 56 eV respectively which are consistent with the characteristic peak positions for PdSe$_2$.[18,19] After BV doping (red), we observed the Pd 3d peaks shifted by
0.5 eV, while Se 3d peaks shifted by 0.3 eV toward lower BE. This BE shift provides a fundamental understanding to the charge transfer process between BV molecules and PdSe$_2$ which resulted in a decrease in hole charge carriers in the valence band of PdSe$_2$ observed in electrical characterizations. XPS studies can identify the BE of elements shift upon electron occupation (donation) due to the increased (decreased) intra-atomic electron-electron repulsion, a negative BE shift is observed with occupation of electrons and positive BE shift is correlated with electron donation.[20,21] Therefore, the negative shift in the core level spectra observed in our study is an indication that electrons are transferred from BV to PdSe$_2$[22] and is consistent with our electrical transport and Raman study. The electron transfer from BV places more electron density into the valence band and they localize at Pd/Se sites decreasing their core-level BEs.

7.3.6 KPFM observations in work function changes with doping

(Acknowledgements to Ammon Johnston for KPFM data)

To investigate the WF change in PdSe$_2$ due to BV doping, we conducted KPFM measurements on both pristine and BV doped samples. The mapping shown in Figure 61 correspond to the contact potential difference (CPD) between the gold coated KPFM probe and the sample. Highly oriented pyrolytic graphite (HOPG) with WF of 4.6 eV[23] was used as the reference material to calibrate the probe in order to measure the WFs of the samples. The KPFM mapping of the pristine PdSe$_2$ sample is shown in Figure 61 (a) while the mapping for BV doped samples is shown in Figure 61 (b). We measured an average CPD to be -71±10 mV for the pristine sample and 240±20 mV for the BV doped sample. The WFs are calculated using the equation

$$V_{CPD} = \frac{\phi_{tip} - \phi_{sample}}{e}$$

where $V_{CPD}$ is the CPD in volts, $\phi_{tip}$ is the WF of the tip, $\phi_{sample}$ is the WF of the sample and $e$ is the electron charge. With the HOPG calibration, $\phi_{tip}$ was found to be
4.81±0.01 eV. The WFs of the pristine sample was calculated to be 4.88 ±0.02 eV. This WF is consistent with the anticipated VBM (-5.1 eV) and CBM (-4.4 eV) discussed earlier for 20 L PdSe$_2$ since it shows that the Fermi level stays closer to the valence band of the intrinsic p-type PdSe$_2$. The WF of BV doped film was calculated as 4.57 ±0.03 eV, the WF lowering by ~0.3 eV after BV doping further confirms that BV molecules donated electrons (n-doping) to the PdSe$_2$ film.[23,24]

Figure 61: KPFM contact potential mapping of (a) pristine and (b) BV doped PdSe$_2$. Scale bar is 1 µm in each image.

7.3.7 Lateral heterojunction fabrication

To show an application of the PdSe$_2$ WF modulation via BV doping, we fabricated lateral heterojunction devices by implementing selective area doping of a PdSe$_2$ channel. For selective area BV doping and heterojunction fabrication, we used the PMMA/metal mask patterning technique[25] shown schematically in Figure 62 (a). First, the PdSe$_2$ devices were fabricated as described in the experimental methods. Then the substrate was spin coated with poly-methyl methacrylate (PMMA) followed by Au deposition through a shadow mask which was aligned to cover half of the PdSe$_2$ channel. After the Au deposition, the sample was exposed to oxygen plasma to etch the PMMA that was not covered by gold to partially expose the PdSe$_2$ thin film for BV doping. The substrate was then immersed in the BV solution for 30 min. This allowed the uncovered area of the PdSe$_2$ channel to dope while covered area remained undoped. As a result, a
heterojunction is created between doped and undoped section of the PdSe$_2$ channel. I-V characteristics of a representative heterojunction device is shown in Figure 62 (b). The I-V characteristics of the device shows a diode-like behavior (black curve) confirming that a heterojunction has been formed. Breakdown of the PdSe$_2$ heterojunction device was not observed until -5 V. The rectification ratio for the device was calculated by the ratio of $I_{forward}/I_{reverse}$ for the range of voltage in the I-V curve and the maximum rectification ratio was found to be ~ 55. To verify that this rectification behavior is solely an effect of BV doping, we conducted I-V measurements in each fabrication steps and observed linear I-V curves with similar current values indicating that the rectification behavior is not due to fabrication steps before doping (Figure 63). Therefore, the rectifying behavior is exclusively a consequence of the band offset occurred at the junction of pristine and BV doped PdSe$_2$. The KPFM study show the work function of pristine and BV doped PdSe$_2$ to be 4.88 eV and 4.57 eV, respectively. This leads to a band offset at the junction of pristine and BV doped PdSe$_2$ as shown in Figure 62 (c). This band offset allows the flow of charge carriers in forward bias while preventing the flow in reverse bias leading to a diode like behavior.
Figure 62: (a) Schematic diagrams showing the fabrication steps of PdSe₂ lateral heterojunctions by selective BV doping. (b) I-V characteristics of a heterojunction device in linear scale (black) and log scale (red). The inset shows an optical image of the device. (c) An illustration of the band offset with energy barrier ($\Delta E$) created at the junction between pristine and BV doped PdSe₂.

Figure 63: I-V curve for a pristine device and after the PMMA/metal mask and oxygen plasma processing step
7.4 Conclusions

In conclusion, we demonstrated an effective SCTD of 2D PdSe$_2$ thin films by using BV molecules. Patterned PdSe$_2$ samples were obtained by low pressure selenization of a pre-deposited Pd film. Pristine PdSe$_2$ device showed p-type conduction with a mobility of 0.58 cm$^2$V$^{-1}$s$^{-1}$ and average resistance of 2.1 M$\Omega$. A ~ 1700 percent increase in resistance and a decrease in mobility to 0.44 cm$^2$V$^{-1}$s$^{-1}$ was observed due to n-doping of PdSe$_2$ by BV molecules. Raman and XPS characterizations further confirmed the decrease in carrier concentration in doped sample is due to the electron transfer from BV to PdSe$_2$ (n-doping). KPFM measurements showed that the WF of PdSe$_2$ was effectively modulated by BV doping, a decrease of ~ 0.3 eV in the WF of PdSe$_2$ was measured after doping. A selective doping was implemented for the fabrication of heterojunction between pristine and BV doped PdSe$_2$, which showed good current rectification behavior with a rectification ratio of up to ~55 demonstrating the importance of SCTD to modify electrical properties of the PdSe$_2$. The facile, non-destructive doping method we discussed here can be used toward fabrication of high performance PdSe$_2$ electronic devices.

7.5 References


CHAPTER 8: SUMMARY AND FUTURE DIRECTIONS

8.1 Summary

In this dissertation, I introduced a new precursor design to achieve better vapor phase control in the co-evaporation CVD growth of monolayer MoS$_2$ crystals. Contrasting to the commonly used MoO$_3$ powder, thin films MoO$_3$ precursor used in this study facilitated precise control over the amount of MoO$_3$ and uniform evaporation rate of these films creates a stable vapor pressure at the growth phase, hence resulted in much controlled, uniform, clean single crystal growth. For the large area MoS$_2$ films grown on Si/SiO$_2$ via TVS route, I showed the effect of growth temperature on the electrical properties of the films by studying the resistance variation of the MoS$_2$ devices. I further discussed the challenges in using Si/SiO$_2$ substrates for the growth, specially at high temperature, showing the evidence for diffusion and formation of surface layer of SiO$_2$ covering the MoS$_2$. In the next chapter, I showed the low-pressure CVD growth of PdSe$_2$ films by selenization of patterned Pd films. The complete conversion of Pd to PdSe$_2$ was shown at a temperature as low as 250 °C which is the lowest growth temperature reported for PdSe$_2$. I systematically studied the electrical, chemical, and crystalline quality of the PdSe$_2$ in a range of growth temperatures from 250 °C to 375 °C. A vertical heterojunction diode with a high rectification ratio of 232 was realized by directly growing PdSe$_2$ on a pre-grown MoSe$_2$ film showing good electrical quality and uniformity of grown PdSe$_2$ films. To modulate the electrical properties of PdSe$_2$, surface charge transfer doping with BV molecules was employed and n-doping of the films was achieved. This electrical property modulation was used toward fabrication of lateral heterojunction diode by selective area doping of a PdSe$_2$ device.
8.2 Future Directions

With further research, the controllable synthesis method introduced in this dissertation for MoS\(_2\) monolayer crystal growth can be extended for the growth of other TMDs, large area growth and heterojunction integration as well. I initiated the large area monolayer MoS\(_2\) growth with the assistance of nucleation promoters such as sodium chloride (NaCl). Figure 64 show a summary of such large area monolayer growth. A schematic diagram of growth setup and an optical image of a centimeter scale as-grown MoS\(_2\) film is shown in Figure 64 (a). Figure 64 (b) elucidates the growth mechanism. Briefly, NaCl provide nucleation support for large area growth by corroding SiO\(_2\) in the presence of MoO\(_3\) (foaming Na\(_2\)SiO\(_3\)) and trapping highly mobile Na\(_2\)MoO\(_4\) intermediates at the substrate surface. Sulfurization of these intermediates grow MoS\(_2\) on the substrates leaving the craters and promoter residue (Na\(_2\)O) underneath the film. Figure 64 (c) show an AFM image of a transferred film with the inset showing a photograph of transferred film on a marked Si/SiO\(_2\) chip for device fabrication. These films showed good PL response (Figure 64 (d)) and composed of 80% monolayer regions as revealed from the Raman analysis (Figure 64 (e)). Further studies to improve this large area growth and reliable transfer methods for different TMDs will provide an opportunity to investigate exciting physics and device applications for various heterostructures. This study has also revealed numerous challenges in large area growth of monolayer TMDs by using seeding promoters. For an example, the corrosion occurred due to Na\(_2\)SiO\(_3\) formation created craters in the SiO\(_2\) layer which caused quenching in PL signal at the crater sites. Further research needs to address these issues in order to enhance the optical and electrical quality of these large area films.
Figure 64: Large area MoS$_2$ growth and transfer by using NaCl promoter. (a) Schematic representation of experimental setup and an optical image of as-grown monolayer film on Si/SiO$_2$ substrate. (b) A diagram representing the growth mechanism. (c) AFM topography of transferred MoS$_2$ film. Inset show an optical image of the transferred film on a marked Si chip. (d) Averaged PL spectra of 30 µm x 30 µm region of the transferred film. (e) The histogram of Raman peak separation showing that the film composed of 80% monolayer.

PdSe$_2$ show a relatively easy tunability of the material properties compared to other TMDs. Some reports have discussed that the structural anisotropy of the material due to its unique puckered pentagonal structure could be the root cause for such extraordinary changes. Therefore, exiting new applications can be realized by doping, strain modulation, and electrostatic modulation of PdSe$_2$ films. For an example, we tested the electrical property changes in PdSe$_2$ large area films by oxygen plasma exposure, some characteristics are shown in Figure 65.
Figure 65: PdSe$_2$ film property modulation with oxygen plasma exposure. (a) AFM topography of pristine and plasma exposed films. Scale bars are 1 um in each image. (b) Raman single spectra for pristine (black) and plasma exposed (red) films. A clear blue-shift and broadening is observed after the exposure. (c) the output characteristics of the heterojunction device shown in the inset.

This showed topographical changes (Figure 65 (a)) and extraordinary p-doping with ~ 6 cm$^{-1}$ blue shift in characteristic Raman peaks of PdSe$_2$ as shown in Figure 65 (b). A lateral heterojunction between pristine and exposed regions showed gate tunable non-linear I-V characteristics (Figure 65 (c)). Applications such as polarized light detection[1], pressure tunability[2] have shown and topological applications have predicted[3] for PdSe$_2$ and its heterojunctions in the literature as well. A comprehensive study with both theoretical and experimental investigations to show how these qualities are embedded to the structural anisotropy would be an interesting field to study.
8.3 References


APPENDIX: COPYRIGHT PERMISSIONS
Figure 3

Figure 4 (a), (b)
Figure 4 (c)

Figure 5
Figures 6 & 7

Figure 8
Figures 9 (a) & 10

Figure 9 (b)
Figure 13

Figure 19
**Figure 21 (a)**

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Figure 25 (b)
Chapter 4

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