2006

**Study Of Nanoscale Cmos Device And Circuit Reliability**

Chuanzhao Yu  
*University of Central Florida*

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STUDY OF NANOSCALE CMOS DEVICE AND CIRCUIT RELIABILITY

by

CHUANZHAO YU
B.S. Shanghai Jiaotong University, 1997
M.S. Tsinghua University, 2000

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the School of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

Spring Term
2006

Major Professor: Dr. Jiann S. Yuan
ABSTRACT

The development of semiconductor technology has led to the significant scaling of the transistor dimensions. The transistor gate length drops down to tens of nanometers and the gate oxide thickness to 1 nm. In the future several years, the deep submicron devices will dominate the semiconductor industry for the high transistor density and the corresponding performance enhancement. For these devices, the reliability issues are the first concern for the commercialization. The major reliability issues caused by voltage and/or temperature stress are gate oxide breakdown (BD), hot carrier effects (HCs), and negative bias temperature instability (NBTI). They become even more important for the nanoscale CMOS devices, because of the high electrical field due to the small device size and high temperature due to the high transistor densities and high-speed performances.

This dissertation focuses on the study of voltage and temperature stress-induced reliability issues in nanoscale CMOS devices and circuits. The physical mechanisms for BD, HCs, and NBTI have been presented. A practical and accurate equivalent circuit model for nanoscale devices was employed to simulate the RF performance degradation in circuit level. The parameter measurement and model extraction have been addressed. Furthermore, a methodology was developed to predict the HC, TDDB, and NBTI effects on the RF circuits with the nanoscale CMOS. It provides guidance for the reliability considerations of the RF circuit design. The BD, HC, and NBTI effects on digital gates and RF building blocks with the nanoscale devices – low noise amplifier, oscillator, mixer, and power amplifier, have been investigated systematically.

The contributions of this dissertation include: It provides a thorough study of the reliability issues caused by voltage and/or temperature stresses on nanoscale devices – from
device level to circuit level; The more real voltage stress case – high frequency (900 MHz) dynamic stress, has been first explored and compared with the traditional DC stress; A simple and practical analytical method to predict RF performance degradation due to voltage stress in the nanoscale devices and RF circuits was given based on the normalized parameter degradations in device models. It provides a quick way for the designers to evaluate the performance degradations; Measurement and model extraction technologies, special for the nanoscale MOSFETs with ultra-thin, ultra-leaky gate oxide, were addressed and employed for the model establishments; Using the present existing computer-aided design tools (Cadence, Agilent ADS) with the developed models for performance degradation evaluation due to voltage or/and temperature stress by simulations provides a potential way that industry could use to save tens of millions of dollars annually in testing costs.

The world now stands at the threshold of the age of nanotechnology, and scientists and engineers have been exploring here for years. The reliability is the first challenge for the commercialization of the nanoscale CMOS devices, which will be further downscaling into several tens or ten nanometers. The reliability is no longer the post-design evaluation, but the pre-design consideration. The successful and fruitful results of this dissertation, from device level to circuit level, provide not only an insight on how the voltage and/or temperature stress effects on the performances, but also methods and guidance for the designers to achieve more reliable circuits with nanoscale MOSFETs in the future.
To my wife Yanhua Chen and my child Savannah J. Yu
ACKNOWLEDGMENTS

I would like to express my gratitude to my advisor, Professor Jiann S. Yuan, for his warm, sincere, and approachable support, patience, and encouragement throughout my graduate studies. He contributed many critical directions and suggestions to this work while offering freedom to pursue and manage my own research. His technical and editorial advice was essential to the completion of this dissertation and has taught me innumerable insights on the workings of academic research in general. The knowledge and the philosophy that he taught me will be the guide for my professional life.

My thanks also go to the members of my dissertation committee, Drs. Issa Batarseh, John Z. Shen, Morgan C. Wang, and Thomas X. Wu for reading previous drafts of this dissertation and providing many valuable comments that improved the presentation and contents of this dissertation.

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<td>AC</td>
<td>Alternating Current</td>
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<td>ACPR</td>
<td>Adjacent Channel Power Ratio</td>
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<td>ADC</td>
<td>Analog to Digital Converter</td>
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<td>BD</td>
<td>Breakdown BPF Band Pass Filter</td>
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<td>BSIM</td>
<td>Berkeley Short-Channel IGFET Model</td>
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<td>CDMA</td>
<td>Code Division Multiple Access</td>
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<td>CHE</td>
<td>Channel Hot Electron</td>
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<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
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<td>C-V</td>
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<td>CVS</td>
<td>Constant Voltage Stress</td>
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<td>DAHC</td>
<td>Drain Avalanche Hot Carrier</td>
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<td>DC</td>
<td>Direct Current</td>
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<td>DSB</td>
<td>Double-Side Band</td>
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<td>DUT</td>
<td>Device-Under-Test</td>
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<td>EOS</td>
<td>Electrostatic Discharge</td>
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<td>Electrical Over-stress</td>
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<td>FOM</td>
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<td>HBD</td>
<td>Hard Breakdown</td>
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<td>HC</td>
<td>Hot Carrier</td>
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<td>HCI</td>
<td>Hot Carrier Injection</td>
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<td>HF</td>
<td>High Frequency</td>
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<td>Abbreviation</td>
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<td>IC</td>
<td>Integrated Circuit</td>
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<td>IGFET</td>
<td>Insulated-Gate Field-Effect Transistor</td>
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<td>IIP3</td>
<td>Input Third-Order Intercept Point</td>
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<td>IM3</td>
<td>Third-Order Intermodulation Distortion</td>
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<td>I-V</td>
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<td>Kirchhoff's Current Law</td>
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<td>KVL</td>
<td>Kirchhoff's Voltage Law</td>
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<tr>
<td>LCO</td>
<td>LC Oscillator</td>
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<tr>
<td>LCR</td>
<td>Inductance Capacitance Resistance</td>
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<td>LF</td>
<td>Low Frequency</td>
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<td>LNA</td>
<td>Low Noise Amplifier</td>
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<td>LO</td>
<td>Local Oscillator</td>
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<td>LS</td>
<td>Large Signal</td>
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<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<td>NB</td>
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<td>NBH</td>
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<td>NQS</td>
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<td>OIP3</td>
<td>Output Third-Order Intercept Point</td>
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<td>PA</td>
<td>Power Amplifier</td>
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<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
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<td>PLL</td>
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<td>PMOSFET</td>
<td>P-type MOS Field Effect Transistor</td>
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<td>PSD</td>
<td>Power Spectral Densities</td>
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<td>PSS</td>
<td>Periodic Steady State</td>
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<td>QPSK</td>
<td>Quaternary Phase Shift Keying</td>
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<td>RAM</td>
<td>Random access memory</td>
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<td>RF</td>
<td>Radio Frequency</td>
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<td>SBD</td>
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<td>SDRAM</td>
<td>Synchronous Dynamic Random Access Memory</td>
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<td>SGHE</td>
<td>Secondary Generated Hot Electron</td>
</tr>
<tr>
<td>SHE</td>
<td>Substrate Hot Electron</td>
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<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
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<td>SOC</td>
<td>System on Chip</td>
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<td>SOI</td>
<td>Silicon-on- Insulator</td>
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<td>SS</td>
<td>Small Signal</td>
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<td>SSB</td>
<td>Single-Side Band</td>
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<td>TDDB</td>
<td>Time Dependent Dielectric Breakdown</td>
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<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
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<td>VIP3</td>
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CHAPTER ONE: INTRODUCTION

1.1 Motivation

With continuous downscaling of device geometry and increasing demands for high performance, the two major reliability issues - gate oxide breakdown (BD) due to high vertical field in the oxide and hot carriers (HCs) because of high lateral field in short-channel MOSFETs [1] - [3], become even more important. Oxide breakdown and hot carriers result in performance degradation in RF circuits [4] - [7]. On the other hand, with the smaller dimensions for improving speed and functionality, each successive generation of transistors, which dissipates larger mount of power and results in heat flux to the ambient, requires sophisticated thermal management for reliability. High performance integrated circuit can have hot spots leading to large temperature gradients across a chip. Using the MEDICI simulation, the temperature at the gate-drain opening for the bulk devices was estimated 315 K [8]. For the silicon-on-insulator devices, the simulated temperature was up to 550 K. The net result is pattern dependent dispersion in the activation of NBTI processes and negative bias temperature instability (NBTI) drifts. If care is not taken to understand these issues, timing degradation dependent paths can lead to accelerated circuit failures during burn-in or field operations. Detection of these failures may become difficult due to circuit complexity and hence lead to erroneous data or output conditions. NBTI is one of the major temperature-induced reliability issues for p-channel MOSFET, which is caused by the interface traps under high temperature and negative gate voltage bias.
Even though much is known about the HC, BD and NBTI effects on the device dc characteristics, little is understood of the interaction of NBTI with BD and HCI, and the impact on RF performance, such as noise and linearity. The practical dynamic stress on the RFICs is first investigated here. An impact and accurate model to evaluate the RF performance in circuits is necessary.

1.2 Research Goals

The research presented here focuses on the following issues:

1. Reliability Issues in the deep submicron devices
2. Modeling the MOSFETs’ degradations
3. Mixed HC, BD, and NBTI effects on RF performance degradation on MOSFETs.
4. Performance degradation in MOSFETs RFIC, including LNA, mixer, VCO, PA, and buffer amplifier
5. HC and BD effects on the RF performance of 60 nm high-k dielectrics CMOS devices and circuits

1.3 Outlines

Chapter 2 presents the basic voltage and temperature stress-induced reliability issues – HC, BD, and NBFI in MOSFETs. The RF performance degradation in devices is given in chapter 3. Analytical analysis to relate the performance to device parameters for the LNA, PA, mixer, and VCO is presented in the beginning of chapter 4. Then, the RFIC performance degradation is
given. In chapter 5, the stress induced performance degradations in 60 nm high-k dielectrics CMOS devices and circuits, are described. Chapter 6 gives the conclusions.
2.1 BSIM Models

BSIM is a physics-based, accurate, scalable, robustic and predictive MOSFET SPICE model for circuit simulation and CMOS technology development. It is developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. The third iteration of BSIM3 was established by SEMATECH as the first industry-wide standard of its kind in December of 1996. BSIM3v3 has since been widely used by most semiconductor and IC design companies world-wide for device modeling and CMOS IC design. It is a consortium of semiconductor companies and simulator vendor world-wide promoting BSIM3v3 development as the industry standard compact model [9]. The Bsim model will be adopted as the basic model for our devices.

2.2 Equivalent Circuit Model

The increasing importance to improve the reliability of circuits makes it necessary to evaluating the performance degradation due to these effects during the RFIC design phase before fabrication. Therefore, a compact model to predict the stressed MOS transistor behaviors accurately is important. The BSIM3v3 models are extracted from DC characteristics and does not account for the gate leakage current – the significant indicator of BD. Based on [7], a model,
which represents the stressed device behaviors, is developed and shown in Fig. 1. The equivalent circuit includes the terminal resistances ($R_g$, $R_d$, $R_s$), substrate network equivalent resistances ($R_{db}$, $R_{sb}$, $R_{dsb}$), junction capacitances ($C_{db}$, $C_{sb}$), and two inter-terminal resistances ($R_{gd}$, $R_{gs}$). The intrinsic transistor is a BSIM3v3 model, which is extracted from the fresh or stressed devices using BSIMpro at different temperatures. Agilent 4156B is used as the $I$-$V$ meter. $R_{gs}$ and $R_{gd}$ are used to account for equivalent resistances between the gate and the source and between the gate and the drain, respectively. The resistances come from the resistor-like behaviors for post-hard breakdown MOSFETs. They are extracted from the $I_g$-$V_g$ curve of the stressed device. Other parameters – $C_{gs}$, $C_{gd}$, $R_g$, $R_d$, $R_s$, $C_{db}$, $R_{ds}$, $R_{dsb}$ are extracted from $Y$-parameters that were converted from measured $S$-parameters. $R_{bsd}$ and $C_{sb}$ are obtained by optimizing the entire model to fit measured $S$-parameters. In the BSIM3v3 model, the parameters are temperature dependent.

![Diagram](image)

Figure 2.1: Improved Model for RF simulation.

Other parameters are extracted from $Y$-parameters that were converted from measured $S$-
parameters. The details are given in Appendix I. Parameter extraction is given as:

\[ C_{gs} = \frac{\text{Im}(Y_{11})}{\omega} \]  
(5)

\[ C_{gd} = \frac{\text{Im}(Y_{12})}{\omega} \]  
(6)

\[ C_{gs} = C_{gg} - C_{gd} \]  
(7)

\[ C_{db} \approx C_{sb} = \frac{\text{Im}(Y_{22} - Y_{12})}{\omega} \]  
(8)

\[ R_g = \frac{\text{Im}(Y_{21}) - \omega C_{gd}}{\omega g_m C_{gg}} \]  
(9)

\[ R_d = \frac{\text{Re}(Y_{12}) + \omega^2 C_{gs} C_{gd} R_g + 1/R_{gd}}{\omega^2 (C_{gd} + C_{db}) C_{gd}} \]  
(10)

\[ R_s = \frac{\text{Re}(Y_{11}) - 1/R_{gs} - 1/R_{gd} - C_{gs}^2 \omega^2 R_g - C_{gs}^2 \omega^2 R_g}{\omega^2 C_{gs}^2} \]  
(11)

\[ R_{bsd} \text{ and } C_{sb} \] are obtained by optimizing the entire model to fit measured Y-parameters.

2.3 On-Wafer Structure Design and Measurement

The standard “open” deembedding method was first proposed in 1987 and employs a technique in which the pad capacitance is accounted for and calibrated by using an “OPEN” test structure (i.e., no transistor). Several other deembedding methods were subsequently proposed, and which use additional test structures (including the “SHORT” and “THROUGH,” etc.) to calibrate both the pad and interconnect parasitic in the device-under-test (DUT).

The current industry paradigm is the so-called “open–short” standard. However, since this approach assumes lumped-component approximations, it begins to lose accuracy as the
frequency increases above approximately 30 GHz. For more robust-parameter extraction, several high-frequency deembedding techniques have been recently proposed [6], [7]. These methods either use equivalent two-port analysis (with cascade, series, or parallel structures) or complicated equivalent circuit models, which simplify the parasitic under suitable approximations (e.g., the cascade structure neglects the parasitic feedback from the output to input).

To generalize the problem and avoid the potential inaccuracy caused by the above assumptions or simplifications, a four-port system calibration methodology was introduced by Rizzoli et al. for noise analysis [8]. As shown in [8] and [9], any two-port measurement can be modeled as a four-port system, which captures all of the parasitics surrounding the intrinsic device (Fig. 1). Once the 4x4 matrix of the system is solved, the intrinsic parameters can be accurately extracted. However, the 4x4 matrix was solved either using equivalent-circuit [8], [9] or electrical magnetic (EM) simulations, together with additional calibration [10]. Clearly, the accuracy of such methods depends on the validity of the lumped or distributive model.
Figure 2.2: Device under test and surrounding deembedding structures.
CHAPTER THREE: DEVICE RELIABILITY

3.1 Introduction

With the smaller dimensions for each successive generation of transistors for improving speed and functionality, the power dissipation, which results in heat flux to be removed to the ambient, required development of thermal management for reliability. High performance silicon-on-insulator (SOC) can have hot spots in a circuit design leading to large temperature gradients across a chip. Using MEDICI simulation, the temperature at the gate-drain opening for the bulk devices was estimated to be 315 K [1]. While for the SOC devices, the simulated temperature was up to 550 K. The net result is pattern dependent dispersion in the activation of negative bias temperature instability (NBTI) processes and NBTI drift. If care is not taken to understand these issues, timing degradation dependent paths can lead to accelerated circuit failures during burn-in or field operations. Detection of these failures may become difficult due to circuit complexity and hence lead to erroneous data or output conditions. NBTI is one of the major temperature-induced reliability issues for p-channel MOSFET, which is caused by the interface traps under high temperature and negative gate voltage bias. Beside the NBTI effects, the pMOS transistors in real circuits also suffer from the gate oxide breakdown (BD) due to high vertical electrical field in the oxide and the hot carriers injection (HCI) because of high lateral electrical field in short-channel MOSFETs [2]-[6]. Increased temperature accelerates the combined NBTI, BD and HCI degradation significantly in our test transistors. Consequently the RF performance degradation in circuits follows.
3.1.1 Hot Carrier Effects

The term 'hot carriers' refers to either holes or electrons (also referred to as 'hot electrons') that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor (especially MOS) device. Because of their high kinetic energy, hot carriers can get injected and trapped in areas of the device where they shouldn't be, forming a space charge that causes the device to degrade or become unstable. The term 'hot carrier effects', therefore, refers to device degradation or instability caused by hot carrier injection.

There are four commonly encountered hot carrier injection mechanisms. These are 1) the drain avalanche hot carrier injection; 2) the channel hot electron injection; 3) the substrate hot electron injection; and 4) the secondary generated hot electron injection. The drain avalanche hot carrier (DAHC) injection, as shown in Fig. 2.1, is said to produce the worst device degradation under normal operating temperature range. This occurs when a high voltage applied at the drain under non-saturated conditions ($V_D > V_G$) results in very high electric fields near the drain, which accelerate channel carriers into the drain's depletion region. Studies have shown that the worst effects occur when $V_D = 2V_G$. The acceleration of the channel carriers causes them to collide with Si lattice atoms, creating dislodged electron-hole pairs in the process. This phenomenon is known as impact ionization, with some of the displaced electron-hole (e-h) pairs also gaining enough energy to overcome the electric potential barrier between the silicon substrate and the gate oxide. Under the influence of drain-to-gate field, hot carriers that surmount the substrate-gate oxide barrier get injected into the gate oxide layer where they are sometimes trapped. This hot carrier injection process occurs mainly in a narrow injection zone at the drain end of the device where the lateral field is at its maximum. Hot carriers can be trapped at the Si-SiO$_2$ interface (hence referred to as 'interface states') or within the oxide itself, forming a space charge (volume charge) that increases over time as more charges are trapped. These trapped charges shift some of the characteristics of the device, such as its threshold voltage ($V_{th}$) and its conveyed conductance ($g_m$). Injected carriers do not get trapped in the gate oxide become gate current. On the other hand, majority of the holes from the e-h pairs generated by impact ionization flow back to the substrate, comprising a large
portion of the substrate's drift current. Excessive substrate current may therefore be an indication of hot carrier degradation. In gross cases, abnormally high substrate current can upset the balance of carrier flow and facilitate latch-up. Channel hot electron (CHE) injection occurs when both the gate voltage and the drain voltage are significantly higher than the source voltage, with $V_G \approx V_D$. Channel carriers that travel from the source to the drain are sometimes driven towards the gate oxide even before they reach the drain because of the high gate voltage. Substrate hot electron (SHE) injection occurs when the substrate back bias is very positive or very negative, i.e., $|V_B| >> 0$. Under this condition, carriers of one type in the substrate are driven by the substrate field toward the Si-SiO$_2$ interface. As they move toward the substrate-oxide interface, they further gain kinetic energy from the high field in surface depletion region. They eventually overcome the surface energy barrier and get injected into the gate oxide, where some of them are trapped. Substrate hot electron (SHE) injection occurs when the substrate back bias is very positive or very negative, i.e., $|V_B| >> 0$. Under this condition, carriers of one type in the substrate are driven by the substrate field toward the Si-SiO$_2$ interface. As they move toward the substrate-oxide interface, they further gain kinetic energy from the high field in surface depletion region. They eventually overcome the surface energy barrier and get injected into the gate oxide, where some of them are trapped. Secondary generated hot electron (SGHE) injection involves the generation of hot carriers from impact ionization involving a secondary carrier that was likewise created by an earlier incident of impact ionization. This occurs under conditions similar to DAHC, i.e., the applied voltage at the drain is high or $V_D > V_G$, which is the driving condition for impact ionization. The main difference, however, is the influence of the substrate's back bias in the hot carrier generation. This back bias results in a field that tends to drive the hot carriers generated by the secondary carriers toward the surface region, where they further gain kinetic energy to overcome the surface energy barrier. Hot carrier effects are brought about or aggravated by reductions in device dimensions without corresponding reductions in operating voltages, resulting in higher electric fields internal to the device. Problems due to hot carrier injection therefore constitute a major obstacle towards higher circuit densities. Recent studies have even shown that voltage reduction alone will not eliminate hot carrier effects, which were observed to manifest even at reduced drain voltages, e.g., 1.8 V. Thus, optimum design of devices to minimize, if not
prevent, hot carrier effects is the best solution for hot carrier problems. Common design techniques for preventing hot carrier effects include: 1) increase in channel lengths; 2) n+ / n-double diffusion of sources and drains; 3) use of graded drain junctions; 4) introduction of self-aligned n-regions between the channel and the n+ junctions to create an offset gate; and 5) use of buried p+ channels. Hot carrier phenomena are accelerated by low temperature, mainly because this condition reduces charge detrapping.

Figure 3.1: Mechanisms of Hot Carrier Effects. (a) DAHC injection involves impact ionization of carriers near the drain area; (b) CHE injection involves propelling of carriers in the channel toward the oxide even before they reach the drain area; (c) SHE injection involves trapping of
carriers from the substrate; (d) SGHE injection involves hot carriers generated by secondary carriers.

3.1.2 Breakdown

Oxide Breakdown refers to the destruction of an oxide layer (usually silicon dioxide or SiO2) in a semiconductor device. Oxide layers are used in many parts of the device: as gate oxide between the metal and the semiconductor in MOS transistors, as dielectric layer in capacitors, as inter-layer dielectric to isolate conductors from each other, etc. Oxide breakdown is also referred to as 'oxide rupture' or 'oxide punch-through.

Oxide breakdown has always been of serious reliability concern in the semiconductor industry because of the continuous trek towards smaller and smaller devices. As other features of the device are scaled down, the oxide thickness must be reduced. Oxides become more vulnerable to the voltages as they get thinner. The thinnest oxide layers today are already less than 50 angstroms thick. An oxide layer can break down instantaneously at 8-11 MV per cm of thickness, or 0.8-1.1 V per angstrom of thickness.

Oxide breakdowns may be classified as one of the following: 1) EOS/ESD-induced dielectric breakdown; 2) early-life dielectric breakdown; 3) time-dependent dielectric breakdown (TDDB). The first classification is self-explanatory, referring merely to oxide destruction due to the application of excessive voltage or current to the device.

Early-life and time-dependent dielectric breakdowns are technically the same failure mechanism, except that the former involves a breakdown that occurs early in the life of the device (say, within the first 2 years of normal operation), while the latter involves a breakdown
that occurs after a longer time of use (mainly in the 'wear-out' stage). Both categories involve
destruction of the dielectric while under normal bias or operation.

Early life and time-dependent dielectric breakdowns are primarily due to the presence of
weak spots within the dielectric layer arising from its poor processing or uneven growth. These
weak spots or dielectric defects may be caused by: 1) the presence of mobile sodium (Na) ions in
the oxide; 2) radiation damage; 3) contamination, wherein particles or impurities are trapped on
the silicon prior to oxidation; and 4) crystalline defects in the silicon such as stacking faults and
dislocations.

The risk of dielectric breakdown generally increases with the area of the oxide layer,
since a larger area means the presence of more defects and greater exposure to
contaminants. The worse cases of oxide defects are the ones that result in early life dielectric
breakdowns. It must be pointed out, however, that even very high quality oxides can suffer
breakdown with time, especially in the 'wear-out' period of its lifetime. This latter case is the
classic 'TDDB' mechanism.

Previous studies have shown that SiO$_2$ TDDB is a charge injection mechanism, the
process of which may be divided into 2 stages - the build-up stage and the runaway
stage. During the build-up stage, charges invariably get trapped in various parts of the oxide as
current flows in the oxide. The trapped charges increase in number with time, forming high
electric fields (electric field = voltage/oxide thickness) and high current regions along the
way. This process of electric field build-up continues until the runaway stage is reached. During
the runaway stage, the sum of the electric field built up by charge injection and the electric fields
applied to the device exceeds the dielectric breakdown threshold in some of the weakest points
of the dielectric. These points start conducting large currents that further heat up the dielectric,
which further increases the current flow. This positive feedback loop eventually results in electrical and thermal runaway, destroying the oxide in the end. The runaway stage happens in a very short period of time.

The presence of defects in the dielectric greatly reduces the time needed to transition from the build-up to the runaway stage. These defects actually have the effect of 'thinning' down the oxide where they are located, since they are occupying space that should have been occupied by the dielectric. The effective electric field is higher in these thinned-out areas compared to defect-free areas for any given voltage. This is why it takes a lower voltage and shorter time to break down the dielectric at its defect points.

3.1.3 Negative Bias Temperature Instability

Under high negative gate voltage bias in pMOSFETs at elevated temperature-NBTI stress, the electrochemical reaction at Si-SiO2 interface is:

\[
\text{Si-H} + \text{O}_3\text{-Si-O-Si} + h^+ \leftrightarrow \text{Si} + \text{O}_3\text{-Si-OH}^+\text{-Si}
\]  

The interface state (Si-) is generated from the dissociation of hydrogen terminated trivalent Si bonds (Si-H) by holes (h+) in the Si inversion layer. The released hydrogenated species (H+) diffuse and are trapped near the oxide interface resulting in the positive oxide charges (Si-OH+-Si). Experiments show that the positively charged hydrogen (H+) reacts with the SiO2 lattice to form an OH group bonded to an oxide atom, leaving a trivalent Si atom (Si\text{0+}) in the oxide and one trivalent Si at the Si surface. The Si\text{0+} forms the fixed positive charge (Nf) and the Si forms the interface trap (Nit). NBTI stress causes Nit and Nf shifts, contributing mainly to the shift in device characteristics. The Nit and Nf shifts are given by:
\[ \Delta N_{it}(E_{ox}, T, t, t_{ox}) = 9 \times 10^{-4} E_{ox}^{1.5} t^{0.25} \exp(-0.2 / kT) / t_{ox} \]

(2.2)

\[ \Delta N_f(E_{ox}, T, t) = 490 E_{ox}^{1.5} t^{0.14} \exp(-0.15 / kT) \]

(2.3)

where \( E_{ox} \) is the electric field in the oxide, \( T \) is the temperature, \( t \) is the stress time, \( t_{ox} \) is the oxide thickness, and \( k \) is Boltzmann’s constant. The shift of threshold voltage is:

\[ \Delta V_{th}(\Delta N_{it}, \Delta N_f) = B_1 [1 - \exp(-t / \tau_1)] + B_2 [1 - \exp(-t / \tau_2)] \]

(2.4)

where \( B_1 \) and \( B_2 \) relate to \( \Delta N_{it} \) and \( \Delta N_f \), \( \tau_1 \) and \( \tau_2 \) are the reaction limiting time constants. The channel mobility degradation (\( \Delta \mu \)) also depends on the interface traps.

The NBTI induced \( N_{it} \) and \( N_f \) shifts cause the change in device characteristics, as well as the performance degradation. The degradation is thermally activated (See Eqs. (2) and (3)) and, therefore, is sensitive to temperature. It degrades severely under higher temperature.

Companying with NBTI under high gate voltage bias and temperature, hydrogen release, hole injection and thermo-chemical electric field create defects in the oxide and likely trigger breakdown. On the other hand, constant high voltage at the drain terminal in real pMOS devices can also result in another reliability issue - hot carrier effects. The carriers accumulate sufficient energy to surmount the Si-SiO\(_2\) surface and enter the oxide. The injected carriers enhance the interface state generation and increase the NBTI sensitivity.

### 3.1.4 Dynamic and Static Stress

It showed that dynamic stress with 25 MHz inverter-like voltage stress on the gate and the drain provided more degradation than a quasi-static sum of DC stresses [12], [13]. It was further claimed that the falling gate voltage, not the rising edge, is responsible for the performance degradation [14], [15]. Increasing frequency also led to more degradation and the maximum
damage was attained at frequencies in the range of 1 – 100 MHz [16] - [18]. At very high frequencies, the damage from dynamic stress drops significantly [18]. In the case of dynamic stress, the degradation due to inverter-like voltage stress on both gate and drain contacts is smaller than that of AC gate voltage stress with a fixed drain voltage [17]. The dynamic stress induced degradation is frequency dependent [12] - [18]. In the range of kHz or tens MHz, the damage from AC stress attains the maximum [12] - [14]. While at high frequencies, it drops significantly [17], [18], [19], [20]. In other words, a threshold frequency divides the stress frequency into two regimes: the low-frequency regime where the degradation rate is large and the high-frequency regime where the degradation is small.

3.2 Effects on Device Models

The model parameter shifts due to voltage and temperature stresses have been studied in [4] - [7], [21], [22]. Two mechanisms are traditionally suggested as key to the degradation of MOS devices by stresses [10], [11]. One involves the oxide-trapped charge, and the other is the generation of interface-states. As MOS devices shrink and gate oxide thickness is reduced, oxide-trapped charge more likely occurs in deep submicron devices because channel hot carriers reach velocity saturation easily, thus increasing the possibility of band-to-band tunneling [19]. Literature suggests both electrons and holes can be trapped in the oxide layer under different stress conditions [20], [27]. Measuring the shift in the threshold voltage after hot carrier stress is the most convenient way to identify which carriers are trapped in the oxide during stress. In N-MOSFETs, the threshold voltage increases after hot carrier stress if electrons are trapped, and decreases after hot carrier stress if holes are trapped.
Under high negative gate voltage bias in pMOSFETs at elevated temperature-NBTI stress, the electrochemical reaction at Si-SiO$_2$ interface is [28]:

$$\text{Si-H} + \text{O}_2^{-}\text{Si-O-Si} + h^+ \leftrightarrow \text{Si} + \text{O}_2^{-}\text{Si-OH}^+ - \text{Si}$$

(3.1)

The interface state ($\text{Si}^-$) is generated from the dissociation of hydrogen terminated trivalent Si bonds (Si-H) by holes ($h^+$) in the Si inversion layer. The released hydrogenated species (H$^+$) diffuse and are trapped near the oxide interface resulting in the positive oxide charges (Si-OH$^+$-Si). Experiments show that the positively charged hydrogen (H$^+$) reacts with the SiO$_2$ lattice to form an OH group bonded to an oxide atom, leaving a trivalent Si atom (Si$_{ox}^+$) in the oxide and one trivalent Si$_s$ at the Si surface. The Si$_{ox}^+$ forms the fixed positive charge ($N_f$) and the Si$_s$ forms the interface trap ($N_{it}$). NBTI stress causes $N_{it}$ and $N_f$ shifts, contributing mainly to the shift in device characteristics. The $N_{it}$ and $N_f$ shifts are given by:

$$\Delta N_{it}(E_{ox}, T, t, t_{ox}) = 9 \times 10^{-4} E_{ox}^{1.5} t^{0.25} \exp(-0.2 / kT) / t_{ox}$$

(3.2)

$$\Delta N_f(E_{ox}, T, t) = 490 E_{ox}^{1.5} t^{0.14} \exp(-0.15 / kT)$$

(3.3)

where $E_{ox}$ is the electric field in the oxide, $T$ is the temperature, $t$ is the stress time, $t_{ox}$ is the oxide thickness, and $k$ is Boltzmann’s constant. The shift of threshold voltage is:

$$\Delta V_{th}(\Delta N_{it}, \Delta N_f) = B_1[1 - \exp(-t / \tau_1)] + B_2[1 - \exp(-t / \tau_2)]$$

(3.4)

where $B_1$ and $B_2$ relate to $\Delta N_{it}$ and $\Delta N_f$ [7], $\tau_1$ and $\tau_2$ are the reaction limiting time constants. The channel mobility degradation ($\Delta \mu$) also depends on the interface traps.

The NBTI induced $N_{it}$ and $N_f$ shifts causes the change in device characteristics, as well as the performance degradation. The degradation is thermally activated (See Eqs. (3.2) and (3.3)) and, therefore, is sensitive to temperature. It degrades severely under higher temperature [28].
Companying with NBTI under high gate voltage bias and temperature, hydrogen release, hole injection and thermo-chemical electric field create defects in the oxide and likely trigger breakdown. On the other hand, constant high voltage at the drain terminal in real pMOS devices can also result in another reliability issue - hot carrier effects. The carriers accumulate sufficient energy to surmount the Si-SiO₂ surface and enter the oxide. The injected carriers enhance the interface state generation and increase the NBTI sensitivity.

MOSFET devices under voltage and temperature stresses suffer from the hot carrier, BD, and NBTI effects. The parameter shifts due to these effects degrade the RF performance in MOSFETs.

3.3 Effects on RF Performances in Devices

3.3.1 Analysis

The main figures of merit (FOMs) in MOSFET devices are cutoff frequency and maximum frequency, linearity performance and noise figure. The FOMs relate to the model parameters of devices, which will be changed due to voltage and temperature stresses. Therefore, the alternatives of FOMs are anticipated.

3.3.1.1 Cutoff Frequency and Maximum Frequency

In the high-frequency performance, two figures of merit are particularly popular - the cutoff frequency \( (f_T) \) and maximum frequency \( (f_{\text{max}}) \). They are the frequencies at which the
current and power gain are extrapolated to fall to unity, respectively. The cutoff frequency and maximum frequency are given as:

\[ f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \] (3.5)

\[ f_{\text{max}} = \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + g_{ds} R_{in}}} \] (3.6)

It is clear that the cutoff frequency and maximum frequency depend on the transconductance terminal resistances and parasitic capacitances.

### 3.3.1.2 Linearity

Analysis of MOSFETs linearity to relate the linearity performance with the device parameters is useful. Taking into account the velocity saturation effect, the drain current of the MOSFET in the saturation region is given by

\[ I = W C_{ox} v_{sat} \frac{(V_{gs} - V_{th})^2 \mu_0}{(V_{gs} - V_{th})(\mu_0 + 2L v_{sat} \theta) + 2L v_{sat}} \] (3.7)

where \( C_{ox} \) is the gate oxide capacitance per area, \( v_{sat} \) is the saturation velocity, \( V_{gs} \) is the gate-source voltage, \( \mu_0 \) is the mobility, \( \theta \) is the mobility degradation factor, and \( W \) and \( L \) are the channel width and length, respectively.

Without considering the memory effect in a weak nonlinear application, the drain current \( I_d \) as a function of \( v_{gs} \) in Taylor series is

\[ I_d = T_0 + T_1 v_{gs} + T_2 v_{gs}^2 + T_3 v_{gs}^3 + T_4 v_{gs}^4 + T_5 v_{gs}^5 + \ldots \] (3.8)

where

\[ T_i = \frac{1}{i!} \frac{\partial^i I_d}{\partial V_d^i} \] (3.9)
and \( V_d = V_{gs} - V_{th} \). Usually, the coefficient \( T_1 \) is seen as the transconductance of transistors. High-order coefficients are introduced by the transistor nonlinearity. The third harmonic intercept voltage (VIP3) is used as a criterion for linearity

\[
V_{ip3}(dBV) = 10 \log \left( \frac{4T_1}{T_3} \right)
\]

(3.10)

If the distortion components are small enough in applications such as low noise amplifiers (LNAs), the Taylor expansion is a simple way to describe the linearity of MOSFETs. Considering the input impedance components, gate-source capacitance, and feedback component through gate-drain capacitance at high frequency, the Taylor expansion, which is based on the coefficients derived from \( I-V \) characteristics, becomes inappropriate. The Volterra series is then employed to analyze the device linearity with two-tone input signals. Typical examples are mixers. The Volterra series gives

\[
i_0 = A_1(s)v_m + A_2(s_1, s_2)v_m^2 + A_3(s_1, s_2, s_3)v_m^3 + \ldots
\]

(3.11)

where \( s(= j\omega) \) is the Laplace variable. \( s_1 = j\omega_1, s_2 = j\omega_2, s_3 = -j\omega_2, \omega_1 \) and \( \omega_2 \) are the angular frequencies of two-tone input, and \( \omega = \omega_1 \approx \omega_2 \). These coefficients are a function of \( g_{m0}, C_{gs} \), operation frequency \( \omega \), and other circuit components. From (5) and using KCL at the small-signal model, we can obtain the coefficients \( A_1(s), A_2(s_1, s_2) \) and \( A_3(s_1, s_2, s_3) \). This is given in Appendix. VIP3 using the Volterra series is

\[
V_{ip3}(dBV) = 10 \log \left( \frac{4 |A_1(s)|}{|A_3(s_1, s_2, s_3)|} \right)
\]

(3.12)

For a short-channel MOSFET, however, the output conductance is also an important nonlinear source and must be included in the analysis at high frequencies. The third-order intermodulation current caused by the transconductance and output-conductance nonlinearities is
approximated as [29]:

\[ i_{d,3} = \frac{3}{4} \left[ g_{m3} + \frac{g_{d3}^2 g_m}{(g_d + 1/R_{load})^3} \right] \frac{V^3}{1 + g_d R_{load}} \]  \hspace{1cm} (3.13)

where \( R_{load} \) is the load resistance. \( V \) is the fundamental voltage amplitude at the gate. The fundamental voltage amplitude at drain is given by

\[ v_{ds} = \frac{g_m R_{load}}{1 + g_d R_{load}} V \]  \hspace{1cm} (3.14)

The load resistance \( R_{load} = 50 \ \Omega \) is used at the device drain terminal in the analysis and simulation below.

3.3.1.3 Noise

To understand the noise behavior, a single MOSFET can be considered as a small circuit with different resistive, capacitive, and active components as we have seen in Fig. 1. Different noise sources exist in a MOS transistor with their power spectral densities (PSDs) (cf. Fig. 1), including (1) terminal resistance thermal noise at the gate, source, and drain; (2) thermal noise and the flicker noise in the channel; (3) substrate resistance thermal noise, and (4) induced gate noise.

Analysis of MOSFETs noise to relate the performance with the device parameters is useful. Taking into account the terminal resistors, the minimum noise figure of the MOSFET in the saturation region is given by

\[ NF_{\text{min}} = 1 + 2 \pi K_f f (C_{gs} + C_{gd})(R_G + R_s)^{1/2} / g_m^{1/2} \]  \hspace{1cm} (3.15)

where \( g_m \) is the transconductance, \( f \) is the operation frequency, \( K_f \) is FuKui factor, \( C_{gs} \) and \( C_{gd} \) are gate-source and gate-drain capacitances, respectively; \( R_G \) and \( R_S \) are gate and source equal
resistances, respectively.

The noise figure with input source impedance \((G_s + jB_s)\) is

\[
NF = NF_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2 \right]
\]  

(3.16)

where \(R_n\) is the noise resistance, \(G_{\text{opt}}\) and \(B_{\text{opt}}\) are the real and image part of the optimum source admittance, respectively. They are given as:

\[
R_n = \frac{g_{d0}}{[g_m - \omega^2 C_{gd} C_{gg} R_g - \omega^2 (C_{gd} + C_{db}) C_{gd} R_d]^2 + \omega^2 (C_{gd} + g_m C_{gg} R_g)^2 + R_g}  
\]  

(3.17)

\[
G_{\text{opt}} = \omega C_{gs} \sqrt{\frac{\delta (1 - |c|^2)}{5g_{d0}^2 (1 + \omega C_{gs} R_g)^2 g_m^2 + 5g_{d0} R_g}} \]  

(3.18)

\[
B_{\text{opt}} = -\omega C_{gs} (1 + |c| \sqrt{\frac{\delta}{5\gamma}}) \]  

(3.19)

where \(g_{d0}\) is the output-conductance, \(c\) \(( \approx 0.395j \)\) is the correlation coefficient, \(\delta\) is the coefficient of gate noise, \(\gamma\) is the coefficient of channel current noise. For long-channel devices, the value of \(2/3\) holds when the device is saturated, and the value of one is valid when the drain-source voltage is zero. For short-channel devices, however, \(\gamma\) is much greater than \(2/3\) in saturation region.

These equations include the effects of terminal resistances and give an indication of the impact of parameters on the HF noise performance. One can see that the HF noise performance of MOSFETs relates to \(C_{gs}, C_{gd}, g_m, g_d,\) and the terminal poly-silicon resistances. They are the key components determining the HF noise characteristics of the NMOSFETs. The next section presents the experimental results of these parameters before and after stress. Most of them shift...
significantly after stress. Therefore, the degradation of the HF noise performance in NMOSFETs is expected.
(b)
Figure 3.2. (a) Threshold voltage degradation versus time; (b) Mobility degradation versus time; (c) $I$-$V$ characteristics for fresh (□), NB stress (x), and NBH stress (Δ). (marks: measurement, lines: simulation).

All stresses were performed at 400 K. The stress time is 7200 seconds; (d) Transconductance versus gate source voltage for fresh (▽), NB stress (◇), and NBH stress (□). (marks: measurement, lines: simulation).

All stresses were performed at 400 K. The stress time is 7200 seconds. $V_{ds} = -1.5$ V.

### 3.3.2 Results

The study of RF linearity degradation was based on the nMOSFET BSIM3 models, which were extracted from devices using BSIMpro before and after stress. Agilent 4156B was
used as the I-V meter for BSIMpro. Stress conditions are described in Sec. III, and the stress time is 1000 seconds. In the extracted model files, many parameters were adjusted to represent the stressed device behaviors, including Vth0, K1, K2, K3, U0, Ua, Ub, Uc, Voff, NFactor, Cj, Cgdo, Cgso, etc. The simulated $I$-$V$ characteristics using these models are shown in Fig. 3.7. Measured $I$-$V$ characteristics are also given in the same figure to prove the accuracy of the models. Good agreement between the simulated and measured results is obtained.

As in Sec. II, the MOSFET input voltage has small perturbations around the bias point in weak nonlinear applications and the Volterra series analysis holds. The drain current shows considerable depression as a result of stress, as evidenced in Fig. 3.7. It is assumed that the dominant source of nonlinearity is the channel current $I_d$. The expression for $I_d$ and the load line trajectory determine the nonlinear operation of the MOSFETs. With a decrease in drain current after stress, the output power is decreased. The drain current has more compression in the linear region than in the saturation region. Therefore, the output power will be more depressed at low gate-source voltage biases than at high gate-source voltage biases. And the third-order intermodulation distortion (IM3) is smaller at low gate-source voltage biases. The output power and IM3 follow the shape of $|g_m|$ and $|g_{m3}|$.

IM3 and output power are shown in Fig. 3.8. The calculated values using the Volterra series analysis (lines) agree very well with the extracted data (marks) from measurement. In the context of the Volterra series, it is known that the distortion of MOSFETs comes from the nonlinear device parameters such as $C_{gd}$, $C_{ds}$, $g_m$, and $g_d$. 

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Figure 3.3. $I-V$ characteristics and load line. (△: fresh measurement; △: after stress measurement; line: simulation for fresh device; dash: simulation for device after stress).

The output power decreases after stress. When $V_{gs}$ is greater than 1.2 V, IM3 of the stressed device is greater than that of the fresh device. Therefore, one can predict a large distortion in this region. The simulated output power and IM3 versus input power is shown in Figs. 3.9 (a) and (b) at $V_{gs} = 0.8$ and 1.2 V, respectively. The two-tone input ($\omega_1 = 900$ MHz, $\omega_2 = 920$ MHz) is used in SpectreRF periodic steady-state (PSS) simulation. The supply voltage is 2.0 V and the load resistor is 50 Ω. The source and bulk are grounded. With –20 dBm input power. IM3 decreases by 1 dBm at $V_{gs} = 0.8$ V and 4 dBm at $V_{gs} =$1.2 V.

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The input impedance of MOSFETs is also a major source of nonlinearity at high frequencies. It consists of two major nonlinear components, $C_{gs}$ and $C_{gd}$. As presented in Section III, $C_{gs}$ changes significantly after stress, while $C_{gd}$ shows a slight change. The extracted third-order intercept point (IIP3) is shown in Fig. 3.9 (c). At low drain currents, the degradation of IIP3 is about 1 dBm ($I_d = 1.0 \text{ mA}$). And at high drain currents, the linearity degradation is larger (about 8 dBm at $I_d = 4.5 \text{ mA}$).

Figure 3.4. Calculated (lines) and extracted (marks. open marks: Fresh; closed marks: after stress) small signal output power and third-order IMD (IM3). $V_{gs} = 1 \text{ V}, V_{ds} = 1.5 \text{ V}$ and load resistor is 50 $\Omega$. NMOS ($W \times L = 10 \times 0.16 \mu\text{m}^2$) with source and bulk grounded. Input power = -10 dBm.
Figure 3.5. Simulated output power and IM3 versus input power at (a) $V_{gs} = 0.8$ V and (b) $V_{gs} = 1.2$ V. (open marks: fresh; closed marks: after stress); (c) Linearity of MOSFET versus drain current obtained from the extracted data of transconductance and output-conductance before and after stress. Here, a 50 Ω resistor is used as the output load.

For the noise performance, the valid extraction region is up to 10 GHz. The mean values from 1 GHz to 10 GHz are selected as the extracted parameters. After breakdown, a leakage path exists across the gate oxide, which adds another noise source to the transistor, thus degrading the noise performance. Also, the drastic increase in the gate current due to stress effects increases the real part of the complex input impedance. The immediate impact of such a change affects the impedance matching condition, which is critical for the NMOSFET noise performance. The
optimum noise conductance \( G_{opt} \) and susceptance \( B_{opt} \) are extracted using Eqns. (3.18) and (3.19) from the measured parameters. They change strongly due to the dynamic stress, as evidence in Fig. 3.10 (a) and (b). The equivalent noise resistance \( R_{n} \) does not shift significantly, as shown in Fig. 3.10 (c). Minimum noise figure \( NF_{min} \) relates to \( C_{gs}, C_{gd}, R_{g}, R_{s}, \) and \( g_{m} \). All the parameters shift after stress, as described in Sec. III. Therefore, the degradation of \( NF_{min} \) is expected. The extracted \( NF_{min} \) using Eqn. (3.20) is shown in Fig. 3.10 (d). Noise figure at 50 \( \Omega \) versus frequency before and after stress is given in Fig. 3.11 (a). It degrades significantly. The simulated results using the developed model are also shown in the same picture, there are good agreements between the extracted and simulated results from 1 GHz to 10 GHz. Because the parameter extraction is valid from 1 GHz to 10 GHz, the disagreement exists out of this range. The noise figures at 50 \( \Omega \) versus drain current were measured using Y-factor method with Alitech 6716 noise generator and HP 8560 RF spectrum analyzer. The results for fresh and stressed device are given in Fig. 3.11 (b). One can see that the noise figure decreases with the increasing drain current. The average degradation of noise figure is about 1 dB. Simulated results are also plot in the same figure.
Figure 3.6. Extracted noise parameters versus frequency before and after stress. (a) Normalized noise resistance; (b) Optimum noise conductance; (c) optimum noise susceptance; (d) Minimum noise figure.

Stress condition: 0 - 2.8 V inverter-like dynamic stress on NMOS (W×L = 20×0.16 μm2) for 2 hours.

Parameter measurement conditions: Source and bulk were grounded. Vgs = 0.86 and Vds = 1.5 V.
Figure 3.7. (a) Extracted and simulated noise figure @ 50 Ω versus frequency. (b) Measured and simulated noise figure @ 50 Ω versus drain current. Frequency is 900 MHz. marks: measurement, lines: simulation.
The cutoff frequency before and after stress is plotted as a function of DC gate voltage in Fig. 3.12. The cutoff frequency ($f_T$) reduced 20% approximately after dynamic stress. The degradation is mainly due to the shift of transconductance and overlap capacitances due to dynamic stress. The maximum frequency ($f_{\text{max}}$) is also shown in the same figure, it degraded significantly after AC stress. For our device ($L = 160$ nm), $f_{\text{max}} \sim g_m^{1/2}$, it degrades with the decrease of $g_m$ after AC stress.

![Figure 3.8. Cutoff-frequency versus gate-source voltage. Drain-source voltage is set at 1.5 V.](image-url)
CHAPTER FOUR: RF CIRCUIT DESIGN AND PERFORMANCE ANALYSIS

4.1 Introduction

The low noise amplifier function plays an important role in the receiver design. Its main function is to amplify extremely low signals without adding noise, thus preserving the required signal-to-noise ratio (SNR) of the system at extremely low power levels. Additionally, for large signal levels, the LNA amplifies the received signal without introducing any distortions, which eliminates channel interference. Proper LNA design is crucial in today’s communication technology. Because of the complexity of the signals in today’s digital communications, additional design considerations need to be addressed during an LNA design procedure.

Power amplifiers, also known as PAs, are used in the transmit side of RF circuits, typically to drive antennas. Power amplifiers typically trade off efficiency and linearity, and this tradeoff is very important in a fully monolithic implementation. Higher efficiency leads to extended battery life, and this is especially important in the realization of small, portable products. There are some additional challenges specifically related to being fully integrated. Integrated circuits typically have a limited power supply voltage to avoid breakdown, as well as a metal migration limit for current. Thus, simply achieving the desired output power can be a challenge. Power amplifiers dissipate power and generate heat, which has to be removed. Due to the small size of integrated circuits, this is a challenging exercise in design and packaging. Several recent overview presentations have highlighted the special problems with achieving high efficiency and linearity in fully integrated power amplifiers.
The purpose of the mixer is to convert a signal from one frequency to another. In a receiver, this conversion is from radio frequency to intermediate frequency. Mixing requires a circuit with a nonlinear transfer function, since nonlinearity is fundamentally necessary to generate new frequencies. If an input RF signal and a local oscillator signal are passed through a system with a second-order nonlinearity, the output signals will have components at the sum and difference frequencies. A circuit realizing such nonlinearity could be as simple as a diode followed by some filtering to remove unwanted components. On the other hand, it could be more complex, such as the double balanced cross-coupled circuit, commonly called the Gilbert cell. In an integrated circuit, the more complex structures are often preferred, since extra transistors can be used with little extra cost but with improved performance.

An oscillator is a circuit that generates a periodic waveform whether it be sinusoidal, square, triangular, or, more likely, some distorted combination of all three. Oscillators are used in a number of applications in which a reference tone is required. For instance, they can be used as the clock for digital circuits or as the source of the LO signal in transmitters. In receivers, oscillator waveforms are used as the reference frequency to mix down the received RF to an IF or to baseband. In most RF applications, sinusoidal references with a high degree of spectral purity (low phase noise) are required.

This chapter focuses on the performance degradation in these basic RFICs. Parameter shifts in devices have been studied in chapter 3. They induce the mismatching in the input or output for LNA or PA, decreasing gain in LNA, PA, and Mixer, alternating the tank capacitance in VCO, etc. In this chapter, the basic RF circuits, including low noise amplifier (LNA), power amplifier (PA), mixer, oscillator, and buffer, are analyzed first. The derived equations give the relationships between the performance of these RF circuits and device parameters. The
performance degradations due to voltage and temperature stresses are studied systematically through the developed model and Cadence Spectre-RF simulations. The future work, which focused on the performance degradation due to voltage stress in buffer, SiGe HBT VCO, and Gaas LNA, will be performed.

4.2 Analysis

4.2.1 Low Noise Amplifier

A folded low noise amplifier (LNA), as shown in Fig. 4.1, is used as an example to demonstrate the RF performance degradation subject to the NBH stress. The folded structure is for low-voltage design [45]. The cascade transistor M2 reduces the input capacitance and enables a good reverse isolation, hereby enhancing the stability. On the other hand, because M2 is placed between the supply and ground tail, it more likely suffers from the NBH effects. The devices used in the LNA simulation have 0.16 µm channel length. NMOS transistor has 10 fingers 20 µm each and pMOS transistor has 3 fingers 50µm each. The supply voltage is 1.5 V and the gate biasing of the device is consistent with the measurement condition for the model extraction. The extracted ‘fresh’ and ‘stressed’ models are used for each finger. For the ‘stressed’ model, the stress time is 2 hours.

The total noise figure is given by [46]
\[ NF = 1 + \frac{r_{gs} + r_g}{R_s} + \left\lbrace \alpha_1^2 |c|^2 \frac{\delta}{5 \gamma} \right\rbrace + (Q_L \alpha_1 |c| \sqrt{\frac{\delta}{5 \gamma}} + 1)^2 \]
\[ + (1 - |c|^2 \alpha_1^2 (1 + Q_L^2) \frac{\delta}{5 \gamma}) \frac{g_{ds01} \gamma}{g_{m1} R_s Q_L^2} \]
\[ + \frac{\alpha_2^2 C_{gs1}^2}{g_{d0}^2} \frac{\delta}{5 \gamma} + \frac{\alpha_2^2 C_{d1}}{(g_{m2} + g_{d0})^2} \frac{g_{ds02} (1 + Q_L g_{m1} L \omega_0)^2}{g_{m1}^2 R_s Q_L^2} \]
\[ + \frac{(g_{m2} + g_{d0})^2 + \alpha_2^2 C_{d1}^2}{(g_{m2} + g_{d0})^2} \frac{g_{ds02} (1 + Q_L g_{m1} L \omega_0)^2}{g_{m1}^2 R_s Q_L^2} \] (4.1)

Where \( C_{gs1} \) is the parasitic gate-source capacitance of transistor \( M_1 \), \( g_{ml} \) is the transconductance of \( M_1 \), \( R_s \) is the bias-dependent gate resistance. \( \beta, \gamma \) are Gate induced current noise factor and Channel current noise factor respectively. For long-channel model, \( \beta = 8/45, \gamma = 1 \); For short-channel model, they need to be modified slightly to include the effect of short-channel effects, \( \beta = 4/15 \) and \( \gamma = 2/3 \).

The gain is approximately equal to
\[ G = g_{m1} R_L \] (4.2)

Aside from exhibiting low noise performance and high gain, an LNA should provide sufficient linearity to minimize IM3 from interference in adjacent frequency bands. The total VIP3 performance (in V) of the LNA is expressed as:
\[ V_{IP3} = \left( \frac{1}{V_{IP3,1}} + \frac{G_1^2}{V_{IP3,2}} \right)^{-1/2} \] (4.3)

where \( V_{IP3,1} \) is VIP3 (in V) of M1, \( V_{IP3,2} \) is VIP3 (in V) of M2, \( G_1 \) is the voltage gain of the first stage.
Figure 4.1. Simplified folded low noise amplifier. $R1$ is 1 kΩ, $L1$, $L2$, and $L3$ are 0.5 nH, 2.8 nH, and 2.8 nH, respectively. $C1$ is the DC block. $C2$, $C3$, and $C4$ are 300 fF, 600 fF, and 600 fF, respectively. The sizes of M1 and M2 are 0.16×200 μm$^2$ and 0.16×150 μm$^2$, respectively. $Vdd$ is 1.5 V. The operation frequency is 5 GHz.

### 4.2.2 Power Amplifier

The simplified schematic of power amplifier under study is shown in Fig. 4.2. The supply voltage is 1.5 V and the gate bias is 0.86 V. It is operated in class-AB mode. The power supply is given by

$$P_{cc} = \frac{V_{cc} I_{cc}}{\pi} (\sin \theta - \theta \cos \theta)$$  \hspace{1cm} (4.4)

Efficiency for this maximum possible voltage swing is given by

$$\eta_{max} = \frac{2 \theta - \sin 2\theta}{4(\sin \theta - \theta \cos \theta)}$$  \hspace{1cm} (4.5)

The actual output power for an output peak voltage of $V_{op}$ can be found as a function of $\theta$:  

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\[ P_{\text{out}} = \frac{V_{\text{opt}} I_{\text{cc}}}{4\pi} (2\theta - \sin \theta) \]  

(4.6)

Figure 4.2. Schematic of PA

4.2.3 Mixer

The single-balanced Gilbert mixer includes two stages – transconductance or drive stage with a single transistor and a switching pair.

Figure 4.3. Schematic of single-balanced Gilbert mixer
The local oscillator signal is large enough to switch the tail current from one side to the other. In other words, the tail current is multiplied by the local oscillator wave. The conversion gain can be written as

\[ G_c = \frac{2}{\pi} g_{m3} R_L \]  \hspace{1cm} (4.7)

\( g_{m3} \) is the transconductance of M3, and \( R_L \) is the load resistance.

The total third harmonic intercept voltage is [47]

\[ V_{ip3}(dBV) = 10 \log \left( \frac{4 |C_1(s)|}{|C_3(s_1, s_2, s_3)|} \right) \]  \hspace{1cm} (4.8)

where \( C_1(s) \) and \( C_3(s_1, s_2, s_3) \) are Volterra coefficients that describe the total mixer distortion. \( s(= j\omega) \) is the Laplace variable. \( s_1 = j\omega_1, s_2 = j\omega_2, s_3 = -j\omega_2 \). \( \omega_1 \) and \( \omega_2 \) are the angular frequencies of two-tone input, and \( \omega = \omega_1 \approx \omega_2 \). \( C_1(s) \) and \( C_3(s_1, s_2, s_3) \) are given below:

\[ C_1(s) = A'_1(s)B'_1(s) \]  \hspace{1cm} (4.9)

\[ C_3(s) = A'_1(s_1, s_2, s_3)B'_1(s_1 + s_2 + s_3) + 2A'_1(s_1)A'_2(s_2, s_3)B'_2(s_1, s_2 + s_3) + A'_1(s_2)A'_2(s_1, s_3)B'_2(s_1, s_2, s_3) \]  \hspace{1cm} (4.10)

\( A'_1(s_1), A'_2(s_1, s_2), A'_3(s_1, s_2, s_3) \) and \( B'_1(s_1), B'_2(s_1, s_2), B'_3(s_1, s_2, s_3) \) are Volterra coefficients that describe the distortion of transconductance and switching stages, respectively. These coefficients are a function of transconductance, parasitic capacitances, operation frequency \( \omega \), and other circuit components.

The single-sideband (SSB) noise figure for the Gilbert is [48]

\[ NF_{SSB} = \frac{\alpha}{c_2} + \frac{2\alpha g_m3(\gamma_3 + R_g3g_m3) + 4\gamma_1G + 4R_gG^2 + 1/ R_L}{c_2g_m3^2R_g} \]  \hspace{1cm} (4.11)
where $\alpha$ is the coefficient of PSD in M3. $c$ is the fitting factor for conversion gain. $\gamma_1$ and $\gamma_3$ are the coefficients of channel current noise in M1 and M2, $R_{g1}$ and $R_{g3}$ are the gate resistances of M1 and M3, respectively. And:

$$\overline{G} = \frac{2I_{ss}}{\pi V_{LO}}$$  \hspace{1cm} (4.12)

$$G^2 \approx 8\left(\frac{\ln(\sqrt{2} + 1)}{\sqrt{2}} - \frac{1}{3}\right) \frac{K_{1}^{1/2} I_{ss}^{3/2}}{\pi V_{LO}}$$  \hspace{1cm} (4.13)

$I_{ss}$ is the biasing current of Gilbert cell, $V_{LO}$ is the amplitude of input signal from local oscillator, $K_f$ is the $K$ parameter of transistor M1 or M2.

### 4.2.4 LC Oscillator

The LC tank oscillator and its equivalent circuit are shown in Fig. 4.4. A capacitor and an inductor in parallel form an LC tank that resonates at a frequency of

$$\omega_0 = \frac{1}{\sqrt{LC}}$$  \hspace{1cm} (4.14)

If both the inductor and the capacitor are lossless and some energy is trapped in the resonator tank, there will be an oscillation. However, since it is impractical to fabricate any lossless passive components, as a result, the oscillation dies. Now if a negative resistance is connected to the tank, the loss in the parasitic resistances of the passive components is recovered by the energy supplied by the negative resistance, therefore, the circuit oscillates.
Figure 4.4. (a) LC Oscillator and (b) its equivalent circuit.

The equivalent resistance of the tank is $R_{eq} = R_{LC} \parallel (2/g_{m})$, where, $R_{LC}$ represents the parasitic resistance for the inductor and capacitor. The condition for sustained oscillation is $|2/g_m| \leq R_{eq}$. In other words, the amount of energy supplied by the negative resistance has to be bigger than the amount of energy lost in the tank. Therefore, there is a minimum value of the transconductance $g_{m0} = 2/R_{eq}$ that ensures the oscillation.

The fundamental component of the current is

$$I_0 = \frac{1}{\pi} \int_0^{2\pi} i(t) \sin(\omega t) d(\omega t) = \frac{4}{\pi} \int_0^{\pi} i(t) \sin(\omega t) d(\omega t)$$

The current follows a sine waveform until it reaches its maximum value of $I_{tail}/2$ at an offset angle of $\theta$. Thus,

$$I_0 = \frac{4}{\pi} I_{tail} \left( \frac{\theta}{4 \sin \theta} + \frac{3 \cos \theta}{4} \right)$$

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As a result, the resonator tank amplitude can be approximated as

\[ V_m = \alpha \frac{4}{\pi} L_{\text{tail}} R_{eq} \]  

(4.17)

where \( \alpha = \frac{\theta}{4 \sin \theta} + \frac{3 \cos \theta}{4} \) is a fitting parameter. The parameter \( \alpha \) for different offset angle \( \theta \) is plotted in Fig. 2 (b). The parameter \( \theta \) is obtained from the relation \( \theta + 1.5 \sin 2\theta = \pi / g_m R_{eq} \).

This mode of operation is the current limited operation. On the other hand, the power supply limits the largest possible amplitude to \( V_{dd} \), when the tail current source transistor shuts off at each negative peak of the oscillation.

The amplitude of oscillation is simulated for varying tail currents for different supply voltages using SpectreRF circuit simulator. Corresponding values are calculated using the analytical expression given in (4.17). The simulated and calculated tank voltage amplitude versus tail current is shown in Fig. 4.5. Obviously, a nonlinear relationship between the tail current and the tank voltage amplitude exists. Simulated results (lines) agree with analytical values very well. The parasitic series resistance of a reasonable quality inductor is very small (order of few ohms), therefore the voltage drop across it is negligible. Also, the overdrive voltage at the tail current source \( V_{\text{osat,tail}} \) is usually kept low to allow a higher output swing. Thus, the transistors at the differential pair experience a DC bias voltage of \( V_{\text{os}} = V_{\text{gs}} \approx V_{\text{dd}} \). Moreover, the transient voltage across the transistors can reach as high as \( 2V_{\text{dd}} \). As a result, if the oscillator is in operation for a prolonged time the transistors experience HC and BD simultaneously.

To evaluate the HC and gate oxide BD on the LC oscillator, the transistor models are extracted from device measurements under the HC and SBD combined stress using BSIMPro software. While model parameters for the transistors degrade across the board, an increase of
threshold voltage and decrease in mobility are most noticeable and are given in Figs. 4 (a) and 4 (b) respectively.

(a)
(b)
Figure 4.5. Threshold voltage, mobility and transconductance versus stress time. The 50/0.16 μm NMOS devices are stressed at \( V_G = V_D = 2.6 \) V and BSIM 3 transistor models are extracted from measurement results with a bias condition of \( V_G = V_D = 2.6 \) V. Degradation of transconductance is obtained from direct measurements. The stress was interrupted every 1800 s to measure various transistor parameters.

Experimental data show that the transconductance of the transistor degrades significantly subject to stress. Figure 4 (c) shows the transconductance versus stress time due to the HC effects. The transconductance was measured at a bias current of 7 mA.
CHAPTER FIVE: DEGRADATION SUBJECT TO ELECTRICAL AND TEMPERATURE STRESS

5.1 Introduction

In the previous chapters, both measured and simulated results show that the FOM degraded in device after voltage and temperature stress. It is predictive that the RF circuit performance degradation will follow. It is important to examine the stress effect on RF circuits. Good agreement between simulation and measurement verify that the developed model is suitable to evaluate the RF performance degradation in RFICs. Here, we take several building blocks – LNA, VCO, mixer, PA, as examples to exhibit the RF performance degradation due to dynamic stress.

5.2 Analysis

The inner sidewall depletion region near the drain or source in MOSFETs, which forms a partial capacitance of $C_{db}$, is controlled by surface potential along the channel [49]. Hot carrier induced interface charges alter the surface potential and increase $C_{db}$. The trapped charges at the drain end of the channel cause the change of $C_{gs}$. It showed a significant increase after stress. On the other hand, midgap interface states generated by hot-carrier stress will act as extra recombination centers and will lead to a decrease in $R_{db}$. The increase in $R_d$ is attributed to the interface traps and oxide trapped charged generated the drain region during stress [50], [51]. The decrease in $R_s$ comes from the increase of effective source potential of the stressed MOSFET as $R_d$ increases [50]. $R_g$ includes two parts: polysilicon sheet resistance and non-quasi-static (NQS)
distributed channel resistance [52]. The NQS distributed channel resistance, which is inversely proportional to the transconductance, will change with the shift of transconductance due to stress. The shifts of these parameters are also reported in [50], [51], and [53].

The figure of merit degradation due to these parameter shifts can be expressed as:

$$\Delta F = \sum \frac{\partial F}{\partial P_i} \Delta P_i$$

(4.18)

where $P_i$ is the $i$th parameter, which is a factor of $F$ and shifts after voltage and temperature stress.

5.3 Performance Degradation

5.3.1 Low Noise Amplifier

As the first stage of a receiver, the essential requirements of an LNA are low noise, high gain, and high linearity. Moreover, the matching conditions are also important in the LNA for power delivery and noise optimization. $S$-parameters as a function of frequency are shown in Fig. 4.6 (a). At 5.0 GHz, $S_{11}$ and $S_{21}$ change slightly. The amplitude of $S_{12}$ diminishes from -46 to -50 dB at 5 GHz (8.6 % reduction); $S_{22}$ changes from -9 to -8 dB at 5 GHz. The power gain is degraded significantly after stress, as shown in Fig. 4.6 (b). This is mainly due to the decrease of the transconductance of the transistor. The noise figure versus frequency is plotted in Fig. 4.6 (c) as a function of frequency. After breakdown, leakage paths exist across the gate oxide, which form a noise source to the transistor, thus degrading the noise performance. Also, the drastic increase in the gate current due to NBH stress increases the real part of the complex input
impedance. The immediate impact of such a change affects the impedance matching condition, which is critical for the LNA noise performance. For linearity degradation, two-tone simulations were performed on the LNA at 5 GHz, with separation of 20 MHz in frequency. The power levels in Fig. 4.6 (d) are given for the fundamental and the third-order inter-modulation product (IM3). The increase of IM3 after stress results the linearity degradation. IIP3 before and after stress are 4.2 and -1.1 dBm, respectively. In Figs. 7-10, the temperature is 400 K and the stress time is 2 hours.
Figure 5.1. (a) Amplitude of S-parameters before (□) and after (+) NBH stress for the LNA; (b) Power gain before and after NBH stress for the LNA; (c) Noise figure (@ 50 Ω) before and after NBH stress for the LNA; (d) Output power and IM3 versus input power before and after NBH stress for the LNA.

5.3.2 Power Amplifier

In the previous chapter, both measured and simulated results show that the FOMs degrade in device after dynamic stress. It is predictive that the RF circuit performance degradation will follow. Good agreement between simulation and measurement verify that the developed model is suitable to evaluate the RF performance degradation in RFICs. Here, we take the class-AB power amplifier as an example to exhibit the RF performance degradation due to dynamic stress.
The biasing of device corresponds to the condition for the model extraction measurement. The stress time is 2 hours. The device used in the PA simulation has 0.16 μm of channel length and 900 μm of channel width. It has multi-fingers and each finger of the 45 fingers is modeled by the extracted 0.16×20 μm² nMOS transistor model for the fresh device as well as stressed device.

A 1.0 MHz channel bandwidth quaternary phase shift keying excitation signal (QPSK) excitation signal at 900 MHz for CDMA is used as the input. Fig. 4.7 (a) shows the output spectrum at –30 input power. The in-band output power is reduced due to ac stress. The power-added efficiency (PAE) as a function of the input power is given in Fig. 4.7 (b) with a 900 MHz input signal. It shows obvious degradation due to stress, changing from 32% to 28% with 5 dBm of input power. In realistic applications, PAs are operated with wideband input signals that can carry information, not with the standardized tow-tone excitation. A 1.0 MHz channel bandwidth QPSK at 900 MHz for Code Division Multiple Access applications is used as the input. The simulated adjacent channel power ratio (ACPR) versus output power shown in Fig. 4.7 (c) before and after stress. ACPR becomes worse after stress. This means the out-of-band power emission level effects become larger after stress. For the noise power ratio (NPR) simulation, the PA is excited with an input consisting of band-pass filtered white (Gaussian) noise with a small notch (0.25 MHz) at the center of the frequency band. The simulated NPR is given in Fig. 4.7 (d). NPR degrades after stress.
ACPR (dB) vs Output power (dBm)

(c)

- ACPR (dB)
- Output power (dBm)

Before stress
After stress

(d)

-NPR (dB) vs Input Power (dBm)

Before stress
After stress
Figure 5.2. (a) Output spectrum before stress and after stress of the PA for –30 dBm input power with a 1.0 MHz-wide QPSK input signal. Center frequency is 900 MHz; (b) Simulated PAE versus input power; (c) Adjacent channel power ratio versus output power before stress and after stress; (d) Noise power ratio versus input power before stress and after stress.

### 5.3.3 Mixer

The single-balanced Gilbert mixer used for investigation of HC effects is used as a down-converter with RF frequency of 1.0 GHz, LO frequency of 920 MHz, $V_{LO}$ of 0.8 V and supply voltage of 3.3 V. The SSB noise figure and conversion gain are plotted as functions of biasing current in Fig. 4.8 (a). One can see that there is significant degradation at the small biasing current region. While at the high biasing current region, the degradation becomes smaller. The reason is that the drain current has more compression at the high biasing current region. The degradation of linearity for the Gilbert mixer is shown in Fig. 4.8 (b). The IIP3 changed from 3.168 to 1.182 after stress. The output power becomes lower and the third-order intermodulation distortion (IM3) shifts upward after HC stress.
Before Stress
After Stress

(a)

SSB Noise Figure (dB)

Conversion Gain (dB)

Bias Current (mA)

(b)

Output Power and IM3 (dBm)

Input Power (dBm)
Figure 5.3. (a) Simulated SSB noise figure and conversion gain versus bias current before and
after stress. (b) Simulated output power and IM3 versus input power before and after stress.

5.3.4 Oscillator

The frequency drift for an LC oscillator is caused by two mechanisms. First, the
degradation of amplitude due to the gate oxide BD of the varactor transistors cause the effective
average capacitance to change; whether the capacitance will increase or decrease depends on the
gate bias voltage $V_{gs}$ and $V_{os}$. Second, the small-signal capacitance of the varactor is reduced for
some internal mechanisms.

As the hardness of breakdown increases, the breakdown spot resistance is reduced to few
kΩ, as a result, the amplitude decreases. A 2.4 GHz LC oscillator has been designed and
simulated using an inversion type varactor. The varactor transistors have five fingers with 50 μm
in width and 0.16 μm in length (the size of the measured devices) each. For SpectreRF
simulation in Cadence, a 10 kΩ breakdown spot resistance is assumed for each broken finger.
BSIM3 model parameters extracted from the measured data are used in the simulation. The
amplitude of the oscillator has been evaluated with the different numbers of fingers experiencing
hard BD using the analytical models in section 4.2.4 and by computer simulation. The simulation
and analytical results for the amplitude of oscillation are shown in Fig. 4.9. Good agreement
between the model predictions and SpectreRF simulation is obtained.
The mechanisms for phase noise have been analyzed in [54], [55]. The phase noise of an LC oscillator at an offset frequency of \( \omega_m \) from the frequency of oscillation \( \omega_b \) normalized with respect to the carrier is given by

\[
\mathcal{Z}(\omega_m) = 10 \log \left[ \frac{4kTFR_{LC} \cdot \left( \frac{\omega_b}{2Q\omega_m} \right)^2}{V_m^2} \right]
\]

(4.19)

where \( F = 2 + \frac{8\gamma R_{eq\text{tail}}}{\pi V_m^4} + \frac{8}{9} g_{\text{bias}} R_{eq} \). The three terms in \( F \) account for thermal noise for the tank resistance, the differential pair, and the tail current source, respectively. \( R_{LC} = R_c \parallel R_e \) is the equivalent resistance of the resonator tank. The loaded quality factor \( Q \) depends on the inductors and the capacitors. In CMOS technology on-chip inductors have low quality factor and usually dominates in overall quality factor. However, as we have seen the quality of the varactor can degrade significantly as the transistors experience BD. Also, as the amplitude of oscillation
degrades as the gate oxide BD progresses, the phase noise of the oscillator increases. Fig. 4.10 shows the phase noise of the oscillator for different numbers of varactor transistor finger experiencing breakdown, where solid lines show SpectreRF simulation results and discrete points are calculated. Since we have used ideal current source during the simulation of the oscillator, we ignored the noise coming from the tail current source in our calculation. There is a good agreement between the simulation results and the model prediction. At a given offset frequency, the higher the number of finger breakdown, the higher the phase noise of the oscillator.

Figure 5.5. Amplitude Normalized phase noise of the oscillator versus offset frequency.
CHAPTER SIX: 60/90 NM MOSFETS WITH HIGH-K DIELECTRICS

6.1 Introduction

The insulators with high-κ dielectrics are motivated by the necessity of reducing the gate leakage current of MOSFETs, while avoiding the problems which arise when the SiO₂ thickness is reduced below the 1.5-1.0 nm range, as demanded by device scaling. Many materials are currently under consideration as potential replacement for SiO₂ as the gate dielectric material for sub-100 nm CMOS technology [76]. The most commonly studied high-κ gate dielectric candidates are the Ta₂O₅ [77]-[78], SrTiO₃ [79]-[80], and Al₂O₃ [81]-[82] due to their maturity in memory applications. Recently, a substantial amount investigation has gone into the TiO₂ [83]-[84], ZrO₂ [85]-[86], and HfO₂ [87]-[88], which have shown much promise in overall materials properties as candidates to replace SiO₂. HfO₂ appears promising due to its relatively high dielectric constant (~ 25) as compared to Al₂O₃ [89], high free energy of reaction with Si (47.6 Kcal/mole at 727 °C) as compared to TiO₂ and Ta₂O₅ [90], large bandgap [91], and good thermal stability.

However, satisfying the reliability requirements, such as threshold voltage stability and dielectric reliability for alternative gate insulators, remains a significant challenge for integration [92], [93]. It is the time for the present research status of high-κ dielectrics to shift from material selection to reliability phase. High-κ dielectric gate insulators reduce the gate leakage and alleviate the associated problems in the scaling down MOSFETs. However, aggressive scaling of MOSFET dimensions results in the high lateral electrical field and HC effects. The reliability
issues for sub-100 nm MOSFETs should be paid more attention. Lugui, et. al. gave the gate oxide breakdown effects on 90 nm NMOSFETs [94].

As the gate oxide thickness continues to shrink, the use of high-k dielectrics to reduce the gate leakage current becomes more attractive. Among most promising high-k materials, HfO$_2$ particularly appears a good candidate compared to Al$_2$O$_3$, TiO$_2$, and Ta$_2$O$_5$ due to its relatively high dielectric constant, high free energy of reaction with Si, large bandgap, and good thermal stability [89]-[91].

Recently, many papers on HfO$_2$ devices have been published [95] - [100]. Degrave et al. [100] observed that polarity dependent breakdown (BD) through the Weibull slope. Loh et al. [101] reported the high-k or interfacial layer initiated breakdown using carrier separation measurement technique. Under negative stress, breakdown is initiated from high-k film, while under positive stress, the breakdown is initiated from the interface layer. Pantisano et al., [94] and Degrave et al., [103] showed that breakdown location in the short channel has different impact on RF performances. The impact of high-k dielectrics breakdown on circuits, however, is still not well understood.

It is critical to evaluate the breakdown-induced effect on analog or digital integrated circuits through simulation. The equivalent circuit for simulating the SiO$_2$ post-breakdown behavior has been presented [104], [105]. The post-breakdown RF characteristics were evaluated using the breakdown resistances between the gate and the source and between the gate and the drain. Rodriguez et al. [106] and Miranda et al. [107] modeled the soft breakdown using a current source, instead of the breakdown resistance for digital switching.

This chapter gives a thorough study on the impact of HCs on the state-of-the-art 60nm MOSFET with high-κ dielectrics. In section II, the analysis of RF performance, which is related
to the parameters of devices, is given. Experimental details are described in Section III. The experimental results including degradation in DC characteristics, RF FOM such as the cutoff frequency ($f_T$), noise figure ($NF$), linearity ($VIP3$, $IIP3$), and $1/f$ noise level are also presented. Discussions give the insight of degradation of these RF performances due to HCs in 60 nm nMOSFETs. The HC effects on performance of integrated circuit are also investigated. This chapter also examines the polarity dependence and charge trapping characteristics of p- and n-MOSFETs. A compact model of the leakage current through the breakdown path is employed. Transfer characteristics of a CMOS inverter and a three-stage inverter circuit subject to breakdown are examined by measurement and simulation. The low noise amplifier (LNA) for RF application is also studied using Cadence SpectreRF simulation. The effect of breakdown location on digital and RF circuits is also investigated.

6.2 Analysis

For circuit applications, the RF performance is more important. Noise figure and linearity are key parameters for RF circuits RF such as low-noise amplifiers (LNAs) and mixers. Low-frequency noise is important for the phase noise of RF circuits such as voltage-controlled oscillators (VCOs). Phase noise and linearity specifications are severe for future wide-band communication systems. Optimization of these performances is the major concentration of an RF circuit designer. With the scaling of MOSFETs, one of the major reliability issues - hot carriers (HCs) because of high lateral field in short-channel MOSFETs, become even more important. The figures of merit (FOMs) such as the cutoff frequency, third-order inter-modulation intercept
point (IIP3), minimum noise figure (NF), and 1/f noise power density of drain current as functions of device parameters are given as [108]:

\[
f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{1}
\]

\[
NF_{\text{min}} = 1 + 2\pi K_f f(C_{gs} + C_{gd}) \sqrt{\frac{R_G + R_S}{g_m}} \tag{2}
\]

\[
IIP_3 = \frac{2}{3} \left| \frac{g_m}{g_{m3}} \right| \frac{1}{R_{IN}} \tag{3}
\]

\[
S_{td} = \frac{K'}{f^\alpha C_{ox} LW} \tag{4}
\]

where \(g_m, g_{m2}, \) and \(g_{m3}\) are the first-, second- and third-order transconductance, respectively, \(f\) is the operation frequency, \(K_f\) is the Fukuui factor, and \(R_{IN}\) is the signal resistance, \(C_{gs}\) and \(C_{gd}\) are the gate-source and gate-drain capacitances, respectively, \(R_G\) and \(R_S\) are the gate and source series resistances, respectively, \(\omega (= 2\pi f)\) is the angle frequency, \(\Delta \omega\) is the difference between the two angle frequencies in the two-tone input signal for IIP3 test, \(G_0(\omega) (= 1/R_L + g_{ds} + j\omega C_{gd})\) is a factor, \(g_{ds}, g_{ds2}\) is the first- and second-order output-conductance, respectively. \(C_{ox}\) is the oxide capacitance of devices, \(L\) and \(W\) are the effective length and width of devices, and \(\alpha\) is a fitting coefficient.

From (1) – (4), one gets the normalized degradation of the FOMs. The details are given in Appendix A.

\[
-\frac{\Delta f_T}{f_T} \approx -\frac{\Delta g_m}{g_m} + \frac{\Delta \text{Im} Y_{11}}{\text{Im} Y_{11}} \tag{5}
\]

\[
\frac{\Delta NF_{\text{min}}}{NF_{\text{min}} - 1} \approx \frac{\Delta \text{Im} Y_{11}}{\text{Im} Y_{11}} + c_1 \frac{\Delta \text{Re} Z_{11}}{\text{Re} Z_{11}} + c_2 \frac{\Delta g_m}{g_m} \tag{6}
\]
\[-\frac{\Delta IIP_3}{IIP_3} = -\frac{\Delta g_m}{g_m} + \frac{\Delta g_{m3}}{g_{m3}}\]  \hspace{1cm} (7)

\[\frac{\Delta S_{ld}}{S_{ld}} \approx c_3 \frac{\Delta \alpha}{\alpha} + \frac{\Delta V_{GT}}{V_{GT}} + \frac{\Delta \mu}{\mu} + \frac{\Delta g_m}{g_m}\]  \hspace{1cm} (8)

where \(YII\) and \(ZII\) are the \(Y\)-parameter and \(Z\)-parameter, \(V_{GT} ( = V_{GS} - V_T)\) is the effective gate bias, \(\mu\) is the mobility factor. \(c_1, c_2,\) and \(c_3\) are coefficients given in Appendix A.

Equations (5) – (8) give the approximate evaluation of normalized degradation for RF performances in the basic DC characteristics, two-port impedance and admittance matrix. The impedance and admittance matrix can be obtained from the scattering matrix – \(S\)-parameters. Therefore, the RF performance degradation can be evaluated from the degradation of basic DC characteristics and \(S\)-parameters, which can be easily measured by parameter analyzer and network analyzer. This will give a quick insight for RF designer to evaluate the RF performance degradation and lifetime subject to HC effects.

6.3 Device Degradation for 60 nm High-K MOSFETS due to HC

6.3.1 Experiments

The tested devices are \(60 \times 100\, \text{nm}^2\) nMOSFETs with dielectrics of 10 Å SiO\(_2\) and 30 Å HfO\(_2\). The wafer was tested in a Cascade 12000 Probe Station. Agilent 4156B Precision Semiconductor Parameter Analyzer was used for dc biasing and \(I-V\) characterization. \(S\)-parameters were measured up to 20 GHz using a HP8510 Network Analyzer. The gate-source and drain-source voltages of fresh devices were set at 2.5 V and 1.0 V for the HC stress, respectively. The source and bulk were grounded. Thermo-Chuck TP0315 was used to set test
temperatures (300 K). It has excellent temperature uniformity (± 0.5 °C) of the chuck temperature over the entire temperature range. Then, the stress was interrupted every 600 seconds to measure various transistor parameters at different temperatures.

6.3.2 Results

Measured I-V characteristics are given in Fig. 1. The drain currents shift downward after HC stress. Fig. 2 displays shift of S-parameters before and after stress. The gate-source bias voltage for S-parameters measurement is 0.95 V and the drain-source voltage is set at 1.5 V. The devices are operated in the saturation region. One can see that all S-parameters changed after dynamic stress for 4800 s. The decreases in the amplitude of $S_{21}$ after stress indicated the degradation of the drain to gate power gain. The amplitude of $S_{12}$ is twice that of the gate to drain voltage gain, it also shows degradation after stress. The input impedance is proportional to $|(1+S_{11})/(1-S_{11})|$. After stress, $S_{11}$ shifts left, which means a decrease in the input impedance.

The minimum noise figure was measured (Fig. 3). Using the HP 8560 RF spectrum analyzer, Ailtech noise generator, and the $Y$-factor noise figure measurement method described in [116], the $NF_{\text{min}}$ was measured. The drain and gate voltages were set at 1.5 V and 1.0 V, respectively. The noise figure relates to the transconductance, overlap capacitances, and terminal resistance ($R_G$, $R_S$) (Eqn. (2)) and increases with stress. In the saturation region, $|g_{m3}|$ increases, while $|g_m|$ decreases after stress. VIP3 is proportional to $|g_m/g_{m3}|$. Therefore, the degradation of VIP3 in the saturation region is anticipated. Fig. 4 (a) gives VIP3 before and after stress. One can see that it degrades after stress in the saturation region. The peak in VIP3 comes from the close zero point of $g_{m3}$. The output power versus input power at $V_{GS} = 0.95$ V and $V_{DS} = 1.5$ V. A two-tone
input \((\omega_1 = 1.0 \text{ GHz}, \omega_2 = 1.002 \text{ GHz})\) is used in experiment and simulation. HP 8560 RF Spectrum Analyzer was used to measure the fundamental \((P_{\text{Fund}})\) and inter-modulation (IM3) power. IIP3 decreases after HC stress for 4800 seconds. Fig. 4 (b) shows the output power \((P_{\text{out}})\) and IM3 versus the gate bias voltage. After stress, the output power reduced, and IM3 of the stressed device was larger than that of the fresh one when the input power is smaller than \(-25 \text{ dBm}\). That means the linearity was degraded due to stress in this region. The low frequency noise before and after stress is plotted as a function of frequency in Fig. 5. It increases after HC stress.

Figure 6.1. Drain current before and after HC stress. Measured from 0 V to 1.5 V for the drain-source voltage.
Figure 6.2. $S$-parameters before and after HC stress. Stress time is 4800 seconds. Measurement condition: $V_{GS} = 0.95$ V and $V_{DS} = 1.5$ V.

Figure 6.3. Noise figure versus frequency before and after stress. Measurement condition: $V_{gs} = 0.95$ V and $V_{ds} = 1.5$ V.
Figure 6.4. (a) VIP3 versus gate-source voltage before and after stress; (b) output power and IM3 versus input power before and after stress.
The Eqn. (5) – (8) gives the relationship of normalized degradations in RF performances with DC characteristics, $Y_{II}$, and $Z_{II}$ degradations. $Y_{II}$ and $Z_{II}$ can be obtained from $S$-parameters. The degradation in RF performance can be predicted from the degradation of DC characteristics and $S$-parameters directly. Fig. 6 (a) gives the normalized degradations in drain current, transconductance, $Y_{II}$ and $Z_{II}$. The ‘fresh’ values for drain current, $g_m$, and $g_{m3}$ are 2.5 mA, 10.8 mA/V, and 40 mA/V$^3$, respectively. They are measured under $V_{GS} = 1$ V and $V_{DS} = 1.5$ V. While the fresh $\text{Im}(Y_{II})$ and $\text{Re}(Z_{II})$ at 2 GHz are $2.2 \times 10^{-4}$ S and 96.73 Ω. The normalized degradations in cutoff frequency, IIP3, minimum noise figure, which are measured under the same conditions, are given in Fig. 6 (b). The fresh values for cutoff frequency, IIP3, and minimum noise figure are 18.1 GHz, -5 dBm, and 0.3 dB. Good agreements are obtained between prediction and measurement. The errors ($\varepsilon = \sqrt{\sum_{i=1}^{N} (X_i - Y_i)^2 / (n-1)} \times 100\%$, where $i$ is the sample number, from 0 to n. $X_i$ is the predicted value and $Y_i$ is the measured value.) are also calculated. They are 0.29%, 0.77%, and 0.25% for cutoff frequency, IIP3, and minimum noise figure, respectively. From these figures and Eqn. (5)-(8), one can get that the degradation of cutoff frequency due to HC effects comes from the changes in transconductance ($g_m$) and capacitance - $C_{gg}$ ($\approx \text{IM}(Y_{II})/\omega$). After stress, the trans-conductance diminished and $C_{gg}$ increased. Cutoff frequency decreased significantly. IIP3 degrades with the shifts in transconductance and third-order transconductance ($g_{m3}$). The decrease of $|g_m|$ and increase of $|g_{m3}|$ after stress result in the degradation of IIP3. Degradation of $NF_{min}$ is dominated by the shifts in $g_m$, $g_{m3}$, $C_{gg}$, $R_G$, and $R_S$. 

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In Eqn. (8), the fitting factor ($\alpha$) for flicker noise increases after stress, as shown in Fig. 6 (c). It changed from 1.01 to 0.85 after 4800 seconds stress. The phenomena are also observed in other works. The changes of fitting factor have significant effects on low frequency noise degradation. The normalized mobility ($\mu$) and $V_{GT} (= V_G - V_T)$ degradation are shown in the same figure. The reduction in mobility may inherently come from the remote phonon scattering at the high-k film interface. The $V_T$ increases after stress. The major mechanism is likely to be interface state generation. The measured and predicted normalized degradations of $S_{id}$ are given in Fig. 6 (c). The error between analytical predictions and experiments is 1.08%. The normalized degradations of $V_{GT}$ and $\mu$ are also given in the same figure. The ‘fresh’ $V_T$ and $\mu$ are 0.457 V and 100.72 cm$^2$/Vsec, respectively.

6.4 **HC Stress Effects on Circuit**

A cascade low noise amplifier, as shown in Fig. 7, is used as an example to demonstrate the RF performance degradation subject to the HC stress in integrated circuit in 60 nm transistors of high-$\kappa$ dielectrics. The cascade transistor M2 reduces the input capacitance and enables a good reverse isolation, hereby enhancing the stability. Here, M1 and M2 are multi-fingered devices, and both of them contain 6 fingers ($60 \times 100$ nm$^2$). Each finger in simulation is modeled by the equivalent circuit model. The BSIM core is extracted from the devices using Cascade 12000 Probe Station. Other terminal resistances and capacitances are extracted from measured $S$-parameters. The matching conditions and noise figure are optimized at the operation frequency (2.2 GHz).

The supply voltage is biased either at the normal mode of operation (2 V), or at the stress
mode (4.2 V), which accelerates the HC effects on transistors. In the stress mode, the simulation gives the stress conditions of the transistors: 2.5 V of drain-source voltage and 1 V of gate-source voltage for M1; 1.5 V of drain-source voltage and 1.5 V of gate-source voltage for M2. The M1 suffers from the HC stress. The stress conditions are the same with HC acceleration experiments and the biasing of normal operation for M1 is the same with S-parameter measurement. The models extracted from fresh and stressed devices are applied to M1 for each stress time slot to evaluate the performance degradation in LNA due to HC stress. In the extracted core model files, many parameters were adjusted to represent the stressed device behaviors, including $V_{th0}$, $K_1$, $K_2$, $K_3$, $U_0$, $U_a$, $U_b$, $U_c$, $V_{off}$, $N_{factor}$, etc.

As the first stage of a receiver, the essential requirements of an LNA are low noise and high gain. Moreover, the matching conditions are also important in the LNA for power delivery and noise optimization. The performance of LNA is sensitive to the device parameter changes, thus degrades with the HC stress. S-parameters before and after stress as a function of frequency are shown in Fig. 8. At 2.2 GHz, S12 changes slightly. The amplitude of S21 diminishes from 20.7 to 20.3 dB at 2.2 GHz after stress for 2400 seconds and to 20.0 dB after stress for 4800 seconds; S11 changes from -35 to -27 dB at 2.2 GHz after stress for 2400 seconds and to -24 dB after stress for 4800 seconds; S22 changes from -27.5 to -26.8 dB at 2.2 GHz after stress for 2400 seconds and to -24 dB after stress for 4800 seconds.

Based on [110], one can get the normalized degradation of power gain ($G \equiv P_{out}/P_{in}$) at resonant frequency and minimum noise figure. The details are given in Appendix B.

$$\frac{\Delta G}{G} = 2 \frac{\Delta g_{m1}}{g_{m1}}$$ (9)
where $g_{m1}$ is the transconductance of M1, and $C_{gs1}$ is the equivalent capacitance between gate and source of M1.

High performance integrated circuits with small size devices (e.g., 60 nm nMOSFETs with high-$\kappa$ dielectric) suffer from the hot carrier effects. If care is not taken to understand these issues, HC induced degradation can lead to accelerated circuit failures during operations. Detection of these failures may become difficult due to circuit complexity and hence lead to erroneous data or output conditions. The equations (9) and (10) gives a quick guidance for RF circuit designer that which ones are the dominant factors for the RF performance degradations in circuits, and how much it will affect the RF performances.

The power gain is degraded significantly after stress, as shown in Fig. 9. This is mainly due to the decrease of the transconductance of the transistor. The minimum noise figure degradation for each stress time slot is also plotted in the same figure. The fresh values for power gain and minimum noise figure of the LNA are 10.37 dB and 0.8 dB, respectively. The predictions using Eqns. (9) and (10) are also given. There is good agreement between simulation and prediction. The errors for power gain and noise figure are 0.93% and 0.33%, respectively.

6.5 Device Degradation due to Breakdown Stress

6.5.1 Experiments

The tested devices are $0.15 \times 20 \ \mu m^2$ pFETs and $0.20 \times 20 \ \mu m^2$ nFETs with 30 Å of
HfO$_2$ dielectrics, 10 Å of SiO$_2$ interfacial layer, and polysilicon gate. The wafer was tested in a Cascade 12000 Probe Station. Agilent 4156B Precision Semiconductor Parameter Analyzer was used for DC biasing and $I$-$V$ characterization. The breakdowns are carried out by the constant voltage stress (CVS). During the stress, the gate-source was set at 4.0 V for positive bias stress and - 4.0 V for the negative bias stress. The drain, source, and bulk were grounded.

### 6.5.2 Results and Discussions

The evolution of the gate leakage current during the CVS for several p- and nFETs are shown in Fig. 1. The time-to-breakdown ($t_{BD}$) distributions are displayed in Fig. 2. The experimental data show that the negative bias stress is easier to trigger the gate breakdown than the positive bias stress for both p- and n-channel transistors. In addition, nFET is harder than pFET to break down the gate dielectric under the same polarity stress. The gate oxide stacks can be seen as two capacitances in series – one is the bulk layer (high-k) and the other is the interfacial layer (SiO$_2$). We use $C_{\text{bulk}}$ and $C_{\text{interfacial}}$ to represent these two capacitances. They function as a voltage divider during the CVS stress. Therefore, the voltage across the bulk layer is $\pm 4\cdot \frac{C_{\text{bulk}}}{C_{\text{Bulk}} + C_{\text{Interfacial}}} \ (\approx \pm 0.4 V \text{ for } C_{\text{Interfacial}} \approx 8.33 \cdot C_{\text{Bulk}})$, while the voltage across the interfacial layer is $\pm 4\cdot \frac{C_{\text{interfacial}}}{C_{\text{Bulk}} + C_{\text{Interfacial}}} \ (\approx \pm 3.6 V \). The high stress voltage on thin interfacial layer initiates the interfacial layer breakdown. The Weibull slopes ($\beta$) for the breakdown distributions are about 1.85, similar to the Weibull slope for SiO$_2$ of the same thickness ($\sim 10$ Å) [111]. Because the defect density of p-channel device is larger than that of n-channel device by a
factor of 10 for the same thickness and stress voltage, the time to breakdown for the nFET is longer than the pFET. Under the gate injection, the high hole trapping rate and interface state creation suggest a fast degradation of the interfacial layer. While under the substrate injection, the trap creation occurs mainly in the bulk layer [111]. For either n- or p-device, the breakdown under gate injection (negative CVS) is easier than that under substrate injection (positive CVS).

6.5.3 Modeling

A compact model [13] to evaluate the stressed transistor is reported in [9]. The equivalent circuit model includes the terminal resistances \((R_g, R_d, R_s)\), substrate network resistances \((R_{db}, R_{sb}, R_{dsb})\), overlap capacitances \((C_{gdo}, C_{gso})\), junction capacitances \((C_{db}, C_{sb})\), and two internal resistances \((R_{gd}, R_{gs})\). The post-breakdown RF characteristics can be accounted for by using the two breakdown resistances \(R_{gs}\) and \(R_{gd}\). The intrinsic transistor is a BSIM3V3 model extracted from fresh or stressed devices using BSIMPro.

The potential for the BD path is \(\Phi(V_{GS}, V_{DS}, x)\) and the voltage across the BD path is \(V_{GS}-\Phi(V_{GS}, V_{DS}, x)\). The currents flowing through the source \((I_{GS})\) and drain \((I_{GD})\) are derived (see detail in Appendix). They are expressed as

\[
I_{GS} = (1-x)K[V_{GS} - V_{FB} - \Phi_s(V_{DS}, V_{GS}, x)]^\alpha \\
I_{GD} = xK[V_{GS} - V_{FB} - \Phi_s(V_{DS}, V_{GS}, x)]^\alpha
\]

where \(x (= y/L)\) is the normalized position along the channel, \(K\) and \(\alpha\) are constants, and \(\Phi_s\) is the surface potential.

The breakdown equivalent circuit model is given in Fig. 4. The current source \(I_{GS}\) and \(I_{GD}\) represent the gate current partitions into the source and drain, respectively. The BD path is above
the source or drain extension region, i.e., with \( x < 0.01 \) or \( x > 0.99 \). The gate current can be expressed as \( KV_{GS}^x \) or \( KV_{GD}^x \). For small-signal excitation at a given bias, one may use the two equivalent resistances \( R_{GS} \) and \( R_{GD} \) to replace the current sources \( I_{GS} \) and \( I_{GD} \). For large-signal applications, (1) and (2) could be used to account for post-breakdown behavior. A simple model for the voltage across the BD path is expressed as (see derivation in Appendix):

\[
V_{Cross} \approx V_{GS} - (aV_{DS} + b\sqrt{V_{DS}} + c)
\]

(3)

where \( V_{DS} = V_{GS} - V_{GD} \) and \( a, b, \) and \( c \) are fitting coefficients.

The gate leakage current for various n- and p-FETs after breakdown is shown in Fig. 5. In this figure lines represent the model predictions and symbols represent the experimental data. Good agreement between the measurement and simulation over a wide range of gate current is obtained. After breakdown, the gate leakage current density goes beyond \( 10^4 \) A/cm\(^2\). At high gate leakage, it is difficult to obtain an accurate capacitance using the conventional C-V measurement or LCR meter [112]. The extraction of capacitance from \( S \)-parameters at high frequency may be more suitable [104].
Figure 6.5. Gate leakage current during stress for (a) pFET and (b) nFET.
Figure 6.6. Weibull plot of the cumulative failure (F) distribution for (a) pFET and (b) nFET.
Figure 6.7. Schematic of breakdown path in the MOS transistor
6.6 RF Performance Degradations

The S-parameters before and after breakdown were obtained through HP8510 Network Analyzer. The gate-source bias voltage for S-parameters measurement is set at 1 V and the drain-source voltage is 1.5 V. The devices are operated in the saturation region. All S-parameters changed after breakdown. The mean values of resistances and capacitances from 1 to 10 GHz are
extracted [13]. In the BSIM3V3 model file, many model parameters were adjusted to represent the stressed device behavior. The shifts of these parameters are explained in [104]. The extracted ‘fresh’ as well as ‘stressed’ models are used in the simulation to evaluate the breakdown-induced degradation. Using Agilent 8560 RF Spectrum Analyzer, Ailtech noise generator, and Y-factor noise figure \((NF)\) measurement method described in [116], the noise figure for a source impedance of 50 \(\Omega\) was measured. Noise figure versus frequency before and after stress is shown in Fig. 6. In Fig. 6 lines represent the model predictions and symbols represent the measurement data for \(x\) ranging from 0.1 to 0.9. The breakdown changes noise figures, but the breakdown location does not have significant impact on the noise figure of the MOSFET.

Fig. 7(a) displays \(VIP3\) versus gate-source voltage before and after stress for \(x = 0.1\) to 0.9. In the saturation region, \(|g_{m3}|\) increases, while \(|g_m|\) decreases after stress. The degradation of \(VIP3\) in the saturation region is anticipated since \(VIP3 = \sqrt{24|g_m / g_{m3}|}\) [108]. In Fig. 7(a) the peak of \(VIP3\) results from a near zero value of \(g_{m3}\). Because of the shifts of threshold voltages in nFET and pFET after breakdown, \(VIP3\) shifts right for n-device and left for p-device after breakdown. In Fig. 7 the breakdown position affects \(VIP3\) at low \(V_{GS}\) (or in saturation) more than that at high \(V_{GS}\) (or in the linear region).
Figure 6.9. (a) – (d) Characterizations of gate leakage current for n- and p-channel transistors after breakdown. Lines: modeling results using fitting coefficients given in Table I; Marks: measurement data. ∀: $V_{ds} = 0$ V; M: $V_{ds} = 0.5$ V; +: $V_{ds} = 1.0$ V; −: $V_{ds} = 1.5$ V.
Figure 6.10. Noise figure of a 50 Ω output before and after breakdown for (a) pMOS #2, (b) pMOS #4, (c) nMOS #1, and (d) nMOS #3. Biasing is at $V_{gs} = 1.0 \, V$ and $V_{ds} = 1.5 \, V$. N-channel device is $0.225 \times 10 \, \mu m^2$ and p-channel device is $15 \times 10 \, \mu m^2$. 
Figure 6.11. *VIP3* before and after breakdown for (a) pMOS #2, (b) pMOS #4, (c) nMOS #1, and (d) nMOS #3
6.7 Integrated Circuit Degradations

6.7.1 Invertors

The inverters used in this paper were fabricated using nFET of $0.225 \times 10 \mu m^2$ and pFET of $0.15 \times 10 \mu m^2$. The DC transfer curves of the CMOS inverter subject to breakdown in n- and p-device independently are examined. The experimental data and Cadence simulation results are shown in Fig. 8. On-wafer measurements are done through HP4156 Precision Semiconductor Parameter Analyzer and Cascade 12000 Probe Station. Good agreement between simulation and measurement results in the transfer curve characteristics is obtained. From these output voltage versus input voltage curves, one can see that the effect of soft breakdown (SBD) (Figs. 8 (a) and (b)) is less severe compared to that of hard breakdown (HBD) (Fig. 8 (c)). The effect due to SBD at the source end (Fig. 8 (a)) is smaller than that at the drain end (Fig. 8 (b)). The breakdown in p-channel transistor results in a left shift of the transfer curve. The output voltage shifts downward with the breakdown in pMOSFET. While for nMOSFET, the increase of threshold voltage causes the transfer curves shift right (or the output voltage shifts upward).

Table 1 Parameters used to model gate leakage current after breakdown

<table>
<thead>
<tr>
<th>Devices</th>
<th>$K$</th>
<th>$\alpha$</th>
<th>$a$</th>
<th>$b$</th>
<th>$c$</th>
<th>$x$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS #1</td>
<td>$1.8 \times 10^{-4}$</td>
<td>3</td>
<td>0.001</td>
<td>0.28</td>
<td>0.01</td>
<td>0.3</td>
</tr>
<tr>
<td>NMOS #2</td>
<td>$4.2 \times 10^{-4}$</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$\approx 0$</td>
</tr>
<tr>
<td>NMOS #3</td>
<td>$1.6 \times 10^{-4}$</td>
<td>1.3</td>
<td>0.12</td>
<td>0.256</td>
<td>0.04</td>
<td>0.8</td>
</tr>
<tr>
<td>NMOS #4</td>
<td>$1.3 \times 10^{-4}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$\approx 0$</td>
</tr>
<tr>
<td>PMOS #1</td>
<td>$2.9 \times 10^{-5}$</td>
<td>3.2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$\approx 0$</td>
</tr>
<tr>
<td>Devices</td>
<td>$V_T$ (V)</td>
<td>$\mu$ (cm$^2$/V⋅sec)</td>
<td>$C_{gs}$ (fF)</td>
<td>NFactor</td>
<td>$V_{off}$ (V)</td>
<td></td>
</tr>
<tr>
<td>-------------</td>
<td>-----------</td>
<td>-----------------------</td>
<td>--------------</td>
<td>---------</td>
<td>--------------</td>
<td></td>
</tr>
<tr>
<td>Fresh PMOS</td>
<td>-0.521</td>
<td>120.01</td>
<td>83</td>
<td>2.024</td>
<td>-0.098</td>
<td></td>
</tr>
<tr>
<td>PMOS #1</td>
<td>-0.543</td>
<td>110.23</td>
<td>92</td>
<td>2.256</td>
<td>-0.092</td>
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</tr>
<tr>
<td>PMOS #4</td>
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<td>101</td>
<td>3.123</td>
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<td></td>
</tr>
<tr>
<td>Fresh NMOS</td>
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<td>61</td>
<td>2.321</td>
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<tr>
<td>NMOS #1</td>
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<td>90.32</td>
<td>67</td>
<td>2.568</td>
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<td></td>
</tr>
<tr>
<td>NMOS #4</td>
<td>0.561</td>
<td>81.03</td>
<td>84</td>
<td>3.238</td>
<td>-0.081</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Main extracted model parameters for FOM simulations

The devices (nMOS #1, nMOS #3, pMOS #2, pMOS #4) in Fig. 1 are used to evaluate the position-dependent breakdown effect on the inverter. nMOS #1 and pMOS #2 are subject to soft breakdown and nMOS #3 and pMOS #4 are subject to hard breakdown. The coefficients of the leakage currents $I_{GS}$ and $I_{GD}$ are given in Table I. Based on Cadence simulation, the high output voltage ($V_{OH}$) and low output voltage ($V_{OL}$) as a function of normalized position are displayed in Fig. 9. For both n- and pMOSFETs, the breakdown near the drain end has most significant impact on the output voltage of the inverter. Hard breakdown is more detrimental than soft breakdown and can make the inverter malfunctional (e.g., $V_{OH}$ is less than 1 V or $V_{OL}$ is more than 0.2 V).

A three-stage inverter structure is investigated to understand the circuit interaction before and after the main inverter. Here, the second stage inverter is considered having the breakdown.
Figs. 10(a) and 10(b) give the simulated transfer curves for p- and n-FET breakdown, respectively. The breakdown position changes from the source side to the drain side ($x = 0.1$ to $0.9$) of the MOSFET. The first and second inverter performances degrade significantly. The degradation of the first stage inverter comes from the reduction of output impedance due to breakdown of the following second stage. The output response of the third stage inverter, however, is quite good. The transfer curve shifts right due to increased nFET threshold voltage. The robust binary-level digital circuitry following the affected stage then rectifies the logic level. The circuit remains functional well even after hard breakdown. This suggests relaxation of digital circuit design.
Figure 6.12. Output voltage versus input voltage characteristics
Figure 6.13. Output voltage versus input voltage of an inverter for different breakdown positions
Figure 6.14. (a) Transfer curves after (a) pMOS breakdown and (b) nMOS breakdown
6.7.2 Ring Oscillator

A ring oscillator with 49 stage inverters and an output buffer is also studied. The transistors used in the ring oscillator have channel length of 0.15 \( \mu \text{m} \) and channel width of 1.5 \( \mu \text{m} \) (nMOS) and 2 \( \mu \text{m} \) (pMOS). Both n- and pMOSFETs have 10 Å of SiO\(_2\) and 30 Å of HfO\(_2\) dielectric in the polysilicon gate. The ring oscillator was biased either at the normal mode of operation \((V_{DD} = 2.8 \text{ V})\) or at the stress mode \((V_{DD} = 0 \text{ V})\). The gate bias for the first stage is 4 V. The gate current was monitored during stress. Once a jump in the gate current was observed, the bias was then stopped to record the transistor characteristics. After the measurement, the ring oscillator was stress continuously. The gate current during stress is shown in Fig. 11 (a). In this figure, the nMOS breaks down at positions 2, 3, and 5 and pMOS breaks down at positions 4 and 6. The corresponding measured oscillation waveforms are displayed in Fig. 11 (b). As seen in Fig. 11(b), the ring oscillator remains functional after soft and hard breakdown. Fig. 11(c) shows the normalized degradation in oscillation frequency and amplitude at various breakdown points.

6.7.3 Low Noise Amplifier

A folded low noise amplifier is used as an example to demonstrate the RF performance degradation [19] in analog application subject to breakdown. The folded structure is preferred for low-voltage design [119]. The devices used in the LNA have 0.15 \( \mu \text{m} \) channel length. The nMOS transistor has 100 fingers with 10 \( \mu \text{m} \) each and the pMOS transistor has 50 fingers with 20\( \mu \text{m} \) each. The supply voltage is 1.5 V and the gate bias is 1 V. The biasing of the circuit is consistent with the device measurement for the model parameters extraction.
(a)

Point #1 (f = 75.376 MHz, Vamp = 2.76 V)

Point #5 (f = 75.106 MHz, Vamp = 1.84 V)

Point #3 (f = 75.248 MHz, Vamp = 2.03 V)

Point #6 (f = 74.990 MHz, Vamp = 1.17 V)

(b)
As the first stage of a receiver, the essential requirements of an LNA are low noise and high gain. Moreover, the matching conditions are also important in the LNA for power delivery and noise optimization. The breakdown in nMOS has a significant impact on the matching condition of the LNA, while the breakdown in pMOS has little effect on S-parameters (data shown in Table II). The noise figure versus frequency is plotted in Fig. 12. The noise figure degradation subject to nMOS breakdown is much more significant than that to pMOS breakdown because the input transistor dominates the overall noise figure of the LNA. Leakage current exists across the gate oxide forming a noise source to the transistor. In addition, the drastic
increase in gate current due to breakdown increases the real part of the input impedance. This affects the impedance matching. Thus, the low noise amplifier performance is degraded. However, the breakdown location has virtually no impact on the noise figure of the LNA.

Figure 6.16. Noise figure versus frequency for a 50 Ω output before and after breakdown
Figure 6.17. Noise figure degradation due to breakdown in LNA
CHAPTER SEVEN: CONCLUSIONS

7.1 Achievement

This dissertation has studied the voltage and temperature stress-induced performance degradation in CMOS devices and circuits. An improved model, which is extracted from the measured data, is used to evaluate the RF performance degradation in MOSFETs due to voltage and temperature. Good agreement between measurement and simulation has verified the accuracy of the model. Dynamic stress effects, which cause a smaller degradation than DC stress, are first investigated in RFICs. The investigations of performance degradation due to stress in MOSFET in low noise amplifier, mixer, oscillator, power amplifier are studied. The channel hot carrier and dielectric breakdown-induced DC and RF performance degradations in 60 nm high-k nMOSFETs are examined experimentally. RF performances such as the cutoff frequency, noise figure, linearity, and flicker noise of high-k MOSFETs show vulnerability to the HC/BD effect. Analytical equations for normalized RF degradations relating to the device DC and AC parameters are derived. This method provides a practical and simply way to evaluate the performance degradation in devices and circuits due to voltage and temperature stresses.

7.2 Future Work

Voltage stress-induced effects on the VLSI performance are practical and important issues in the future VLSI designs with the devices scaling into sub-micron or even nano-scale. However, these issues have not been studied systematically so far. One of the major reasons is
that it is really difficult to determine which parts of the system suffer from the stress-induced effects. To study the reliability problem is also not practical when the voltage stress on the whole system. Therefore, the simulation presents a suitable way to study these kinds of effects. The VLSIs – SDRAM, PLL, and ADC will be considered for my future research.
APPENDIX A. PARAMETERS EXTRACTION FOR RF MODEL
The equivalent circuit for the RF model presented in Chapter Two is given in Fig. A1. The extraction method based on the assumptions that (1) terminal resistances and substrate network equivalent resistances are bias- and frequency-independent; (2) $C_{gb} \ll C_{gd}$, $C_{gs}$ in the saturation region and $C_{gg} \approx C_{gd} + C_{gs}$; (3) $R_{dsb} \ll R_{db}$, $R_{sb}$ and $R_{db} \approx R_{sb}$ for the single-finger device [16]; and (4) $I_{mb} \ll I_m$, $I_{mb}$ is the substrate current, $I_m (\approx g_m V_{gd})$ is the drain current.

The ‘Π’ network consisting of $R_{db}$, $R_{sb}$, and $R_{dsb}$ in the substrate network is transferred to ‘Y’ network consisting of $R_1$, $R_2$, and $R_3$ as shown in Fig. A2 (a). The ‘Y’ network is transferred back to the ‘Π’ network ($Y_4$, $Y_5$ and $Y_6$) after combining $R_1$ and $C_{sb}$ to $Z_1$, $R_2$ and $C_{db}$ to $Z_2$. Further, we combined $Y_4$ and $R_{gd}$ to $Y_4'$, $Y_5$, and $R_s$ to $Y_5'$. Then, one obtains:

\[
Y_4' = Y_4 + 1/R_{db}
\]
\[
\approx 1/R_{ds} - \frac{\omega^2 R_{db} C_{sb} C_{db}}{4} [2 - j \omega (C_{sb} + C_{db}) R_{db}]
\]

(A1)

\[
Y_5' = Y_5 + 1/R_s \approx 1/R_s + j \omega C_{sb}
\]

(A2)

\[
Y_6' \approx R_{db} \omega^2 (C_{db}^2 + C_{db} C_{sb})/2 + j \omega C_{db}
\]

(A3)

\[
Y_7 = j \omega C_{gs} + 1/R_{gs}
\]

(A4)

\[
Y_8 = j \omega C_{gd} + 1/R_{gd}
\]

(A5)

After the transformation, one obtains the simplified equivalent circuit in Fig. A2 (b) and $Y$-parameters ($Y'$) of the network without the influence of $R_s$ and $R_d$ are given as:

\[
Y_{11}' = \frac{Y_7}{g_m + Y_7 + Y_4' + Y_5'} + Y_8
\]

(A6)

\[
Y_{12}' = -\frac{Y_4' Y_7}{g_m + Y_7 + Y_4' + Y_5'} - Y_8
\]

(A7)
\[ Y_{21}' = \frac{g_m Y_5' - Y_4' Y_7'}{g_m + Y_7' + Y_4' Y_5'} - Y_8 \]  \hspace{1cm} (A8)

\[ Y_{22}' = Y_8 + Y_6' - Y_4' \frac{Y_7' + Y_5'}{g_m + Y_7' + Y_4' Y_5'} \]  \hspace{1cm} (A9)

Taking into account \( R_g \) and \( R_d \), \( Y \)-parameters of the whole equivalent circuit is given as:

\[ Y_{11} = \frac{Y_{11} - Y_{12} Y_{21}' R_g}{1 + R_g Y_{11} - Y_{12}' Y_{21}' R_g R_g / (1 + R_g Y_{22}') \right) \approx \frac{1}{R_g} + \frac{1}{R_{gd}} + \omega^2 C_{gd}^2 R_g + \omega^2 C_{gd}^2 R_g + j\omega C_{gd} \]  \hspace{1cm} (A10)

\[ Y_{12} = \frac{Y_{12} - Y_{11} Y_{22}' R_g}{1 + R_g Y_{12} - Y_{11}' Y_{22}' R_g R_g / (1 + R_g Y_{12}') \right) \approx \frac{1}{R_g} + \frac{1}{R_{gd}} + \omega^2 C_{gd}^2 R_g - 1/R_g - \omega^2 C_{gd}^2 C_{gd} R_g - j\omega C_{gd} \]  \hspace{1cm} (A11)

\[ Y_{21} = \frac{Y_{21} - Y_{21}' Y_{11}' R_g}{1 + R_g Y_{22} - Y_{21}' Y_{21}' R_g R_g / (1 + R_g Y_{11}') \right) \approx \frac{1}{R_g} - \frac{1}{R_{gd}} - \omega^2 C_{gd}^2 C_{gd} R_g - \omega^2 (C_{gd} + C_{db}) C_{gd} R_g - j\omega (C_{gd} + g_m C_{gd} R_g) \]  \hspace{1cm} (A12)

\[ Y_{22} = \frac{Y_{22} - Y_{21} Y_{21}' R_g}{1 + R_g Y_{22} - Y_{21}' Y_{21}' R_g R_g / (1 + R_g Y_{11}') \right) \approx j\omega (C_{gd} + C_{db}) + 1/R_{gd} + 1/R_{db} + \frac{R_{dd}}{2} \omega^2 C_{dd}^2 + \omega^2 C_{gd}^2 R_g \]  \hspace{1cm} (A13)
Fig. A1 The equivalent circuit for the RF model

Fig. A2 Simplified models (a) and (b)
APPENDIX B. COEFFICIENTS OF VOLTERRA SERIES
Kirchhoff’s voltage law (KVL) for the small-signal model shown in Fig. 3.1 gives

\[ v_{in} = Z_g(i_{gs} + i_{gd}) + v_{gs} + Z_s(i_{gs} + g_m V_{gs} + i_{ds}) \]  

(B1)

where

\[ i_{ds} = g_{ds}(C_{gd}sV_{gs} + i_d - g_m V_{gs})/(g_{ds} + C_{gs}s) \]  

(B2)

\[ i_{gl} = g_{ml}V_{gs} - i_d + g_{mL}(C_{gl}sV_{gs} + i_d - g_m V_{gs})/(g_{ds} + C_{gs}s) \]  

(B3)

Combining (B1), (B2) and (B3), one gets

\[ v_{in} = \alpha(s)i_d + [1 + \beta(s)]v_{gs} \]  

(B4)

where

\[ \alpha(s) = (g_{ds}Z_s - C_{gs}sZ_g)/(g_{ds} + C_{gs}s) \]  

(B5)

\[ \beta(s) = (Z_g + Z_s)[C_{gs}s + g_{ml}(C_{gl}sV_{gs} + i_d - g_m V_{gs})/(g_{ds} + C_{gs}s)] \]  

(B6)

In the saturation region, the drain current can be expressed in the Taylor series as

\[ i_d = T_1v_{gs} + T_2v_{gs}^2 + T_3v_{gs}^3 + T_4v_{gs}^4 + T_5v_{gs}^5 + ...... \]  

(B7)

In the Volterra series form, \( v_{gs} \) is given by

\[ v_{gs} = C_1(s)v_{in} + C_2(s_1, s_2)v_{in}^2 + C_3(s_1, s_2, s_3)v_{in}^3 + ... \]  

(B8)

Combining (B4), (B7) and (B8) yields

\[ C_1(s) = 1 / (1 + \beta(s) + T_1\alpha(s)) \]  

(B9)

\[ C_2(s_1, s_2) = -\frac{T_2C_1(s_1)C_1(s_2)\alpha(s_1 + s_2)}{1 + \beta(s_1 + s_2) + T_1\alpha(s_1 + s_2)} \]  

(B10)
\[ C_3(s_1, s_2, s_3) = -\frac{\alpha(s_1, s_2, s_3)[2T_i C_i C_2 + T_i C_i C_1(s_1)C_i(s_2)C_i(s_3)]}{1 + \beta(s_1, s_2, s_3) + T_i \alpha(s_1, s_2, s_3)} \]  

(B11)

\[ \overline{C_1 C_2} = \frac{[C_1(s_1)C_2(s_2, s_3) + C_1(s_2)C_2(s_1, s_3) + C_1(s_3)C_2(s_1, s_2)]}{3} \]  

(B12)

The Volterra series is

\[ i_d = A_1(s)v_{in} + A_2(s_1, s_2)v_{in}^2 + A_3(s_1, s_2, s_3)v_{in}^3 + \ldots \]  

(B13)

Combining (B7), (B8) and (B13) gives

\[ A_1(s) = T_i C_1(s) \]  

(B14)

\[ A_2(s_1, s_2) = T_i C_2(s_1, s_2) + T_i C_1(s_1)C_1(s_2) \]  

(B15)

\[ A_3(s_1, s_2, s_3) = T_i C_3(s_1, s_2, s_3) + 2T_i \overline{C_1 C_2} \]  
\[ + T_i C_1(s_1)C_1(s_2)C_1(s_3) \]  

(B16)
APPENDIX C. TRANSFORMATION BETWEEN S- TO Y- PARAMETERS
$Y$- and $S$-parameters provide a complete description of the network. $Y$-parameters relate the total voltages and currents at the ports, while $S$-parameters relate the voltage waves incident on the ports to those reflected from the ports. For a two-port network, $S_{11}$ is the input reflection coefficient, and the squared magnitude of $S_{21}$ is the forward transducer power gain with $Z_0$ (characteristic impedance) as source and lead impedance. $S_{22}$ is the output reflection coefficient, and the squared magnitude of $S_{12}$ is the reverse transducer power gain with $Z_0$ as source and lead impedance. The transformation between $Y$-parameters and $S$-parameters for two-port network is:

$$Y_{11} = \frac{Y_0 \left(1 - S_{11}\right) \left(1 + S_{22}\right) + S_{12} S_{21}}{\left(1 + S_{11}\right) \left(1 + S_{22}\right) - S_{12} S_{21}}$$  \hspace{1cm} (C1)$$

$$Y_{12} = \frac{-2S_{12}}{\left(1 + S_{11}\right) \left(1 + S_{22}\right) - S_{12} S_{21}}$$  \hspace{1cm} (C2)$$

$$Y_{21} = \frac{-2S_{21}}{\left(1 + S_{11}\right) \left(1 + S_{22}\right) - S_{12} S_{21}}$$  \hspace{1cm} (C3)$$

$$Y_{22} = \frac{Y_0 \left(1 + S_{11}\right) \left(1 - S_{22}\right) + S_{12} S_{21}}{\left(1 + S_{11}\right) \left(1 + S_{22}\right) - S_{12} S_{21}}$$  \hspace{1cm} (C4)$$

where $Y_0$ is the characteristic conductance, which is often $1/50$ $\text{S}$ in the practical situations.
APPENDIX D. NORMALIZED DEGRADATION IN FOM
From the equations (1), one gets the degradation of cutoff frequency:

\[ f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \]

\[ \Rightarrow \Delta f_T \approx \Delta g_m \cdot \frac{\partial f_T}{\partial g_m} + \Delta C_{gd} \cdot \frac{\partial f_T}{\partial C_{gd}} + \Delta C_{gs} \cdot \frac{\partial f_T}{\partial C_{gs}} \]

\[ = \Delta g_m \frac{1}{2\pi(C_{gd} + C_{gs})} - (\Delta C_{gd} + \Delta C_{gs}) \frac{g_m}{2\pi(C_{gd} + C_{gs})^2} \]

\[ = \frac{\Delta g_m}{g_m} \frac{1}{f_T} = \frac{\Delta(C_{gd} + C_{gs})}{C_{gd} + C_{gs}} \frac{g_m}{f_T} \]  

\[
(D1)
\]

The parasitic capacitances of MOSFETs can be extracted from \( Y \)-parameters:

\[ C_{gd} + C_{gs} = C_{gs} \approx \frac{\text{Im}(Y11)}{\omega} \]  

\[
(D2)
\]

The normalized degradation of cutoff frequency can be expressed as:

\[ -\frac{\Delta f_T}{f_T} = -\frac{\Delta g_m}{g_m} + \frac{\Delta(C_{gd} + C_{gs})}{C_{gd} + C_{gs}} \]

\[ = -\frac{\Delta g_m}{g_m} + \frac{\Delta \text{Im}(Y11)}{\text{Im}(Y11)} \]  

\[
(D3)
\]

The minimum noise figure is

\[ NF_{\text{min}} = 1 + 2\pi K f (C_{gs} + C_{gd}) \sqrt{\frac{R_G + R_S}{g_m}} \]  

\[
(D4)
\]

The normalized shifts of fitting coefficient \( (\Delta K_f / K_f) \) are 0.2\% after 2400s stress and 0.3\% after 4800s stress. \( \Delta K_f / K_f \ll \max\left\{ \frac{\Delta(C_{gs} + C_{gd})}{C_{gs} + C_{gd}}, \frac{\Delta(R_G + R_{gd})}{(R_G + R_{gd})}, \frac{\Delta g_m}{g_m} \right\} \). Therefore, the degradation of minimum noise figure can be express as:
\[ \Delta N F_{\text{min}} \approx \Delta (C_{gs} + C_{gd}) \cdot \frac{\partial N F_{\text{min}}}{\partial (C_{gs} + C_{gd})} + \Delta (R_G + R_S) \cdot \frac{\partial N F_{\text{min}}}{\partial (R_G + R_S)} + 1 \cdot \frac{\partial g_m}{g_m} \cdot \frac{\partial N F_{\text{min}}}{\partial g_m} \]

\[ = \frac{\Delta (C_{gs} + C_{gd})}{(C_{gs} + C_{gd})} \cdot 2\pi K_f f(C_{gs} + C_{gd}) \sqrt{\frac{R_G + R_S}{g_m}} \]

\[ + \frac{1}{2} \frac{\Delta (R_G + R_S)}{(R_G + R_S)} \cdot 2\pi K_f f(C_{gs} + C_{gd}) \sqrt{\frac{R_G + R_S}{g_m}} \]

\[ - \frac{1}{2} \frac{\Delta g_m}{g_m} \cdot 2\pi K_f f(C_{gs} + C_{gd}) \sqrt{\frac{R_G + R_S}{g_m}} \]

\[ = \frac{\Delta (C_{gs} + C_{gd})}{(C_{gs} + C_{gd})} \cdot (N F_{\text{min}} - 1) + \frac{1}{2} \frac{\Delta (R_G + R_S)}{(R_G + R_S)} \cdot (N F_{\text{min}} - 1) - \frac{1}{2} \frac{\Delta g_m}{g_m} \cdot (N F_{\text{min}} - 1) \]

\[ \Rightarrow \frac{\Delta N F_{\text{min}}}{N F_{\text{min}} - 1} = \frac{\Delta (C_{gs} + C_{gd})}{C_{gs} + C_{gd}} + \frac{1}{2} \frac{\Delta (R_G + R_S)}{R_G + R_S} - \frac{1}{2} \frac{\Delta g_m}{g_m} \]

The terminal resistances can be extracted from Z-parameters when \( \omega < 2\pi \times 10^{10} \) rad/s:

\[ R_G + R_S \approx \text{Re}(Z_{11}) - \frac{1}{g_m} \] (D6)

Therefore, the normalized degradation of minimum noise figure can be expressed as:

\[ \frac{\Delta N F_{\text{min}}}{N F_{\text{min}} - 1} \approx \frac{\Delta \text{Im} Y_{11}}{\text{Im} Y_{11}} + c_1 \frac{\Delta \text{Re} Z_{11}}{\text{Re} Z_{11}} + c_2 \frac{\Delta g_m}{g_m} \] (D7)

where \( c_1 \) and \( c_2 \) are coefficients and \( c_1 = \frac{1}{2} \frac{\text{Re} Z_{11}}{\text{Re} Z_{11} - 1/g_m} \), \( c_2 = -\frac{1}{2} \frac{\text{Re} Z_{11} - 3/g_m}{\text{Re} Z_{11} - 1/g_m} \).

Similarly,
\[ II_{P3} = -\frac{2}{3} g_m \frac{1}{R_{IN}} \]

\[ \Delta II_{P3} \approx \Delta g_m \cdot \frac{\partial II_{P3}}{\partial g_m} + \Delta g_{m3} \cdot \frac{\partial II_{P3}}{\partial g_{m3}} \]

\[ = -\frac{\Delta g_m}{g_m} \frac{2}{3} \frac{g_m}{R_{IN}} \frac{1}{g_{m3}} \frac{2}{3} \frac{g_m}{R_{IN}} \]

\[ = -\frac{\Delta g_m}{g_m} II_{P3} + \frac{\Delta g_{m3}}{g_{m3}} II_{P3} \]

\[ \Rightarrow \frac{\Delta II_{P3}}{II_{P3}} \approx -\frac{\Delta g_m}{g_m} + \frac{\Delta g_{m3}}{g_{m3}} \]

In the saturation region, the transconductance \( g_m \approx \frac{\mu C_{ox} W}{L} V_{GT} \). Combining with Eqn. (4), one gets

\[ S_{ld} = \frac{K' g_m V_{GT}^\mu}{f^\alpha L^2} \]

(D9)

The fitting factor \((K')\) keeps unchanged after stress. Therefore,

\[ \Delta S_{ld} \approx \Delta \alpha \cdot \frac{\partial S_{ld}}{\partial \alpha} + \Delta g_m \cdot \frac{\partial S_{ld}}{\partial g_m} + \Delta V_{GT} \cdot \frac{\partial S_{ld}}{\partial V_{GT}} + \Delta \mu \cdot \frac{\partial S_{ld}}{\partial \mu} \]

\[ = -\alpha \ln f \cdot \frac{\Delta \alpha}{\alpha} \frac{K' g_m V_{GT}^\mu}{f^\alpha L^2} + \frac{\Delta g_m}{g_m} \frac{K' g_m V_{GT}^\mu}{f^\alpha L^2} + \frac{\Delta V_{GT}}{V_{GT}} \frac{\Delta \mu}{\mu} \frac{K' g_m V_{GT}^\mu}{f^\alpha L^2} \]

\[ \Rightarrow \]

\[ \frac{\Delta S_{ld}}{S_{ld}} \approx c_3 \frac{\Delta \alpha}{\alpha} + \frac{\Delta V_{GT}}{V_{GT}} + \frac{\Delta \mu}{\mu} + \frac{\Delta g_m}{g_m} \]

where \( c_3 = -\alpha \ln f^\alpha \).
APPENDIX E. NORMALIZED DEGRADATION IN LNA
The power gain and minimum noise figure for two-stage cascade LNA are [110]:

\[ G \approx (g_{m1} \cdot R_L)^2 \]  \hspace{1cm} (E1)

\[ NF_{\text{min}} \approx 1 + K'' \omega \frac{C_{g_{s1}}}{g_{m1}} \]  \hspace{1cm} (E2)

where \( g_{m1} \) is the transconductance of the device for the first stage, \( R_L \) is the equivalent output resistance, \( K'' \) is a coefficient, \( C_{g_{s1}} \) is the equivalent capacitor between the gate and the source of the device for the first stage.

From (E1) and (E2), one can get:

\[
\frac{\Delta G}{G} \approx \Delta g_{m1} \cdot \frac{\partial G}{\partial g_{m1}} \cdot \frac{1}{g_{m1}} \\
= \Delta g_{m1} \cdot 2 g_{m1} R_L^2 \cdot \frac{1}{(g_{m1} R_L)^2} \\
= \frac{2 \Delta g_{m1}}{g_{m1}}
\]  \hspace{1cm} (E3)

\[
\Delta NF_{\text{min}} \approx \Delta C_{g_{s1}} \cdot \frac{\partial NF_{\text{min}}}{\partial C_{g_{s1}}} + \Delta g_{m1} \cdot \frac{\partial NF_{\text{min}}}{\partial g_{m1}} \\
= \frac{\Delta C_{g_{s1}}}{C_{g_{s1}}} \cdot K'' \omega \frac{C_{g_{s1}}}{g_{m1}} - \Delta g_{m1} \cdot K'' \omega \frac{C_{g_{s1}}}{g_{m1}} \\
\Rightarrow \frac{\Delta NF_{\text{min}}}{NF_{\text{min}} - 1} \approx \frac{\Delta g_{m1}}{g_{m1}} + \frac{\Delta C_{g_{s1}}}{C_{g_{s1}}}
\]  \hspace{1cm} (E4)
APPENDIX F. DERIVATION FOR THE GATE LEAKAGE CURRENT
The surface potential is given by [120]:

\[ \phi_s(x) = \phi_m + H[1 - \sqrt{1 - \frac{2 \phi}{H}(x-x_m)}] \]  

(F1)

where \( \phi_m = (\phi_s + \phi_{sd})/2 \) is the midpoint potential, \( \phi_s \) and \( \phi_{sd} \) denote the surface potentials at the source and drain ends of the channel respectively, \( x_m = \frac{1}{2}(1 + \frac{\phi}{4H}) \) is the coordinate of the midpoint potential and \( H = (q_{im}/\alpha + \phi)(1 + \delta_0 \phi/r_1 V_c)^{-1} \), where \( q_{im} \) is the midpoint inversion charge, \( \alpha \) is the linearization coefficient, \( \phi \equiv kT/q \), \( \delta_0 \) is introduced to sharpen the drift velocity dependence on the lateral field, \( V_c = E_c L \) ( \( E_c \) is the critical field).

\( \phi_s \) as a function of \( \phi \) in the Taylor series is

\[ \phi_s = \phi_m + H \sum_{k=1}^{\infty} \frac{(2k-3)!!}{2^k} (x-x_m)(\frac{2 \phi}{H})^{1/2} \]

\[ \approx \phi_m - \frac{1}{2} H (\frac{2 \phi}{H})^{1/2} + \frac{\phi}{2} \]  

(F2)

where \( \phi_m = (\phi_s + \phi_{sd})/2 \approx \frac{\eta}{2} V_{DS} \) and \( \phi = \phi_{sd} - \phi_s \approx \eta V_{DS} \).

(F2) reduces to

\[ \phi_s = aV_{DS} + b\sqrt{V_{DS}} \]  

(F3)

The voltage across the dielectrics is given by

\[ V_{Cross} = V_{GS} - \phi_s - V_{bi} = V_{GS} - aV_{DS} - b\sqrt{V_{DS}} - c \]  

(F4)

where \( V_{bi} \) is the built-in voltage.
Assume that the current density flow through the breakdown path at \( x \) is much larger than that of other position \((J_g(x) >> J_g(y), y \neq x)\). The gate leakage current is therefore

\[
I_g = W \int_0^L J_g(x)\,dx \\
\approx W \int_{x'}^{x'} J_g(x)\,dy \\
= J_g(x)A
\]  

(F5)

The current flows to the drain is

\[
I_{gd} = W \int_0^L J_g(y)\,dy \\
\approx W \int_{x'}^{x'} J_g(x)\,xdy \\
= xJ_g(x)A \\
= xI_g
\]  

(F6)

and the current flows to the source is

\[
I_{gs} = I_g - I_{gd} = (1-x)I_g
\]  

(F7)
LIST OF REFERENCES


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