The Effect Of Hot Carrier Stress On Low Noise Amplifier Radio Frequency Performance Under Weak And Strong Inversion

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THE EFFECT OF HOT CARRIER STRESS ON LOW NOISE AMPLIFIER RF PERFORMANCE UNDER WEAK AND STRONG INVERSION

by

LIN SHEN
B.S. University of Florida, 2004

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in the Department of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

Spring Term
2006
ABSTRACT

This thesis work is mainly focused on studying RF performance degradation of a low noise amplifier (LNA) circuit due to hot carrier effect (HCE) in both the weak and strong inversion regions. Since the figures of merit for the RF circuit characterization are gain, noise figure, input, and output matching, the LNA RF performance drift is evaluated in a Cadence SpectreRF simulator subject to these features. This thesis presents hot carrier induced degradation results of an LNA to show that the HCE phenomenon is one of the serious reliability issues in the aggressively scaled RF CMOS design, especially for long-term operation of these devices. The predicted degradation from simulation results can be used design reliable CMOS RF circuits.
To the greatest mom in the world, Hong Shen
ACKNOWLEDGMENTS

First of all, I am very grateful to have Dr. Yuan as my advisor. His passion and enthusiasm for teaching and research has had large influence on my graduate studies. I would like to thank him for tremendous support, guidance, and encouragement over the period of this work. Besides the wonderful advice Dr. Yuan has given me to help me to reach my academic goals, he has also taught me the meaning of life by sharing his life experience.

Next, I would like to thank Brian Chang for encouraging me and convincing me to attend graduate school. His strong support and good advice have benefited me in so many ways.

Third, I would like to thank my lab mate Chuanzhao Yu for his help throughout this work. His hard work and dedication has been a good example for me.

And lastly, I would like to give sincere gratitude to all of my relatives and friends for their endless support and caring. Without them, my life would not be complete.
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<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
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<td>AC</td>
<td>Alternating Current</td>
<td></td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
<td></td>
</tr>
<tr>
<td>BSIM3</td>
<td>Berkeley Short-Channel IGFET Model 3</td>
<td></td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
<td></td>
</tr>
<tr>
<td>DIBL</td>
<td>Drain Induced Barrier Lowering</td>
<td></td>
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<tr>
<td>GHz</td>
<td>Gigahertz</td>
<td></td>
</tr>
<tr>
<td>GPS</td>
<td>Global Position System</td>
<td></td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communication</td>
<td></td>
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<tr>
<td>HCE</td>
<td>Hot Carrier Effect</td>
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<tr>
<td>HCS</td>
<td>Hot Carrier Stress</td>
<td></td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
<td></td>
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<tr>
<td>IGFET</td>
<td>Insulated Gate Field Effect Transistor</td>
<td></td>
</tr>
<tr>
<td>IIP3</td>
<td>Input Third Order Intercept Point</td>
<td></td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
<td></td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
<td></td>
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<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<tr>
<td>NF</td>
<td>Noise Figure</td>
<td></td>
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<tr>
<td>nMOSFET</td>
<td>N-type Metal Oxide Semiconductor Field Effect Transistor</td>
<td></td>
</tr>
<tr>
<td>IIP3</td>
<td>Third-Order Intercept Point</td>
<td></td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
<td></td>
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<td>---</td>
<td>---</td>
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<tr>
<td>S</td>
<td>Scattering</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td></td>
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<tr>
<td>VCO</td>
<td>Voltage Control Oscillator</td>
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</table>
CHAPTER ONE: INTRODUCTION

1.1 Motivation

A lot of research has been done in Complementary Metal Oxide Semiconductor (CMOS) technology because of its low cost, high speed, and high integration capability. The CMOS combines both a p-channel MOSFET (pMOSFET) and an n-channel MOSFET (nMOSFET). Due to continuous decrease in channel length of MOSFETs into deep micrometer range, its maximum useable frequency has gone up to a few GHzs. Therefore, CMOS processes have been frequently adopted in the design of radio frequency (RF) communication.

In the past few years, the wireless communication industry has grown tremendously. Cordless telephones, GSM, GPS, Blue Tooth, and notebook computers are some of the most widely used portable computing and communication devices in our daily lives. A majority of these applications demand a transceiver of small size, which utilizes as low amount of power as possible to maximize battery lifetime. In very low power applications, the use of MOSFETs operating in the weak inversion region is very attractive. In [1], a full demonstration of weak inversion operation of MOSFETs can be used expediently to design both analog DC and AC circuits, especially in CMOS technology.

A low power LNA is suitable for wireless sensor network, and a few other wireless applications that require very low power consumption [2]. A single front-end narrow band LNA circuitry has been designed and simulated as part of this thesis. The LNA has three major parts of design
specifications consisting of input matching, gain, and noise. These will be further discussed in later chapters.

The advancement of CMOS technology has led to larger electrical field and higher carrier velocity in MOSFET’s which results in faster switching speed. However, this also results in “Hot Carriers,” which are carriers that have gained enough energy while traversing the channel region to be injected into the gate oxide. MOSFET leakage has also increased rapidly. According to [3], device scaling increases the transistor leakage by 5 times with every new generation of CMOS technology. The transistor leakage current includes subthreshold and gate leakage currents. That leakage power becomes a serious issue for portable computing and communication components such as the ones mentioned earlier due to shortened battery lifetime.

HCE phenomenon also causes device instability and can degrade the reliability of MOSFET devices. Therefore, it is necessary to demonstrate and study HC degradation results in terms of variation of the device parameters in CMOS RF circuits to provide guidance for avoiding such problems.

1.2 Thesis Outline

The current understanding of the physical mechanisms behind both weak and strong inversion is presented in Chapter Two. Based on the BSIM3 model, analytical equations of drain current from weak and strong inversion are listed. This chapter also highlights a major reliability issue
of aggressively scaled MOSFET – HCE phenomenon which causes physical HC degradation of device performance.

In Chapter Three, we describe the most important figures of merit for RF design. A single-ended LNA circuit design is adopted in this work. A design topology and steps of LNA are discussed in details in this chapter.

In Chapter Four, a more precise nMOSFET device is used in order to obtain more accurate results for before and after HCS. A list of figures and tables are shown to present the S-parameters and NF as the RF performance parameters of LNA in term of two comparisons. One is to compare LNA RF performance before and after HCS under strong inversion. The other one is a comparison of LNA RF performance under weak and strong inversion without HCS.
CHAPTER TWO: OVERVIEW OF MOSFETS

2.1 Strong Inversion Operation Region

2.1.1 Physical Explanation of Strong Inversion

In this thesis, a BSIM3 model, which was developed at the University of California, Berkeley, is used. It is the most accurate and popular short-channel MOSFET model used in the industry [4]. The SPICE Level 1, 2, and 3 Models can’t handle short channel effects because short channel devices were not available at the time when these models were developed. BSIM3 concentrates on incorporating the physical mechanisms involved in three regions of the device’s operation: the strong inversion region, the weak inversion (or subthreshold) region, and the transition region [5]. Since this thesis touches the first two of these three regions, BSIM3 model is an adequate model to use.

A schematic of a MOSFET is shown in Figure 2.1 [6]. Its operation is analogous to the operation of a water faucet. If the faucet is turned on, water can flow from the faucet (source) into the sink (drain). For example, in an nMOSFET, electrons will flow from the source terminal to the drain terminal when the gate terminal is charged. Normal operation of MOSFETs involves the region below the gate area, which is at the semiconductor-insulator interface, being inverted with minority charges to form a so-called “channel.” The threshold voltage ($V_{th}$) of the device plays a key role in determining the inversion of the channel.
In strong inversion, the density of the inverted n-channel is larger than the substrate doping concentration. Therefore, drift current is dominant. When gate voltage \( V_{gs} \) is less than \( V_{th} \), nothing happens; the device is described as “cut-off”.

In the strong inversion condition, as the increase of \( V_{gs} \) becomes larger than \( V_{th} \), the nMOSFET will experience three operation modes: linear, pinch off, and saturation modes. When \( V_{gs} \) is greater than \( V_{th} \), and drain voltage \( (V_{ds}) \) is small, an inversion layer or a channel is formed with charges. At that time, drain current \( I_{ds} \) flows from source to drain, and the nMOSFET acts like a resistor. Therefore, the linear region is entered.
If \( V_{ds} \) keeps increasing, it reaches the value of \( V_{dsat} (V_{dsat} = V_{gs} - V_{th}) \), which is called saturation voltage. The inversion layer charge near the drain decreases to zero eventually, and leaves a pinch off point at the drain. Therefore, this region is called the pinch off region or onset saturation region because the drain current starts to saturate.

The third operation region, the saturation region, is normally used when working with RF circuit design. Saturation occurs when \( V_{ds} \) starts to become much bigger compared to \( V_{dsat} \). In this region, the pinch off point moves towards the source, and the drain current remains constant because inside the channel, the potential is fixed at \( V_{dsat} \). See Figure 2.2 for more illustrations on these three operation modes.

![Figure 2.2: \( I_{ds} \) vs. \( V_{ds} \) plot](image)

---

6
2.1.2 Analytical Equations of $I_{ds}$ under Strong Inversion

The drain current equation in the linear region can be expressed as [5]

$$I_{ds} = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} \left( \frac{1}{4} \frac{V_{\text{ds}}}{E_{\text{sat}}} \right) \left( V_{\text{gs}} - V_{\text{th}} - \frac{V_{\text{ds}}}{2} \right) V_{\text{ds}}$$

where $\mu_{\text{eff}}$ is the effective mobility, $C_{\text{ox}}$ is the oxide capacitance per unit area, $W$ is the width of MOSFET, $L$ is the length of MOSFET, $V_{\text{ds}}$, $V_{\text{gs}}$, and $V_{\text{th}}$ are the drain to source voltage, gate to source voltage, and threshold voltage, respectively. $E_{\text{sat}}$ is the critical electrical field value at which the carrier velocity becomes saturated. This equation is accurate before carrier velocity saturates.

When the drain voltage is increased to a high value, the carrier velocity and the lateral electrical field near the drain saturates. Therefore the saturation current is expressed as [5]

$$I_{dsat} = \nu_{\text{sat}} W C_{\text{ox}} \frac{V_{\text{gs}}^2}{E_{\text{sat}} L + V_{\text{gs}}^2}$$

where $V_{\text{gs}}$ is equal to $V_{\text{gs}} - V_{\text{th}}$, and $\nu_{\text{sat}}$ is the saturated carrier velocity.

2.2 Weak Inversion Operation Region

2.2.1 Physical Explanation of Weak Inversion

In a simple model, drain current is assumed to be zero when $V_{\text{gs}}$ is less than $V_{\text{th}}$ [7]. However, this assumption is very inaccurate. When $V_{\text{gs}}$ of an nMOSFET is less than $V_{\text{th}}$, the device operates in the weak inversion or subthreshold region. The subthreshold region is also called the
weak inversion region owing to the small concentration of the minority electron carriers in the channel. In this region, the drain current falls to zero. However, in fact it never goes to zero, instead it decreases exponentially.

This small but finite subthreshold drain current flows between the drain terminal and source terminal, and is due to a finite concentration of the minority electron carriers near the oxide-substrate interface. In a weakly inverted MOSFET, diffusion current not drift current dominates the mechanism of drain current generation. Drift current is assumed to be zero under weak inversion. In the weak inversion region, the number of free electron carriers in the channel is very small. \( V_{ds} \) drops across the drain depletion region, therefore the majority electron carrier drift current is negligible. However, diffusion current flows in the channel and the MOSFET acts like an n-p-n Bipolar Junction Transistor (BJT).

The drain and source terminals behave like the collector and emitter terminals respectively, and the channel behaves like the base terminal. Similar to the exponential dependence of the collector current on the base-to-emitter voltage \( (V_{BE}) \), the subthreshold drain current is also exponentially dependent on \( V_{gs} \).

Of course, the MOSFET doesn’t move rapidly from the strong inversion region to the weak inversion region as drain current decreases. The transition region or moderate inversion region represents a transition from the strong inversion region to weak inversion region. In the moderate inversion region, both drift and diffusion components are important.
2.2.2 Analytical Equations of $I_d$ under Weak Inversion

In BSIM3, the drain current equation under weak inversion is [5]

$$I_d = I_0(1 - \exp\left(-\frac{V_{ds}}{V_{tm}}\right)) \exp\left(\frac{V_{gs} - V_{th} - V_{off} + \theta_{dibl} V_{ds}}{n V_{tm}}\right)$$

with

$$I_{so} = \mu_0 \frac{W}{L} \sqrt{\frac{q\varepsilon_{si}N_a V_{tm}^2}{2\phi_s}}$$

$$n = 1 + \sqrt{\frac{\varepsilon_{si}qN_{peak}}{2(\phi_s - V_{bs})C_{ox}}}$$

$$\theta_{dibl} = \exp\left(-\frac{L}{2l_t}\right) + 2 \exp\left(-\frac{L}{l_t}\right)$$

where, $V_{tm}$ is the thermal voltage given by $k_t T / q$, $V_{off}$ is the offset voltage, $\theta_{dibl} V_{ds}$ is the threshold voltage shift due to drain induced barrier lowering (DIBL) effect, and $n$ is the subthreshold swing parameter.

2.3 Comparison of Analog Circuits under Weak and Strong Inversion

The accuracy of drain current is very significant in analog circuits, however it may not be a problem in digital circuits [7]. Since analog circuit design takes place in the weak inversion region, it is important to know the advantages and disadvantages of operating in weak inversion compared to operating in strong inversion.

A list of disadvantages of operating in weak inversion are summarized below:

1. Operating below the strong inversion region leads to a lower bandwidth ($f_T$).
2. The weak inversion region also has worse noise performance (NF).

3. When analog circuits operate at very low currents, poor linearity is expected.

Besides the disadvantages of operating in the weak inversion region, there are still some good reasons to design analog circuits in this region. They are the following:

1. Operating in weak inversion consumes less power. This is good for low power design.

2. Voltage gain is the greatest near the lower edge of the strong inversion region [7].

3. Total harmonic distortion (THD) of the output signal is reduced at the operating maximum voltage gain point [7].

2.4 MOSFETs Reliability Issue

2.4.1 Hot Carrier Effect Physical Mechanism

While MOSFET dimensions keep shrinking down into sub-micrometer regime, hot carrier effect becomes one of the major reliability concerns for RF design engineers [8]. There is excess thermal noise exhibited by sub-micron CMOS devices, and this noise is believed to arise from hot electron effects in the presence of high electric fields [9]. The channel length of the MOSFET keeps being scaled down but the power supply level is kept the same in order to maintain compatibility with circuits [10]. This leads to larger electrical field in the channel, which causes acceleration and heating of charge carriers. The majority of RF integrated circuits used in wireless devices are analog circuits, which are very sensitive to device parameter
variation [11]. Therefore, it is necessary to understand the MOSFET degradation phenomena, which is caused by hot electrons. In this thesis, a study of the hot carrier effect induced RF performance degradation of an LNA is presented, especially in the strong inversion region (saturation mode).

Although these high electric fields result in increased carrier velocities and hence a higher operating speed, as the electric field increases, the carrier velocity saturates at a certain critical field. Electric fields in excess of this value have no beneficial effects on device performance. On the contrary, under such high electric fields, the mobile carriers in the silicon substrate can attain relatively high energies and result in incorrect circuit operation through a variety of mechanisms [12] (Table 1). While most of these problems can be minimized, even eliminated in some cases, through appropriate circuit and device design, the injection of energetic carriers into the gate oxide and subsequent parameter shift through carrier trapping and interface trap generation poses one of the most significant long-term reliability concerns in extensively scaled MOSFETs.

Table 1 Mechanisms associated with performance degradation due to high electric fields in MOSFETs

<table>
<thead>
<tr>
<th>Carrier Energy (E)</th>
<th>Mechanism</th>
<th>Effect on Device Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E &gt; 1.12eV$</td>
<td>Light emission</td>
<td>Leakage currents</td>
</tr>
<tr>
<td>$1.3eV &lt; E &lt; 1.8eV$</td>
<td>Impact ionization</td>
<td>Snap-back, latch-up, leakage.</td>
</tr>
<tr>
<td>$E &gt; 3.2eV$</td>
<td>Hot-electron injection</td>
<td>Parameter shift due to carrier trapping and interface trap generation</td>
</tr>
<tr>
<td>$E &gt; 4.8eV$</td>
<td>Hot-hole injection</td>
<td></td>
</tr>
</tbody>
</table>
The hot electron effect is caused by the lateral channel electric field, $E_m$, which occurs at the drain end of the channel. As described in Figure 2.3 [13], because of the high $E_m$, impact ionization takes place. Those electron-hole pairs generated by impact ionization will produce photons by radiative recombination and cause light emission. Also, some of the holes will flow to the substrate and become substrate current. Some of the electrons will flow towards gate terminal and get trapped in gate oxide. Those trapped electrons cause defects in the oxide as well as damage to the interface between the oxide and substrate.

Figure 2.3: Conceptual view of the HCE problem

The HCS degrades the MOSFET performance by increasing its threshold voltage or by reducing its transconductance and drain current [14]. Eventually, the RF circuit’s reliability is affected when the MOSFET fails to meet some minimum accepted criterion for performance over its operation lifetime.
HCE occurs when there is very high electrical field in the channel near the drain terminal which means $V_{ds}$ is very high. This high field imparts enough energy to the electrons, which generates electron-hole pairs through impact ionization. The electrons are swept toward the drain and the holes are attracted to the substrate terminal, contributing to the substrate current $I_{sub}$, as shown in Figure 2.4 [10]. Some electrons, which have higher momentum than that of the barrier energy, gain enough energy to reach the substrate and oxide interface. Hence, these electrons are injected into the gate oxide, and account for gate current $I_g$.

![Figure 2.4: A schematic for hot carrier mechanisms](image)

**2.4.2 Comparison of Hot Carrier Effect under Weak and Strong Inversion**

As described in the above sections, $V_{gs}$ controls the number of carriers in the channel. Under strong inversion, there are much more electrons in the channel than when under weak inversion.
Therefore, carriers injected into the gate oxide are a function of $V_{gs}$ and $V_{ds}$. Their relation is summarized in Figure 2.5 below:

![Figure 2.5: The relationship between the injection of carriers and $V_{gs}$, $V_{ds}$](image)

As we can see from Figure 2.5, during weak inversion operation, MOSFETs are less vulnerable to HCE due to a low amount of carrier injection. Therefore, this thesis work will only focus on studying the behavior of HC induced performance degradation in LNA operating in the strong inversion region.
CHAPTER THREE: REVIEW OF LNA DESIGN

3.1 General RF Design

3.1.1 RF Design Specifications

The design space for RF circuit design is very wide. RF design specifications are the following:

1. Power Dissipation
2. Supply Voltage
3. Noise
4. Linearity
5. Gain
6. Input/Output Impedance
7. Voltage Swings
8. Speed

Many of these parameters can be exchanged with one another, thus complicating the job of the designer. This can be described by the "Analog Design Octagon" [15] shown in Figure 3.1.
3.1.2 High Frequency Figures of Merit

The first figure of merit is the cut off frequency \( f_T \) at which current gain is 0 dB. It is the most common expression for high frequency in a MOSFET. It assumes that the drain is terminated in an incremental short circuit while the gate is driven by an ideal current source. Due to these assumptions, this figure fails to account for the effect of drain-bulk capacitance, series gate resistance and the feed forward contribution of drain-to-source capacitance. A simple approximation gives us the following simple relationship [11]:

\[
 f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad \text{(Hz)}
\]

where \( g_m \) is the transconductance of a MOSFET, \( C_{gs} \) and \( C_{gd} \) are gate-to-source and gate-to-drain capacitances, respectively.
A simple approximation gives us the following simple relationship:

$$\omega_T \approx \frac{g_{m}}{C_{gs}} \text{ (rad/s)}$$

This expression is an approximation because the $C_{gd}$ is neglected.

The second figure of merit is maximum frequency ($f_{\text{max}}$) at which the power gain reaches 0 dB. This gain becomes unity at the frequency in which

$$f_{\text{max}} = \frac{f_T}{2\sqrt{(R_g + R_{in})(g_{ds} + 2\pi f_T C_{gd})}} \text{ (Hz)}$$

where $g_{ds}$ is the output conductance, $R_{in}$ is the input resistance consisting of gate, source, and channel components and $R_g$ is the gate resistance.

### 3.2 Review of LNA Design

#### 3.2.1 Introduction

LNAs, voltage control oscillators (VCOs) and mixers are three critical building blocks in RF front-end wireless receivers. They are shown in Figure 3.2 [16].

As shown in Figure 3.2, the LNA amplifies the input RF signal, which is detected by the antenna, while introducing a minimum amount of noise to the signal. The mixer translates the input RF signal down to intermediate frequency (IF). The other input to the mixer is the local oscillator (LO) signal provided by a VCO inside a frequency synthesizer. In a receiver design, it is critical
to have a good front end in order to have good overall system performance. The front end LNA plays a key role in the receiver since it is the first block of this architecture [8].

![Antenna](image)

**Figure 3.2: A simple wireless receiver structure**

The first stage of a receiver is the LNA, which amplifies the weak signal coming from the antenna. The noise factor (F) is a figure of merit of noise produced by amplifiers and mixers. It is defined in general as

\[
F = \frac{\text{Total output noise}}{\text{Total output noise due to the source}}
\]

The equation to calculate F is [16]

\[
F = \frac{P_A + P_{50\Omega}}{P_{50\Omega}}
\]

where \(P_A\) is the noise power due to the LNA, and \(P_{50\Omega}\) is the noise power due to the thermal noise of a 50ohm resistor.
For a cascaded receiver system, shown in Figure 3.3, $F_1$ and $F_2$ represent the noise factor of the first and second stages. $G_1$ and $G_2$ are the gain for the first and second stages.

The $F$ of the entire cascaded receiver system can be calculated using the following equation:

$$F_{tot} = F_1 + \frac{F_2}{G_1}$$

The $F$ of the entire cascaded receiver is dominated by the $F$ of the first stage. It is seen that the noise content of the block gets directly added while the noise figure (NF) of remaining stages are degraded by gains of previous stages. Hence a proper design needs to be done for this stage in order to suppress the next stage’s noise contribution. This produces a good power gain and minimum noise contribution in the receiver front-end. This gain ($G$) can be represented as $S_{21}$, one of the S-parameters of LNAs.

However, NF is used instead of $F$ to characterize LNAs. The equation to calculate NF is given by the following:
The figure of merit for the characterization of RF performance is $NF_{\text{min}}$. $NF_{\text{min}}$ can be expressed as follows [11]:

$$TF_{\text{min}} = 1 + K \sum_{f_i}^f \sqrt{g_m(R_\text{i} + R_\text{f} + R_\text{c})}$$

where $K$ is a constant.

Another LNA design specification that needs to be mentioned is the third order intercept point (IIP3). It is a figure of merit for linearity or distortion. We want the IIP3 value of an LNA to be as high as possible to obtain better linearity and less distortion. Due to the nature of imperfect linearity, the LNA produces two third-order intermodulation (IM3) products, which are very close in frequency to the desired signals as shown in Figure 3.4.

![Figure 3.4: IM3 in a nonlinear system](image-url)
If the difference between $\omega_1$ and $\omega_2$ of the input signals is small, then IM3 products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will be located very near to the fundamental signals. These unwanted signals may cause errors in the detection of the wanted signals. They are hard to remove by filtering. To reduce these IM3 distortion products, the IIP3 specification needs to be as high as possible. The higher the value of IIP3, the lower the IM3 distortion will be. In Figure 3.5, IIP3 is plotted [16].

![Figure 3.5: IIP3 interception](image)

The intercept of line A and line B in Figure 3.5 is IIP3. The input power at this point is the input IIP3 and the output power is output IIP3. Line A is the output power vs. input power curve for
the fundamental signal. Line B is the IM3 distortion output power vs. input power curve. The term dBc means the number of dB below the fundamental.

While dealing with the receiver's front-end LNA, another important factor also needs to be considered. The LNA is connected to the antenna directly or through a transmission line. For maximum power transfer between these two, the input impedance of the LNA should be equal to the output impedance of the line. The transmission lines have very low characteristic impedance (generally 50 Ω). Hence the LNA has to be custom designed for low input impedance equal to 50 Ω. S_{11}, one of the scattering (S) parameters of LNAs, is called the input reflection coefficient, and is used to measure the input matching condition. The LNA output impedance should be matched closely to 50 Ω to maximize the transferred power to the load. This output matching can be presented by S_{22}, the output reflection coefficient. Therefore, LNA input and output matching is very important in the design. Finally, the LNA must have good reverse isolation in order to prevent the LO signal produced by the mixer from traveling backwards through the LNA into the antenna. It is used to reduce the LO leakage phenomenon. This reverse isolation can also be represented by S_{12}, known as the reverse transmission coefficient. In addition to the above LNA S-parameters, the stability of LNA’s is a big concern also. To calculate the stability of a transistor with S-parameters, the intermediate quantity, D_s must be obtained first [16]:

\[
D_s = S_{11}S_{22} - S_{12}S_{21}
\]

where S_{11} and S_{22} are input and output return loss, S_{12} and S_{21} are the reverse isolation and forward gain. Return loss is a figure of merit for signal reflection, which also indicates the fraction of the incident power being reflected back to the source. The Rollet Stability Factor represents the stability of a transistor. It is derived as following [16]:
If $K > 1$, then the device will be unconditionally stable for any combination of source and load impedances. However, for $K < 1$, the device is potentially unstable and will most likely oscillate with certain combinations of source and load impedance.

All these constraints added with the requirement of low power dissipation complicate LNA design. In summary, below is a list of some RF performance benchmarks, which the LNA has to specify in order to meet the overall requirements from the receiver.

1. Gain: more than 15 dB
2. Noise figure (NF): Less than 3 dB
3. IIP3: more than -10 dBm
4. Reverse isolation: 20-30 dB
5. Frequency of operation ($f_0$): as desired
6. Input voltage standing wave ratio (VSWR) < 2:1
7. Power dissipation ($P$) < 25 mW
8. Low voltage supply ($V_{DD}$) (3.3 V, 2.5 V etc.)
9. Output Impedance = 50 ohms (may be relaxed for direct conversion receivers)
10. Input Impedance = 50 ohms
11. Unconditional stability
3.2.2 LNA Circuit Design Topology

Extensive research on CMOS LNA design using submicron technologies has been done in the past few years [2], [8],[9], [18], [19],[20], [21]. Other than the inductive degeneration approach for LNA design which is used in this thesis, there are also other different LNA architectures which are all summarized in Figure 3.6 [9]. It is believed that the inductive degeneration approach offers the possibility of achieving the best noise performance of any architecture [9]. Since noise is one of the biggest concerns of LNA design, an inductive degenerated amplifier is used.

Figure 3.6: (a) Common-source amplifier with shunt-input resistor (b) Common-gate amplifier (c) Shunt-series amplifier (d) Inductive degenerated amplifier
Let’s take a closer look at the noise factor of this LNA in (d) of Figure 3.6. From the next Figure 3.7 [9], we can see there are three major noise sources contributing to the noise factor: output noise power density due to the source 50 $\Omega$, output noise power density due to the parasitic resistance $R_l$ and $R_g$, and finally the channel current noise of the MOSFET. Among these three noise contributors, the channel current noise dominates.

Output noise power density due to the source 50 $\Omega$, is given by

$$S_{u,src}(\omega_0) = \frac{4KT \omega_r^2}{\omega_0^2 R_s(1 + \frac{\omega L_s}{R_s})^2}$$

Similarly, output noise power density due to $R_l$ and $R_g$ can be expressed as

$$S_{u, R_l, R_g}(\omega_0) = \frac{4KT (R_l + R_g) \omega_r^2}{\omega_0^2 R_s(1 + \frac{\omega L_s}{R_s})^2}$$

The channel current noise of the CMOS transistor, assuming 1 Hz bandwidth, is giving by
Substituting the above three equations to the F’s general equation, yields

\[ F = 1 + \frac{R_i}{R_s} + \frac{R_g}{R_s} + Y g_{d0} R_s \left( \frac{\omega_0}{\omega_r} \right)^2 \]

Also the transconductance of the input stage is given by:

\[ G_m = g_m Q_m = \frac{g_m}{\omega_0 C_m (R_s + \omega r L_s)} = \frac{\omega_r}{\omega_0 R_s (1 + \frac{\omega r L_s}{R_s})} \]

In this thesis, a cascode, single-ended, inductive source degenerated LNA designed by Lee is used [22]. It is shown in Figure 3.8 below.

![Figure 3.8: Cascode single-end inductive source degenerated LNA](image)
A number of reasons exist for selecting cascode transistors for the reverse isolation between the source and output. Doing so improves linearity and stability, and also minimizes the miller effect of gate to drain capacitance of the amplifying device.

We have two MOS devices to be biased. The cascode transistor \( M_2 \) can be directly biased by the \( V_{DD} \) supply. We use a simple current mirror transistor \( M_3 \) to bias the amplifying transistor \( M_1 \). To minimize the power requirement of the bias circuit, the transistor dimension of \( M_3 \) is chosen to be one tenth of the value of that of \( M_1 \). Choosing the dimension of \( M_1 \) is a challenge. It has to be of the shortest length possible so as to minimize the noise effect. The bias resistor \( R_{bias} \) value is chosen to be large enough so that its equivalent noise contribution becomes small enough to be neglected. The value of the DC block capacitor \( C_b \) is chosen to have a negligible reactance at the signal frequency. Gate inductance \( L_g \) and source inductance \( L_s \) values are chosen to design a perfect input matching circuit. The load inductance \( L_d \) value is optimized to design an output matching circuit. \( C_L \) is the total capacitive load due to the mixer as seen by the LNA. The details of designing these circuit parameters are described in the next section.

### 3.2.3 LNA Design Steps

1. Choose the device width using the following equation:

   \[
   W_{opt} = \frac{1}{3\omega_0 L C_{ox} R_s}
   \]

   where \( C_{ox} \), operation frequency \( (f_0) \), and series resistance \( (R_s) \) are given, and the minimum gate length \( (L) \) should be used.
2. Choose bias point (I_D) to satisfy the power constraint. Then R_{ref} can be chosen to set the I_D to a desired value.

\[ P = V_{DD}I_D \quad \text{in mW} \]

3. The input impedance of the MOS amplifier can be degenerated by using inductors. From the input stage shown in Figure 3.9 [9], choose the value of L_g and L_s.

\[ Z_{\text{in}} = \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \]

where C_{gs} is the transistor gate-source capacitance, and g_m is the transistor transconductance. In the above equation, at the resonance frequency (\( \omega_0 \)) of the circuit, the real part of the equation should be R_s, which is 50 ohms. Therefore,

\[ \frac{g_m}{C_{gs}} L_s = 50 \]
From the above equation, \( L_s \) can be calculated by knowing \( g_m \) and \( C_{gs} \), which can be calculated from the following:

\[
g_m = \frac{\partial I_D}{\partial V_{gs}}
\]

\[
C_{gs} = \frac{\varepsilon \alpha}{t_{ox}} W L D + \frac{2}{3} [C_{ox} W (L - 2 L_D)]
\]

If we ignore the overlap capacitance of the transistor, \( C_{gs} \) is given by

\[
C_{gs} = \frac{2}{3} C_{ox} W L
\]

After the \( L_s \) value is obtained, \( L_g \) can be calculated using the following resonance frequency (\( \omega_0 \)) equation.

\[
\omega_0 = \frac{1}{\sqrt{L_s C_{gs}}}
\]

4. In order to compute \( L_d \), it is required to know the value of \( C_L \). Once \( C_L \) is determined, \( L_d \) can be calculated by the equation below:

\[
\omega_0 = \frac{1}{\sqrt{L_d C_L}}
\]

Those design steps outlined by Lee [22] below are used to obtain the initial values of the dimensions of the transistors and the inductors. When the LNA circuit is simulated in the simulator known as Cadence’s SpectreRF, these values are adjusted to optimize the circuit’s performance.
4.1 Equivalent Circuit Model of a MOSFET before and after HCS

It is critical to evaluate the device performance degradation due to HCE through predictive simulation before fabricating RF IC designs. It is necessary to obtain a compact model to accurately predict the stressed MOS transistor behaviors. Based on [23], a model, which represents the stressed device behaviors, is developed and shown in Fig. 4.1. The equivalent circuit includes the terminal resistances ($R_g, R_d, R_s$), substrate network equivalent resistances ($R_{db}, R_{sb}, R_{dsb}$), overlap additional capacitances ($C_{gd0}, C_{gs0}$), and junction capacitances ($C_{db}, C_{sb}$). The ‘fresh’ BSIM3 model, as well as the ‘stressed’ BSIM3 model, were extracted from the test devices using a Cascade Probe Station. They were used in the simulation to evaluate the HCS effect on LNA RF performance under weak and strong inversion.

![Equivalent circuit model of an nMOSFET before and after HCS](image)

Figure 4.1: Equivalent circuit model of an nMOSFET before and after HCS
The terminal resistances and capacitances values shown in the above circuit that were extracted from measured S-parameters are listed in Table 2.

Table 2 Values of terminal capacitances and resistances before and after HCS

<table>
<thead>
<tr>
<th>Parameters’ Name</th>
<th>Values Before HCS</th>
<th>Values After HCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{gs0}</td>
<td>185 fF</td>
<td>220 fF</td>
</tr>
<tr>
<td>C_{gdo}</td>
<td>45 fF</td>
<td>45 fF</td>
</tr>
<tr>
<td>R_{g}</td>
<td>27 Ω</td>
<td>24 Ω</td>
</tr>
<tr>
<td>R_{d}</td>
<td>1.38 Ω</td>
<td>1.21 Ω</td>
</tr>
<tr>
<td>R_{s}</td>
<td>3 Ω</td>
<td>6 Ω</td>
</tr>
<tr>
<td>C_{db}</td>
<td>160 fF</td>
<td>195 fF</td>
</tr>
<tr>
<td>C_{sb}</td>
<td>370 fF</td>
<td>390 fF</td>
</tr>
<tr>
<td>R_{dsb}</td>
<td>10 Ω</td>
<td>8 Ω</td>
</tr>
<tr>
<td>R_{db}</td>
<td>100 Ω</td>
<td>80 Ω</td>
</tr>
<tr>
<td>R_{sb}</td>
<td>100 Ω</td>
<td>80 Ω</td>
</tr>
</tbody>
</table>

The devices used in this work were fabricated with 60nm CMOS technology with channel length \( L = 0.06 \) μm and channel width \( W = 10 \) μm. The oxide thickness \( t_{ox} \) was 1.0 nm. The Agilent 4156B Precision Semiconductor Parameter Analyzer was used for DC biasing and I-V characterization. The S-parameters were measured using an Agilent 8510C Network Analyzer. The students at the Chip Design and Reliability Laboratory (CDRL) at the University of Central Florida performed these measuring tests.
4.2 RF Performance of an LNA Operating under Strong Inversion before HCS

Once parameter data was extracted from the experiment, and initial LNA circuit design calculations done in Mathcad were ready, we started the Cadence SpectreRF simulation. At the frequency of operation, 1.5 GHz, hand calculations determined the component values and device sizes of the LNA. Overall, the hand calculations produced results which were quite different from the optimized simulated values.

The schematic used in the Cadence SpectreRF simulation of an LNA is shown in Figure 4.2.

Figure 4.2: Schematic of the simulated LNA
The LNA circuit was first simulated in strong inversion operation before HCS. To start off the simulation, we used same values of $V_{DD} = 3.3\, \text{V}$, $C_L = 104\, \text{fF}$, $R_{\text{bias}} = 3K\, \Omega$, $C_B = 5\, \text{pF}$, $L_g = 10\, \text{nH}$, $L_s = 1.8\, \text{nH}$, and $L_d = 20\, \text{nH}$ as the ones used in [20] to design the components of the LNA. Then the values of the parameters extracted from fresh devices in Table 2, and minimum sizes of the nMOSFETs were also used. In this simulation, the values of $V_{DD}$, $R_{\text{bias}}$, $C_L$, $L$ and the listed parameters in Table 2 are constants. The other components of the LNA are design valuables, which need to be optimized. The last value to be determined in LNA circuit was $R_{\text{eff}}$, which was used for DC bias point for $M_1$. A simulation of DC analysis was started after setup the LNA circuit was complete. After a few trials, the $R_{\text{eff}}$ and $W$ were determined. The results of DC operating points for strong inversion are shown in the Table 3 below.

**Table 3 Optimal DC operation points of LNA operating under strong inversion before HCS**

<table>
<thead>
<tr>
<th>DC Operation Points</th>
<th>Fresh Device under Strong Inversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{eff}}$</td>
<td>500 $\Omega$</td>
</tr>
<tr>
<td>$W_1 (M_1)$</td>
<td>50 $\mu$m</td>
</tr>
<tr>
<td>$W_2 (M_2)$</td>
<td>200 $\mu$m</td>
</tr>
<tr>
<td>$V_{gs} (M_1)$</td>
<td>0.955 V</td>
</tr>
<tr>
<td>$V_{ds} (M_1)$</td>
<td>1.842 V</td>
</tr>
<tr>
<td>$I_{ds} (M_1)$</td>
<td>25.12 mA</td>
</tr>
</tbody>
</table>

The next step was to perform S-parameter plus noise analysis. A helpful tool called Parametric
Analysis was used to obtain the best values for $L_g$, $L_s$, and $L_d$ (shown in Table 4) in order to achieve the most optimized circuit performance.

Table 4 Optimal design for LNA operating under strong inversion

<table>
<thead>
<tr>
<th>Components’ name</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>36 nH</td>
</tr>
<tr>
<td>$L_s$</td>
<td>0.75 nH</td>
</tr>
<tr>
<td>$L_d$</td>
<td>27 nH</td>
</tr>
</tbody>
</table>

The optimized LNA RF performance at operation frequency 1.5 GHz is shown in Figure 4.3. S-parameters and NF values are within the LNA design requirements; see Figure 4.4 – 4.8 for details.

Figure 4.3: S-parameters and NF vs. frequency under strong inversion, S-parameters and NF are optimized at $f_0 = 1.5$ GHz
Figure 4.4: $S_{11}$ vs. frequency under strong inversion, $S_{11} = -37.07 \text{ dB}$ at $f_0 = 1.5 \text{ GHz}$

Figure 4.5: $S_{12}$ vs. frequency under strong inversion, $S_{12} = -35.35 \text{ dB}$ at $f_0 = 1.5 \text{ GHz}$
Figure 4.6: $S_{21}$ vs. frequency under strong inversion, $S_{21} = 28.97$ dB at $f_0 = 1.5$ GHz

Figure 4.7: $S_{22}$ vs. frequency under strong inversion, $S_{22} = -16.42$ dB at $f_0 = 1.5$ GHz
Our design can provide a reasonable gain and NF at the resonance frequency. Before HCS, the LNA RF performance under strong inversion is optimized and summarized in Table 5.

Table 5 Optimal LNA RF performances at operation frequency 1.5GHz before HCS under strong inversion

<table>
<thead>
<tr>
<th>S-parameters and NF</th>
<th>Design Requirements</th>
<th>Cadence Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$</td>
<td>&lt; -10 dB</td>
<td>-37.07 dB</td>
</tr>
<tr>
<td>$S_{21}$</td>
<td>&gt; 15 dB</td>
<td>28.97 dB</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>&lt; -10 dB</td>
<td>-16.42 dB</td>
</tr>
<tr>
<td>NF</td>
<td>&lt; 3 dB</td>
<td>2.28 dB</td>
</tr>
</tbody>
</table>
4.3 RF Performance of an LNA Operating under Strong Inversion after HCS

In order to see HCS induced RF performance degradation of an LNA, the BSIM model parameters extracted from stressed devices was applied to $M_1$. As we know, after HCS, interface states and oxide traps are created close to the drain junction. Therefore, this HC phenomenon will cause the variation of device parameters; $C_{gs}$, $V_T$, and $v_{sat}$ will increase, and $\mu_0$ will decrease for nMOSFETs. Please see Table 6 for details.

Table 6 Device parameters of an nMOSFET before and after HCS under strong inversion

<table>
<thead>
<tr>
<th>Device Parameters</th>
<th>Values before HCS</th>
<th>Values after HCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gs}$</td>
<td>185 fF</td>
<td>220 fF</td>
</tr>
<tr>
<td>$V_T$</td>
<td>0.457 V</td>
<td>0.516 V</td>
</tr>
<tr>
<td>$v_{sat}$</td>
<td>4.18E6 cm/s</td>
<td>4.66E6 cm/s</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>100.7 cm^2/(V*s)</td>
<td>90.1 cm^2/(V*s)</td>
</tr>
</tbody>
</table>

By inspecting the BSIM3v3 model files, we found that many model parameters were adjusted to represent the stressed device behaviors, including $Vth0$, $U0$, $Ua$, $Voff$, $NFactor$, etc. Because of the variation of device parameters, DC characteristics of LNA also change. From Table 7, we can see that the HC phenomenon degrades drain current. Decreasing of drain current means lower $gm$ will be obtained. This is the explanation of why $f_T$, $f_{max}$, and $F_{min}$ also degrade after HCS.
Table 7 DC operation points of LNA before and after HCS under strong inversion

<table>
<thead>
<tr>
<th>DC Operation Points</th>
<th>Values before HCS</th>
<th>Values after HCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{eff}}$</td>
<td>500 $\Omega$</td>
<td>500 $\Omega$</td>
</tr>
<tr>
<td>$W_1$</td>
<td>50 um</td>
<td>50 um</td>
</tr>
<tr>
<td>$W_2$</td>
<td>200 um</td>
<td>200 um</td>
</tr>
<tr>
<td>$V_{\text{gs}}$</td>
<td>0.955 V</td>
<td>0.972 V</td>
</tr>
<tr>
<td>$V_{\text{ds}}$</td>
<td>1.842 V</td>
<td>1.912 V</td>
</tr>
<tr>
<td>$I_{\text{ds}}$</td>
<td>25.12 mA</td>
<td>19.7 mA</td>
</tr>
</tbody>
</table>

HC induced degradation of LNA RF performance for strong inversion is presented in this work.

The values of S-parameters and NF have been shifted; please see Figure 4.9 – 4.14 for details.

Figure 4.9: S-parameters and NF after HCS under strong inversion
Figure 4.10: $S_{11}$ changes before and after HCS under strong inversion

Figure 4.11: $S_{12}$ changes before and after HCS under strong inversion
Figure 4.12: $S_{21}$ changes before and after HCS under strong inversion

Figure 4.13: $S_{22}$ changes before and after HCS under strong inversion
The values of S-parameters and NF change before and after HCS from figures 4.9 – 4.14 are summarized in Table 8.

Table 8 S-parameters and NF at operation frequency 1.5GHz change before and after HCS under strong inversion

<table>
<thead>
<tr>
<th>S-parameters and NF</th>
<th>Values before HCS</th>
<th>Values after HCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>S(_{11})</td>
<td>-31.61 dB</td>
<td>-13.18 dB shifts to 1.46GHz (-23.25 dB)</td>
</tr>
<tr>
<td>S(_{12})</td>
<td>-35.22 dB</td>
<td>-36.71 dB</td>
</tr>
<tr>
<td>S(_{21})</td>
<td>28.97 dB</td>
<td>27.66 dB</td>
</tr>
<tr>
<td>S(_{22})</td>
<td>-16.42 dB</td>
<td>-12.32 dB</td>
</tr>
<tr>
<td>NF</td>
<td>2.28 dB</td>
<td>2.28 dB</td>
</tr>
</tbody>
</table>
4.4 RF Performance of an LNA Operating under Weak Inversion before HCS

For the purpose of low power design, a LNA circuit is designed in weak inversion operation. In order to change the bias point for $M_1$ for it to operate under weak inversion, the value of $R_{\text{eff}}$ was increased. For this thesis work, a drain current from weak inversion was 10 times less than that from strong inversion operation. See Table 9 for details.

Table 9 DC operation points under weak and strong inversion before HCS

<table>
<thead>
<tr>
<th>DC Operation Points</th>
<th>Values under Strong Inversion</th>
<th>Values under Weak Inversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{eff}}$</td>
<td>500 $\Omega$</td>
<td>40k $\Omega$</td>
</tr>
<tr>
<td>$W_1 (M_1)$</td>
<td>50 um</td>
<td>25 um</td>
</tr>
<tr>
<td>$W_2 (M_2)$</td>
<td>200 um</td>
<td>200 um</td>
</tr>
<tr>
<td>$V_{\text{gs}} (M_1)$</td>
<td>0.955 V</td>
<td>0.380 V</td>
</tr>
<tr>
<td>$V_{\text{ds}} (M_1)$</td>
<td>1.842 V</td>
<td>2.401 V</td>
</tr>
<tr>
<td>$I_{\text{ds}} (M_1)$</td>
<td>25.12 mA</td>
<td>1.43 mA</td>
</tr>
</tbody>
</table>

After DC analysis of the LNA under weak inversion, a Parametric Analysis tool was used to obtain the best values for $L_g$, $L_s$, and $L_d$ (shown in Table 10) in order to achieve the most optimized circuit performance. These values are also compared with those obtained from strong inversion.
In most applications, high performance must be achieved at low power consumption, resulting in a trade off between power and performance. Therefore, this work also presents the optimized LNA RF performance parameters under weak inversion and compares them with those under strong inversion. Please see Figure 4.15 – 4.20 for details. As predicted, the LNA RF performances are degraded in the weak inversion region.

Table 10 DC optimal components of LNA before HCS under weak and strong inversion

<table>
<thead>
<tr>
<th>Components’ name</th>
<th>Values under Strong Inversion</th>
<th>Values under Weak Inversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$</td>
<td>36 nH</td>
<td>43 nH</td>
</tr>
<tr>
<td>$L_s$</td>
<td>0.75 nH</td>
<td>1.2 nH</td>
</tr>
<tr>
<td>$L_d$</td>
<td>27 nH</td>
<td>28 nH</td>
</tr>
</tbody>
</table>


Figure 4.15: S-parameters and NF vs. frequency under weak inversion

Figure 4.16: $S_{11}$ vs. frequency under weak and strong inversion

Figure 4.17: $S_{12}$ vs. frequency under weak and strong inversion
Figure 4.18: $S_{21}$ vs. frequency under weak and strong inversion

Figure 4.19: $S_{22}$ vs. frequency under weak and strong inversion
Figure 4.20: NF vs. frequency under weak and strong inversion

Operating under weak inversion, S-parameters and NF are degraded compared to those under strong version from Figure 4.15 – 4.20. Table 11 shows the variation of these parameters.

Table 11 S-parameters and NF of LNA at operation frequency 1.5 GHz before HCS under weak and strong inversion

<table>
<thead>
<tr>
<th>S-parameters and NF</th>
<th>Values under Strong Inversion</th>
<th>Values under Weak Inversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_{11}</td>
<td>-37.07 dB</td>
<td>-18.54 dB</td>
</tr>
<tr>
<td>S_{12}</td>
<td>-35.22 dB</td>
<td>-28.33 dB</td>
</tr>
<tr>
<td>S_{21}</td>
<td>28.97 dB</td>
<td>17.60 dB</td>
</tr>
<tr>
<td>S_{22}</td>
<td>-16.42 dB</td>
<td>-11.8 dB</td>
</tr>
<tr>
<td>NF</td>
<td>2.28 dB</td>
<td>2.65 dB</td>
</tr>
</tbody>
</table>
4.5 Discussion on Cadence Simulation Results

This thesis work first simulated a LNA circuit operating under strong inversion using “fresh” BSIM3 model parameters. The optimal simulated LNA RF performances under strong inversion are presented in the form of plots and tables, which have been shown in the previous sections.

Then the same LNA circuit was simulated under strong inversion using the “stressed” BSIM3 model parameters. As shown in simulation results, DC characteristics, and RF performance are degraded after HCS under strong inversion. \( I_{ds} \) decreases due to electron trapping and interface state generation and the degradation percentage goes up [20]. After HCS, \( V_{th} \) increases because of electron trapping. Interface state generation also decreases \( \mu_0 \) in the channel. The RF performance degradation due to HCS in an nMOSFET can be explained by the \( gm \) degradation, which is a result of the electron trapping and interface state generation. Because \( f_T, f_{\text{max}} \) and \( F_{\text{min}} \) are functions of \( gm \), \( f_T \) and \( f_{\text{max}} \) should be decreased, and \( F_{\text{min}} \) should be increased after HCS. Under strong inversion, all the devices were operated in the saturation region. Also, as can be seen from the Cadence SpectreRF simulation results, S-parameters have been affected significantly. The degradation of \( gm \) and drift of \( C_{gs} \) after HCS will change both the real and imaginary part of the input impedance [20]. The mismatch will cause the \( S_{11} \) to shift away from the center frequency. \( S_{11} \) shifts left after HCS, which suggests a decrease in the input impedance, because the input impedance is proportional to \(|(1+ S_{11})/(1- S_{11})|\). The decrease in \( S_{21} \) indicates the degradation of the forward power gain after HCS. \( S_{12} \) also degrades a little bit after HCS. The degradation of \( S_{21} \) and \( S_{22} \) can be explained by the decrease of \( gm \) and the increase of \( g_{ds} \), which results in the change of reflected parameters at output port [11], [20]. NF also increased after HCS because of the degradation of \( f_T \). The increase of thermal noise is due to the increased
random thermal motion of carriers in the channel after HCS [11]. Poorly matched devices can cause a large amount of reflected power, poor noise performance, and low gain [25].

Since there is trade of between power and performance, this thesis work has also simulated an LNA operating under weak inversion before HCS. The simulated results are compared with those obtained from strong inversion before HCS. As predicted, $I_{ds}$ under weak inversion is 10 times less than that under strong inversion. The decrease of $I_{ds}$ causes $g_m$ to decrease. Similarly, because $g_m$ decreases, we expect $f_T$ and $f_{\text{max}}$ to decrease, and $NF_{\text{min}}$ to increase. The degradation of $g_m$ also results in decreasing of $S_{21}$. Under weak inversion, $S_{11}$, $f_{21}$, and NF are all degraded. However, they are still within the margin of RF performance figures of merit.
CHAPTER FIVE: CONCLUSION

LNAs are the backbone of RF receivers. CMOS LNAs have drawn researchers’ attention due to their low cost and high integration advantages. As the first stage of a receiver, the essential requirements of an LNA are low NF and high gain. In addition, matching is very important for power and noise optimization.

High performance integrated circuits with small size devices such as 60nm nMOSFETs used in this thesis work suffer from HCE. This thesis work has demonstrated HCS effect on RF performances of an LNA operating under weak and strong inversion. Before HCS, we can design the LNA to operate under weak or strong inversion. The trade off between these two conditions is power and performance. After HCS, DC characteristics and LNA RF performance are degraded under strong inversion. If special care is not taken to understand this issue, HC induced degradations can lead to circuit failures.
LIST OF REFERENCES


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