Nanoelectronic Devices using Carbon Nanotubes and Graphene Electrodes: Fabrication and Electronic Transport Investigations

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NANOELECTRONIC DEVICES USING CARBON NANOTUBES AND
GRAPHENE ELECTRODES: FABRICATION AND ELECTRONIC
TRANSPORT INVESTIGATIONS

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Physics
in the College of Sciences
at the University of Central Florida
Orlando, Florida

Spring Term
2015

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ABSTRACT

Fabrication of high-performance electronic devices using the novel semiconductors is essential for developing future electronics which can be applicable in large-area, flexible and transparent displays, sensors and solar cells. One of the major bottlenecks in the fabrication of high-performance devices is a large interfacial barrier formation at metal/semiconductor interface originated from Schottky barrier and interfacial dipole barrier which causes inefficient charge injection at the interface. Therefore, having a favorable contact at electrode/semiconductor is highly desirable for high-performance devices fabrication.

In this dissertation, the fabrication of nanoelectronic devices and investigation of their transport properties using carbon nanotubes (CNTs) and graphene as electrode materials will be shown. I investigated two types of devices using (i) semiconducting CNTs, and (ii) organic semiconductors (OSC). In the first part of this thesis, I will demonstrate the fabrication of high-performance solution-processed highly enriched (99%) semiconducting CNT thin film transistors (s-CNT TFTs) using densely aligned arrays of metallic CNTs (m-CNTs) for source/drain electrodes. From the electronic transport measurements at room temperature, significant improvements of field-effect mobility, on-conductance, transconductance and current on/off ratio for m-CNT/s-CNT devices were found compared to control palladium (Pd contacted s-CNT devices. From the temperature dependent transport investigation, a lower Schottky barrier height for the m-CNT/s-CNT devices was found compared to the devices with control metal electrodes. The enhanced device performance can be attributed to the unique device geometry as well as strong $\pi-\pi$ interaction at m-CNT/s-CNT interfaces. In addition, I also investigated s-CNT TFTs using reduced graphene oxide (RGO) electrodes.
In the second part of my thesis, I will demonstrate high-performance organic field-effect transistors (OFETs) using different types of graphene electrodes. I show that the performance of OFETs with pentacene as OSC and RGO as electrode can be continuously improved by increasing the carbon $sp^2$ fraction of RGO. The carbon $sp^2$ fractions of RGO were varied by controlling the reduction time. When compared to control Pd electrodes, the mobility of the OFETs shows an improvement of $\sim 200\%$ for 61% $sp^2$ fraction RGO, which further improves to $\sim 500\%$ for 80% RGO electrode. Similarly, I show that when the chemical vapor deposition (CVD) graphene film is used as electrodes in fabricating OFET, the better performance is observed in comparison to RGO electrodes. Our study suggests that, in addition to $\pi-\pi$ interaction at graphene/pentacene interface, the tunable electronic properties of graphene as electrode have a significant role in OFETs performance. For a fundamental understanding of the interface, we fabricated short-channel OFETs with sub-100nm channel length using graphene electrode. From the low temperature electronic transport measurements, a lower charge injection barrier was found compared to control metal electrode. The detailed investigations reported in this thesis clearly indicated that the use of CNT and graphene as electrodes can improve the performance of future nanoelectronic devices.
To my family
ACKNOWLEDGMENTS

I would like to acknowledge and give my great appreciation for his guidance and support of my thesis advisor, Prof. Saiful I. Khondaker who has mentored me throughout my research work over the entire time during the Doctor of Philosophy (Ph.D.) degree in Science at University of Central Florida (UCF). Dr. Khondaker has provided a great opportunity to experience real research at Nanoscience Technology Center (NSTC) and Department of Physics at UCF and guided me throughout my research and beyond. I also would like to thank the committee members, Dr. Lei Zhai, Dr. Lee Chow, and Dr. Michael N. Leuenberger for spending their valuable time to read my thesis and to serve my dissertation committee. I thank you to Dr. Masa Ishigami and his student, Christian Smith for the collaboration of CVD-grown graphene film growth for my doctoral research. I am also specially thankful to Dr. Laurene Tetard for numerous discussions on emerging 2D materials and their optical properties investigations. I would like to send my appreciation to Dr. Youngho Sohn and Dr. Hyungjin Cho for their mentoring towards to my research as well as future career.

Secondly, I strongly would like to acknowledge my group members, especially, Biddut and Daeha for their great help to operate the instruments such as e-beam lithography (EBL), e-beam/thermal evaporation, scanning electron microscopy (SEM), atomic force microscopy (AFM) to fabricate and characterize the nano-scaled devices. I appreciate to Dr. Cho and Xiaochen for the facility access and help to use photolithography systems. I would also like to thank all other members in my group, Feras, Rakib, and Udai. I wish them the best of luck continuing their research and beyond for their future career. I also would like to thank the members of staffs and faculties at Nanoscience Technology Center (NSTC), Advanced Materials
Processing and Analysis Center (AMPAC), and Department of Physics in UCF.

Last of all, my special thanks have to to my family for their endless love and support.
# TABLE OF CONTENTS

LIST OF FIGURES ........................................................................................................ xii
LIST OF TABLES .......................................................................................................... xx
LIST OF ABBREVIATIONS ........................................................................................... xxi

CHAPTER 1 : INTRODUCTION......................................................................................... 1
  1.1 Motivation ................................................................................................................ 1
  1.2 Organization of Thesis .............................................................................................. 7

CHAPTER 2 : BACKGROUND ......................................................................................... 10
  2.1 Carbon Nanotubes (CNTs) .................................................................................... 10
    2.1.1 Historical Overview and Properties of CNTs .................................................. 10
    2.1.2 CNTs for Thin Film Transistors ...................................................................... 13
    2.1.3 Metal Electrodes for CNT Thin Film Transistors ........................................... 17
  2.2 Graphene .............................................................................................................. 21
    2.2.1 Historical Overview and Properties of Graphene ........................................... 21
  2.3 Organic Semiconductors ....................................................................................... 24
    2.3.1 Historical Overview and Properties of Organic Semiconductors .................... 24
    2.3.2 Organic Semiconductors for Organic Field-Effect Transistors ....................... 25
    2.3.2 Metal Electrodes for OFETs ........................................................................... 29
  2.4 Carbon-Based Materials as Alternative Electrodes ............................................... 31
    2.4.1 Carbon Nanotube Electrodes for Nanoelectronic Devices ............................... 32
    2.4.2 Graphene Electrodes for Nanoelectronic Devices .......................................... 34

CHAPTER 3 : DEVICE FABRICATION AND EXPERIMENTAL METHODS .................... 35
  3.1 Introduction ............................................................................................................ 35
  3.2 Fabrication of Metal Electrodes ............................................................................. 36
    3.2.1 Photolithography ............................................................................................ 36
3.2.2 Electron Beam Lithography (EBL) ................................................................. 37
3.3 Fabrication of CNT Electrodes and CNT Thin-Film Transistors ................................................. 40
  3.3.1 Solution-processed CNTs .............................................................................. 40
  3.3.2 Assembly of CNTs via Dielectrophoresis (DEP) ................................................ 40
  3.3.3 CNT Electrode Fabrication ............................................................................ 43
  3.3.4 CNT Thin-Film Transistors (CNT-TFTs) ............................................................ 46
3.4 Fabrication of Graphene Electrodes ................................................................................. 47
  3.4.1 Mechanically Exfoliated Graphene as Electrodes .................................................. 48
  3.4.2 CVD-GR as Electrodes .................................................................................. 49
  3.4.3 RGO as Electrodes ........................................................................................ 51
3.5 Fabrication of OFETs ................................................................................................. 52
3.6. Characterization for High-Resolution Imaging and Transport Measurement Set-up ............ 53
  3.6.1 High-resolution Imaging and Characterization ...................................................... 53
  3.6.1.1 Scanning Electron Microscopy (SEM) .............................................................. 53
  3.6.1.2 Atomic Force Microscopy (AFM) .................................................................. 55
  3.6.2 Electronic Transport Measurements .................................................................... 57

CHAPTER 4 : HIGH PERFORMANCE SOLUTION-PROCESSED SEMICONDUCTING
ENRICHED CARBON NANOTUBES THIN FILM TRANSISTORS WITH METALLIC CNT ELECTRODES ................................................................. 61
  4.1 Introduction .............................................................................................................. 61
  4.2 Current Status and Challenges in s-CNT Thin Film Transistors (s-CNT-TFTs) ............ 63
  4.3 Fabrication of Aligned Array Highly Enriched s-CNT TFTs using Aligned Array m-CNT electrodes ................................................................................................................. 66
  4.4 Characterization of s-CNT TFTs with m-CNT electrodes ............................................. 67
  4.5 Transport Properties of s-CNT TFTs using m-CNT electrodes at Room Temperature ..... 71
  4.6 Temperature Dependent Transport Investigations of s-CNT TFTs .............................. 76
  4.7 Conclusion .............................................................................................................. 81

CHAPTER 5. TUNABLE DENSITY EFFECT OF SEMICONDUCTING CARBON
NANOTUBES ARRAY IN THE THIN FILM TRANSISTORS USING METALLIC CARBON NANOTUBES ELECTRODES ................................................................. 83
8.2 Experimental Set-up and Methods ........................................................................ 123
  8.2.1 Large Area Graphene Film: CVD-GR and RGO Film ................................... 123
  8.2.2 Simple Patterning of Large-Area CVD-GR and RGO Films for Electrodes .... 125
  8.2.3 Fabrication of Pentacene OFETs using Large Area Graphene Electrodes ....... 127
8.3 Characterization of Large Area CVD-GR and RGO Electrodes........................ 128
8.4 Current-Voltage Characteristics of OFETs ...................................................... 130
8.5 Performance Comparison of OFETs ............................................................... 132
8.6 Conclusion ........................................................................................................ 135

CHAPTER 9 : HIGH-PERFORMANCE SHORT-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS WITH GRAPHENE ELECTRODES .................................................. 136
  9.1 Introduction ........................................................................................................ 136
  9.2 Fabrication of Short Channel (Sub-100nm) Graphene Electrodes .................. 138
  9.3 Characterization of Short-Channel Graphene Electrodes ............................... 139
  9.4 Characterization of Pentacene Film Deposition in Short-Channel OFETs using Graphene Electrodes ...................................................................................... 141
  9.5 Current-Voltage Characteristics of OFETs using Short-Channel Graphene Electrodes ... 142
  9.5 Temperature Dependent Charge Injection and Transport Mechanism .......... 144
  9.6 Conclusion ........................................................................................................ 145

CHAPTER 10: CONCLUSION .................................................................................... 147
  10.1 Summary ........................................................................................................... 147
  10.2 Future Work ..................................................................................................... 147

REFERENCES ........................................................................................................ 180
APPENDIX: COPYRIGHT PERMISSION LETTERS .................................................. 149
LIST OF FIGURES

Figure 1. Thin Film Transistors (TFT) based large area applications including (a)-(c) active matrix liquid crystal displays (AMLCDs), active matrix organic liquid emitting diodes (AMOLEDs), thin film printed temperature label, and flat-panel solar cells. Adapted from the ref [5-9].

Figure 2. Different types of graphitic forms as 0D bulkyballs, rolled into 1D nanotubes, 2D graphene or stacked into 3D graphite. Adapted from ref. [103].

Figure 3. (a) A conceptual view of future organic flexible display which can be rolled into a pen-like device when not in use. Images courtesy of Universal Display Corp. (b) A full color, 13-inch OLED display with only 2mm thick. (c) A conceptual view of integrated circuits on flexible, and transparent plastic substrate. Photograph courtesy of T. Jackson, Penn state Univ. Adapted from ref. [23].

Figure 4. Schematic diagram of energy level difference between metal electrode and organic semiconductor (a) without and (b) with an interfacial dipole barrier. Adapted from ref [25].

Figure 5. Different forms of carbon allotropes. Graphene (Top left) is a honeycomb lattice of carbon atoms. Graphite (top right) can be viewed as a stack of graphene laers. Carbon nanotubes are rolled-up cylinders of graphene (bottom left). Fullerences (C60) are molecules consisting of wrapped graphene by the introduction of pentagons on the hexagonal lattice. Adapted from ref [104].

Figure 6. Adapted from Carbon Nanotube Electronics, Adapted from ref [36]. © 2003 IEEE.

Figure 7. The schematic theoretical diagram of CNT structure. The properties of CNTs can be decided depending on its chirality. (a) armchair, (b) zigzag, and (c) chiral. The actual tubules shown in the figure correspond to (n,m) values of : (a) (5,5), (b) (9,0), and (c) (10, 5). Adapted from ref [37].

Figure 8. s-CNT thin films from the literature. (a) Device schematic diagram of random network s-CNT TFTs. Adapted from ref [48] (b) SEM image of s-CNT random arrays. Adapted from ref [48]. (c) SEM images of self-assembled and self-aligned s-CNT arrays. Adapted from ref [44]. (d) AFM images of random network s-CNT arrays. Adapted from ref [14].

Figure 9. Typical current-voltage characteristics of s-CNT TFTs. (a) Output (I_d vs. V_d) and (b) Transfer (I_d vs. V_g) characteristics. Adapted from ref. [14].

Figure 10. (a) Transfer characteristics of CNT FETs using Pd electrodes (b) On-current variation depending on the choice of metal electrodes in CNT TFTs with estimated Schottky Barrier height. Inset: On-current variation depending on the diameter of nanotubes. Adapted from ref. [47].

Figure 11. Schottky barrier heights (hole injection) as a function of diameter from different studies. Adapted from ref. [21].

Figure 12. The Nobel prize in physics in 2010 was awarded jointly to Andre Geim and Konstantin Novoselov for groundbreaking experiments regarding the two-dimensional (2D) material graphene. (Top left) Adapted from http://www.nobelprize.org/nobel_prizes/physics/laureates/2010/ The successful exfoliation of single-layer graphene. Adapted from ref. [53]. (Top right) The cartoon shows the first graphene...
samples were produced by exfoliating atom thick layers from a graphite using Scotch tape leading Nobel prize in 2010. Adapted from www.strippedscience.com. (Bottom) .......................... 22

Figure 13. (a) Electronic dispersion in the honeycomb lattice. Zoom-in of the energy bands close to one of the Dirac points. (b) Schematic diagram showing the band structure and resulting ambipolar field effect in graphene. Conduction and valence bands meet at the Dirac point without an external field. Under gate bias, a significant number of free carriers. Adapted from ref. [104]............................................................................................................. 23

Figure 14. Several representations of ethylene, which has two $sp^2$ bonded carbon atoms. (a) Ball and stick model, (b) a chemical structure, and (c) schematic of orbital diagram showing both pi-bond and sigma-bond. Adapted from ref [60]. Kymissis, Ioannis. "Organic Field Effect Transistors: Theory, Fabrication and Characterization." Page. 7, Springer, 2009, Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission............................... 24

Figure 15. Organic semiconductors: (i) small molecules, or (ii) conjugated polymers.............. 26

Figure 16. Device configurations of OFETs. (a) Bottom-gate with top-contact electrodes, (b) top-gate with bottom-contact electrodes, (c) bottom-gate with bottom-contact electrodes, and (d) top-gate with top-contact electrodes................................................................. 27

Figure 17. Typical (a) output characteristics ($I_d$-$V_d$) with different gate voltage($V_g$) of OFETs with linear regime (red) and saturation regime (orange) and (b) transfer characteristics ($I_d$-$V_g$) with fixed bias voltage showing ON state and OFF state, and the threshold voltage ($V_{th}$). Threshold voltage can be extracted from the x-axis intercept of the linear extrapolation of the slope of ($I_d$) vs. $V_g$. Adapted from ref. [3]............................................................................................................. 28

Figure 18. Interfacial energy level diagram of (a) without and (b) with vacuum level shift. The hole injection barrier ($\phi_B^p$), which is the energy gap between Fermi level of metal electrodes and HOMO level of organic semiconductor, is increased with the broken vacuum level. The vacuum level shift maybe due to formation of interfacial dipole layer at metal-organic contact Adapted from ref. [62]............................................................................................................. 30

Figure 19. Different types of interfacial dipole formation at metal-organic interface. Adapted from ref. [63]............................................................................................................. 31

Figure 20. The examples of enhanced device performance of OFET using CNT electrodes in different studies. (a) Adapted from ref [64]. (b) Adapted from ref. [65]. (c) Adapted from [66]. and (d) Adapted from ref. [67]................................................................. 32

Figure 21. The transmittance as a function of sheet resistance of graphene films reported from several groups. Adapted from ref. [72]............................................................................................................. 34

Figure 22. Schematic diagram of photolithography processing steps. (a) UV light is exposed on photoresist spin-coated Si wafer, then (b) developed, (c) metal evaporated, and finally (d) lift-off by PG remover. ................................................................. 37

Figure 23. (a) Optical patterns of a chip contained contact pads, connecting leads and alignment markers for EBL. (b) Optical microscope image of the zoomed-in area (red square)............................ 37

Figure 24. Schematic diagram of electrode pattern fabrication steps using EBL on Si substrate. First, PMMA is spincoated on the Si substrate and then the electrode patterns are defined by EBL. The desired metal is evaporated. (Normally Au/Cr or Pd/Cr.) Finally, Lift-off is performed using acetone followed by IPA, DI water rinse, and N$_2$ blown dry................................. 38

Figure 25. (a) Optical image of resulting metal electrodes defined using EBL, metal evaporation, and lift-off. (b) Zoomed-in AFM image of the channel gap (~100nm) showing well-defined small size structure using EBL process. .............................................................................. 39
Figure 26. Schematic of experimental setup for dielectrophoresis (DEP) assembly of solution-processed CNTs. The signal with 1MHz frequency (typically) was applied from the function generator to source electrodes and monitored in channel 1 (CH1) of oscilloscope, and then drain electrodes is monitored via CH2 in oscilloscope.

Figure 27. The schematic diagram of DEP assembly of CNTs. (a) The CNT solution is dropped between source and drain electrode. (b) The simulation pictures showing electric field formation when AC voltage is applied between source and drain electrode. (c) After applying AC voltage, CNTs are aligned along E-field between source and drain electrode. Adapted from ref. [73].

Figure 28. m-CNT aligned array (a) SEM images of high density m-CNT aligned array between Pd source and drain electrodes. The current-voltage characteristics are shown in (b) output curve (I_d-V_d) at zero gate voltage and (c) transfer curve (I_d-V_g) at V_d = -0.1 V. Scale bar indicates 2 μm. Figure (b) and (c) are adapted from ref. [74] with permission of The Royal Society of Chemistry [Nanoscale 6 4896 (2014)].

Figure 29. Schematic diagram of m-CNT electrode fabrication of m-CNTs electrode. (a) Drop the m-CNT solution between Pd source and drain electrodes. (b) Assembly of m-CNTs aligned array via DEP between Pd electrodes. (c) Opened a window on the m-CNTs array via electron beam lithography, and (d) etch the m-CNTs by oxygen plasma.

Figure 30. Characterization of individual s-CNTs. (a) SEM image of CNTs dispersed on Si/SiO_2 substrate. (b) Distribution of nanotube length with an average of 1.5 μm and the diameter with an average of 1.7 nm determined from the (c) atomic force microscopy (AFM) image of CNTs dispersed on mica substrate and their height profile is summarized in (d) and (e) from approximately 150 nanobues. Adapted from ref. [68].

Figure 31. Schematic diagram of mechanically exfoliation graphene electrode fabrication. (a) Pristine graphene was mechanically exfoliated onto Si/SiO_2 substrate using conventional tape method. (b) Using EBL, we defined the source and drain contact pads on graphene followed by metal evaporation and lift-off. (c) The device was spin-coated with PMMA layer. Using 2nd EBL process, the desired geometry of window opened and developed. (d) The device with an opened window was kept in O2 plasma, and the opened area of graphene was etched away. (e) After final lift-off of PMMA removal, final graphene electrode can be fabricated. The gap size can be customized and controlled by fine and precise EBL process.

Figure 32. Simple patterning technique of large-area CVD-GR electrodes using sacrificial polymer layer. (a) Thin film of CVD grown graphene film was transferred onto Si/SiO_2 substrate. (b) After transferring, the film was spin-coated with PMMA layer. This PMMA layer acts as sacrificial polymer layer. (c) Through the metal shadow mask, Al is deposited by thermal deposition. (d) The device was kept in plasma etcher to etch all the area where unprotected by Al metal mask. (e) The sample was immersed into aceton for PMMA removal with Al metal mask.

Figure 33. Schematic diagram of RGO thin film electrode fabrication. (a) RGO solution was dropped between Pd source and drain electrode and AC voltage was applied with 1MHz frequency. (b) RGO thin film was assembled between metal source/drain electrode via DEP process. (c) After defining the channel window by EBL and keeping the device under O2 plasma for 2 min followed by acetone lift-off, final RGO electrodes can be fabricated.

Figure 34. Once the electron beam is produced from the electron gun, the beam traveled through electromagnetic fields and lenses and focused to the sample. Detectors collect the emitted electrons such as X-rays, backscattered electrons, and secondary electrons.
Figure 35. Block diagram of Tapping mode AFM using beam deflection detection. The cantilever is oscillated at or slightly below its resonance frequency, and the tip lightly taps the sample surface during the scanning. The feedback loop maintains the constant oscillation amplitude by constant RMS of the oscillation signal acquired by the photodiode detector. The vertical position of the scanner is controlled by setting the amplitude, and the information is transferred to topographic image of the sample surface..............................

Figure 36. Circuit diagram of electrical measurement set up for field-effect transistor with a configuration of top contact source and drain electrodes and bottom contact gate..........................

Figure 37. Experimental set-ups for electrical measurements of OFET devices. (a) The devices are measured using Hewlett Packard (HP) 4145B semiconductor parametric analyzer. This is connected to a probe station inside glove box system, which is filled with N2 gas flow as seen in (b)............................

Figure 38. (a) The part of cryostat that used for low-temperature measurement. Red arrow indicates that the position where sample goes in. (b) Wire bonding machine. (c) The wire-bonded sample with chip carrier. This goes into the place where red arrow indicates in (a)..............

Figure 39. Channel length impact on device performance of highly enriched s-CNT TFTs from different studies. (a) On state current as a function of current on/off ratio for different channel length devices from 0.5 μm to 10 μm. The current on/off ratio decreased with decreasing channel length. Adapted from ref. [44] (b) Mobility vs. Channel length for L=20μm to 100μm. The mobility decreased with decreasing channel length. Adapted from ref. [14] (c) Mobility with different channel length devices. Red plot shows the highly enriched s-CNT TFTs (98%) and showed decreased mobility with decreasing channel length. Adapted from ref. [48]. (d) Red plot (98% s-CNT) showed decreased current on/off ratio with decreasing channel length. Adapted from ref. [48].................................

Figure 40. (a) Schematic diagram of fabrication steps for s-CNT TFTs with CNT electrodes. (i) DEP assembly of CNTs. (ii) Aligned CNT arrays via DEP between Palladium (Pd) patterns. (iii) Opening of a window on the CNT array via EBL and plasma etching. (iv) DEP assembly of s-CNTs in between CNT electrodes. (v) Schematic of s-CNT TFT with CNT electrodes. SEM images of (b) the CNT aligned array and (c) the CNT electrode. The channel length of the CNT electrode is 2 μm, and (d) the AFM image of a part of the CNT electrode shows open ended and parallel tips. The scale bar indicates 1 μm..........................

Figure 41. SEM images of the aligned array of s-CNTs with a linear density of 1 s-CNT per μm between m-CNT electrodes with a channel length of 2 μm. (b) High magnification SEM image shows a longitudinal arrangement between the s-CNT and m-CNT. The scale bar indicates 1 μm in (a), and 300 nm in (b). ..........................................................

Figure 42. SEM image of s-CNT TFT devices with Pd electrodes (control device). The density of s-CNT is ~ 1s-CNT/μm, and the scale bar indicates 1μm..........................

Figure 43. Output characteristics (Id-Vd) for (a) m-CNT/s-CNT and (b) Pd/s-CNT devices at Vg = -30 to -15 V in steps of -1 V (top to bottom). Compared to the Pd/s-CNT device, the m-CNT/s-CNT device shows higher current driving ability. Transfer characteristics (Id-Vg) in the semi-log scale for (c) m-CNT/s-CNT and (d) Pd/s-CNT devices at Vd = -1V. The channel length and width of the both m-CNT/s-WNT and Pd/s-CNT devices are 2 μm and 25 μm, respectively. ....

Figure 44. Statistics for 13 m-CNT/s-CNT devices (red) and 13 Pd/s-CNT devices (blue). The channel length and width for all devices are 2 μm and 25 μm, respectively. (a) On-conductance, (v) transconductance, (c) device mobility, and (d) current on-off ratio. The m-CNT/s-CNT devices show significantly better performance than that of the Pd/s-CNT devices. ................
Figure 45. Current on-off ratio versus mobility of all the m-CNT/s-CNTt and Pd/s-CNT devices. Both the mobility and current on-off ratio of the m-CNT/s-CNT devices are higher than that of Pd/s-CNT devices. .................................................................................................................. 76

Figure 46. Temperature dependent (77-285 K) current-voltage characteristics at Vg=0 V of (a) the m-CNT/s-CNT device and (b) the pd/s-CNT device. The Arrhenius plot of the current at different Vd in the range of -0.1 V to -1 V for (c) the m-CNT/s-CNT device and (d) the Pd/s-CNT device. The bias voltage dependent Schottky barriers are calculated from the slopes of the ln Id versus 1000/T curves at a higher temperature range for different bias voltages. ........................................ 77

Figure 47. Plot of bias voltage dependent Schottky barrier \( \Phi (V_d) \) a function of square root of bias voltage (absolute value) for the m-CNT/s-CNT device (solid circles) and the Pd/s-CNT device (open squares). The zero bias Schottky barrier \( \Phi_0 \) is calculated from the y-intercept. .. 79

Figure 48. (a) Schematic diagram of s-CNT aligned array assembled between m-CNT aligned array electrodes. Two contact configurations are highlighted: end-contact and side-contact. (b) Schematic of the end-contact configuration between the m-CNT and the s-CNT. In the end-contact, the tip of s-CNT is connected directly to the tip of the m-CNT and improved charge injection can occur due to an electric field enhancement at the m-CNT tips. (c) Schematic of the side-contact configuration. Improved charge injection can occur from the side-walls of the m-CNT due to finite overlap with the s-CNT. ................................................................. 80

Figure 49. The impact of nanotube density in terms of device performance. (a) The plot of mobility as a function of nanotube density in the channel. As the tube density increased, the mobility increased. For the devices with smaller channel length (L=20\( \mu \)m), the mobility is smaller than the larger channel length (L=100\( \mu \)m), which indicates the impact of the channel length as well as density of nanotubes. (b) The correlation between mobility and current on-off ratio. As the mobility is higher, the current on-off ratio is lower which is the indication of the presence of metallic nanotube in the channel. Adapted from ref. [14]............. 84

Figure 50. SEM images of (a) m-CNT aligned array, (b) m-CNT electrode (after plasma etching), and aligned array of s-CNT with different linear density of (c) 1 s-CNT/\( \mu \)m, (d) 5 s-CNT/\( \mu \)m, (e) 10 s-CNT/\( \mu \)m, and (f) 25 s-CNT/\( \mu \)m between m-CNT electrodes. The scale bar indicates 1 \( \mu \)m. ................................................................. 86

Figure 51. (a) Output characteristics \( (I_d - V_d) \) of m-CNT/s-CNT device at \( V_g = -30 \) V indicates the current is increased by maximizing the number of s-CNTs in the channel (b) Transfer characteristics \( (I_d - V_g) \) shows clearly that the current is varied with the density of s-CNTs in the CNT electrode. The comparison of device performance of the m-CNT/s-CNT and Pd/s-CNT devices as function of linear density of s-CNT in the channel: (c) \( G_{on} \) (d) \( I_{on}/I_{off} \), (e) \( g_m \), and (f) \( \mu \) as a function of linear density. .................................................................................................................. 87

Figure 52. Temperature dependent (77-285 K) current-voltage characteristics at \( V_g = 0 \) V of m-CNT/s-CNT device with the linear density of (a) 1 s-CNT/\( \mu \)m, (b) 5 s-CNT/\( \mu \)m, (c) 10 s-CNT/\( \mu \)m, (d) 15 s-CNT/\( \mu \)m, (e) 20 s-CNT/\( \mu \)m, and (f) 25 s-CNT/\( \mu \)m. ................................................................. 91

Figure 53. Arrhenius plot of current at different Vd in the range of -0.1 V to -1 V for m-CNT/s-CNT device with the linear density of (a) 1 s-CNT/\( \mu \)m, (b) 5 s-CNT/\( \mu \)m, (c) 10 s-CNT/\( \mu \)m, (d) 15 s-CNT/\( \mu \)m, (e) 20 s-CNT/\( \mu \)m, and (f) 25 s-CNT/\( \mu \)m. The bias dependent Schottky barrier is calculated from the slopes of the ln Id versus 1000/T curves at different bias voltages. ........................................ 92

Figure 54. Plot of bias dependent Schottky barrier \( \Phi (V_d) \) a function of square root of bias voltage for m-CNT/s-CNT device (solid circle) and Pd/s-CNT device (open square) with the linear density of (a) 1 s-CNT/\( \mu \)m, (b) 5 s-CNT/\( \mu \)m, (c) 10 s-CNT/\( \mu \)m, (d) 15 s-CNT/\( \mu \)m, (e) 20
s-CNT/µm, and (f) 25 s-CNT/µm. The zero bias Schottky barrier (Φb) (We call it simply Schottky barrier in the text.) is estimated by extrapolating the linear fitted line to at V_d = 0V. 

Figure 55. Variation of Schottky barrier as a function of density of s-CNT in the channel from 1 to 25 s-CNT/µm. 

Figure 56. Schematic diagram of making RGO electrodes with s-CNT TFTs. (a) GO powder is prepared and diluted with DI water. (b) GO solution (brown color) is reduced by hydrazine reduction to RGO solution (black color). (c) After heating the solution at 90°C for 1hr, the solution is then dropped onto pre-fabricated Pd electrodes. RGO thin film is assembled via AC DEP methods with 5V and 1MHz. (d) RGO thin film is assembled between Pd electrodes, and the sample was coated with PMMA layer, EBL is used to define the channel dimension, and the sample was developed and placed into O2 plasma. The opened area of RGO sheets will be etched away and (e) final RGO electrodes fabricated. (f) Highly enriched s-CNT solution is dropped onto RGO electrodes, and assembled via DEP methods. 

Figure 57. SEM images of (a) RGO thin film assembled between pre-patterned Pd electrodes onto Si/SiO2 substrate, (b) RGO electrodes defined by 2nd EBL process, developing, plasma etching, and acetone lift-off, and (c) s-CNT aligned array via DEP assembly between RGO electrodes. Scale bar indicates 2 µm. 

Figure 58. Electrical transport properties of s-CNT TFTs with RGO electrodes. (a) Output characteristics (I_d vs. V_d) of s-CNT TFTs with RGO electrodes from 0 to -1V with the gate voltage (V_g) range of -15 to -30V in the steps of -1V. (b) Transfer characteristics (I_d vs. V_g) of s-CNT TFTs with RGO electrodes at bias voltage (V_d) as -1V. 

Figure 59. Device statistics (from 13 devices of s-CNT TFTs using RGO electrodes). (a) On-conductance, (b) mobility, (c) transconductance, and (d) current on-off ratio. 

Figure 60. XPS spectra of RGO sheets with different reduction efficiency and deconvolution of the C1’s peaks. The symbols (green square) are the experimental points and the solid lines are the deconvolution of the data. The reduction time is (a) 10, (b) 30, and (c) 60 min. The peaks containing different groups C-C (red curve), C-OH (brown curve), C=O (blue curve), and O=C-OH (black curve) are labeled for clarity. The four deconvoluted peaks indicate the deoxygenated graphene C-C at 284.6 ± 0.1eV, oxygen-containing functional groups for hydroxyl (C-OH) at 286.0 ± 0.1 eV, carbonyl (C=O) at 287.0 ± 0.2 eV, and carboxyl acid (O=C-OH) at 288.6 ±0.1 eV. The percentage of the carbon sp2 fraction (C-C peak) can be determined by the following expression:

\[ \frac{A_{C-C}}{A_{C-C} + A_{C-OH} + A_{C=O} + A_{O=C-OH}} \times 100\% \]

where A denotes the area under the corresponding peaks as marked in Figure 38 (a)-(c). The carbon sp2 fractions are 61%, 66%, and 80% for the reduction time of 10, 30, and 60 min, respectively. Adapted from ref. [111, 112, 117]. 

Figure 61. (a) SEM images of DEP assembled RGO thin film and (b) Current-voltage (I_d-V_d) characteristics of RGO thin films containing different carbon sp2 fraction. (c) Resistance of RGO films with different reduction time. Carbon sp2 fractions are 61% (green square), 66% (blue triangle), and 80% (red circle) for 10, 30, and 60 min reduction time of RGO sheets. (d) SEM image of RGO electrodes after oxidative cutting. 

Figure 62. (a) AFM image of a representative RGO electrode. (b) The height profile of the electrode showing the average thickness of RGO is ~20 nm. Γ line in (a) corresponds to the profile cross-section extracted. Scale bar : 1µm. 

Figure 63. AFM images of the pentacene film deposited on Si/SiO2 substrate containing different electrodes: (a) Pd, (b) 61% RGO, (c) 66% RGO, and (d) 80% RGO electrodes. The pentacene
film morphologies in the channel regions of all the devices are similar with typical grain size of 350-500 nm. Scale bar: 500 nm.

Figure 64. Output characteristics ($I_d$-$V_d$) of pentacene transistors at $V_g$ = 0, -5, -10, -15, and -20 V (bottom to top) for (a) Pd, (b) 61%, (c) 66%, and (d) 80% carbon $sp^2$ fraction RGO in the electrodes. Transfer characteristics ($I_g$-$V_g$) of pentacene transistors at $V_d$ = -50 V (left axis) and ($I_d)^{1/2}$ (right axis) of the devices with (a) Pd, (b) 61%, (c) 66%, and (d) 80% carbon $sp^2$ fraction RGO in the electrodes.

Figure 65. $I_d$-$V_g$ curve in the linear regime for Pd electrodes (yellow), and RGO electrodes with carbon fraction of 61% (green), 66% (blue), and 80% (red) from which we extracted the transconductance ($g_m = dI/dV_g$).

Figure 66. Summary of OFET performance from 40 devices. (a) $\mu$, (b) $I_{on}/I_{off}$, (c) $|I_{on}|$, and (d) $g_m$, for Pd electrode and RGO electrode of 61, 66, and 80% carbon $sp^2$ fraction.

Figure 67. Schematic of energy level diagrams of (a) Pd/pentacene, (b) 61% RGO/pentacene, (c) 66% RGO/pentacene, and (d) 80% RGO/pentacene. This figure shows Fermi level ($E_F$), HOMO level of pentacene, and barrier height ($\phi_b$) at electrode/organic interface.

Figure 68. Room temperature current-voltage characteristics of graphene film on SiO$_2$ substrates. Transfer curve ($I_d$-$V_d$) for (a) CVD-GR ($V_d = 0.1V$), and (b) RGO ($V_d = 0.1V$).

Figure 69. Schematic illustration of fabricating patterned graphene electrodes. (a)-(c) Different types of graphene film are prepared on Si substrate. (d) On top of graphene film, polymer is spin-coated. PMMA is used here as sacrificial layer. Metal is deposited through a metal shadow mask. We used Al. (f) The patterned film protected by etching mask is remained on the substrate after the plasma etching, while the film exposed to plasma etching is completely etched away. (g) After acetone lift-off, patterned graphene is obtained.

Figure 70. Atomic force microscopy (AFM) images of the deposited pentacene film on (a) CVD graphene, (b) RGO, and (c) control Pd electrodes. The height analysis of these films shows the morphology of the films are the similar with an average grain size between 150 to 200 nm and rms surface roughness of 4~6 nm. Scale bar: 500 nm.

Figure 71. Characterization of CVD-GR. (a) SEM image, (b) AFM image, (c) Raman spectra of single-layer CVD-GR, (d) SEM image of resulting patterned CVD-GR electrodes and optical images (inset, scale bar 250 $\mu$m).

Figure 72. Characterization of RGO thin film on Si/SiO$_2$ substrate. (a) SEM image, (b) AFM image, and (c) XPS spectrum of RGO thin film. (d) Final resulting patterned RGO electrodes on Si/SiO$_2$ substrate and optical image (inset, scale bar 250 $\mu$m).

Figure 73. Output ($I_d$-$V_d$) characteristics at different gate voltage ($V_g$) from 0 to -20V in steps of -5V for patterned (a) CVD graphene electrodes, (b) RGO electrode, and (c) Pd electrodes with pentacene. Transfer($I_d$-$V_g$) curve at $V_d$ = -50V for patterned (d) CVD graphene electrodes, (e) RGO electrodes, and (f) Pd electrodes with pentacene.

Figure 74. Mobility is plotted against corresponding current on-off ratio for 10 devices for CVD/pentacene (Red circle), RGO/pentacene (Blue square), and Pd/pentacene (Green triangle).

Figure 75. The examples of current-voltage characteristics of short-channel OFET devices showing the absence of saturation regime. (a) Output characteristics with different gate voltages of channel length 100 nm and oxide thickness 100 nm (top) and channel length 50 nm and oxide thickness 100 nm (bottom) showing diode-like channel behavior. Adapted from ref. [127]. (b) Diode-like behavior output characteristics for 1$\mu$m channel length device with gate voltages from 0 to -60V. Adapted from ref. [128]. (c) Output and transfer (inset) curves of channel length of
70nm OFET devices showing short-channel which preventing saturation. Adapted from ref. [129].

Figure 76. The current-voltage characteristics of pristine graphene film. (a) Output curve at $V_g = 0$V and (b) transfer curve at $V_{ds} = 0.1$V.

Figure 77. Characterization of sub-100nm graphene electrodes. Optical images of (a) pristine exfoliated graphene onto Si/SiO2 substrate, (b) after EBL process to define the channel dimension and developing of PMMA layer, (c) final resulting graphene electrodes with 80nm gap, (d) SEM image and (e) AFM image of well-defined short-channel graphene electrodes.

Figure 78. AFM image of control devices (Au electrodes) with similar channel geometry.

Figure 79. AFM image of pentacene thin film deposition on the devices using (a) Au electrodes and (b) graphene electrodes. The height analysis shows the average grain size of pentacene film on Si/SiO2 substrate is in the range of 150-170nm.

Figure 80. The performance comparison of OFET device using Au electrodes (blue) and graphene electrodes (red). Output/transfer characteristics for Au electrodes (a)-(b) and for graphene electrodes (c)-(d). The table shows the mobility, current ON/OFF ratio, and On current, and threshold voltage for both devices.

Figure 81. (a) In J vs. $V^{1/2}$ plots of short-channel OFET devices at high temperature range of 295K to 230K. The current is strongly depending on the temperature and voltages changes. (b) Arrhenius plot of In ($J_o/T^2$) vs. 1000/T. The value of $J_o$ was extrapolated from the y-intercept of graph (a). From the extracted slope in high temperature range, the charge injection barrier height at graphene/organic was calculated as 0.235 eV.
LIST OF TABLES

Table 1. Comparison of a few recent solution-processed short-channel s-CNT devices ............ 74
Table 2. The current on-off ratio ($I_{on}/I_{off}$), mobility, on-current ($I_{on}$), and transconductance (gm) for the devices with 61, 66, 80 % carbon sp$^2$ fraction and bare Pd electrodes. .......................... 118
LIST OF ABBREVIATIONS

a-Si:H – armorphous silicon hydrogenated
CNT – carbon nanotube
CVD – chemical vapor deposition
DEP – dielectrophoresis
DI water – di-ionized water
EBL – electron beam lithography
HOMO – highest occupied molecular orbital
IPA - isopropyl alcohol
LUMO – lowest occupied molecular orbital
N₂ - nitrogen
OFET – organic field-effect transistor
Pd - palladium
PMMA - Polymethylmethacrylate (Acrylic)
RFID – radio-frequency identification
SEM – scanning emission microscopy
Si – silicon
SiO₂ – silicon di-oxide
CNT – carbon nanotube
CHAPTER 1: INTRODUCTION

1.1 Motivation

Because single-crystal silicon (Si) based electronic devices are fabricated onto Si wafer which cannot be flexible, stretchable and restricted to small areas, a variety of semiconducting materials have been introduced for realizing large-area electronic devices such as thin film transistor (TFT) based active matrix flat panel displays (AMFPDs) based on liquid crystal pixels (LCDs) and organic light emitting diodes (OLEDs), sensors and solarcells as shown in Figure 1.[1-9]

Figure 1. Thin Film Transistors (TFT) based large area applications including (a)-(c) active matrix liquid crystal displays (AMLCDs), active matrix organic liquid emitting diodes (AMOLEDs), thin film printed temperature label, and flat-panel solar cells. Adapted from the ref [5-9].
Polycrystalline Si (poly-Si) was introduced as semiconductors for large-area electronics due to its high mobility (100-200 cm$^2$/Vs for electrons, 10-50 cm$^2$/Vs for holes) but its compatibility with flexible substrate is uncertain and the processing is expensive, complex and non-uniform for large-area products.[10] Amorphous Si (a-Si) was recognized as suitable semiconductors for large-area electronics due to low-cost and low-temperature processing, but it suffers from flexibility, low device stability, and low mobility (1-2 cm$^2$/Vs for electronics and 0.01 cm$^2$/Vs for holes).[11] In addition, a-Si is a photoconductor which caused a large leakage current under light exposure conditions.[12] Therefore, it is highly desirable to find alternative candidates that can be flexible and transparent, low-temperature processing with various substrates, inexpensive, and light-weight with good electrical behavior suitable for large-area electronic applications such as flat panel displays, large-area sensor arrays, smart card, inventory tags, and wearable electronics.

To overcome the issues of Si-based technology towards to large-area electronics, novel semiconducting nanomaterials have been suggested to satisfy the processing issues with temperature and cost, and give a numerous benefits with combination of promising electrical, optical, and mechanical properties. In this thesis, I will focus on two semiconducting nanomaterials as promising candidates for large-area electronics: (i) Carbon nanotubes (CNTs) and (ii) Organic semiconductors. As active channel components, CNTs and organic semiconductors have been studied as possible alternatives for lowering production cost and improving compatibility with various flexible and transparent substrates for next-generation large-area electronic applications. Here, we will discuss extensively the advantages and challenges of such semiconducting nanomaterials for the use of TFTs and their adaptability.
beyond Si technology. In addition, the fundamental understanding of the device performance of TFTs as well as the underlying physics of the fabrication processed will be further discussed.

- **Carbon Nanotube Thin Film Transistors for Large Area Electronics**

Due to the combination of remarkable electronic, optical, and mechanical properties, single-walled carbon nanotubes (CNTs) (Figure 2), a cylindrical rolled-up from thin graphene sheets, have been considered to be an ideal semiconducting materials candidate for large-area electronics. Numerous works have shown that the CNT films can be made by either random networks or aligned array which can serve as excellent active channel components.

![Figure 2. Different types of graphitic forms as 0D bulkyballs, rolled into 1D nanotubes, 2D graphene or stacked into 3D graphite. Adapted from ref. [103].](image-url)
CNT thin film transistors (TFTs) have attracted a great deal of attention as promising components for one of the next generation flexible and transparent electronic devices, sensors, and high frequency devices.[13-19] CNT-TFTs can be advantageous over individual CNT devices due to device-to-device homogeneity, large area coverage, higher output current compared to individual nanotube devices as well as processability over a large-area alternative to conventional Si or other semiconductors for integrated circuitry applications. In order to fabricate high mobility as well as high current on-off switching devices, high purity of semiconducting carbon nanotubes (s-CNTs) as channel material are essential to realize high performance CNT-TFTs. This is because even small fraction (< 2%) of metallic CNTs (m-CNTs) in the channel can degrade the gate modulation of the devices. Solution-based sorting techniques such as density gradient ultracentrifugation have been suggested to provide highly enriched semiconducting CNTs in aqueous solution.[20].

In order to make high-performance of CNT TFTs, having a negligible contact resistance originated at metal-semiconductor interface is required to enhance the charge injection/transport. Despite many experimental and theoretical studies, many contradictory and predictions are still remained concerning the influence of interface states on the Schottky barrier height at metal-semiconductor interface.[21] Improving the metal-semiconductor interface may be considered as one of the major factors, which can significantly enhance the performance of devices.

- **Organic Thin Film Transistors for Large Area Electronics**

Fabrication of high performance organic thin film field-effect transistors (OFETs) has developed for the main building blocks for future flexible and transparent electronic devices due
to low-cost, light-weight, and large-area flexible electronic devices, such as flexible and transparent electronics, sensors, and solar cells (Figure 3).[22-24]

![Figure 3](image)

Figure 3. (a) A conceptual view of future organic flexible display which can be rolled into a pen-like device when not in use. Images courtesy of Universal Display Corp. (b) A full color, 13-inch OLED display with only 2mm tick. (c) A conceptual view of integrated circuits on flexible, and transparent plastic substrate. Photograph courtesy of T. Jackson, Penn state Univ. Adapted from ref. [23].

The conventional noble metals were commonly used for electrode materials including gold (Au), platinum (Pt), nickel (Ni), and palladium (Pd) due to their chemical stability and work function, which can match the highest occupied molecular orbital (HOMO) of p-type organic semiconductors. However, the use of metal electrodes can form several interfacial barriers at metal-organic interface such as the discontinuity in morphology, dipole barriers, and Schottky barriers, which cause low charge injection at metal-organic interface and thus reduce the performance of OFETs.[25-30] Even though the contact at electrode-semiconductor interface is well-studied in Si-based transistors with conventional processes such as semiconductor doping or
metal alloying[31]. The optimization and understanding of improving electrode-semiconductor interface in OFETs is still lack. Figure 4 shows the illustration of possible energy level diagram showing the reduced effective work function of metal electrodes due to vacuum level breakdown by a large interfacial barrier formation at metal-organic interface.[25]

![Figure 4](image)

Figure 4. Schematic diagram of energy level difference between metal electrode and organic semiconductor (a) without and (b) with an interfacial dipole barrier. Adapted from ref [25].

As we discussed above, one of the major bottle necks for making high-performance nanoelectronic devices is to optimize and improve the metal/semiconductor interface. The physical fundamental understanding of improved charge injection/transport mechanism should be further investigated. In order to overcome the contact issues in nanoelectronic devices at metal-semiconductor, we will introduce carbon-based material electrodes used as alternative electrode over conventional metal electrodes. Our simple and novel fabrication techniques of
carbon-based electrodes, nanoelectronic device applications using carbon-based electrodes, and their electrical/optical characterization will be fully investigated in this thesis.

1.2 Organization of Thesis

In Chapter 2, I will discuss the basic structures and working principles of field-effect transistors (FETs). Then, I will introduce the historical overview of novel nanomaterials such as carbon nanotubes, graphene, and organic semiconductors.

Chapter 3 will introduce the details of device fabrication methods used in our devices. First, metal electrodes by photolithography and ebeam lithography will be discussed. Our simple and novel techniques of making carbon nanotubes (CNTs) and graphene electrodes for nanoelectronic devices will be described. In addition, the fabrication of CNT thin film transistors (CNT-TFTs) and organic field-effect transistors will be introduced, and their electrical measurement setups and high-resolution imaging methods will be discussed.

Chapter 4 will show the high performance solution-processed semiconducting enriched carbon nanotubes (s-CNTs) thin film transistors (TFTs) with metallic carbon nanotubes (m-CNTs) electrodes. I will introduce our novel assembly technique of solution-processed s-CNTs via dielectrophoresis (DEP) method using m-CNT electrodes. We measured the devices with room and low temperature to investigate transport properties. Using our unique geometry and interface engineering at m-CNT/s-CNT contacts, we found the high-performance of s-CNT TFTs using m-CNT electrodes is not only from favorable π-π interaction at m-CNT/s-CNT but also from the lower injection barrier height at m-CNT/s-CNT interface. The performance of devices
with m-CNT electrodes was compared with conventional metal electrodes. We will discuss the
detail studies in the Chapter.

Chapter 5 will introduce the tunable density effect of s-CNTs in the TFTs using m-CNTs
electrodes. The density was tuned by varying the solution concentration of s-CNTs, and different
density of s-CNT was assembled between m-CNT electrodes via DEP methods. This
performance was compared to s-CNT TFTs with control Pd electrodes. From the temperature
dependent studies, the injection barrier at each density of s-CNT TFTs were calculated and
compared.

Chapter 6 will show aligned array of s-CNTs with reduced graphene oxide (RGO)
electrodes. We will introduce our simple fabrication of solution-processed RGO electrodes, and
discuss the performance of s-CNT TFTs using RGO electrodes and detailed electrical transport
properties of the devices. The device statistics will be shown and further discussion will be
presented in the Chapter.

Chapter 7 will introduce the solution-processed RGO electrodes for OFETs. The impact
of different carbon \( sp^2 \) fraction in RGO as electrodes for OFETs will be further discussed in this
chapter.

Chapter 8 will show how to pattern the large-area graphene films, such as chemical vapor
deposition (CVD) grown graphene and RGO, with their performance comparison. Our
environmental-friendly and simple patterning method will be shown here.

Chapter 9 will show the fabrication of high-performance short-channel OFETs using
graphene electrodes to study the role of contacts. The graphene films were prepared by
mechanically exfoliated from bulk graphite. The OFET devices were fabricated using the sub-
100 nm channel with graphene electrodes, and the fabrication methods will be described in this chapter. The charge injection mechanism will be shown by temperature dependent investigations.

Finally, in Chapter 10, I will conclude the summary of results and suggestion and future works.
CHAPTER 2 : BACKGROUND

2.1 Carbon Nanotubes (CNTs)

2.1.1 Historical Overview and Properties of CNTs

In 1985, the discovery of fullerenes, the zero-dimensional (0D) form of graphitic carbon, opened up the ways to find a number of carbon allotropes (Figure 5)[32], and new class of research field in carbon-related materials including carbon nanotubes and graphene. Sumio Ijima at IBM discovered multi-walled CNTs from an arc discharge method in 1991 [33], and his paper was generated significant interest in carbon-based nanostructures which has been the great motivation in the area of nanotechnology. Two years later, the single-walled carbon nanotubes (CNTs) was successfully produced by Ijima[34] and Bethune[35], and it has found that CNTs can provide advanced developments in the future electronics due to combination of its unique 1D structure, high mobility, and large current density and high intrinsic cut-off frequency.
Figure 5. Different forms of carbon alltropes. Graphene (Top left) is a honeycomb lattice of carbon atoms. Graphite (top right) can be viewed as a stack of graphene layers. Carbon nanotubes are rolled-up cylinders of graphene (bottom left). Fullerenes (C60) are molecules consisting of wrapped graphene by the introduction of pentagons on the hexagonal lattice. Adapted from ref [104].

The structure, diameter, and electronic types of a single-walled CNTs are determined by the chiral vector (i.e. roll-up vector), $C = na_1 + ma_2$, denoted as (n,m), which defines on the honeycomb lattice by unit vectors $a_1$ and $a_2$, and the chiral angle $\theta$ is measured between $C$ and $a_1$ represented as chirality (Figure 6).[36]
Figure 6. Adapted from Carbon Nanotube Electronics, Adapted from ref [36]. © 2003 IEEE.

Figure 7. The schematic theoretical diagram of CNT structure. The properties of CNTs can be decided depending on its chirality. (a) armchair, (b) zigzag, and (c) chiral. The actual tubules shown in the figure correspond to (n,m) values of: (a) (5,5), (b) (9,0), and (c) (10, 5). Adapted from ref [37].
For example, ‘armchair’ nanotubes, classified (n,n), show metallic behavior, and ‘zigzag’ nanotubes, classified (n,0), show semiconducting behavior as shown in Figure 7.[37] Therefore, it is also important to have a specific electronic types (metallic vs. semiconducting) of nanotubes depending on the purpose of research and target applications. In our thesis, we will use metallic nanotubes (m-CNTs) as electrodes materials, and highly purified semiconducting nanotubes (s-CNTs) as channel materials.

Single-walled CNTs are composed of cylinder shape with graphene sheets rolled in three-dimension (3D) with composed of a diameter of 1-2 nm to several nanometers and a high aspect ratio (i.e. length to diameter ratio) that ranges from $10^2$ to $10^7$. The large aspect ratio makes CNTs to have unique one-dimensional (1D) system, and this offers novel electronic properties such as ballistic transport (without scattering) over long nanotube lengths enabling them to carry high currents[38] and strong field-emission of electrons from the end of tips of CNTs enabling them to be fascinating point sources or have wide applications as probes or emitters[39]. The thin films of CNTs have a high optical transparency in the visible light, high electrical conductivity, and strong mechanical properties such as flexibility and stretchability, which all makes them promising candidates for flexible and transparent electronic applications for electrode materials, field-effect transistors, solar-cell, and sensors.[17]

2.1.2 CNTs for Thin Film Transistors

CNTs have exceptional electronic, mechanical, and optical properties which can be considered as promising candidate materials for next generation large-area electronics. CNT
Thin film transistors (TFTs) can be a main building block for the fabrication of high-performance flexible and transparent applications such as future electronic devices, high frequency devices, and sensors.[15, 17, 40-42] The TFTs can be advantageous over the individual nanotube FETs due to device homogeneity as well as higher output current. The CNT TFTs can be made of either random network or aligned array. The mixed CNTs are grown by the chemical vapor deposition (CVD) method, and contain a number of metallic nanotubes (m-CNTs). Since the metallic pathways tend to dominate the transport in the TFTs which caused lower current on/off ratio, selective removal of m-CNTs are needed. However, the removal of m-CNTs has detrimental effects on the remaining nanotubes in the network. Therefore, it is important to use all semiconducting CNTs (s-CNTs) for high-performance s-CNT TFTs fabrication.

Studies have shown that solution-based sorting techniques can provide highly enriched s-CNTs in aqueous solution.[20] Here we will overview a few studies (Figure 8) reported the fabrication of solution-processed s-CNT TFTs using highly pure s-CNTs either in a random network or in an aligned array. Wang et al reported highly pure s-CNT (95%, separated nanotubes) TFTs in random network for wafer-scale processing, and mobility of 0.03 cm$^2$/Vs with a on/off ratio $>10^4$.[43] They also compared the performance of s-CNT TFTs with the mixed CNT TFTs (67%, mixed nanotubes), and the mobility was found to be 52 cm$^2$/Vs with low on/off ratio $<$10. The lower current on/off ratio with higher mobility is expected in lower portion of s-CNT TFTs due to metallic pathways. For ideal semiconducting device applications, having a high switching current on/off ratio is required. Engel et al reported self-assembly and self-alignedment of s-CNTs from solution on macro- and microscale forming regular arrays of
dense and highly aligned CNT films covering the entire chip.[44] They also used highly pure s-CNTs (99%) and reported the device mobility 10 cm²/Vs of with current on/off ratio ~10⁴. Wang et al showed another study on macroelectronic integrated circuits using CNT TFTs with 98% purity of s-CNTs showing the mobility of 30 cm²/Vs and current on/off ratio of ~10⁵. Interestingly, this study shows the best device performance is found from the large channel length (100 μm) and it becomes poor when the channel length is reduced (4μm). Similar observation is found also from the study by Rouhi et al which indicated that the device performance of mobility from 40 to 11 cm²/Vs as the channel length decreased from 100 to 20 μm.

Figure 8. s-CNT thin films from the literature. (a) Device schematic diagram of random network s-CNT TFTs Adpated from ref [48] (b) SEM image of s-CNT random arrays. Adpated from ref [48]. (c) SEM images of self-assembled and self-aligned s-CNT arranges. Adapted from ref [44]. (d) AFM images of random network s-CNT arrays. Adapted from ref [14].

The device mobility an current on/off ratio are the most important parameters that determine the device performance of CNT TFTs. Here we will show how to extract and calculate
the values. The CNT TFTs is composed of s-CNT thin film as semiconductor, source/drain electrode, and gate electrode which is similar to standard metal oxide field effect transistors (MOSFETs). However, the calculation of capacitance of CNT TFTs is different than conventional MOSFETs because CNT TFTs need a specific capacitance calculation related to the number of CNTs on the gate substrate.

Figure 9 shows the typical output/transfer characteristics of the s-CNT TFT devices. As seen in Figure 9 (a), the devices show a good gate modulation. The performance parameters such as mobility, on-conductance, transconductance, and current on/off ratio can be extracted from the transfer curve ($I_d$-$V_g$).

![Figure 9](image)

Figure 9. Typical current-voltage characteristics of s-CNT TFTs. (a) Output ($I_d$ vs. $V_d$) and (b) Transfer ($I_d$ vs. $V_g$) characteristics. Adapted from ref. [14].
1. **Transconductance** ($g_m = dI_d/dV_g$)

The transconductance can be extracted from the slope of $I_d$ vs. $V_g$ curve. The transconductance ($g_m$) can be extracted by $g_m = dI_d/dV_g$.

2. **The mobility and Specific capacitance (mobility)**

The liner mobility can be extracted from $I_d$ vs. $V_g$ curve, and the mobility is calculated using the standard formula, $\mu = (L/WC_iV_d)(g_m)$ where $C_i$ is the specific capacitance per unit area of s-CNT array in either random network or aligned array. The specific capacitance can be calculated by $C_i = \frac{D}{[C_Q^{-1} + (1/2\pi\varepsilon_\alpha)\ln\sinh(2\pi\alpha D)/\pi Dr]}$ where $C_Q$ is the quantum capacitance of CNT ($4 \times 10^{-10} \text{Fm}^{-1}$), $t_{ox}$ is the oxide thickness, $\varepsilon$ is the dielectric constant of gate dielectric (ex. SiO$_2$=3.9), $\varepsilon_\alpha$ is the permittivity of vacuum, $r$ is the average radius of the s-CNTs and $D$ is the linear density of s-CNTs in the channel.[40]

3. **On-conductance** ($G_{on} = I_{on}/V_d$)

On-conductance can be calculated from $I_d$ vs. $V_g$ curve with the equation of $G_{on} = I_{on}/V_d$.

4. **Current On/Off ratio** ($I_{ON/OFF} = I_{ON}/I_{OFF}$)

Current on/off ratio can be also calculated from $I_d$ vs. $V_g$ curve with the equation of $I_{ON/OFF} = I_{ON}/I_{OFF}$.

2.1.3 Metal Electrodes for CNT Thin Film Transistors

One of the major obstacles for large scale integration of CNT is to realize ohmic contacts between metal electrodes and semiconducting CNTs (s-CNTs).[21] At metal/CNT interface, hole
injection from metal to nanotubes is dependent on the height between Fermi level of metal electrodes and valence band of nanotubes, called Schottky barrier (SB) height. Overall, a small Schottky barrier will be preferable due to lowered contact resistance as well as higher current on/off ratio. In general it is more difficult to make a “good” contact to source/drain electrodes and wide-gap semiconductor due to large barrier formation at the interface.[45] Since the energy gap ($E_g$) of semiconducting nanotubes is inversely proportional to diameter of nanotubes ($d$),[46] the measuring of $d$ is important to obtain the information of energy gap. In order to improve the contact at metal/s-CNT interface, understanding of Schottky barriers formation is required to fabricate high-performance s-CNT TFT devices. Chen et al investigated of the device performance of p-type s-CNT TFTs by changing the metal electrodes (Pd, Ti, Al) as shown in Figure 10 (a).[47]

Figure 10. (a) Transfer characteristics of CNT FETs using Pd electrodes (b) On-current variation depending on the choice of metal electrodes in CNT TFTs with estimated Schottky Barrier height. Inset: On-current variation depending on the diameter of nanotubes. Adapted from ref. [47].
Figure 10 (b) shows the plot of on-current and estimated SB height of CNT TFTs as function of diameter. SB height was calculated assuming all the work function of all nanotubes are consistent, and it is found SB is increases linearly with increasing $E_g$, which means decrease diameter of nanotubes. This study claims that a favorable contact at metal/CNT can be existed by controlling a diameter of CNTs and choice of metal electrodes for high-performance CNT TFT fabrication. In addition, they mentioned the improvements of on-current ($I_{on}$) is and the reproducible device current is essential.

Figure 11. Schottky barrier heights (hole injection) as a function of diameter from different studies. Adapted from ref. [21].

As shown in the Figure 11 reported by Svensson et al,[21] the SB height can be further decreased by increasing the diameter. We wanted to note that our nanotube diameters are in the
range of 1.5 to 1.9 nm, and it was found the SB height of our devices were matched to this plot. In spite of many theoretical and experimental assumptions, there are still many contradictory results and predictions, and deeper understanding SB height in metal/CNT contact is preferred.[21]

Indeed, we found that the performance of solution-processed highly enriched (>98%) s-CNT TFTs decrease with a decreasing channel length from recent studies.[14, 44, 48, 49] All of these devices use conventional metal electrodes. Since there is a small fraction of metallic CNTs (m-CNTs) (<2%) in the s-CNT solution, the decreased current on/off ratio when channel decreased can be explained by the presence of a small portions of m-CNTs. However, the decrease of mobility with decreasing channel length was observed in the s-CNT TFTs where on/off ratio was greater than 100 (meaning no m-CNT percolation). The Burke group speculated that the decrease of mobility with decreasing the channel length may be due to the contact effect at metal/CNT interface, and in longer channel the contact effect will be negligible in comparison with the channel resistance while the contact effect is significant in short channel devices.[14] It should be noted that the short channel CNT TFTs are important for high frequency applications as the on-current increases with a decrease in the channel length and the cutoff frequency is inversely proportional to the square of the channel length.[14, 49] Therefore, there are still room for further improvements of device performance by improving contacts, and this can be a significance to realize the overreaching goals of CNT based TFTs.

In this thesis, we will work on whether the use of carbon-based materials (CNTs or graphene) as alternative electrodes can be further improve the contact at metal/CNT interface, and provide the enhanced device performance.
2.2 Graphene

2.2.1 Historical Overview and Properties of Graphene

The first successful isolation of atomically thin layer of graphene in 2004 amazed the scientific community because more than 70 years ago, Landau and Peierls argued that strictly 2D crystals were thermodynamically unstable and could not exist.[50, 51] Indeed, there was no experimental tool to search for one-atom-thick flakes exfoliated from the bulk graphite in pencil.

Graphene, two-dimensional (2D) sheet of $sp^2$ hybridized carbon, is a basic building block of other important carbon allotropes. It can be stacked to form 3D graphite, rolled into 1D nanotubes, and wrapped into 0D fullerenes (bulkyballs). Long-range $\pi$-conjugation in graphene yields extraordinary thermal, mechanical, and electrical properties, which have long been the interest of many theoretical studies and more recently became an exciting field for experimentalists.[52] Although many theoretical studies and some attempts of mechanical isolation of graphene were made prior to 2004, the first experimental isolation of single-layer graphene was found by Geim and his coworkers[53] using historically significant “Scotch tape” method mechanically exfoliated graphene, which led to Nobel Prize in 2010 (Figure 12).
Figure 12. The Nobel prize in physics in 2010 was awarded jointly to Andre Geim and Konstantin Novoselov for groundbreaking experiments regarding the two-dimensional (2D) material graphene. (Top left) Adapted from http://www.nobelprize.org/nobel_prizes/physics/laureates/2010/ The successful exfoliation of single-layer graphene. Adapted from ref. [53]. (Top right) The cartoon shows the first graphene samples were produced by exfoliating atom thick layers from a graphite using Scotch tape leading Nobel prize in 2010. Adapted from www.strippedscience.com. (Bottom)

Graphene is $sp^2$ bonded network of hexagonally arranged carbon atoms with two atoms per unit cell. Due to the high quality of 2D crystal lattice, single-layer of graphene has unusual low density of defects, and high carrier mobility (upto $200,000 \text{ cm}^2/\text{Vs}$). Figure 13 shows the unique bandstructure of single-layer graphene with zero-bandgap which determines the graphene as semi-metal properties with unusual linearly dispersing electronic excitations called Drac-electrons. The structural flexibility of graphene is also due to its extraordinary electronic properties. The understanding and control of graphene properties can open the new ways for future applications.
In particular, the unique properties such as transparency, flexibility, high-workfunction, high electrical conductivity, large-area coverage, and tunable band-gap makes graphene as promising candidate for alternative electrodes materials for transparent conducting electrodes. In this thesis, we will study the effect of using graphene as alternative electrodes instead of using conventional metal electrodes by investigating the device electrical characteristics.
2.3 Organic Semiconductors

2.3.1 Historical Overview and Properties of Organic Semiconductors

The first organic field-effect transistors (OFETs) based on organic semiconductors in mid-1980 opened up a new field of research in organic electronics, which have many advantages in their potential applications such as large-area coverage with low-cost, light-weight, and flexible and transparent devices for future electronics.[54-57] Some of these applications are available in commercial market as their prototypes.[58, 59]

![Ethylene representations](image)

Figure 14. Several representations of ethylene, which has two $sp^2$ bonded carbon atoms. (a) Ball and stick model, (b) a chemical structure, and (c) schematic of orbital diagram showing both pi-bond and sigma-bond. Adapted from ref [60]. Kymissis, Ioannis. "Organic Field Effect Transistors: Theory, Fabrication and Characterization." Page. 7, Springer, 2009, Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.

In comparison to inorganic semiconductor, organic semiconductors are composed of carbon-rich materials, and carbon atoms have an unusual ability to hybridize the orbitals into a number of bonding configurations by superpositioning of s and p orbitals. The carbon atoms in these compounds are “backbone” structure consisting of sigma bond ($\sigma$-bond) from $sp^2$ hybridized orbitals and pi bond ($\pi$-bond) from unhybridized $p_z$ orbital. (Figure 14)[60] When this
structure is repeated over a large number of carbon atoms, the \( \pi \)-electrons are delocalized above and below the plane which is termed as “conjugation”.[61] Due to the energy difference in organic semiconductor between the occupied binding orbitals and the unoccupied anti-binding orbitals, the energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) is determined. Not too much large energy gap is formed due to \( p_z \) orbitals from \( \pi \)-bond in \( sp^2 \) hybridization leading semiconducting properties not insulating.

2.3.2 Organic Semiconductors for Organic Field-Effect Transistors

Figure 6 shows the two general classes of organic semiconductors: (i) small molecules and (ii) conjugated polymers. In small molecules such as pentacene, the carbon atoms form a series of benzene rings as basic unit and \( \pi \)-electrons are delocalized through the molecules, leading smaller bandgap. On the other hand, conjugated polymer form a longer chain and the \( \pi \)-electrons (along the chain) form a 1D \( \pi \)-electrons systems, resulting in 1D band structure. In this thesis, we will use pentacene as the most common p-type organic semiconductors for OFETs.
‘Pentacene’ is commercially available material, and highly conjugated compound organic semiconductor consisting of five benzene rings (Figure 15). The typical type of pentacene transistors showed p-type behavior due to work function matching with gold (Au) or palladium (Pd) electrodes as ~5.1 eV and its HOMO level resulting smaller barrier than electrons. The common deposition of pentacene is thermally vacuum evaporation, and the film shows better polycrystalline structure than typical solution-processed organic thin film, which led high mobility and current on/off ratio in OFET device performance.

Interest in organic semiconductor brings the development of organic field-effect transisotrs (OFETs). The basic device configurations of OFETs are illustrated in Figure 16: (i)
bottom-gate and bottom-contact, (ii) bottom-gate and top-contact, (iii) top-gate and bottom-contact, and (iv) top-gate and top-contact. In this thesis, we will use ‘bottom-gate and bottom-contact’ configurations for all devices. OFETs is consist of source/drain electrodes, gate dielectric and gate electrodes, and organic semiconductor layer for channel active material.

Figure 16. Device configurations of OFETs. (a) Bottom-gate with top-contact electrodes, (b) top-gate with bottom-contact electrodes, (c) bottom-gate with bottom-contact electrodes, and (d) top-gate with top-contact electrodes.

We called the gap between the source and drain as ‘Channel’. In OFETs, the charge carriers travel in the channel parallel to the surface of the gate dielectric. The source and drain electrodes provide access to the channel and are engineered to inject charge well under all bias conditions. The gate is separated from the channel by the gate dielectric forming a capacitor to the active channel thin film. It is the gate dielectric that allows the creation of a field across the semiconductor and the resultant accumulation and depletion carriers.
Figure 17. Typical (a) output characteristics \((I_d-V_d)\) with different gate voltage\((V_g)\) of OFETs with linear regime (red) and saturation regime (orange) and (b) transfer characteristics \((I_d-V_g)\) with fixed bias voltage showing ON state and OFF state, and the threshold voltage \((V_{th})\). Threshold voltage can be extracted from the x-axis intercept of the linear extrapolation of the slope of \((I_d)^{1/2}\) vs. \(V_g\). Adapted from ref. [3].

The typical current-voltage characteristics of output curve \((I_d-V_d)\) is shown in Figure 17 with linear and saturation regime.

**1-Device mobility**

In the linear regime (Figure 17 (a), red), the drain current \((I_d)\) is directly proportional to gate voltage \((V_g)\), and the field-effect mobility in linear regime \((\mu_{lin})\) can be extracted from \(I_d-V_g\) curve at fixed bias voltage \((V_d)\) with the equation of \(\mu_{lin} = (dI_d/dV_g)(L/WC_iV_d)\) where \(L\) is channel length, \(W\) is channel width, and \(C_i\) is gate capacitance per unit area. The field-effect mobility in the saturation regime \((\mu_{sat})\) (Figure 17 (a), orange) can be extracted using the equation of \(\mu_{sat} = (2LI_{d,sat})(WC_i(V_g-V_{th})^2)\) where \(V_{th}\) is threshold voltage because the square root
of the saturation current is proportional to the $V_g$. The charge carrier mobility is one of the crucial factors to determine the electrical performance of OFETs.

2-On-current ($I_{ON}$)

As shown in Figure 17 (b), on-current can be extracted from output current at ON state in the transfer curve ($I_d$-$V_g$).

3-Current on-off ratio ($I_{ON/OFF}$)

Current on/off ratio ($I_{ON/OFF}$) can be calculated from the equation of $I_{ON/OFF} = I_{ON}/I_{OFF}$ from the transfer curve ($I_d$-$V_g$ curve).

4-Threshold voltage ($V_{th}$)

Threshold voltage can be extracted from the x-axis intercept linearly extrapolating from the ($I_d$)$^{1/2}$ vs. $V_g$ curve.

2.3.2 Metal Electrodes for OFETs

One of the major bottlenecks in fabricating high-performance OFETs is a formation of large interfacial barrier at metal/organic contact. As the charge-injecting electrode for OFETs, conventional noble metals such as Au or Pd have been used due to their chemical stability and work function, which can match the HOMO level of p-type organic semiconductors.
Figure 18. Interfacial energy level diagram of (a) without and (b) with vacuum level shift. The hole injection barrier ($\phi_B^p$), which is the energy gap between Fermi level of metal electrodes and HOMO level of organic semiconductor, is increased with the broken vacuum level. The vacuum level shift is maybe due to formation of interfacial dipole layer at metal-organic contact. Adapted from ref. [62].

However, the use of metal electrodes can form several interfacial barriers at metal electrode/organic semiconductor such as the discontinuity in morphology, dipole barriers, and Schottky barriers, which cause low charge injection at metal-organic interface and thus reduce the performance of OFETs.

As shown in Figure 18, the effective work function of metal electrodes is significantly reduced due to breakdown of vacuum level after the contact with metal electrodes and organic semiconductor, and this is because of interfacial dipole formation at metal/organic interface.[62] Studies have shown that there would be different types of dipole formation will be occur at the metal/organic interface, which reduce the performance of OFETs.[62] The different types of dipole barrier formation at metal-organic semiconductor interface is illustrated in Figure 19.[63]
2.4 Carbon-Based Materials as Alternative Electrodes

Interface engineering plays a important role in determining the charge injection at electrode/semiconductor contact. Having a favorable interfacial contact can be significantly helpful to lower the contact resistance and thus lower injection barrier, which can further enhance the device performance in the future nanoelectronic applications. Here we reviewed the recent studies on nanoelectronic devices (such as s-CNT TFTs and OFETs) using carbon-based electrodes. The remaining challenges and opportunities will be also addressed.
2.4.1 Carbon Nanotube Electrodes for Nanoelectronic Devices

In order to overcome the challenges of large barrier at metal/organic interface, carbon-based materials, such as carbon nanotubes or graphene, have been suggested as promising alternative electrodes materials.[64-67] Recently, several research groups have reported the enhanced device performance of OFETs using CNT electrodes as seen in Figure 20. In these studies, CNT electrodes were fabricated with various techniques using either individual CNT, random network CNTs, CNT/polymer composite, or aligned array CNTs. These studies also suggested that the device performance of OFETs using CNT electrode is enhanced compared to that of OFETs using metal electrodes.

![Figure 20. The examples of enhanced device performance of OFET using CNT electrodes in different studies. (a) Adapted from ref [64]. (b) Adapted from ref. [65]. (c) Adapted from [66]. and (d) Adapted from ref. [67].](image)

The enhanced performance of using CNTs as electrodes has been brought by not only high work function of CNTs matched to HOMO level of organic semiconductor but also
favorable π-π interaction at CNT-organic interface resulting reduced charge injection barrier at electrode/organic interface.[67-69] In addition, CNTs have strong field-emission due to their unique 1D structure which can enhance the charge injection from CNT to organic semiconductors.[39]

One of our group members put extensive effort on fabrication of novel CNT electrodes as well as their integration to OFETs, and found improved device performance.[68-71] In these works, the device performance of OFETs was found to be significantly enhanced, and the direct evidence of barrier height at electrode/organic semiconductor was estimated from the temperature dependent studies showing much less injection barrier height at CNT/organic interface compared to metal/organic interface.[69] We also found the density of CNTs in the electrodes will be a impact on determining the performance of OFETs. From this motivation, we also published the work towards to tunable density of CNTs in the electrodes for pentacene transistors.[68] Interestingly, we found the best performance from the high density of CNT electrodes in OFETs. The low density of CNT electrodes still show the enhanced performance compared to bare metal (Pd) electrodes. In this work[68], we concluded that the interfacial area at CNT/pentacene will be an important role in determining the performance of OFETs.

Based on this motivation, we began to think whether the CNT electrodes can be advantageous to improve the solution-processed highly enriched s-CNT TFTs. We will discuss the detail studies in our thesis.
2.4.2 Graphene Electrodes for Nanoelectronic Devices

Graphene is a promising transparent and flexible conducting electrode material for future generation applications due to its high optical transparency excellent electronic and mechanical properties which can be applied to field-effect transistors, light-emitting diodes, flexible devices and solarcells. The graphene films can be prepared by mechanically exfoliated graphene, solution-processed reduced graphene oxide (RGO), and chemical vapor deposition (CVD) growth. We will review the use of different types graphene film as electrode in applications. The use of graphene electrodes have been highlighted in transistors, light-emitting diodes, solar cells and flexible devices.[72]

![Graphene Electrodes for Nanoelectronic Devices](image)

Figure 21. The transmittance as a function of sheet resistance of graphene films reported from several groups. Adapted from ref. [72].
3.1 Introduction

In this chapter, we will introduce fabrication and characterization techniques of nano-scale electronic devices using state-of-art fabrication tools and methods, which enable to manipulate and probe the new class of nanoscale materials and their related devices.

Firstly, we begin with the overview of fabrication steps of metal electrodes (contact pads) using photolithography, metal evaporation using ebeam/thermal evaporator and lift-off. Then, electron beam lithography (EBL) is introduced by creating small structure which photolithography is not able to fabricate. In order to fabricate carbon nanotube (CNT) and graphene electrodes, solution-processed dielectrophoresis (DEP) assembly, chemical vapor deposition (CVD) growth, and exfoliation techniques followed by plasma etching as well as lift-off will be introduced. Finally, I will introduce the fabrication details of high quality of organic field-effect transistors (OFETs) by introducing thin film deposition such as vacuum thermal deposition.

The electronic transport measurements for both room and low temperature setups and characterization for high-resolution imaging techniques will be further discussed.

3.2 Fabrication of Metal Electrodes

Our devices were fabricated onto heavily doped (<0.005 Ωcm) 3 inch silicon (Si) substrates (350 μm thick, Silicon Quest International) coated with a thermally grown 250 nm thick silicon dioxide (SiO₂) layer.

3.2.1 Photolithography

We performed photolithography to define the large electrode patterns for bonding pads, alignment markers for later EBL process as well as probe measurement contact pads. The electrode leads typically consist of 1 μm or larger features. This saved our processing times for later EBL as well as made easier to produce many chips in each wafer. Figure 22 shows the schematic diagram of photolithography steps to fabricate the large metal electrodes on Si/SiO₂ substrate. The photoresist (Shipley S1813) was spin coated onto Si substrate at 6000 rpm for 30 sec and soft baked in an oven at 100°C for 4 min. After coating the photoresist, the wafer was exposed in a EVG 620 mask aligner (Top side alignment and soft/hard contact, The electrodes patterns are pre-defined on our shadow mask (Au/Cr). UV filter type 405 nm, Lamp power: 11.3 mW/cm²) for 10 sec. After the exposure, the wafer is then developed in diluted developer (CD-26, 90% in DI water) for 25 sec, followed by rinse with DI water and N₂ blown dry. Figure 23 shows the resulting optical patterns defined on Si substrate.
3.2.2 Electron Beam Lithography (EBL)

The advantages of EBL is to define and create the smaller structures (less than 2 μm). Since photolithography requires the shadow mask for each pattern to draw and the price of mask is expensive, photolithography may not be appropriate to create a prototype nanoelectronic devices for our research purpose where various shape and size of patterns are essential to fabricate the nanoelectronic devices. To fulfill the requirements, EBL can be used as promising
process since it is maskless lithography. It requires the electron beam which changes the solubility of the resist and exposed or non-exposed area can be removed by immersing the sample in the solvent (acetone). Also, the minimum resolution of EBL is 10 nm resolution which photolithography cannot draw yet.

Using EBL, we were able to pattern our devices with desired shape and size with DesignCAD software and Nanometer Pattern Generation System (NPGS) program communicated with Zeiss Ultra 55 scanning electron microscopy (SEM) instrument. Figure 24 shows the typical EBL process diagram.

![EBL Process Diagram](image)

**Figure 24.** Schematic diagram of electrode pattern fabrication steps using EBL on Si substrate. First, PMMA is spincoated on the Si substrate and then the electrode patterns are defined by EBL. The desired metal is evaporated. (Normally Au/Cr or Pd/Cr.) Finally, Lift-off is performed using acetone followed by IPA, DI water rinse, and N₂ blown dry.
As described in Figure 24, the single layer e-beam resist, PMMA (950K, C2, 2%, MicroChem) is spin-coated on Si substrate at 4000 rpm for 1 min, and then placed on hot plate to bake during 15 min at 180 °C. The thickness of PMMA is 100-150 nm, which is at least 3 times higher than metal deposition for easy lift-off. Then, the electrode patterns are defined using EBL (Zeiss Ultra 55 SEM) exposed with an area dose of 270-300 μC/cm² and voltage of 28 kV. As for the developing process, the devices are immersed into MIBK:IPA (1:3) for 60 sec and IPA for 10 sec followed by N₂ blown dry. The desired novel conventional metals, such as gold (Au), Palladium (Pd), Crominium (Cr), and other transition metals, depending upon their purpose, can be deposited by thermal/e-beam evaporation. For our device, Pd/Cr or Au/Cr are common electrode materials. Pd and Cr are mostly e-beam evaporated and Au is thermally evaporated. The vacuum pressure is maintained as 10⁻⁶ Torr and the deposition rate is set to lower rate as 0.1-0.2 Å/sec. Finally, the devices are placed into acetone for 3-4 hours to remove the residual of PMMA followed by IPA, DI water washing and N₂ blown dry. Figure 25 shows the atomic force microscopy (AFM) images of one of the resulting electrodes defined and fabricated by EBL process with a gap of 5 μm.

![Figure 25](image)

Figure 25. (a) Optical image of resulting metal electrodes defined using EBL, metal evaporation, and lift-off. (b) Zoomed-in AFM image of the channel gap (~100nm) showing well-defined small size structure using EBL process.
3.3 Fabrication of CNT Electrodes and CNT Thin-Film Transistors

3.3.1 Solution-processed CNTs

We use a high quality aqueous CNT solution for high-performance CNT FETs as well as CNT electrodes fabrication. For electrode material, we used surfactant-free metallic CNT (m-CNT) solutions from Brewer Science. This solution is free from not only surfactant, but also catalytic particles, and bundles. The solution is stable for many months, and contained mostly individual single-walled CNTs. The average diameter of the CNTs in the solution was measured as 1.7 nm and the length of the nanotubes is in the range of from 0.3 to 1.0 μm with an average value of 1.5 μm as determined from atomic force microscopy (AFM) and scanning electron microscopy (SEM) investigations.

3.3.2 Assembly of CNTs via Dielectrophoresis (DEP)

Many advantages, such as easy, simple, low-cost, and CMOS compatible room temperature operation, make DEP assembly more attractive and promising method over the direct growth assembly. Figure 26 shows the schematic diagram of an experimental setup for the DEP process. As illustrated in the figure, we need pre-defined source (S) and drain (D) electrodes. Once the solution dropped between S/D electrodes, AC volatage with 1 MHz frequency is applied for a certain period. For our experiment, we used 5 Vpp with 1 MHz for 30 sec to 1 min as DEP parameters for CNT solution assembly.
Dielectrophoresis (DEP) is the assembly method using the forces and torques exerted by nonuniform electric fields applied on polarizable particles suspended in aqueous media. The DEP force is created by applying nonuniform electric field to the suspended polarizable particles, which induce the surface charges of different polarity of the particle resulting in dipole moment formation caused the particles to experience a net force. [H. A. Pohl; The motion and precipitation of suspensoids in divergent electric fields; J. Appl. Phys. 22, 7869 (1951)] As a result, the particles undergo a translational motion and align along the direction of the electric field lines. It is important to have a nonuniform electric field because no net charge is induced on the particles by uniform electric field resulting in no DEP force generated.

DEP force ($F_{\text{DEP}}$) is given by

$$F_{\text{DEP}} \propto \varepsilon_m \Re\{K_f\} \nabla E_{\text{RMS}}^2$$

$$K_f = (\varepsilon_p^* - \varepsilon_m^*) / \varepsilon_m^*$$

$$\varepsilon_{p,m}^* = \varepsilon_{p,m} - i(\sigma_{p,m}/\omega)$$

Figure 26. Schematic of experimental setup for dielectrophoresis (DEP) assembly of solution-processed CNTs. The signal with 1MHz frequency (typically) was applied from the function generator to source electrodes and monitored in channel 1 (CH1) of oscilloscope, and then drain electrodes is monitored via CH2 in oscilloscope.
where $\varepsilon_p$ and $\varepsilon_m$ are the permittivity of the nanotube and solvent, respectively, $K_f$ is the clausius-Mossotti factor, $\sigma$ is the conductivity, and $\omega = 2\pi f$ is the frequency of the applied AC voltage. The induced dipole moment of the nanotubes interacted with the strong nonuniform electric field causes the nanotubes to move in a translational motion along the electric field gradient. Due to the strong dielectrophoretic force generated, the nanotubes are aligned between source and drain electrodes.

This is shown in Figure 27, where we illustrated the schematic diagram of solution-processed CNT arrays via DEP assembly and the simulation pictures for the electric field formation when AC voltage is applied between source and drain electrodes. [ACS Nano, 5, 1739 (2011)] A simulation of the electric field around the source and drain electrode gap for the parallel electrode patterns is shown in Figure 27(b).[73]

![Figure 27](image)

Figure 27. The schematic diagram of DEP assembly of CNTs. (a) The CNT solution is dropped between source and drain electrode. (b) The simulation pictures showing electric field formation when AC voltage is applied between source and drain electrode. (c) After applying AC voltage, CNTs are aligned along E-field between source and drain electrode. Adapted from ref. [73].

Figure 28 shows the scanning electron microscopy (SEM) image of a representative high density m-CNT aligned array (~30 CNTs/µm) and its electrical transport properties.
Figure 28. m-CNT aligned array (a) SEM images of high density m-CNT aligned array between Pd source and drain electrodes. The current-voltage characteristics are shown in (b) output curve ($I_d$-$V_d$) at zero gate voltage and (c) transfer curve ($I_d$-$V_g$) at $V_d = -0.1$ V. Scale bar indicates 2 μm. Figure (b) and (c) are adapted from ref. [74], with permission of The Royal Society of Chemistry. [Nanoscale 6 4896 (2014)]

Figure 28 (b) shows the output characteristics ($I_d$-$V_d$) of densely aligned CNT array at $V_g = 0$ V. The resistance of this array was found as 550 Ω (two terminal resistance). The transfer curve ($I_d$-$V_g$) characteristics at $V_d = -0.1$ V indicated that the CNT arrays have metallic behavior, and the CNTs used in our electrodes material are dominated by metallic nanotubes.

3.3.3 CNT Electrode Fabrication

Our group have developed a fabrication techniques of solution-processed metallic carbon nanotubes (m-CNTs) aligned array electrodes via dielectrophoresis (DEP) assembly method.[67, 74] Here are the summary of m-CNT aligned array electrode fabrication (See Figure 29).
(a) Assembly of m-CNT solution via DEP method

(b) Characterization of m-CNT array

(c) Open channel window defined by 2nd EBL process

(d) Place the sample under plasma cleaner to etch CNTs in the defined window area

(e) Acetone lift-off and final electrodes fabricated

(f) Characterization of resulting m-CNT electrodes

As described above, the fabrication steps of m-CNT electrodes are simple and easy that can be performed under ambient condition. Figure 29 shows the illustration of fabrication steps of m-CNT aligned array electrodes via DEP assembly. After the assembly of m-CNT aligned arrays, the electrode patterns are defined by EBL followed by a precisely controlled oxidative cutting process of m-CNT arrays through the opened window using plasma etching. The EBL process is similar to section 3.2.2. As ebeam resist, PMMA layer was spin coated on the Si wafer followed by hotplate baking at 180°C for 15 min. The window for CNT electrodes was then defined by opening the PMMA layer via EBL writing. The patterns were further developed using a mixture of MiBK:IPA (1:3) solution. The channel length and width of the electrodes can be customized using DesignCAD software. We fixed the channel geometry (length : width = 2 μm: 25 μm), but varied the density of CNT arrays in the electrodes in order to investigate the density effect in the CNT electrodes. We were also able to tune the density of m-CNT electrodes. The detail fabrication is described in our published work.[68]
Figure 29. Schematic diagram of m-CNT electrode fabrication of m-CNTs electrode. (a) Drop the m-CNT solution between Pd source and drain electrodes. (b) Assembly of m-CNTs aligned array via DEP between Pd electrodes. (c) Opened a window on the m-CNTs array via electron beam lithography, and (d) etch the m-CNTs by oxygen plasma.

As seen in Figure 29 (c) to (d), we used a commercially available plasma etcher (Fischione, 1020 Plasma cleaner) to etch the carbon nanotubes. Our plasma cleaner creates low-energy and high-frequency (13.56 MHz) plasma. Under the non-equilibrium and high-frequency, free electrons are accelerated to high energy states by electromaginetic field generated, and the excited gas atoms are ionized. When the atoms are relaxed to their lower energy state, they release a photon of light associated with plasma. For oxygen plasma, it emits blue glow light. To optimize the cleaning process, we used a mixture gas with 25% oxygen and 75% argon. The carbon-based materials (here, CNT) is chemically comined with diassociated oxygen created by the plasma process. Any organic contaminations reduce to H₂O, CO, and CO₂ which can be evacuated after plasma process. Complete cleaning/etching of CNTs should be done in 2 min or
less. Finally, we kept our device into chloroform for overnight and rinse with acetone-IPA-DIwater and nitrogen blow dry to remove the PMMA layer.

3.3.4 CNT Thin-Film Transistors (CNT-TFTs)

In our study, we used highly enriched s-CNTs (99%) in aqueous solution obtained from Nanointegris made by sorting techniques, such as density gradient ultracentrifugation. The diameter and length of the individual s-CNTs are measured with an average of 1.7 nm and 1.8 μm, determined from SEM image of individual CNTs dispersed on Si/SiO₂ substrate and AFM image of individual CNTs dispersed on mica substrate, respectively as seen in Figure 30. Estimatively 150 nanotubes were investigated.[68]

We started from the original solution with a concentration of 10 μg/mL, and diluted the solution using di-ionized (DI) water to vary the solution densities. For a density of 1 CNT/μm, we diluted the solution up to 2 ng/mL. Then, the solution was dropped between Pd source/drain electrodes, and s-CNTs were assembled via DEP methods with applied 5 Vpp AC voltage at 1MHz for 30 sec.
3.4 Fabrication of Graphene Electrodes

Several methods for production of graphene; from mechanically exfoliated graphene as pristine layer to chemically derived graphene sheets. In this thesis, comparative studies of graphene electrodes will be introduced with the detail of fabrication of each type of graphene electrodes.
3.4.1 Mechanically Exfoliated Graphene as Electrodes

Ultrathin graphene layer was mechanically exfoliated from commercially available bulk graphite (Graphene Supermarket, Natural Kish Graphite Grade 200) using adhesive tape and deposited onto highly doped Si substrate with a thermally grown 250 nm thick SiO\(_2\). The substrate was thoroughly cleaned with acetone, IPA followed by N\(_2\) blow dry. Electron beam lithography (EBL) was performed to pattern the metal contacts on the graphene flakes. First, the sample was spin-coated with MMA/PMMA as a double-layer e-beam resist, baked at 180oC for 15 min separately, and exposed to e-beam, and developed using MIBK:IPA (1:3) developer for 60 sec and IPA for 10 sec. Any graphene film under the exposed window area etched away when the device was kept in O\(_2\) plasma for 2 min. Figure 31 shows the optical images of typical device processed.

Figure 31. Schematic of mechanically exfoliation graphene electrode fabrication. (a) Pristine graphene was mechanically exfoliated onto Si/SiO\(_2\) substrate using conventional tape method. (b) Using EBL, we defined the source and drain contact pads on graphene followed by metal evaporation and lift-off. (c) The device was spin-
coated with PMMA layer. Using 2nd EBL process, the desired geometry of window opened and developed. (d) The device with an opened window was kept in O2 plasma, and the opened area of graphene was etched away. (e) After final lift-off of PMMA removal, final graphene electrode can be fabricated. The gap size can be customized and controlled by fine and precise EBL process.

Once the metal source/drain contact fabricated on the exfoliated graphene flake, 2nd EBL process is needed to define the gap on the flake as seen in Figure 31(b)-(d). The gap is well-defined as illustrated.

3.4.2 CVD-GR as Electrodes

The growth of single-layer by chemical vapor deposition (CVD) was performed by our collaboration, Christian Smith in Prof. Masa Ishigami’s group. The single-layer of large-area CVD grown graphene (CVD-GR) thin film was synthesized using conventional low pressure process on copper. The Single-layer CVD graphene in this study was grown using low pressure chemical vapor deposition (CVD) on copper.[75, 76] Contemporary transfer methods were used to then transfer the graphene film to our target substrate.[77, 78] A sacrificial PMMA supported the graphene film as the copper catalyst was etched using ammonium persulfate solution, before immersion in a subsequent series of modified RCA solutions to remove unwanted contaminants. A final series of DI rinses were performed prior to transfer to the target substrate. The transferred graphene was found to be predominantly single layer by AFM and Raman investigations. The details of resulting single-layer CVD grown graphene sheets on Si/SiO2 substrate and their characterization will be further discussed in Chapter 6.

Figure 32 shows the detail schematic diagram to illustrate a simple and novel fabrication steps of patterning large-area CVD-GR film as electrodes.
Figure 32. Simple patterning technique of large-area CVD-GR electrodes using sacrificial polymer layer. (a) Thin film of CVD grown graphene film was transferred onto Si/SiO$_2$ substrate. (b) After transferring, the film was spin-coated with PMMA layer. This PMMA layer acts as sacrificial polymer layer. (c) Through the metal shadow mask, Al is deposited by thermal deposition. (d) The device was kept in plasma etcher to etch all the area where unprotected by Al metal mask. (e) The sample was immersed into acetone for PMMA removal with Al metal mask.

After transferring of large-area CVD-GR film on to Si/SiO$_2$ substrate, the film was spin-coated with PMMA layer. Our novel technique utilizes a polymethyl methacrylate (PMMA) layer that allows for simple acetone lift-off removal of the etch mask without the use of harmful acid treatments employed by the conventional metal etch mask processes. Additionally, the choice of metal becomes unlimited as compatibility issues with the etchant are alleviated. This new method can be useful because some metals are difficult to remove perfectly from graphene even after strong acid treatment, and this excessive acid can be harmful to the electronic properties of graphene.
3.4.3 RGO as Electrodes

GO powder (Cheap Tubes Inc. 30 mg) is diluted in DI water (30 ml) with sonication followed by 24 hrs magnetic stirring. In GO solution, 200 μl of 5% NH₃ aqueous solution is added to adjust the pH of solution and 30 μl of hydrazine solution is added, and heated at 90°C for 60 min in order to make chemically reduced GO (RGO) solution. Figure 33 illustrates the preparation of RGO from GO powder. The color of solution (brown) changed to black after hydrazine reduction of GO solution indicating chemical properties changes in the solution during the reduction. The carbon $sp^2$ fraction was calculated by taking the ratio of the integrated peak areas corresponding to the C-C peak, to the total area under the C 1s spectrum from the X-ray photoelectron spectroscopy (XPS). The carbon $sp^2$ fraction of 60 min reduction RGO was obtained as 80%.

![Figure 33. Schematic diagram of RGO thin film electrode fabrication. (a) RGO solution was dropped between Pd source and drain electrode and AC voltage was applied with 1MHz frequency. (b) RGO thin film was assembled between metal source/drain electrode via DEP process. (c) After defining the channel window by EBL and keeping the device under O₂ plasma for 2 min followed by acetone lift-off, final RGO electrodes can be fabricated.](image-url)
The assembled RGO thin film between metal electrodes have shown in Figure 33 (c). The film thickness was measured as ~20 nm (details in Chapter 5) regardless of reduction time and different carbon \( sp^2 \) fraction. After the assembly, the sample was placed into O\(_2\) plasma etcher for 2 min, and then defined opened window area by EBL was removed. Final RGO electrodes were shown in Figure 33 (d).

### 3.5 Fabrication of OFETs

After the electrode fabrication, organic field-effect transistors (OFETs) were fabricated using organic semiconductors. Here we used pentacene, a small molecule which can be thermally depositied onto devices.

We used vacuum thermal deposition method to deposit the thin film of small molecule organic semiconductors such as pentacene. Pentacene (Sigma Aldrich, triple sublime >99.995%) is a polycyclic aromatic hydrocarbon consisting of five benzene rings. For the pentacene deposition, we prepared the samples with pre-fabricated electrodes, and then the sample was loaded in the vacuum chamber placed inside N\(_2\) filled glovebox with low oxygen level. The pressure of chamber was maintained as 10\(^6\) Torr, and the deposition rate was kept as low as 0.1-0.2 Å/sec. The deposition rate and the chamber pressure can affect the quality of the pentacene thin film as well as the performance of the pentacene OFETs due to variation of grain size and the morphology. The detail of the thin film characterization and the performance of OFETs will be further discussed in next Chapter.
3.6. Characterization for High-Resolution Imaging and Transport

Measurement Set-up

It is important to electrically characterize the semiconductor device to evaluate their performance by electronic transport properties measurements. There are some performance parameters, such as current on-off ratio (switching behavior), field-effect mobility, transconductance, and on-current which can be extracted and calculated from the current-voltage characteristics of devices.

3.6.1 High-resolution Imaging and Characterization

Investigations of nanomaterials for their advanced characterization are considered as one of the important part in our research, and this can be performed using high resolution imaging techniques including scanning electron microscopy (SEM) and atomic force microscopy (AFM). For imaging, we mainly used low acceleration voltage with Zeiss Ultra 55 SEM and Tapping mode with Veeco Dimension 3100 AFM. For the detail information, we also used Raman and XPS instruments.

3.6.1.1 Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) produces a high resolution image by scanning with a focused electron beam, and the electrons interaced with the sample can generate various signals that can be analyzed to topography and morphology, chemical composition, crystallography and orientation of grains. The SEM imaging technique is a critical methods for the analysis of
nanoscale materials and devices for obtaining their advanced information characterizations and properties. Compared to optical microscopy imaging, SEM has larger depth of field, which allows a large amount of the sample to be in focus at one time and produces an image with high resolution with a high magnification. We used SEM (Zeiss Ultra 55 SEM) instruments for not only imaging but also for e-beam lithography for patterning. For imaging, typically low acceleration voltage (or low beam energies, ~1kV) with InLens secondary electronic detector was used for ultra high resolution without damaging the sample structure and properties. For e-beam lithography (EBL), we use 28kV acceleration voltage.

Electron guns produce a fine, controlled electron beam, and our instrument has a field-emission gun. The field emission gun has a tip of a sharp tungsten needle (radius <0.1 um), and the electric field at the tip is very strong (> $10^7$ V/cm) due to sharp point effect. Electrons are pulled out from the tip by the strong electric field under the ultra high vacuum ($10^{-6}$ Torr) to avoid ion bombardment to the tip from the residual gas.

The vacuum is essential to the electron-optical column and the sample chamber when SEM is operating because if the column is in a gas filled environment, electrons will be scattered by gas molecules which can lead to reduction of the beam intensity and stability. Introduction of other gas molecules from sample or microscope can form compounds and condense on the sample which causes lower the contrast and obscure the detail information in imaging.

For Zeiss Ultra 55 SEM, GEMINI column is used where electrons are emitted, accelerated, bundled, focused, and deflected. As illustrated in Figure 34, the incident beam from the electron gun is introduced to the sample through the column, which contains extractor, anode, objective lens, scanning coils, and detectors. Both photons and electrons are emitted
from the sample, and mostly backscattered electrons and secondary electrons are used for imaging the sample information.

Figure 34. Once the electron beam is produced from the electron gun, the beam traveled through electromagnetic fields and lenses and focused to the sample. Detectors collect the emitted electrons such as X-rays, backscattered electrons, and secondary electrons.

3.6.1.2 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a high-resolution imaging methods of scanning probe microscopy (SPM) with a resolution of nanometer (nm), which is 1000 times greater than typical optical diffraction limit. Tapping mode AFM can be advantageous for lateral high-resolution imaging, measuring, and manipulating nanoscale materials. The imaging process can be performed under ambient condition without destroying the samples. The movement of the tip is controlled by scanner (x,y,z) made from a piezoelectric material. As seen in Figure 35, the cantilever is oscillating in free air with its resonance frequency, and a piezo stack excites the cantilever to move up and down. As the cantilever moves vertically, the reflected laser beam
(return signal) deflects over photodiode detector, generating a sinusoidal electronic signal. The reflected laser beam reveals information about the vertical height of the sample surface and other characteristics of the materials including elasticity, magnetism, and presence of electrical forces. The AFM probes are commonly made of Si, and the radius varied from 5 to 20 nm. Our probe model was purchased from App Nano (ACT Part # ACT-200). The material of tip is Si (n-type, 0.01-0.025 ohm/cm), and the tip radius is less than 10nm (Cantilever L:125um, W: 35um, T: 4.5um), with the frequency of 200-400 kHz and the spring constant of 25-75 N/m.

Figure 35. Block diagram of Tapping mode AFM using beam deflection detection. The cantilever is oscillated at or slightly below its resonance frequency, and the tip lightly taps the sample surface during the scanning. The feedback loop maintains the constant oscillation amplitude by constant RMS of the oscillation signal acquired by the photodiode detector. The vertical position of the scanner is controlled by setpointing amplitude, and the information is transferred to topographic image of the sample surface.
From the Tappin mode AFM, we can acquire height (or topography), amplitude, and phase image. Topography images are common information acquired from AFM, which presented a map of different colored pixels with a colored scale bar related to height. The height profile can be very useful to estimate a diameter, length, and thickness of the nanomaterial precisely. The amplitude (deflection) image is a map of the slope of the sample, and they often display the shape of the sample more easily and realistic. Phase imaging refers to phase shift signal, and the phase shift can be thought of as ‘delay’ in the oscillation of the cantilever. Phase image is a measure of the energy dissipation between tip and the sample, which depends on a number of factors, including such features as viscoelasticity or adhesion. In our experiment, we use Veeco Dimension 3100 AFM with Tapping mode, and the detailed AFM images acquired will be discussed in next Chapters.

3.6.2 Electronic Transport Measurements

The transport measurements of our devices were performed at variable temperature under vacuum or in the air. Some of the organic devices were measured in the glovebox where the oxygen level is below 0.5 ppm. For the general transport measurement set up, we used current preamplifier (DL instruments Model 1211), Data acquisition (DAQ) boards (National Instruments, BNC 2090), and source (voltage) meter (Keithely 2400 or 6517) interfaced with LabView program. The current preamplifier gives a precision, high performance electronic measurement with a capability of measuring sub-pA signal. The instruments has high speed and low noise. All the connections are composed of BNC connectors. BNC-2090 simplifies the
connection of analog signals and digital signals to the DAQ board, which has a GPIB connection to be interfaced with LabVIEW. As voltage supplier, Keithely 2400 or 6517 are used (upto 200 V), and 6517A can measure very low current due to high resistance. All the sourcemeter provide precise voltage with low noise and high repeatability.

![Circuit diagram of electrical measurement set up for field-effect transistor](image)

Figure 36. Circuit diagram of electrical measurement set up for field-effect transistor with a configuration of top contact source and drain electrodes and bottom contact gate.

As illustrated in Figure 36, once the voltage is applied to source electrode, the output current can be measured through ammeter connected to drain electrode. The current level can be manipulated by applied gate voltage from gate electrode. The figure shows the top contact electrodes and bottom contact gate configuration.

For the measurement of organic devices including organic field-effect transistors (OFETs), we used Hewlett-Packard (HP) 4145B semiconductor parametric analyzer interfaced with LabView program. This instrument is connected to a probe station inside an enclosed glove box system with extremely low oxygen level (<0.5 ppm) as shown in Figure 37.
For temperature dependent studies, we used cryostat (Figure 38 (a)), and temperature heater (Lakeshore temperature controller) for controlling the temperature range under vacuum. The sample backgates were connected to metal surface at the bottom of the chip carrier (Leadless chip carrier (LCC02834), Spectrum Semiconductor), and then the samples were bonded into chip carrier (Figure 38 (c)) using silver wire to apply voltage and measure the output current. The samples finally loaded at the end of the cryogenic rod as indicated in Figure 38 (b). We used liquid nitrogen to go up to 77K. The cryostat was loaded into 4L N\textsubscript{2} dewar. The transport measurements were carried out using DL instruments 1211 current preamplifier and Keithley 2400 sourcemeter interfaced with LabVIEW program. For careful measurements at each temperature, we waited at least 15-20 min between successive measurements as well as stabilized temperature before taking the data.
Figure 38. (a) The part of cryostat that used for low-temperature measurement. Red arrow indicates that the position where sample goes in. (b) Wire bonding machine. (c) The wire-bonded sample with chip carrier. This goes into the place where red arrow indicates in (a).
CHAPTER 4 : HIGH PERFORMANCE SOLUTION-PROCESSED SEMICONDUCTING ENRICHED CARBON NANOTUBES THIN FILM TRANSISTORS WITH METALLIC CNT ELECTRODES†

4.1 Introduction

Owing to exceptional electronic and mechanical properties of carbon nanotubes (CNTs), thin film transistors (TFTs) fabricated with CNTs have attracted a great deal of attention as promising components for the next-generation flexible and transparent electronic devices, sensors and high frequency devices.[13, 15, 16, 18, 19, 41, 43, 49, 79-81] The TFTs fabricated using a network of CNTs can be advantageous compared to individual CNT devices as they provide more device to device homogeneity and cover large areas. Another advantage is that in the CNT TFTs a large number of nanotubes contribute in the charge transport simultaneously, which increases the output current significantly.

Several recent studies show that the performance of the CNT TFTs depends on channel length of the TFTs, and content of semiconducting versus metallic CNTs.[14, 19, 40, 43, 44, 48, 80-84] The CNT TFTs have been fabricated using mixed CNTs either in a random network or in an aligned array.[19, 40, 81, 82, 85-87] The mixed CNTs are grown by chemical vapor deposition (CVD) method, and the CVD grown mixed CNTs contain generally a large portion of metallic CNTs (m-CNTs). This can be a disadvantage as the metallic nanotube pathways tend to dominate the transport in the TFTs, which results in a lower current on-off ratio. In order to increase the current on-off ratio, selective removal of metallic CNTs via electrical breakdown

† The portions and contents of this chapter have published in a peer-reviewed journal: *Nanoscale*, 6, 4896 (2014).
has been demonstrated,[40, 86, 87] however, this method has detrimental effects on the remaining nanotubes in the networks.[87, 88] Therefore, it is important to use all semiconducting nanotubes (s-CNTs) for fabricating CNT TFTs.

In this Chapter, we will show our recent published work,[74] high-performance solution-processed short-channel carbon nanotube (CNT) thin film transistors (TFTs) fabricated using densely aligned arrays of metallic CNTs (m-CNTs) as source/drain electrodes, and aligned arrays of semiconducting enriched (99%) CNTs (s-CNTs) as channel material. The electrical transport measurement was performed at room temperature, showing that the s-CNT TFTs using m-CNT electrodes with a 2 μm channel length performed superior to those using conventional metal (Pd) electrodes. The s-CNT TFTs with m-CNT electrodes exhibited a maximum (average) on-conductance of 36.5 µS (19.2 µS), transconductance of 2.6 µS (1.2 µS), mobility of 51 cm²/Vs (25 cm²/Vs), and current on-off ratio of 1.1×10⁶ (2.5×10⁵). These values are almost an order of magnitude higher than that of Pd electrodes (control devices) with the same channel length and s-CNT linear density. The low temperature charge transport measurements suggest that these improved performances may be due to a lower Schottky barrier of m-CNT/s-CNT devices compared to Pd/s-CNT devices. We attributed the reduced Schottky barrier to unique geometry of our devices. Our results suggested that the performance of s-CNT TFTs can be significantly enhanced by using m-CNT as an electrode.
4.2 Current Status and Challenges in s-CNT Thin Film Transistors (s-CNT-TFTs)

Studies have shown that solution based sorting techniques, such as density gradient ultracentrifugation,[20] can provide highly enriched s-CNTs in aqueous solution. A few studies reported the fabrication of TFTs using highly pure s-CNTs either in a random networks or in an aligned arrays.[14, 43, 44, 48, 83, 84] In these studies, metal electrodes (Au, Pd) were used to contact the s-CNTs in the TFTs. It has been found that for the TFTs fabricated with highly enriched (>98% purity) s-CNT have showed better device performance (mainly mobility, and current on-off ratio) when the channel length of the transistors was much larger than the average length of the nanotubes.[14, 48, 49] However, the performance of these highly enriched (>98%) s-CNT TFTs was found to decrease with a decreasing channel length as shown in Figure 39.[14, 44, 48, 49]

As seen in the Figure 39, the decrease of current on/off ratio with decreasing channel length can be explained by presence of small fraction m-CNTs (<2%) in the solution. The probability that m-CNTs form a percolation current path is increased when the channel length is decreased which result in reduced current on/off ratio less than 100.[44, 83] Therefore, the decrease of current on-off ratio with decreasing channel length can be explained by the presence of m-CNTs. However, it is still not clear for the reason why the mobility decreases with decreasing the channel length as seen Figure 39 (b) and (c). This cannot be explained by presence of m-CNTs because it has been found that the presence of m-CNTs in fact increases the mobility of the devices.
Figure 39. Channel length impact on device performance of highly enriched s-CNT TFTs from different studies. (a) On state current as a function of current on/off ratio for different channel length devices from 0.5 μm to 10 μm. The current on/off ratio decreased with decreasing channel length. Adapted from ref. [44] (b) Mobility vs. Channel length for L=20μm to 100μm. The mobility decreased with decreasing channel length. Adapted from ref. [14] (c) Mobility with different channel length devices. Red plot shows the highly enriched s-CNT TFTs (98%) and showed decreased mobility with decreasing channel length. Adapted from ref. [48]. (d) Red plot (98% s-CNT) showed decreased current on/off ratio with decreasing channel length. Adapted from ref. [48].

For example, C. Wang et al have shown that mobility of the 95% pure s-CNT devices is higher than the mobility of 98% pure s-CNT devices.[48] In addition, the mobility of the mixed CNTs device (33% metallic) decreases when m-CNTs are removed by electrical breakdown. [40,
These observations clearly indicated that the presence of m-CNTs in TFTs can increase the mobility. Thus, one could expect that the mobility of the s-CNT devices should be increased with decreasing channel length if the small fraction of m-CNTs make a percolating path between the electrodes. However, the opposite scenario has been observed in reality. The decrease of mobility with decreasing channel length was still observed in the s-CNT devices where the on-off ratio was greater than 100 (meaning no m-CNT percolation).[48]

The Burke group speculated that the decrease of mobility with decreasing the channel length may be due to the effect of contact.[14] In the long channel s-CNT TFTs, the contact resistance may be negligible in comparison to the channel resistance and hence the effect of contact resistance on the performance of long channel devices is small. In contrast, in the short channel devices, the contact resistance can become a significant fraction of the total resistance of the devices due to the reduction in channel resistance, thereby resulting in a reduction of mobility. Therefore, the effect of contact is significant in short channel devices where the typical mobility is in range of 2-15 cm²/Vs and a current on-off ratio is greater than 100.[44, 48, 83, 89]

It should be noted that short channel s-CNT TFTs are important for high frequency applications as the on-current is increased with decreasing the channel length and the cutoff frequency is inversely proportional to the square of the channel length.[14, 49] Thus, enhancing the performance of short channel TFTs are also of great significance for realizing the overarching goals of CNT based TFTs.

One possible way to improve the performance of short channel solution processed CNT TFTs could be to use aligned m-CNTs as electrode material and aligned s-CNTs as channel material where both m-CNTs and s-CNTs are longitudinal to each other. The m-CNTs with
open-ended and parallel tips can enhance charge injection at m-CNT/s-CNTs interface due to electric field enhancement at these tips.[39, 90] In addition, longitudinal arrangement can also result in finite overlap of some m-CNT/s-CNT which will also enhance charge injection. Because of the higher charge injection from the m-CNTs, we can expect that the interfacial barrier at the m-CNT/s-CNT interface will be reduced which will improve the performance of the CNT TFTs.

Based on this motivation, here we introduce such a longitudinal arrangement between m-CNTs electrode and high enriched (99%) s-CNT channel, and demonstrate that high performance short channel s-CNT TFTs can be realized from such an arrangement. We will discuss our detailed fabrication and device characterization at both room and low temperature with electronic transport measurement and barrier height estimation.

4.3 Fabrication of Aligned Array Highly Enriched s-CNT TFTs using Aligned Array m-CNT electrodes

High-quality, stable, and surfactant-free m-CNT aqueous solution was used to fabricate the CNT source and drain electrodes. As seen in Figure 40 (a), A small amount of m-CNT solution (3 µl) was dropped between Pd source/drain electrodes and an AC voltage of 5V_{pp} with a frequency of 1MHz was applied for 30 sec. The AC voltage creates a time averaged DEP force and aligns the m-CNTs in the direction of the electric field between the Pd patterns. After the m-CNT assembly, a layer of PMMA was spin-coated at 4000 rpm for 60 sec, then baked at 180°C for 15 min on a hot plate. Then, the m-CNT source and drain electrodes (with a channel length of
2 µm and a width 25 µm) were defined using EBL followed by precisely cutting the m-CNTs by oxygen (O\textsubscript{2}) plasma etching. Finally, the chip containing the CNT electrodes was kept in chloroform for 12 hrs to remove the remaining PMMA. The devices were rinsed by acetone, IPA, and DI water and blown with nitrogen (N\textsubscript{2}) gas. More details of the m-CNT assembly and m-CNT electrode fabrication can be found in our previous published works.[67-71, 73, 91]

After the fabrication of m-CNT electrodes, we assembled highly enriched (99%) s-CNT arrays in the channel with m-CNT electrodes (m-CNT/s-CNT). To assemble the tunable density of s-CNTs array using DEP, the original s-CNT solution was diluted to 2 ng/ml to obtain 1 s-CNT/µm. The DEP method was used again to assemble the s-CNTs in between the m-CNT electrodes by applying an AC voltage of 5 V\textsubscript{pp} at 1 MHz for 30 sec. We also fabricated control devices using bare Pd electrodes for s-CNT devices (Pd/s-CNT) via DEP assembly of highly enriched (99%) s-CNTs following our previously reported technique. The Pd electrodes deposited on Si/SiO\textsubscript{2} substrate had a channel length of 2 µm and width of 25 µm, similar to the dimension of the m-CNT electrodes. The parameters for the DEP assembly of the s-CNTs using Pd electrodes were the same as what has been used for m-CNTs electrodes. Both the m-CNT contacted and Pd contacted s-CNT devices were annealed at 200°C for one hour in an argon/hydrogen (Ar/H\textsubscript{2}) environment.

4.4 Characterization of s-CNT TFTs with m-CNT electrodes

The SEM and AFM images of the devices were taken by the Zeiss Ultra-55 SEM and the Dimension 3100 AFM (Veeco).
Figure 40. (a) Schematic diagram of fabrication steps for s-CNT TFTs with CNT electrodes. (i) DEP assembly of CNTs. (ii) Aligned CNT arrays via DEP between Palladium (Pd) patterns. (iii) Opening of a window on the CNT array via EBL and plasma etching. (iv) DEP assembly of s-CNTs in between CNT electrodes. (v) Schematic of s-CNT TFT with CNT electrodes. SEM images of (b) the CNT aligned array and (c) the CNT electrode. The channel length of the CNT electrode is 2 μm, and (d) the AFM image of a part of the CNT electrode shows open ended and parallel tips. The scale bar indicates 1 μm.

A schematic diagram of the fabrication steps of the s-CNT aligned array TFTs with aligned array m-CNT electrodes is shown in Figure 40(a). Figure 40 (b) shows a SEM image of a part of the CNT aligned array. The linear density of this array ~ 30 m-CNT/μm and a resistance of 550 Ω
(Figure 40, See section 3.3.2) which corresponds to a sheet resistance of 2.75 kΩ/sq. Although we used mixed CNTs for this assembly, it has been shown that the DEP process favors m-CNTs over s-CNTs.[92] The densely aligned m-CNT arrays do not show any gate-voltage dependence, further implying the metallic behavior of the CNTs arrays. The low sheet resistance and absence of gate dependence of the arrays confirm the metallic behavior and make them ideal material for electrode fabrication.

After the m-CNT assembly, we opened an window of channel length of 2 µm and width of 25 µm on the m-CNTs aligned arrays via electron beam lithography (EBL) and etched away the exposed area using oxygen plasma.[67-69] Figure 40 (c) shows the SEM image and Figure 40 (d) shows the AFM image of a part of a m-CNT electrode. The AFM image clearly shows that the m-CNTs in the electrode have open-ended tips and they are parallel to each other.

![AFM image of m-CNT electrode](image)

Figure 41. SEM images of the aligned array of s-CNTs with a linear density of 1 s-CNT per µm between m-CNT electrodes with a channel length of 2 µm. (b) High magnification SEM image shows a longitudinal arrangement between the s-CNT and m-CNT. The scale bar indicates 1 µm in (a), and 300 nm in (b).
The s-CNT array was then assembled via DEP process between the fabricated m-CNT electrodes. Figure 41 (a) shows an SEM image of a typical m-CNT/s-CNT device with a linear density of ~1 s-CNT/µm in the channel. Figure 41 (b) shows a high magnification SEM image of the interface between m-CNT and s-CNT. This image demonstrates unique longitudinal arrangement between the m-CNT electrodes and the s-CNTs in the channel, with a possible end-contact configuration where the m-CNTs and s-CNTs are connected in a head-to-head arrangement without any gap. All the devices reported in this study have the same linear density of s-CNT. For comparison, we also fabricated control Pd contacted s-CNT devices of the same density, channel length and width as shown in Figure 42.

Figure 42. SEM image of s-CNT TFT devices with Pd electrodes (control device). The density of s-CNT is ~ 1s-CNT/µm, and the scale bar indicates 1µm.
The electronic transport measurements of s-CNT TFTs using m-CNT electrodes at room temperatures were performed using DL instruments 1211 current preamplifier and Keithley 2400 source meter interfaced with LabView program. Figure 43 (a) and 26 (b) show room temperature drain-current ($I_d$) versus bias-voltage ($V_d$) curves (output characteristics) at different gate-voltages ($V_g$) for representative m-CNT/s-CNT and Pd/s-CNT devices, respectively. We used highly doped silicon as a back-gate and SiO$_2$ as dielectric. Both devices show p-channel transistor behavior along with good current modulation with the gate voltage. The linear $I_d$-$V_d$ curves at a low $V_d$ indicate that both Pd and m-CNT electrodes form a good interfacial contact with s-CNTs. However, the maximum drain-current (at $V_g = -30$ V and $V_d = -1$ V) for Pd/s-CNT devices is only 0.6 µA, whereas it is 12 µA for the m-CNT/s-CNT devices, a value more than an order of magnitude higher.
Figure 43. Output characteristics (Id-Vd) for (a) m-CNT/s-CNT and (b) Pd/s-CNT devices at Vg = -30 to -15 V in steps of -1 V (top to bottom). Compared to the Pd/s-CNT device, the m-CNT/s-CNT device shows higher current driving ability. Transfer characteristics (Id-Vg) in the semi-log scale for (c) m-CNT/s-CNT and (d) Pd/s-CNT devices at Vd = -1 V. The channel length and width of the both m-CNT/s-WNT and Pd/s-CNT devices are 2 um and 25 um, respectively.

Figure 43 (c) and (d) show I_d-V_g curves (transfer characteristics) at V_d = -1 V for the devices shown in Figure 43 (a) and (b), respectively. The figure of merits for the device performance such as on-conductance (G_on=I_{on}/V_d), current on-off ratio (I_{on}/I_{off}), transconductance (g_m = dI_d/dV_g), and linear mobility (μ) were extracted from the I_d-V_g curves. We calculated linear mobility (μ) using the standard formula[83]:

\[ \mu = (L/WC_iV_d)(g_m) \]

where C_i is the specific capacitance per unit area of aligned array,
\[ C_i = D/[C_Q^{-1} + (1/2\pi\varepsilon_0\varepsilon)\ln[\sinh(2\pi\varepsilon_0 D / \pi D r)]] \]

\( C_Q \) is the quantum capacitance of CNT (4 \times 10^{-10} \text{ F/m}), \( t_{\text{ox}} \) is the oxide thickness (250 nm), \( \varepsilon \) is the dielectric constant of SiO\(_2\) (3.9), \( \varepsilon_0 \) is the permittivity of vacuum, \( r \) is the average radius of the s-CNTs, and \( D \) is the linear density of the s-CNTs in the channel. The \( G_{\text{on}} \) (at \( V_g = -30 \text{ V} \)), \( I_{\text{on}}/I_{\text{off}} \), \( g_m \) and \( \mu \) for the Pd/s-CNT device are 0.9 \( \mu \text{S} \), 1.1 \times 10^3, 0.4 \( \mu \text{S} \) and 5 cm\(^2\)/Vs, respectively, while for the m-CNT/s-CNT device these values are 15.7 \( \mu \text{S} \), 2.5 \times 10^4, 1.5 \( \mu \text{S} \) and 51 cm\(^2\)/Vs respectively. We would like to point out that these values for the m-CNT/s-CNT device are again approximately an order of magnitude higher than that of the control Pd/s-CNT device.

![Graphs showing comparison between m-CNT/s-CNT and Pd/s-CNT devices](image)

Figure 44. Statistics for 13 m-CNT/s-CNT devices (red) and 13 Pd/s-CNT devices (blue). The channel length and width for all devices are 2 um and 25 um, respectively. (a) On-conductance, (v) transconductance, (c) device mobility, and (d) current on-off ratio. The m-CNT/s-CNT devices show significantly better performance than that of the Pd/s-CNT devices.
We characterized a total of 26 devices (13 m-CNT/s-CNT and 13 Pd/s-CNT) with the same linear density of 1 s-CNT/µm in the channel. The summary of the device performance are shown in the box plots in Figure 44 (also see Table 1).

Table 1. Comparison of a few recent solution-processed short-channel s-CNT devices

<table>
<thead>
<tr>
<th>Type of s-CNT (% purity)</th>
<th>Electrode</th>
<th>Channel length (µm)</th>
<th>Channel width (µm)</th>
<th>Mobility (cm²/Vs)</th>
<th>On-off ratio</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aligned (99%)</td>
<td>Ti/Pd/Au</td>
<td>2</td>
<td>10</td>
<td>10</td>
<td>10⁹</td>
<td>ACS Nano, 2, 2445 (2008)</td>
</tr>
<tr>
<td>Random (98%)</td>
<td>Ti/Pd</td>
<td>4</td>
<td>100</td>
<td>17</td>
<td>10⁴</td>
<td>ACS Nano, 4, 7123 (2010)</td>
</tr>
<tr>
<td>Random (99%)</td>
<td>Pd/Au</td>
<td>2</td>
<td>200</td>
<td>8</td>
<td>-</td>
<td>Adv. Mater., 23, 94 (2011)</td>
</tr>
<tr>
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<td>Cr/Au</td>
<td>5</td>
<td>60</td>
<td>2</td>
<td>10⁵</td>
<td>Appl. Phys. Lett. 92, 243112 (2008)</td>
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<tr>
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<td>Cr/Pd</td>
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<td>25</td>
<td>7.8</td>
<td>1.1×10⁴</td>
<td>This work</td>
</tr>
<tr>
<td>Aligned (99%)</td>
<td>m-CNT</td>
<td>2</td>
<td>25</td>
<td>51</td>
<td>1.1×10⁶</td>
<td>This work</td>
</tr>
</tbody>
</table>

*In this table the devices which have current on-off ratio less than 100 (percolating transport through m-CNT) are not included.

* Mobility of 8 cm²/Vs for L=2 µm is extrapolated from the mobility versus channel length data.

* Percentage of purity is not given.

Figure 44(a) shows that the maximum on-conductance for the Pd/s-CNT devices is 10.1 µS with an average of 2.4 µS. In contrast, the maximum and average on-conductance values for the m-CNT/s-CNT devices are 36.5 µS and 19.2 µS respectively, which are significantly higher than those of the Pd/s-CNT devices. Similarly, the maximum and average transconductance of the m-CNT/s-CNT devices are 2.6 and 1.2 µS, respectively, which are almost one order of magnitude higher than those of the Pd/s-CNT devices, 0.32 and 0.11 µS, respectively, (Figure 44 b). Figure 44 (c) shows that the maximum mobility of the m-CNT/s-CNT devices is 51 cm²/Vs with an average of 25 cm²/Vs, whereas the maximum mobility of the Pd/s-CNT devices is only 7.8 cm²/Vs with an average of 4 cm²/Vs. Notably, the on-off ratio of the m-CNT/s-CNT devices exceeds that of the Pd/s-CNT devices by two orders of magnitudes. The maximum (average) current on-off ratio of the m-CNT/s-CNT devices is 1.1×10⁶ (2.5×10⁵), whereas it is 1.1×10⁴
(2.8×10^3) for the Pd/s-CNT devices (Figure 44(d)). The average current on-off ratio of m-CNT/s-CNT devices is 100 times higher than Pd/s-CNT devices, while the average on-current of m-CNT/s-CNT devices is 10 times higher than Pd/s-CNT devices. The additional improvement in the current on-off ratio is from the decrement of average off-current by one order magnitude in the m-CNT contacted devices compared to Pd-contacted devices. We also compared the performance of our devices with a few recent solution processed short channel (channel length similar to our devices) s-CNT TFT (>98% purity, aligned or random array) devices, as shown in Table 1. From this table we can see that the mobility and current on-off ratio of our Pd/s-CNT TFTs (control devices) are in agreement with what have been reported in the literature for metal contacted s-CNT TFTs. In contrast, the performance of our m-CNT/s-CNT devices are significantly better than that of our control Pd/s-CNT devices as well as other metal contacted s-CNT devices.

In order to practical applicable in high speed digital electronic devices, transistors should have both a higher mobility and a higher current on-off ratio.[14, 49] In Figure 45, we plot the current on-off ratio against mobility for all devices. The star symbols represent the m-CNT contacted devices while the dots represent Pd contacted devices. As shown in Figure 45, the m-CNT contacted devices have shown consistently higher mobility along with a higher on-off ratio compared to that of the Pd contacted devices. Achieving such a high mobility along with a high current on-off ratio using an m-CNT electrode is a very significant for CNT based electronics devices. The improved performance of a transistor is attributed generally to several factors including the reduction of traps and impurities in the channel material, improved gate dielectric and improved charge injection due to a lower interface barrier between the metal and
semiconductor. Since we used identical channel materials, substrates and gate dielectrics in this work, we believe that the improvement of our m-CNT/s-CNT devices is due to better m-CNT/s-CNT interface compared to the Pd/s-CNT interface.

Figure 45. Current on-off ratio versus mobility of all the m-CNT/s-CNT and Pd/s-CNT devices. Both the mobility and current on-off ratio of the m-CNT/s-CNT devices are higher than that of Pd/s-CNT devices.

4.6 Temperature Dependent Transport Investigations of s-CNT TFTs

To clearly understand the reason for improved performance of s-CNT devices using m-CNT electrodes, we calculated the interfacial barriers (Schottky barrier) of our devices from the temperature dependent electronic transport measurements. To perform the temperature dependent transport measurements, the devices were bonded in chip carriers and loaded into a
cryostat. The temperature was then controlled by the Lakeshore temperature controller. Before taking any data, we waited 10 minutes for the temperature to stabilize and we waited 15 minutes between successive measurements.

Figure 46. Temperature dependent (77-285 K) current-voltage characteristics at $V_g=0$ V of (a) the m-CNT/s-CNT device and (b) the Pd/s-CNT device. The Arrhenius plot of the current at different $V_d$ in the range of -0.1 V to -1 V for (c) the m-CNT/s-CNT device and (d) the Pd/s-CNT device. The bias voltage dependent Schottky barriers are calculated from the slopes of the $\ln I_d$ versus $1000/T$ curves at a higher temperature range for different bias voltages.

The $I_d-V_d$ curves at $V_g = 0$ V of the representative m-CNT/s-CNT and Pd/s-CNT devices in the temperature range of 77 K to 285 K are shown in Figure 46 (a) and (b), respectively. These figures show that the drain-currents of both devices decrease with decreasing temperature,
indicating a thermally activated transport. From this data, we calculated the Schottky barrier following the analysis of Martel et. al[93] and others[94-96] by modeling the current using the Arrhenius equation $I_d \sim \exp(-\Phi/kT)$, where $k$ is the Boltzmann constant, $T$ is the temperature and $\Phi$ is the Schottky barrier for the s-CNT devices. It was also noted by Martel et. al. and others that $\Phi$ depends on the bias voltage and that the Schottky barrier at zero bias ($\Phi_b$) is the “true” Schottky barrier, which should be calculated by plotting $\Phi(V_d)$ (voltage-dependent Schottky barrier ) as function of the square root of bias voltage ($V_d^{1/2}$) and then extrapolating the linear fit to $V_d^{1/2} = 0V$. [93, 97]

Figure 46 (c) and (d) show an Arrhenius plot of the current ($\ln I_d$ versus $1000/T$) with $V_d$ ranging from -0.1 to -1 V in intervals of -0.1V for the m-CNT/s-CNT and Pd/s-CNT devices, respectively. The observed linear relationship between $\ln I_d$ and $1/T$ at higher temperature range confirms that the transport mechanism in our devices is mainly due to transport of thermally activated charge carriers. The deviation from linear behavior to saturation is due to tunneling. [93] From the slopes of the $\ln I_d$ versus $1000/T$ curves at higher temperature range, we calculated $\Phi(V_d)$ for both the m-CNT/s-CNT and Pd/s-CNT devices at different $V_d$.

In Figure 47, we plotted $\Phi(V_d)$ as a function of the square root of bias voltage ($V_d^{1/2}$) and determined the Schottky barrier at zero bias ($\Phi_b$) from the intercept of the linear fit of the data. We obtained a value of 45 meV for $\Phi_b$ for the m-CNT/s-CNT device and a value of 139 meV for the Pd/s-CNT device. Interestingly, the Schottky barrier of our aligned arrays Pd/s-CNT devices (average diameter = 1.7 nm) is similar to the Schottky barrier measured for the Pd contacted individual s-CNT with diameter of 1.7 nm. [21]
We have analyzed 3 m-CNT/s-CNT and 3 Pd/s-CNT devices at low temperature. The average $\Phi_b$ of the m-CNT/s-CNT devices is 60 meV, which is significantly lower than the average $\Phi_b$ for the Pd/s-CNT devices (161 meV). The possible reason for a small Schottky barrier of our m-CNT/s-CNT devices can be explained by considering the unique contact configuration between our m-CNTs and s-CNTs at the interfaces. In a previous study, a large Schottky barrier was reported between m-CNT and s-CNT.[98] However, it should be noted that the structure was a cross junction where the CNTs were orthogonal to each other and the contact between them was a point contact. On the other hand, the contact configurations of our m-CNT/s-CNTs devices devices are completely different. In our devices the aligned arrays of s-CNTs are connected between aligned arrays of m-CNTs. This can result in two possible contact
configurations: (i) end-contact or (ii) longitudinal side-contact (Figure 48). It has been reported that CNTs have field emission properties due to its one-dimensional character and that the field emission can occur from both the sidewall and tips of the nanotubes.[39, 90, 99-101]

![Diagram of CNT configurations](image)

Figure 48. (a) Schematic diagram of s-CNT aligned array assembled between m-CNT aligned array electrodes. Two contact configurations are highlighted: end-contact and side-contact. (b) Schematic of the end-contact configuration between the m-CNT and the s-CNT. In the end-contact, the tip of s-CNT is connected directly to the tip of the m-CNT and improved charge injection can occur due to an electric field enhancement at the m-CNT tips. (c) Schematic of the side-contact configuration. Improved charge injection can occur from the side-walls of the m-CNT due to finite overlap with the s-CNT.

It is believed that the field emission properties can enhance charge injection when m-CNTs are used as an electrode material.[64, 67, 69] In the end-contact configuration, the tips of s-CNTs are connected directly to the tips of the m-CNTs (head-to-head connection without any gap) and improved charge injection can occur from the m-CNTs tips due to electric field enhancement at the tips (Figure 48 (b)).[64, 69] This is because when a voltage is applied to m-CNT electrodes, a large local field is generated at the nanotube apex due to their one-
dimensional structure which increases charge injection.\cite{64, 69} Moreover, since the m-CNTs electrodes are fabricated by cutting the nanotube arrays, the tips of m-CNTs are open-ended (Figure 40d) and such tips may provide further electric field enhancement and the charge injection.\cite{39, 69} In the side-contact configuration, the m-CNTs and s-CNTs are connected in the longitudinal direction (side walls are parallel) and enhanced charge injection can be occurred from the side-wall of the m-CNTs (Figure 48 (c)) due to a finite overlap between the tubes, as well as from the tip of the m-CNTs. In contrast, Pd does not have any field emission properties and hence no electric field enhancement can be expected from Pd electrode, despite there is a finite overlap between Pd and s-CNT. Further theoretical and experimental studies will be needed to confirm our hypothesis.

4.7 Conclusion

In summary, we have shown that the performance of the short channel semiconducting enriched aligned array carbon nanotube field effect transistors can be improved significantly by employing metallic carbon nanotube as the electrodes. It has been found that the on-conductance, transconductance, mobility and current on-off ratio of the devices with metallic carbon nanotube electrodes are up to an order of magnitude higher than those of devices fabricated using metal electrodes. From the low temperature electronic transport measurements of our devices, we demonstrated that the improved device performances are due to the lower Schottky barrier of the s-CNT devices with metallic carbon nanotube electrodes compared to that in the devices with metal electrodes. We speculated that this lower Schottky barrier results from the unique one
dimensional contact geometry at the interface. This work suggests that, in addition to using semiconducting enriched carbon nanotubes, using metallic carbon nanotube as an electrode can significantly enhance the performance of CNT TFTs.
CHAPTER 5. TUNABLE DENSITY EFFECT OF SEMICONDUCTING CARBON NANTOBUES ARRAY IN THE THIN FILM TRANSISTORS USING METALLIC CARBON NANTOBUE ELECTRODES

5.1 Introduction

In the previous chapter, we demonstrated that the device performance of solution-processed highly enriched s-CNT TFTs (density of 1 s-CNT/μm) can be improved by using aligned array m-CNTs as electrodes.[74] The enhanced performance was attributed to the unique interface of m-CNTs with open-ended and parallel tips for better charge injection at m-CNT/s-CNTs interface due to electric field enhancement at these tips in addition to finite overlap of some m-CNT/s-CNT which will also enhance charge injection. From the temperature dependent investigation, we found that the interfacial barrier at m-CNT/s-CNT interface is reduced due to a favorable interaction and higher charge injection at m-CNT/s-CNT interface.

It is generally believed that the device performance can be affected by the density of nanotubes in the channel, and the device performance can be possibly further improved when the density of nanotube in the channel is increased and thus optimized.[14, 49] Figure 49 shows the increased device mobility as the density of nanotubes in the channel increased. The study found that the increased nanotubes density will increase the chance of having metallic nanotubes in the channel, which increase the on-current as well as off-current.[14] In fact, the authors found the correlation between mobility increase with current on-off ratio decrease as the nanotube density increased.
Figure 49. The impact of nanotube density in terms of device performance. (a) The plot of mobility as a function of nanotube density in the channel. As the tube density increased, the mobility increased. For the devices with smaller channel length (L=20μm), the mobility is smaller than the larger channel length (L=100μm), which indicates the impact of the channel length as well as density of nanotubes. (b) The correlation found between mobility and current on-off ratio. As the mobility is higher, the current on-off ratio is lower which is the indication of the presence of metallic nanotube in the channel. Adapted from ref. [14].

Therefore, it is a great importance to explore the device performance of s-CNT TFTs by varying the density of s-CNTs in the channel as well as by improving the contact at electrode/semiconductor interface using m-CNT electrodes.

In this chapter, we expanded our previous work[74] in understanding the effect of tunable density of s-CNTs using m-CNT electrodes on the transport properties of TFTs. We also compared the performance of s-CNT TFTs using m-CNT electrodes with our control devices using metal electrodes. We first fabricated m-CNT aligned array electrodes as we discussed in Chapter 4. To achieve the tunable density of s-CNTs assembly, the solution concentration of s-CNT is varied from 2ng/mL to 500 ng/mL. The different solution concentration of s-CNTs were
then assembled via AC DEP assembly (See also section 4.3) in order to obtain tunable density of aligned array of s-CNTs from 1 to 25 s-CNT/µm. The electrical transport measurements at room temperature showed that the on-conductance, and transconductance increase as the s-CNT density increases, while the mobility is not changed much but the current on-off ratio decreases dramatically as the density of s-CNT increased. The value of mobility was found to be all the time higher compared to our control devices using metal electrodes at all nanotube density in the channel. We will discuss more detail about our novel fabrication of tuning the nanotube density in the channel with m-CNT electrodes, and their electronic transport investigations at room and low temperature.

5.2 Fabrication of Tunable Density of s-CNT TFTs using m-CNT Electrodes

In the previous chapter (Chapter 4), we have discussed our novel fabrication of aligned array m-CNT electrodes via DEP assembly.[74] Using the same method for m-CNT electrodes fabrication, we prepared the pre-fabricated m-CNT electrodes for tunable density of s-CNT TFTs.

We used the highly enriched (99%) s-CNT solution from Nanointegris. The original solution concentration was ~10µg/mL. The solution is diluted with DI-water to vary the density of the nanotube in the solution from 2, 5, 10, 25, 50 to 200 ng/mL to obtain 1, 5, 10, 15, 20 to 25 s-CNT/µm in the channel, respectively. The different density of nanotubes were assembled via DEP methods. The detail of DEP assembly of CNTs was discussed in the previous chapter and our other publications.[68, 69, 83] The aim of our study is to explore the impact of s-CNT density in TFTs as well as improving contacts using m-CNT electrodes compared to bare Pd electrodes.
5.3 Characterization of Tunable Density of s-CNT TFTs using m-CNT Electrodes

Figure 50 (a) shows the SEM images of tunable density of aligned array s-CNTs in TFTs using m-CNT aligned array electrodes, and Figure 50 (b) shows the open-ended tips of m-CNT electrodes after cutting with 2nd lithography steps and plasma etching. The images in Figure 50 (c)-(f) show that the linear density of s-CNTs were well controlled to obtain 1 s-CNT/µm to 25 s-CNT/µm in the channel.

![SEM images of (a) m-CNT aligned array, (b) m-CNT electrode (after plasma etching), and aligned array of s-CNT with different linear density of (c) 1 s-CNT/µm, (d) 5 s-CNT/µm, (e) 15 s-CNT/µm, and (f) 25 s-CNT/µm between m-CNT electrodes. The scale bar indicates 1 µm.](image_url)
5.4 Transport Properties of Tunable Density of s-CNT TFTs using m-CNT Electrodes at Room Temperature

At each nanotube density, we measured the electronic transport properties of at least 5 devices. The representative output characteristics (drain current – drain voltage ($I_d$-$V_d$)) curves of m-CNT/s-CNT devices with various density (at $V_g$ = -30 V) are shown in Figure 51 (a).

Figure 51. (a) Output characteristics ($I_d$-$V_d$) of m-CNT/s-CNT device at $V_g$ = -30 V indicates the current is increased by maximizing the number of s-CNTs in the channel (b) Transfer characteristics ($I_d$-$V_g$) shows clearly that the current is varied with the density of s-CNTs in the CNT electrode. The comparison of device performance of the m-CNT/s-CNT and Pd/s-CNT devices as functions of linear density of s-CNT in the channel: (c) $G_{on}$ (d) $I_{on}/I_{off}$, (e) $g_m$, and (f) $\mu$ as a function of linear density.

As shown in Figure 51 (a), the output drain-current ($I_d$) increases with increasing the linear density of s-CNTs because higher density of s-CNT arrays provide a higher conducting
path in the channel between the source and drain electrodes. For example, the output current at $V_d = -1.0V$ with $V_g = -30V$ is 6.7 μA to 400 μA as the nanotube density increased from 1 to 25 s-CNT/μm, which is more than 60 times increase. Figure 51 (b) shows transfer characteristics (drain current – gate voltage ($I_d$-$V_g$)) curves at a fixed $V_d = -1V$ for m-CNT/s-CNT devices with different density of s-CNTs in the channel. From the transfer ($I_d$-$V_g$) curve, the device performance parameters such as on-conductance ($G_{on} = I_{on}/V_d$), current on-off ratio ($I_{on}/I_{off}$), transconductance ($g_m = dI_d/dV_g$), and linear mobility ($\mu$) can be extracted.

As shown in Figure 51 (c), average on-conductance (Gon) for m-CNT/s-CNT devices is increased from 17, 31.35, 61, 111, 129, and 311 μS with the density of s-CNT of 1, 5, 10, 15, 20, and 25 s-CNT/μm, respectively. As the nanotube density increased, we found on-conductance increased. For Pd/s-CNT devices, the similar observation was found. The on-conductance of Pd/s-CNT is increased from 2, 3, 16, 37, 68, and 202 μS with the density of s-CNT as 1, 5, 10, 15, 20, and 25 s-CNT/μm, respectively. The values of on-conductance of m-CNT/s-CNT devices were much higher compared to Pd/s-CNT, and it becomes similar after 20 s-CNT/μm.

The average values of current on-off ratios (Ion/Ioff) (Figure 51 (d)) for m-CNT/s-CNT devices were $2.6 \times 10^5$, 500, 30, 10, 6, 2.8 for 1, 5, 10, 15, 20, and 25 s-CNT/μm, respectively. As the density of nanotube increased, the chance of having metallic nanotube increased together, which result in lower on-off ratio. Similar behavior of decreasing current on-off ratio was found in Pd/s-CNT devices. The average current on-off ratios for Pd/s-CNT were $2.1 \times 10^3$, 38, 11, 5.3, 2.8, and 1.8 for 1, 5, 10, 15, 20, and 25 s-CNT/μm, respectively. We noted that the current on-off ratio in low density (< 5 s-CNT/μm), the output current of m-CNT/s-CNT is significantly higher than that of Pd/s-CNT, and this can be the reason for having higher current on-off ratio in low
density. In higher density, the chance of having metallic nanotubes increased, both on-current and off-current increased which caused the reduced current on-off ratio in both m-CNT/s-CNT and Pd/s-CNT devices.

The transconductance ($g_m$) and the linear mobility ($\mu$) for all the devices are extracted and plotted in Figures 51 (e) and (f), respectively. We calculated linear mobility ($\mu$) using the standard formula[83]:

$$\mu = \frac{(L/W) V_d}{C_i (g_m)}$$

where $C_i$ is the specific capacitance per unit area of aligned array,

$$C_i = D \left[ \frac{1}{C_Q} + (1/2 \pi \varepsilon_0 \varepsilon) \ln \left( \frac{\sinh(2 \pi \varepsilon_0 D)}{\pi D r} \right) \right]$$

$C_Q$ is the quantum capacitance of CNT (4×10$^{-10}$ F/m), $t_{ox}$ is the oxide thickness (250 nm), $\varepsilon$ is the dielectric constant of SiO$_2$ (3.9), $\varepsilon_0$ is the permittivity of vacuum, $r$ is the average radius of the s-CNTs, and $D$ is the linear density of the s-CNTs in the channel. The average mobility ($\mu$) of s-CNT TFTs using m-CNT electrodes (m-CNT/s-CNT) is 20 (±5) cm$^2$/Vs for the nanotube density of 1 to 25 s-CNT/μm. On the other hand, the mobility of s-CNT TFTs using metal electrodes (Pd/s-CNT) is significantly increased from 3 to 15 cm$^2$/Vs for the nanotube density from 1 to 25 s-CNT/μm. Here it can be clearly seen that the value of mobility for m-CNT/s-CNT devices is not affected much by increased nanotube density, while the mobility for Pd/s-CNT devices is much affected by increased nanotube density. It should be noted that the probability of having metallic nanotubes in the channel is similar for both m-CNT/s-CNT and Pd/s-CNT devices as the nanotube density increased. The only difference will be the contact at electrode/semiconductor interface, and we can predict that the interfacial contact at m-CNT/s-CNT interface maintained favorable at all the nanotube density. For Pd/s-CNT devices, the poor contact at Pd/s-CNT
interface lowered the mobility in low density of nanotubes, however, the mobility increased as the nanotube density increased due to the amount of metallic nanotube presence becomes higher which can suppress the contact issue. We also noted that the average mobility value were higher for s-CNT/m-CNT devices compared to Pd/s-CNT devices from 1 to 15 s-CNT/μm and becomes similar and comparable in 20-25 s-CNT/μm. We further investigated the device transport properties using temperature dependent studies with electronic transport measurements.

5.5 Temperature Dependent Transport Investigations of Tunable Density of s-CNT TFTs using m-CNT Electrodes

We performed the temperature dependent transport investigations from 77 to 285K and calculated the effective interfacial barriers height (Schottky barrier) for all different nanotube density using both m-CNT electrodes and Pd electrodes. From this calculation, the charge carrier injection mechanism at electrode/semiconductor interface at different nanotube density in the channel will be studied. We will also discuss whether the density of nanotube can be an impact in determining the injection barrier at electrode/semiconductor interface.

Figure 52 shows the temperature dependent drain current- drain voltage (I_{d}-V_{d}) curves at V_{g} = 0 V for representative m-CNT/s-CNT devices with different linear density of s-CNTs in the temperature range of 77 to 285 K. We noted that although the devices with 1 s-CNT/μm has already shown in the previous chapter, we used the data from the same density of 1-CNT/μm to
show how the device performance can be changed with the manner of increased linear density of s-CNTs in the devices from 1 to 25 s-CNT/μm.

![Temperature dependent (77-285 K) current-voltage characteristics at V_g = 0V of m-CNT/s-CNT device with the linear density of (a) 1 s-CNT/um, (b) 5 s-CNT/um, (c) 10 s-CNT/um, (d) 15 s-CNT/um, (e) 20 s-CNT/um, and (f) 25 s-CNT/um.](image)

Figure 52. Temperature dependent (77-285 K) current-voltage characteristics at V_g = 0V of m-CNT/s-CNT device with the linear density of (a) 1 s-CNT/um, (b) 5 s-CNT/um, (c) 10 s-CNT/um, (d) 15 s-CNT/um, (e) 20 s-CNT/um, and (f) 25 s-CNT/um.

The figures showed that the drain-currents (I_d) of the devices decrease with decreasing temperature, indicating a thermally activated transport. From the temperature dependent data, we calculated the Schottky barrier following the analysis of Martel et. al.[93] and others[94-96] by modeling the current using the Arrhenius equation I_d ~ exp (-Φ/kT), where k is the Boltzmann constant, T is the temperature and Φ is the Schottky barrier for the s-CNT TFT devices. It is also noted by Martel et. al. and others that Φ depends on the bias voltage and that the Schottky barrier at zero bias (Φ_b) is the “true” Schottky barrier, which should be calculated by plotting Φ(V_d)
(voltage-dependent Schottky barrier) as function of the square root of bias voltage ($V_d^{1/2}$) and then extrapolating the linear fit to $V_g = 0$. [93]

Figure 53. Arrhenius plot of current at different $V_d$ in the range of $-0.1$ V to $-1$ V for m-CNT/s-CNT device with the linear density of (a) 1 s-CNT/µm, (b) 5 s-CNT/µm, (c) 10 s-CNT/µm, (d) 15 s-CNT/µm, (e) 20 s-CNT/µm, and (f) 25 s-CNT/µm. The bias dependent Schottky barrier is calculated from the slopes of the ln$I_d$ versus 1000/T curves at different bias voltage.

Figure 53 (a)-(f) show an Arrhenius plot of the current (ln $I_d$ versus 1000/T) with $V_d$ ranging from $-0.1$ to $-1$ V in intervals of $-0.1$V for m-CNT/s-CNT devices with different densities of s-CNT from 1 to 25 s-CNT/µm, respectively. The linear relationship between ln $I_d$ and 1000/T confirms that the transport mechanism in our devices is mainly due to thermally activated charge carriers. From the slopes of the ln $I_d$ versus 1000/T curves, we calculated $\Phi(V_d)$.
for both m-CNT/s-CNT devices at different $V_d$ in the range of -0.1 V to -1 V. As seen in Figure 54 (a)-(f), $\Phi(V_d)$ decreases with increasing bias voltage. This is probably due to increase of the population of charge carriers in the interfacial states at the electrode/semiconductor interfaces with increasing bias-voltage which leads to reduce the Schottky barrier.

![Graph showing bias dependent Schottky barrier](image)

Figure 54. Plot of bias dependent Schottky barrier $\Phi(V_d)$ as a function of square root of bias voltage for m-CNT/s-CNT device (solid circle) and Pd/s-CNT device (open square) with the linear density of (a) 1 s-CNT/µm, (b) 5 s-CNT/µm, (c) 10 s-CNT/µm, (d) 15 s-CNT/µm, (e) 20 s-CNT/µm, and (f) 25 s-CNT/µm. The zero bias Schottky barrier ($\Phi_b$) (We call it simply Schottky barrier in the text.) is estimated by extrapolating the linear fitted line to at $V_d = 0V$.

As shown in Figure 54, We obtained the values of $\Phi_b$ as 44.8 meV (1/µm), 22.4 meV (5/µm), 22.2 meV (10/µm), 16.9 meV (15/µm), 14.5 meV (20/µm), and 13.1 meV (25/µm) for different densities of m-CNT/s-CNT device. The values of $\Phi_b$ for Pd/s-CNT device are 139.1
meV, 35.1 meV, 26.0 meV, 25.2 meV, 18.7 meV, and 13.0 meV for 1, 5, 10, 15, 20, and 25/µm, respectively. It is interesting that the average $\Phi_b$ of 1/µm for m-CNT/s-CNT devices (60.3 meV) is significantly lower than the average $\Phi_b$ for Pd/s-CNT devices (161.7 meV), however, this becomes almost similar when the density of s-CNTs in the channel is higher for both m-CNT/s-CNT and Pd/s-CNT devices. We found that in m-CNT/s-CNT devices, there is no such huge decreasing of barrier height as the density varied, however, in Pd/s-CNT devices, the density play a significant role in determining barrier height.

![Graph showing the variation of Schottky barrier as a function of density of s-CNT in the channel from 1 to 25 s-CNT/µm.](image)

**Figure 55.** Variation of Schottky barrier as a function of density of s-CNT in the channel from 1 to 25 s-CNT/µm.

Figure 55 shows a plot of average $\Phi_b$ versus s-CNT density for the both m-CNT/s-CNT and Pd/s-CNT devices. The average values of $\Phi_b$ for m-CNT/s-CNT devices are 60.3 (±13.8) meV, 25.2 (±4.2) meV, 23 (±6) meV, 17.6 (±0.14) meV, 14.7 (±1) meV, 14.05 (±1) meV while Pd/s-CNT devices have the values of 161.7 (±56.5) meV, 53.2 (±24.7) meV, 22(±6.5) meV, 22 (±2.1) meV, 18.6 (±0.2) meV, and 13.4 (±2.0) meV for 1, 5, 10, 15, 20, and 25 s-CNT/µm,
respectively. Here, we found two important features: (i) at lower densities (1-5 s-CNTs/µm), the \( \Phi_b \) for the m-CNT/s-CNT devices is significantly lower than that for the Pd/s-CNT device, while at higher densities the \( \Phi_b \) values are almost the same for both types of devices, and (ii) as the s-CNT density increases, the Schottky barrier for Pd/s-CNT devices decreases significantly, whereas the Schottky barriers for m-CNT/s-CNT devices change minimally. This explains why we observed much improved device performance for m-CNT contacted devices with lower s-CNT densities and only a small improvement in device performance at higher densities.

We speculate that the decrease of Schottky barrier with increasing s-CNT density in Pd/s-CNT may be due to an improvement in contact homogeneity, higher chances of having surfactant-free and larger diameter of s-CNTs in the channel. It has been shown that for individual Pd/s-CNT devices, the Schottky barrier decreases from 400 meV to almost zero with increasing nanotube diameter, implying that s-CNTs with a larger diameter have a lower Schottky barrier. By increasing s-CNT density in our device, the chances of having more nanotubes with larger diameters is also increased, which in turns may decrease the overall interfacial barrier. Even though we treated our s-CNT s in the channel by thermal annealing, there may be some residual surfactant existed remained in s-CNT giving rise to poor charge injection from electrode to channel.[102] Ideal temperature is above 800°C to remove all the surfactant in the CNTs, however, this is not compatible.

The possible reasons for a small decrease of Schottky barrier with increasing s-CNT density of the m-CNT/s-CNTs devices can be explained by considering the contact configuration between m-CNTs and s-CNTs at the interfaces. Since the s-CNTs are aligned in between aligned arrays of m-CNTs in our devices, we believe that the s-CNTs are connected with m-CNTs by
either end-contact or longitudinal side-end contact, or combination both of them. In the side-contacts, the tip of s-CNTs are connected directly to the tips of the m-CNTs (head-to-head connection) and charge injection mainly occurs from the m-CNTs tips due to electric field enhancement at the tips.[64, 67, 69] On the other hand, in the side-contact the m-CNTs and s-CNTs are connected in the longitudinal direction (side walls are parallel connected) and charge injection occurs mainly from the side-wall of the m-CNTs.

5.6 Conclusion

In conclusion, we fabricated the tunable density of s-CNT TFTs using m-CNT aligned array electrodes. The impact of s-CNT density in the channel was investigated by measuring electronic transport properties of tunable density s-CNT TFTs using both m-CNT electrodes and Pd electrodes. Not only density impact of s-CNT for TFTs but also the effect of using favorable contact at m-CNT/s-CNT were studied as compared to Pd electrodes. It is found that the on-conductance and transconductance increased as the nanotube density increased for both m-CNT/s-CNT and Pd/s-CNT devices which can be the indication of increased portion of metallic nanotubes in the channel. Due to better contact at m-CNT/s-CNT devices, the on-conductance and transconductance value in m-CNT/s-CNT devices with low s-CNT density was higher than that of Pd/s-CNTs. As the density of s-CNT increased, both devices have similar behavior with having similar values. The mobility of m-CNT/s-CNT devices was higher in the low density of s-CNTs compared to Pd/s-CNT devices, and the value was not changed much as s-CNT density increased. This suggests that the density impacts on m-CNT/s-CNT were not significant
compared to Pd/s-CNT devices due to favorable contact at m-CNT/s-CNT interface. Both current on-off ratio decreased dramatically in m-CNT/s-CNT and Pd/s-CNT devices with increase having metallic nanotubes in the channel.

The improvements of m-CNT/s-CNT devices can be attributed to unique 1D structure of CNT at m-CNT/s-CNT interface as well as favorable interface contact over metal/s-CNT interface. Similar improvements were observed in the higher density (>5 s-CNT/µm), however, the values of Pd/s-CNT devices approach those of m-CNT/s-CNT devices as s-CNT density was increased. This is due to the higher chances of having surfactant-free and larger diameter of s-CNTs in the channel when the density of s-CNT is increased.
6.1 Introduction

It has been reported that two-dimensional (2D) graphene can also have promising properties like CNTs including strong $\pi-\pi$ interaction, high workfunction, and low interfacial dipole formation compared to metal electrodes. In recent years, 2D graphene has attracted tremendous attention due to its unique electrical, physical, mechanical, and optical properties.[52, 103-105] It has been demonstrated that graphene can also have great potentials in various applications, such as flexible and transparent electrodes, energy-storage materials, composites, chemical and bio-sensing, and many other areas.[106-108] Therefore we began to think whether graphene also can be a promising candidate electrode material for s-CNT TFTs like CNT electrodes as we discussed in Chapter 4 and 5.

Among different chemically driven graphene films, reduced graphene oxide (RGO), a solution-processed route for producing graphene sheets, can offer many advantages such as large-area coverage with low-cost, easy processing, and large quantities of graphene sheets.[108, 109] In addition, RGO can be compatible with various substrates including plastics and papers which can be a promising candidate for future applications.[110]

In this chapter, we will introduce the fabrication of reduced graphene oxide (RGO) as alternative electrode materials for s-CNT TFTs. Our simple approach to fabricate solution-
processed graphene electrodes and its integration with highly enriched (99%) s-CNT aligned arrays for TFTs will be discussed in detail. To assemble both RGO thin film as electrodes and s-CNT arrays as channel materials, dielectrophoresis (DEP) method was used at ambient condition. The performance of s-CNT TFTs with RGO electrodes was evaluated using electronic transport measurements.

6.2 Fabrication of Aligned Array of Semiconducting Enriched CNT (s-CNT) TFTs using RGO Electrodes

In order to fabricate RGO electrodes, we first prepared the commercially available graphene oxide (GO) powder (Figure 56 (a)) (Cheap Tubes Inc. 30 mg), and the powder was diluted by deionized (DI, 30 ml) water with sonication followed by 24 hrs magnetic stirring (Also see section 3.4.3). To obtain chemically reduced- GO (RGO) solution, 200 µL of 5% NH₃ aqueous solution is added to adjust the pH of solution, and 30 µL of hydrazine solution is added (Figure 56(b)), and heated at 90°C for 60 min (Figure 56 (c)). The reduction efficiency was determined from carbon sp² fraction using x-ray photoelectron spectroscopy (XPS).[111-113] From XPS spectrum of RGO sheets, the carbon sp² fractions are calculated as 80%.[111]
Figure 56. Schematic diagram of making RGO electrodes with s-CNT TFTs. (a) GO powder is prepared and diluted with DI water. (b) GO solution (brown color) is reduced by hydrazine reduction to RGO solution (black color). (c) After heating the solution at 90°C for 1hr, the solution is then dropped onto pre-fabricated Pd electrodes. RGO thin film is assembled via AC DEP methods with 5V and 1MHz. (d) RGO thin film is assembled between Pd electrodes, and the sample was coated with PMMA layer, EBL is used to define the channel dimension, and the sample was developed and placed into O2 plasma. The opened area of RGO sheets will be etched away and (e) final RGO electrodes fabricated. (f) Highly enriched s-CNT solution is dropped onto RGO electrodes, and assembled via DEP methods.

Our devices were fabricated onto heavily doped silicon (Si) substrates with 250 nm thermally grown silicon dioxide (SiO2). Pd patterns (L : W = 5µm : 25µm) were defined using e-beam lithography (EBL) and e-beam evaporation of Cr (3 nm)/Pd (27 nm) followed by acetone lift-off. RGO solution was then dropped between Pd source and drain, and an AC voltage of 5 V
with 1 MHz frequency is applied for 30 sec. Finally, RGO sheets are assembled due to DEP force. The details of the RGO assembly can be found in our previous publications.[113]

After making RGO electrodes, we dropped the highly enriched s-CNT solution onto RGO electrodes. Using DEP assembly, s-CNTs arrays were aligned between RGO electrodes. The process of s-CNT assembly via DEP is the same as we discussed in the previous Chapter 4 and 5. The details of the s-CNT assembly can be also found in our previous publications.[69, 83]

6.3 Characterization of s-CNT TFTs using RGO Electrodes

Figure 57 (a) shows scanning electron microscopy (SEM) image of RGO thin film assembled via DEP methods. In our previous study[113] which is performed by one of our group members, we focused on a few RGO flakes assembly in a short channel (500nm), however, here we optimized the DEP assembly technique to obtain a thin RGO film in a larger channel geometry (2µm). After assembly of RGO thin film, the RGO sheets were then cut by 2nd EBL (L:W = 2 µm:25 µm) and subsequently oxygen plasma etched for 2 min. Finally, the devices were kept into acetone for 3 hrs to remove the residual PMMA on the devices. The SEM image of the resulting RGO electrodes is shown in the Figure 57 (b) showing well-defined channel. We investigated the thickness of RGO sheets using AFM and all the films have similar morphology with an average thickness of ~20 nm. Figure 57 (c) shows the s-CNT arrays were aligned via DEP assembly methods. We used 2 ng/mL of highly enriched (99%) s-CNT solution. The SEM images of s-CNT TFTs with RGO electrodes shows the density of s-CNT arrays were approximately 1 s-CNT/µm.
Figure 57. SEM images of (a) RGO thin film assembled between pre-patterned Pd electrodes onto Si/SiO$_2$ substrate, (b) RGO electrodes defined by 2$^{nd}$ EBL process, developing, plasma etching, and acetone lift-off, and (c) s-CNT aligned array via DEP assembly between RGO electrodes. Scale bar indicates 2 μm.

6.4 Transport Properties of s-CNT TFTs using RGO Electrodes

The output characteristics ($I_d$ vs $V_d$ curve) at different gate voltage ($V_g = -15$ to $-30V$) in the steps of -1V for representative s-CNT TFT device using RGO electrodes is shown in Figure 58 (a). The devices showed p-channel behavior with a good gate modulation. The linear $I_d$-$V_d$ curve at low bias voltages indicate a good interfacial contact with s-CNTs and RGO electrodes. The maximum drain current ($I_d$) at $V_d = -1V$ and $V_g = -30V$ was 1.1 μA. Figure 58 (b) showed the transfer characteristics ($I_d$ vs $V_g$ curve) of the same devices at $V_d = -1V$. The performance parameters such as on-conductance, field-effect mobility, transconductance, and current on-off ratio were extracted from the curve as seen in Figure 58.
Figure 58. Electrical transport properties of s-CNT TFTs with RGO electrodes. (a) Output characteristics ($I_d$ vs $V_d$) of s-CNT TFTs with RGO electrodes from 0 to -1V with the gate voltage ($V_g$) range of -15 to -30V in the steps of -1V. (b) Transfer characteristics ($I_d$ vs. $V_g$) of s-CNT TFTs with RGO electrodes at bias voltage ($V_d$) as -1V.

The on-conductance ($G_{on}$) is calculated from $G_{on} = I_{on}/V_d$, the field-effect mobility ($\mu$) is calculated from the standard formula, $\mu = (L/WC_iV_d)(g_m)$, the transconductance ($g_m$) is extracted from $g_m = dI_d/dV_g$, and the current on-off ratio ($I_{on/off}$) is extracted from $I_{on/off} = I_{on}/I_{off}$. We characterized total 13 devices of s-CNT TFTs using RGO electrodes with the linear s-CNT density of 1 s-CNT/µm. The summary of the device performance is shown in the box plots in Figure 59. The maximum (average) on-conductance ($G_{on}$) is 7.07 (1.62) µS, the field-effect mobility is 8.62 (4.20) cm²/Vs, transconductance ($g_m$) 0.102 (0.064), and the current on-off ratio ($I_{on/off}$) is $3.35\times10^4$ ($1.39\times10^3$).
Figure 59. Device statistics (from 13 devices of s-CNT TFTs using RGO electrodes). (a) On-conductance, (b) mobility, (c) transconductance, and (d) current on-off ratio.

We found the small improvements of device performance when compared to other published works on s-CNT TFTs using metal electrodes.[83] We attributed this improvements to better interfacial contact between graphene/s-CNT interface compared to metal/s-CNT interface. We also found that our previous work on s-CNT TFTs using m-CNT electrodes show much better improvements compared to the devices RGO electrodes. This maybe due to the conductivity of electrodes. We will also discuss in detail how the conductivity will affects on the
organic field-effect transistors (OFETs) device performance in next chapter (Chapter 7) by controlling carbon sp² fractions of RGO electrodes with different reduction efficiency.

6.5 Conclusion

In conclusion, we showed the simple fabrication of highly enriched s-CNT TFTs using solution-processed RGO electrodes. The thin film of RGO was first assembled between pre-patterned Pd electrodes, and then cut by standard ebeam lithography, plasma etching, and acetone lift-off process. After making RGO electrodes, s-CNT arrays are assembled by DEP method. We found a good gate modulation and the device performance with field-effect mobility of >6 cm²/Vs and current on-off ratio of >10⁴. This new way of fabricate s-CNT TFTs using RGO electrodes can be a significant step forward in realizing scaled up fabrication of carbon-based nanoelectronic devices for future low-cost and large-area flexible and transparent applications.
CHAPTER 7 : OFETS WITH REDUCED GRAPHENE OXIDE ELECTRODES

7.1 Current Status, Challenges, and Progress in OFETs

Organic field-effect transistors (OFETs) have attracted a great deal of research attention due to their flexibility, transparency, easy processing, low-cost of fabrication and large-area coverage.[22-24, 114] Due to these advantages, OFETs are expected to have substantial impacts on developing next generation applications such as flexible displays, flexible solar cells, sensors and radio-frequency identification (RFID) tags.[24, 114]

The noble metal electrodes such as gold (Au) or palladium (Pd) were used as electrode material for OFET devices, however, the use of metal electrodes can significantly limit the device performance of OFETs due to inefficient charge injection from metal electrode to organic semiconductor by large injection barrier at metal/organic interface due to discontinuity in morphology, interfacial dipole barrier and Schottky barrier formation at the interface.[25-29]

In order to overcome the challenges of the large injection barrier and the reduced charge injection at metal/organic interface, one-dimensional (1D) carbon nanotubes have been suggested as promising alternative electrode materials for OFETs.[64, 65, 67-71, 91, 115, 116] One of our group members published the extensive works towards to novel fabrication and characterization of CNT aligned array electrodes for high-performance pentacene transistors.[67-71, 91] It has been found that the injection barrier at CNT/organic interface is significantly

‡ The portions of this chapter have been published in Appl. Phys. Lett. 101, 233302 (2012), and Appl. Phys. Lett. 105, 223301 (2014)
lowered than metal/organic interface due to reduced barrier height at electrode/organic interface as well as strong π-π interaction between CNT and organic semiconductor.[69] The high frequency OFET devices were also fabricated using the advantages of CNT electrodes for OFETs.[67] The effect of density dependence of CNT aligne array electrodes were fully discussed in our recent publications which indicates the high density of CNT electrodes give the best performance compared to low density of CNT electrodes with OFET devices.[68] In addition, CNTs have strong field-emission due to their unique 1D structure which can enhance the charge injection from CNT to organic semiconductors.[64, 67, 69]

Since graphene, atomically thin layer with two-dimensional (2D) hexagonally packed carbon-sheet, is also carbon-based material like CNTs which can share the carbon sp² hybridized π-orbitals with organic semiconductors and its unique 2D structures, we began to think that the use of graphene as electrodes can maximize in the manner of interfacial area densities at graphene/organic contacts and thus improve the device performance of OFETs by using graphene electrodes. Also, the high work function and high conductivity of graphene film make it more promising alternative electrode materials as well as CNT electrodes.

In this Chapter, we will discuss our recent published work[117] in OFET devices using solution-processed graphene electrodes with different reduction efficiency. Reduced graphene oxide (RGO) was chosen as electrode materials due to its solution-processing to produce graphene sheets in large quantities at low cost and its compatibility with various substrates including plastics, makes them attractive for future applications.[108-110] It has been shown that RGO consists of sp² graphene domains surrounded by a continuous matrix of sp³ networks, which contains oxygen functional groups such as hydroxyl, epoxy, and carboxyl.[107, 118]
Interestingly, the ratio of $sp^2/sp^3$ fractions, can be tuned by controlling the reduction condition giving rise to tunable electronic and optical properties. Such $sp^2$ fraction tuning can also lead to a variation of work function and bandgap of RGO.[111, 112, 118-122] However, how the variation of carbon $sp^2$ fraction of RGO will affect the performance of RGO-contacted OFETs remains unexplored.

In order to see the impact of RGO electrodes with different reduction efficiency, we prepared three different carbon $sp^2$ fraction (61, 66, and 80%) of RGO solutions for making graphene electrodes. The solution was assembled via dielectrophoresis (DEP) method for RGO thin film, and then the channel was defined using ebeam lithography with final lift-off. After fabrication different reduction efficiency of RGO electrodes, pentacene film was depositied as organic semiconductor. We compared the performance of OFET devices with our control Pd electrodes. The fabrication and characterization of graphene electrodes will be discussed in detail with the investigation of electronic transport studies and possible charge injection mechanism with energy level diagram at electrode/organic interface.

### 7.2 Fabrication of Different Reduction Efficiency of RGO Electrodes

As we discussed earlier in Chapter 6, we prepare the reduced graphene oxide (RGO) solution from graphene oxide (GO) powder with DI-water, hydrazine and ammonia solution. The detail process was discussed in Chapter 6 (See Section 6.2). The RGO solution is then heated at 90°C for 10, 30, and 60 min in order to obtain the different reduction efficiency of RGO sheets in the solution.
We prepared heavily doped silicon (Si) substrates with a 250 nm thermally grown silicon dioxide (SiO$_2$) for device fabrication. At first, Pd patterns (L : W = 5 µm : 25 µm) are defined using ebeam lithography (EBL) and ebeam evaporation of Cr (3 nm) and Pd (27 nm) followed by lift off. Then, the different reduction efficiency of RGO solutions were dropped between the Pd patterns, and an AC voltage of 5 V with 1MHz frequency is applied for 30 sec. The thin film of RGO sheets were assembled via dielectrophoretic (DEP) method. The detail of DEP assembly was discussed in our previous Chapter 4-6 and our previous work.[111-113]

In our previous work, produced by one of our group members, the assembly of a few RGO flakes in a short channel (500 nm) was investigated.[113] Here, we optimized the DEP assembly parameters to obtain a large thin RGO films in a large channel geometry (5 µm). After the DEP assembly of RGO thin film of different reduction efficiency, RGO films were cut by EBL (channel length (L) : channel width (W) = 2 µm : 25 µm) and subsequent oxygen plasma etching for 2 min. To remove residual PMMA layer on the devices, the samples were immersed in acetone for 3 hrs, and then final RGO electrodes were fabricated.

7.3 Characterization of RGO Electrodes with Different Carbon $sp^2$ Fraction

The carbon $sp^2$ fraction for the different reduction time of RGO thin film was calculated as 61, 66, and 80 % for 10, 30, and 60 min of reduction time of RGO sheets, respectively. The carbon $sp^2$ fraction was obtained by taking the ratio of the integrated peak areas corresponding to the C-C peak, to the total area under the $C1s$ spectrum from the X-ray photoelectron spectroscopy (XPS) as shown in Figure 60.
Figure 60. XPS spectra of RGO sheets with different reduction efficiency and deconvolution of the C1’s peaks. The symbols (green square) are the experimental points and the solid lines are the deconvolution of the data. The reduction time is (a) 10, (b) 30, and (c) 60 min. The peaks containing different groups C-C (red curve), C-OH (brown curve), C=O (blue curve), and O=C-OH (black curve) are labeled for clarity. The four deconvoluted peaks indicate the deoxygenated graphene C-C at 284.6 ± 0.1 eV, oxygen-containing functional groups for hydroxyl (C-OH) at 286.0 ± 0.1 eV, carbonyl (C=O) at 287.0 ± 0.2 eV, and carboxyl acid (O=C-OH) at 288.6 ±0.1 eV. The percentage of the carbon sp² fraction (C-C peak) can be determined by the following expression:

\[
\frac{A_{C-C}}{A_{C-C} + A_{C-OH} + A_{C=O} + A_{O=C-OH}} \times 100\%,
\]

where A denotes the area under the corresponding peaks as marked in Figure 38 (a)-(c). The carbon sp² fractions are 61%, 66%, and 80% for the reduction time of 10, 30, and 60 min, respectively. Adapted from ref. [111, 112, 117].

Figure 61 (a) shows a representative SEM image of a RGO thin film assembled between Pd electrodes. The image was taken using a Zeiss Ultra 55 SEM with an in-lens secondary electron detector at 1.2 kV. Figure 61 (b) shows the representative current-voltage (Id-Vd) characteristics of the assembled RGO sheets with different reduction efficiency. The increase in carbon sp² fraction resulted in a decrease of room-temperature resistance (R). The average two-terminal R is 20.5 MΩ, 702 kΩ, and 165 kΩ for RGO sheets with carbon sp² fraction of 61% (green square), 66% (blue triangle), and 80% (red circle) (Figure 61 (c)). The decrease of
resistance with increasing $sp^2$ fraction demonstrates that the restoration of $\pi$-$\pi$ bond improves charge percolation pathways in the RGO sheets.

![Image](image1.png)

**Figure 61.** (a) SEM images of DEP assembled RGO thin film and (b) Current-voltage ($I_d-V_d$) characteristics of RGO thin films containing different carbon $sp^2$ fraction. (c) Resistance of RGO films with different reduction time. Carbon $sp^2$ fractions are 61% (green square), 66% (blue triangle), and 80% (red circle) for 10, 30, and 60 min reduction time of RGO sheets. (d) SEM image of RGO electrodes after oxidative cutting

The SEM image of the resulting RGO electrodes is shown in the Figure 61 (d), showing well-defined channel dimension. Regardless of different reduction efficiency, the average thickness of all the RGO thin film was approximately 20 nm determined by the atomic force microscopy (AFM) study shown in Figure 62.
Figure 62. (a) AFM image of a representative RGO electrode. (b) The height profile of the electrode showing the average thickness of RGO is ~20 nm. Γ line in (a) corresponds to the profile cross-section extracted. Scale bar: 1 µm.

A total of 30 devices using RGO electrodes were made, 10 devices for each $sp^2$ fraction. For control devices, we also fabricated 10 devices using bare Pd electrodes with the same dimension as RGO electrodes. The electrical measurements of all the devices were carried out in a probe station placed inside a glove box with an oxygen content of less than 0.5 ppm and the data was recorded using a HP 4145B semiconductor parametric analyzer.

### 7.4 Characterization of Pentacene Thin film on RGO Electrodes

After the RGO electrodes fabrication and characterization, the samples were then loaded into a thermal evaporator for pentacene deposition. Pentacene (Sigma Aldrich, ≥ 99.9%) film with a thickness of 30 nm was then thermally deposited under the vacuum at a pressure of $1 \times 10^{-6}$ mbar. In order to minimize the device-to-device fluctuation from the active materials morphology, all of the pentacene films were deposited under identical conditions. The
morphological investigation carried out by an AFM shows that all the films have similar morphology with an average grain size of 350-500 nm described in Figure 63.

Figure 63. AFM images of the pentacene film deposited on Si/SiO₂ substrate containing different electrodes: (a) Pd, (b) 61% RGO, (c) 66% RGO, and (d) 80% RGO electrodes. The pentacene film morphologies in the channel regions of all the devices are similar with typical grain size of 350-500 nm. Scale bar : 500 nm.

7.5 Transport Properties of OFETs using Different Carbon $sp^2$ Fraction of RGO Electrodes

Figures 64 (a)-(d) show the drain current ($I_d$) vs source-drain bias voltage ($V_{sd}$) curves (output characteristics) at different gate-voltages ($V_g$) for our representative pentacene FET
devices with Pd electrodes, and RGO electrodes of 61%, 66%, and 80% carbon $sp^2$ fraction, respectively.

![Graph showing output characteristics of pentacene transistors](image)

Figure 64. Output characteristics ($I_d$-$V_d$) of pentacene transistors at $V_g = 0$, -5, -10, -15, and -20 V (bottom to top) for (a) Pd, (b) 61%, (c) 66%, and (d) 80% carbon $sp^2$ fraction RGO in the electrodes. Transfer characteristics ($I_d$-$V_g$) of pentacene transistors at $V_d = -50$ V (left axis) and ($I_d$)$^{1/2}$ (right axis) of the devices with (a) Pd, (b) 61%, (c) 66%, and (d) 80% carbon $sp^2$ fraction RGO in the electrodes.

The $V_g$ was varied from 0 to -20 V in a step of -5 V. All the devices show p-type FET behavior with a good gate modulation along with a linear behavior at low bias and a saturation behavior at higher bias voltage. For a clear comparison, we plotted all the curves in the same scale. From here, we observe that the magnitude of the output current of the pentacene FET increases with increasing $sp^2$ fraction of the RGO electrodes. The magnitude of the output current (at $V_d = -50$ V and $V_g = -20$ V) for Pd contact is 1.06 µA, while it is 2.62, 4.93, 7.6 µA for the RGO electrode devices with 61, 66, and 80%, $sp^2$ fraction, respectively. The magnitude of the output current is more than 2 and 7 times higher for RGO electrodes with 61% and 80% $sp^2$
fraction, respectively, compared to the control Pd device. Since the morphology of all the devices is similar, the increase of output current with increasing RGO reduction efficiency clearly shows that the carbon $sp^2$ fraction of RGO has a significant impact on the output characteristics of the devices.

For further investigation of the effect of carbon $sp^2$ fraction of RGO electrodes on the device performance, we also measured the corresponding transfer curves ($I_d$ vs $V_g$) of the same devices at saturation regime ($V_d = -50$ V) (Figure 64 (e)-(h)) and calculated $\mu$, $I_{on}/I_{off}$, and $|I_{on}|$ of the devices. The mobility is calculated using the standard formula: $\mu = (2LI_{d,sat})/(WC_i(V_g-V_T)^2)$, where $I_{d,sat}$ is saturation current, $C_i$ is the gate capacitance (13.8 nF/cm$^2$) and $V_T$ is the threshold voltage. The values of $\mu$ for Pd, 61%, 66%, and 80% carbon $sp^2$ fraction of RGO are 0.052, 0.144, 0.205, and 0.319 cm$^2$/Vs, respectively. This demonstrates that the mobility of the pentacene FETs also increases with increasing the carbon $sp^2$ fraction of RGO electrodes. The values of $\mu$ are 2.5 times higher for 61% RGO and 6 times higher for 80% RGO compared to the control Pd contacted device. The transfer curves also show that the $I_{on}/I_{off}$ and $|I_{on}|$ ($I_d$ at $V_g = -40$ V) increases with increasing carbon $sp^2$ fraction of RGO electrodes. The $I_{on}/I_{off}$ and $|I_{on}|$ are $3.9 \times 10^3$ and $6.13 \mu$A for the control Pd electrodes, $5.4 \times 10^3$ and $19.7 \mu$A for 61% RGO electrodes, $1.7 \times 10^4$ and $24.2 \mu$A for 66%, and $2.2 \times 10^4$ and $32.2 \mu$A for 80% RGO electrodes. In addition, we have also extracted the transconductance ($g_m = dI/dV_g$) in the linear regime (at $V_d = -10$ V and $V_g = -40$V) of the transfer curve (Figure 65).
Figure 65. $I_d-V_g$ curve in the linear regime for Pd electrodes (yellow), and RGO electrodes with carbon fraction of 61% (green), 66% (blue), and 80% (red) from which we extracted the transconductance ($g_m = dI/dV_g$).

The $g_m$ was found to be 0.06 $\mu$S, 0.10 $\mu$S, 0.18 $\mu$S and 0.23 $\mu$S for the control Pd, 61%, 66%, and 80% RGO electrodes, respectively. Therefore, $\mu$, $I_{on}/I_{off}$, $|I_{on}|$, and $g_m$ are improved significantly with increasing the carbon $sp^2$ fraction of RGO electrodes.
7.6 Performance Comparison of OFETs using Different Carbon $sp^2$ Fraction of RGO Electrodes

The characteristics measured from all the devices (10 in each category) are summarized in Figure 6.6 (see also Table 1), where we plot the $\mu$, $I_{on}/I_{off}$, $|I_{on}|$, and $g_m$ as a function of the carbon $sp^2$ fraction of RGO electrodes. Figure 6.6 shows that, similar to our representative devices, the average $\mu$ is increased from 0.06 for Pd to 0.11, 0.20, and 0.31 cm$^2$/Vs for 61%, 66% and 80% of RGO electrodes, respectively.
Table 2. The current on-off ratio (I_{on}/I_{off}), mobility, on-current (I_{on}), and transconductance (g_m) for the devices with 61, 66, 80 % carbon sp² fraction and bare Pd electrodes.

<table>
<thead>
<tr>
<th></th>
<th>I_{on}/I_{off}</th>
<th>µ (cm²/Vs)</th>
<th>I_{on} (µA)</th>
<th>g_m (µS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>80%</td>
<td>max 2.8×10⁴</td>
<td>0.35</td>
<td>33.1</td>
<td>0.26</td>
</tr>
<tr>
<td></td>
<td>(avg) (2.1×10⁴)</td>
<td>(0.31)</td>
<td>(29.3)</td>
<td>(0.22)</td>
</tr>
<tr>
<td>66%</td>
<td>max 1.7×10⁴</td>
<td>0.29</td>
<td>26.5</td>
<td>0.21</td>
</tr>
<tr>
<td></td>
<td>(avg) (1.1×10⁴)</td>
<td>(0.20)</td>
<td>(22.7)</td>
<td>(0.14)</td>
</tr>
<tr>
<td>61%</td>
<td>max 5.4×10³</td>
<td>0.20</td>
<td>21.9</td>
<td>0.13</td>
</tr>
<tr>
<td></td>
<td>(avg) (3.5×10³)</td>
<td>(0.11)</td>
<td>(14.9)</td>
<td>(0.08)</td>
</tr>
<tr>
<td>Pd</td>
<td>max 4.4×10³</td>
<td>0.12</td>
<td>10.06</td>
<td>0.10</td>
</tr>
<tr>
<td></td>
<td>(avg) (2.4×10³)</td>
<td>(0.06)</td>
<td>(5.5)</td>
<td>(0.05)</td>
</tr>
</tbody>
</table>

The increase in the average µ for our OFETs is more than 5 times higher for 80% compared to the Pd contacted control devices. Similar significant increase can also be observed in the average value of the I_{on}/I_{off}, |I_{on}|, and g_m with increased reduction efficiency of RGO electrodes (Figure 66 (b)-(d)). For the control Pd electrode devices, the average value of I_{on}/I_{off}, |I_{on}|, and g_m are 2.4×10³, 5.5 µA, and 0.05 µS, respectively. These values increased to 3.5×10³ (1.5 times), 14.9 µA (3 times), and 0.08 µS (1.5 times) for 61%, 1.1×10⁴ (4 times), 22.7 µA (4 times), and 0.14 µS (3 times) for 66%, and 2.1×10⁴ (10 times), 29.3 µA (6 times), and 0.22 µS (4 times), for 80% of carbon sp² fraction in RGO electrodes.

From this study, it is clear that the different reduction efficiency of RGO electrode, which controls the carbon sp² fraction, resistance, and work function of RGO, plays an important role in determining the performance of OFETs. Our study also demonstrates that, although a few
minutes (10 min, 61%) of reduction efficiency of RGO electrodes can enhance the device performance compared to the control Pd contacted devices, the maximum performance is achieved using the highest reduction efficiency (60 min, 80%) of RGO electrodes. Since all the devices have the same organic semiconductor as channel materials deposited under identical conditions, the variation in device performance should be related to the electrode materials and electrode/pentacene interface.

If the interfacial Schottky barrier is \( \phi_B \), the current flowing through the device at a fixed bias voltage and temperature (T) can be approximated as \( I_d \propto \exp(-\phi_B/k) \),[69] where k is a Boltzmann constant. A decrease in \( \phi_B \) will result in an increased charge injection and higher device current. However, \( \phi_B \) is related to the work function difference between the pentacene and the electrode. The work function of Pd is 5.1 eV which is close to the highest occupied molecular orbital (HOMO) level of pentacene (5.0 eV). On the other hand, the typical work function of highly reduced RGO is reported to be in the range of 4.6-5.0 eV,[109, 122-124] close to the work function of conventional metal electrodes. Recently, Kumar et al[121] reported that the work function of RGO can be further tuned up to \( \sim 7 \) eV by varying the degree of reduction (lower reduction has a higher work function). This suggests that the work function of 80% \( sp^2 \) fraction RGO is close to the HOMO level of pentacene, while the work function of 66% and 61% carbon \( sp^2 \) fraction of RGO should be higher than 5.0 eV.

Figure 67 shows the schematic diagram of the energy level for different reduction efficiency of RGO (with the carbon \( sp^2 \) fraction of 61, 66, and 80%), and Pd with pentacene. Even though the work function of Pd is very close to the HOMO level of pentacene, in Figure 67 (a) we show a significant barrier between Pd and pentacene. This is due to the fact that when Pd
is contacted with pentacene, the effective work function of Pd is significantly lowered due to large dipole barrier formation at Pd/pentacene interface known as the ‘push back effect’.[28] This gives rise to a large Schottky barrier for hole injection at electrode/organic interface and causes an inferior device performance.

Figure 67. Schematic of energy level diagrams of (a) Pd/pentacene, (b) 61% RGO/pentacene, (c) 66% RGO/pentacene, and (d) 80% RGO/pentacene. This figure shows Fermi level ($E_F$), HOMO level of pentacene, and barrier height ($\phi_B$) at electrode/organic interface.

In contrast, due to a strong $\pi-\pi$ interaction existing at RGO/pentacene interface (organic-organic interface), significant dipole formation may not occur and the effective work function of RGO will not be significantly modified. In Figures 67 (b), (c) and (d) we show the energy level diagrams for 61%, 66% and 80% RGO electrodes, respectively. Based on this diagram, there are no hole injection barriers for 61% and 66% RGO, while the barrier for 80% RGO is negligible. Therefore, considering only the work function, one would have expected that the device performance for pentacene OFETs should be independent of the carbon $sp^2$ fraction of RGO.
electrode. This is in contrast to our experimental observation. Our results suggest that the carbon $sp^2$ fraction of RGO in the electrode, which tunes the conductivity of RGO, has a significant role in the OFET device performance. This can be understood from the charge carrier injection consideration. Even though all the RGO have favorable interfacial barriers, if the electrode does not have enough charge carriers to inject into the organic semiconductor, it cannot do an efficient carrier injection.[125] Since the conductivity of RGO depends upon the carbon $sp^2$ fraction and the conductivity of 61% RGO is two orders of magnitude lower than that of 80% RGO (Figure 61 (c)), the 61% RGO does not have enough carrier to inject into pentacene, compared to 80% RGO. As a result, the 80% RGO contacted pentacene devices show the best device performance.

### 7.7 Conclusion

In conclusion, we investigated electron transport properties of pentacene FETs where RGO of different carbon $sp^2$ fraction (reduction efficiency) was used as electrodes. We found that, although the device performance such as mobility, current on-off ratio, on-current and transconductance of all the RGO contacted devices show improvement compared to control Pd contacted devices, the best performance was achieved from the highest reduction efficiency RGO electrode. Since all the RGO electrodes have favorable work function for hole injection into pentacene, our study suggests that the tunable electronic properties of RGO is an important parameter that needs to be considered in fabricating RGO contacted organic devices.
CHAPTER 8: COMPARATIVE STUDY OF OFETS WITH LARGE AREA GRAPHENE ELECTRODES USING SIMPLE PATTERNING

8.1 Introduction

We have shown that the use of reduced graphene oxide (RGO) electrodes can be advantageous over the metal electrodes for organic field-effect transistors (OFET) devices due to its solution-processing, favorable π-π interaction and high workfunction match with p-type organic semiconductors as discussed in previous chapter (Chapter 7). Likewise, other chemical driven graphene films have been introduced as promising graphene electrode materials in recent studies.

The development of the large-area graphene film with large-quantities of production opened up the possibilities of making large-area graphene electrodes for future large-area applications. In recent studies, both chemical vapor deposition (CVD) grown graphene, and reduced graphene oxide (RGO) films have been used for electrode materials for OFETs and found improved charge injection compared to metal electrodes. However, the effect of types of graphene electrodes on the performance of OFETs have not been investigated yet which will be of great interest for future applications.

In this Chapter, we introduced a comparative study of OFETs using different types of large-area graphene film (CVD-GR and RGO) as electrodes. The electrodes were patterned using our novel simple patterning technique with a sacrificial polymer layer and a metal shadow mask. To investigate the device performance of OFETs using different types of large-area graphene
films, we fabricated pentacene field-effect transistors using patterned graphene films as source/drain electrodes. Then, we compared the device performance of OFETs using CVD-GR, RGO, and metal (Pd) electrodes. The details of fabrication methods and their characterization of OFETs using different types of large-area graphene films will be further discussed in this Chapter.

8.2 Experimental Set-up and Methods

We used our unique simple patterning techniques to pattern the large-area graphene film of both CVD-GR and RGO film. This patterning method does not include any acid etching process which can be environmental-friendly. First, the large-area graphene films of different types of graphene films were prepared, and then patterned using a metal ‘etch mask’ deposited by a metal shadow mask. This ‘etch mask’ protects the graphene electrodes while the unwanted film is exposed to plasma. The size and shape of patterned graphene film can be the exactly same as the metal etch mask. We keep the same device geometry for both CVD and RGO electrodes.

8.2.1 Large Area Graphene Film: CVD-GR and RGO Film

The growth of chemical vapor deposition (CVD) grown graphene films were performed by our collaboration, Christian Smith (Prof. Masa ishigami’s group). The single-layer of CVD graphene is prepared using a low pressure chemical vapor deposition on copper foil (Alpha Aesar no. 46986) treated in 5.4% by weight HNO$_3$ followed by a triple rinse in deionized (DI)
water prior to placing into a quartz tube furnace. The growth chamber was evacuated to below 30 mTorr before flushing with hydrogen and annealing the copper foil at 1040°C for 2 hrs. Methane was then introduced for an hour growth synthesis. The copper foil was rapidly cooled by removing the tube from the furnace completely. Contemporary transfer methods were then used to transfer the graphene film to our target substrate. A sacrificial PMMA supported the graphene film as the copper catalyst was etched using ammonium persulfate solution, before immersion in a subsequent series of modified RCA solutions.

The large-area RGO films were prepared by spin-coating of RGO solution. The detail fabrication of RGO solutions was discussed in previous chapter (Chapter 6 and 7). The solution was then spin-coated onto Si/SiO₂ substrate at 1000 rpm for 30 sec, which is repeated ~20 times to give a 20-30 nm thick layer. It should be noted that the thickness of the spin-coated RGO film can be easily controlled by adjusting the concentration of GO, the spin-coating speed, and the number of spin-coating cycles.

We measured the electronic transport properties of the films for both CVD-GR and RGO. Figure 68 shows the current-voltage characteristics for both graphene films which exhibit a standard ambipolar behavior as intrinsic properties of graphene with a field-effect mobility of 1000 cm²/Vs for CVD-GR and 0.1 cm²/Vs for RGO.
8.2.2 Simple Patterning of Large-Area CVD-GR and RGO Films for Electrodes

After the large-area graphene films (both CVD graphene and RGO) were placed on heavily doped silicon (Si) substrates with 250 nm thermally grown silicon dioxide (SiO$_2$) as a dielectric layer, polymer (950 PMMA C2, Micro Chem) is spin-coated on top of the graphene at 4000 rpm for 1 min to give a ~300 nm thick layer. Then, metal (Al) is thermally evaporated through shadow mask with the thickness of ~ 60 nm. The sample is exposed to plasma etching for 40 min and areas not protected by Al are etched away during plasma exposure. The metal fills the role of the ‘etching mask’, which protects the graphene during the plasma etching process. Finally, patterned graphene is obtained after simple removal of polymer by immersing the sample in acetone at 60°C for 1 hr. To minimize the effect of residual polymer on patterned graphene, the samples are annealed under H$_2$/Ar gas at 300°C for 2 hrs. The fabrication steps of...
schematic diagram of simple patterning for the large-area graphene films were illustrated in Figure 69. (See also Section 3.4.2).

Our simple patterning technique utilizes a polymethyl methacrylate (PMMA) layer that allows for simple acetone lift-off removal of the etch mask without the use of harmful acid treatments employed by the conventional metal etch mask processes. Additionally, the choice of metal becomes unlimited as compatibility issues with the etchant are alleviated. This new method can be useful because some metals are difficult to remove perfectly from graphene even after strong acid treatment, and this excessive acid can be harmful to the electronic properties of graphene.
8.2.3 Fabrication of Pentacene OFETs using Large Area Graphene Electrodes

To evaluate the device performance OFETs using different types of large-area graphene film as electrodes, we fabricate pentacene field-effect transistors using patterned graphene as source/drain electrodes. All the samples were then loaded into a vacuum thermal evaporator for pentacene deposition. Pentacene (Sigma Aldrich, ≥ 99.9%) film with a thickness of ~30 nm was then thermally deposited under the vacuum at a pressure of 1×10⁻⁶ mbar. In order to minimize the device-to-device fluctuation from the active materials morphology, all of the pentacene films were deposited under identical conditions. The morphological investigation carried out by an AFM shows that all the films have similar morphology with an average grain size of 150-200 nm as seen in Figure 70.

![AFM images](image)

Figure 70. Atomic force microscopy (AFM) images of the deposited pentacene film on (a) CVD graphene, (b) RGO, and (c) control Pd electrodes. The height analysis of these films shows the morphology of the films are the similar with an average grain size between 150 to 200 nm and rms surface roughness of 4~6 nm. Scale bar is 500nm.
8.3 Characterization of Large Area CVD-GR and RGO Electrodes

The characterization of single-layer CVD-GR transferred on Si/SiO$_2$ substrate is shown in Figure 71. SEM image of single-layer CVD-GR was taken using a Zeiss Ultra 55 SEM with an in-lens secondary electron detector at 1.2 kV. AFM and Raman investigations were performed on single-layer CVD-GR thin film on Si/SiO$_2$ substrate.

![Figure 71](image)

Figure 71. Characterization of CVD-GR. (a) SEM image, (b) AFM image, (c) Raman spectra of single-layer CVD-GR. (d) SEM image of resulting patterned CVD-GR electrodes and optical images (inset, scale bar 250 μm).

Figure 72 shows the characterization of RGO large-area thin film spin-coated on Si/SiO$_2$ substrate. The reduction efficiency was determined from carbon $sp^2$ fraction using x-ray
photoelectron spectroscopy (XPS). From XPS spectrum of RGO sheets of different reduction efficiency (Figure 72 (c)), the carbon $sp^2$ fractions are calculated as 80% for 60 min of reduction time of RGO sheets. The details of the RGO synthesis can be found in our previous publications.

Figure 72. Characterization of RGO thin film on Si/SiO$_2$ substrate. (a) SEM image, (b) AFM image, and (c) XPS spectrum of RGO thin film. (d) Final resulting patterned RGO electrodes on Si/SiO$_2$ substrate and optical image (inset, scale bar 250 μm).
As seen in the Figure 71 (d) and 72 (d), the size and shape of the pattern is exactly consistent with the etching mask and the sharp and regular contact edges can be clearly seen from the images.

8.4 Current-Voltage Characteristics of OFETs

We measured the electrical characteristics of OFETs using different types of large-area graphene films (CVD-GR vs. RGO) as electrode materials. We also fabricated and measured our control devices using metal electrodes with similar device geometry. The current-voltage (I_d-V_d) characteristics at different gate voltage (V_g) from 0 to -20 V in steps of -5 V of typical pentacene field-effect transistors using CVD-GR, RGO, and Pd electrodes are shown in Figure 73 (a)-(c). All the devices show a good gate modulation with linear behavior at low V_d, and saturation behavior at higher V_d, typical of p-channel OFETs. The lack of nonlinear behavior at low bias indicates an ideal ohmic contact existing between the graphene (or metal) and pentacene layers. For comparison of device characteristics, we plotted all the curves in the same scale. The output current (at V_d = -50V, and V_g = -20V) of the devices with CVD graphene electrodes, RGO electrodes, and Pd electrodes is 3.25, 1.73, and 0.48 µA, respectively. Compared to control Pd electrodes, CVD graphene/pentacene device shows almost an order of magnitude higher output current.
Figure 73. Output ($I_d$-$V_d$) characteristics at different gate voltage ($V_g$) from 0 to -20V in steps of -5V for patterned (a) CVD graphene electrodes, (b) RGO electrode, and (c) Pd electrodes with pentacene. Transfer($I_d$-$V_g$) curve at $V_d = -50V$ for patterned (d) CVD graphene electrodes, (e) RGO electrodes, and (f) Pd electrodes with pentacene.

For further investigation, we also measured the corresponding transfer curve (drain current vs. gate voltage ($I_d$-$V_g$)) at fixed $V_d = -50V$ (Figure 73 (d)-(f)). From the transfer characteristics, the field effect mobility ($\mu$), on-off ratio ($I_{on}/I_{off}$), and on-current ($I_{on}$) of the devices are calculated. The mobility $\mu$ is calculated using the standard formula, $\mu = (2LI_{d,sat})/(WC_g(V_g - V_T)^2)$, where L is the channel length, W is the channel width, $I_{d,sat}$ is saturation current, $V_T$ is threshold voltage, and $C_g$ is the gate dielectric capacitance. The $\mu$ of the devices is 0.33, 0.07, and 0.005 cm$^2$/Vs for CVD graphene, RGO, and Pd electrodes respectively. In addition to $\mu$, other important parameters to evaluate the performance of the transistors are
\( I_{on}/I_{off} \) and \( I_{on} \). The transfer curves show that the \( I_{on} \) (\( I_d \) at \( V_g = -80V \)) and \( I_{on}/I_{off} \) for CVD/pentacene and RGO/pentacene is more than an order of magnitude higher than control Pd electrodes. The \( I_{on}/I_{off} \) and \( I_{on} \) for CVD/pentacene and RGO/pentacene are \( 4.01 \times 10^4 \) and \( 122 \mu A \), \( 1.91 \times 10^4 \) and \( 23.5 \mu A \), respectively, whereas they are \( 1.83 \times 10^3 \) and \( 0.263 \mu A \) for Pd/pentacene (control device). Both OFETs with patterned graphene electrodes exhibit improved performance compared to Pd electrodes with significantly increased \( I_{on}/I_{off} \) and \( I_{on} \).

**8.5 Performance Comparison of OFETs**

We fabricated 10 devices for CVD/pentacene, RGO/pentacene, and Pd/pentacene devices, and all the devices have shown similar saturation behavior and good gate modulation with linear behavior at low bias regime.
Figure 74. Mobility is plotted against corresponding current on-off ratio for 10 devices for CVD/pentacene(Red circle), RGO/pentacene(Blue square), and Pd/pentacene(Green triangle).

For CVD/pentacene devices, the maximum (average) mobility is $0.33 \text{ cm}^2/\text{Vs}$ ($0.21(\pm0.04) \text{ cm}^2/\text{Vs}$), with corresponding current on-off ratio varying from $3.5 \times 10^4$ to $5.9 \times 10^4$ and on-current in the range of $74.1 \mu\text{A}$ to $125 \mu\text{A}$. The maximum (average) mobility of RGO/pentacene is varying from $0.07 \text{ cm}^2/\text{Vs}$ ($0.064(\pm0.005) \text{ cm}^2/\text{Vs}$), with corresponding on-off ratio varying from $1.3 \times 10^3$ to $2.5 \times 10^3$ and on-current varying from $21.2 \mu\text{A}$ to $26.5 \mu\text{A}$. The maximum (average) mobility of Pd/pentacene is $0.005 \text{ cm}^2/\text{Vs}$ ($0.003(\pm0.001) \text{ cm}^2/\text{Vs}$), with corresponding on-off ratio varying from $2.4 \times 10^2$ to $2.6 \times 10^3$ and on-current in the range of $1.1 \mu\text{A}$ to $2.6 \mu\text{A}$. Figure 74 shows a summary of the device characteristics for all pentacene FETs using CVD, RGO, and Pd electrodes. From here, we found that the maximum mobility, and on-off ratio of CVD/pentacene is 5 times and one order of magnitude higher than that of devices using
RGO/pentacene and 60 times and 2 order of magnitude higher than that of devices using Pd/pentacene. In addition, the mobility of RGO/pentacene is two times higher than the previous reported values of RGO/pentacene. To see a clear performance difference depending only on the electrode/organic interface is rather impressive, considering the fact that no surface treatments were performed on our devices. Overall, the performance of CVD/pentacene shows improvements compared to RGO/pentacene and Pd/pentacene, and this can be attributed to the less amount of charge carrier injected from the electrode to organic semiconductors. [ref] The conductivity of graphene film can be affected to the device performance of OFETs as also discussed in Chapter 7.

The improved performance of OFETs using graphene electrodes (both CVD graphene and RGO) over the control Pd electrode is attributed to enhanced charge injection at graphene/pentacene interface. Even though the work function of Pd (5.1 eV) is very close to the HOMO level of pentacene (5.0 eV), when Pd is contacted with pentacene, the effective work function of Pd is significantly lowered due to large dipole barrier formation at Pd/pentacene interface known as the ‘push back effect’. As a result, the effective work function of the Pd electrodes is significantly reduced, giving rise to a large Schottky barrier for hole injection at the electrode/organic interface. Therefore, despite this high work function, the charge injection at the Pd/pentacene interface is hurt by a high injection barrier. In contrast, due to a strong π-π interaction existing at the graphene/pentacene interface (organic-organic interface), significant dipole formation may not occur and the work function of graphene may not be significantly lowered. When comparing the performance of CVD/pentacene and RGO/pentacene, the improved performance from CVD/pentacene may come from the higher conductivity. Ou et al
reported that not only the work function but also conductivity of the electrode is a factor in determining the performance of OFET devices. As the conductivity of CVD graphene is higher than that of RGO graphene, therefore, the number of charge carriers from the electrode to organic layer is higher for CVD/pentacene than RGO/pentacene, which may lead to future improvements in charge injection.

8.6 Conclusion

In conclusion, we report a new approach of the simple patterning of graphene by metal mask using polymer sacrificial layer. We found that this method can apply to both CVD graphene and RGO electrodes and this approach can be generalized for manufacturing other carbon-based thin film such as different types of graphene and carbon nanotubes. Using patterned graphene electrodes, we found that comparable or even better charge injection at the interface between graphene electrodes and organic semiconductor compared to conventional metal electrodes. Simple patterning of large-area graphene will be a significant step forward in realizing scaled up fabrication of graphene based nanoelectronic devices.
CHAPTER 9 : HIGH-PERFORMANCE SHORT-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS WITH GRAPHENE ELECTRODES

9.1 Introduction

Fabrication of high-performance short-channel OFET devices can have potentials to increase both output current-level and field-effect mobility by strongly focused electric fields as well as decreased the number of grain boundaries in the channel. The short-channel OFETs can be also advantageous for the aim of high-frequency device ($f_c$ is proportional to $\mu/L^2$) manufacturing and lowered operation voltages.[67, 126]

However, studies have shown that the problems and limitations of the performance of short-channel OFET devices mainly result in the absence of “saturation” of the current (diode-like behavior), finite current flow in the saturation regime under normally “OFF” condition, and thus may decrease current ON/OFF ratio (Figure 75).[127-129] The short-channel effect may be induced by choice of electrode material, increased relative effects of parasitic contact resistance with reduction in channel length, limited current by trap-charged in the film, the channel ratio of the channel length to the gate insulator thickness.[127-129]
In this chapter, we introduced high-performance short-channel (sub-100 nm) OFET devices using graphene as electrode material. As we discussed in previous Chapters (5 through 8), graphene has been suggested as a promising electrode material for OFETs due to its high work function (~5.0 eV) which matched to HOMO level of p-type organic semiconductor, as well as strong π-π interaction with organic molecule which can lower the injection barrier at the electrode/organic interface. We will show the high-performance OFET behaviors from the devices using graphene electrodes compared to devices with Au electrodes. The charge injection
barrier height will be calculated and further analyzed by introducing thermionic emission model to investigate at graphene/organic interface.

9.2 Fabrication of Short Channel (Sub-100nm) Graphene Electrodes

Atomically thin graphene layer was mechanically exfoliated from commercially available bulk graphite (Graphene Supermarket, Natural Kish Graphite Grade 200) using adhesive tape and deposited onto heavily doped Si substrate with thermally grown SiO₂ as dielectric layer. Before the exfoliation, Si substrate was thoroughly cleaned using acetone, and IPA followed with N₂ blown dry. After obtaining desired size, shape, and thickness of the graphene layer, the sample was spin-coated with PMMA layer for EBL processing. The pattern design was defined for source/drain electrodes, and the sample kept in evaporator for the metal deposition and then final lift-off in acetone for 3 hrs. Cr layer was deposited using ebeam evaporation for 3 nm and Au layer was deposited using thermal evaporation for 27 nm. Once the contact pads have made, the device then spin-coated with PMMA layer for the 2nd EBL processing to define channel dimension onto graphene flake. This channel dimension will be used for graphene electrodes for OFETs. We fabricated sub-100 nm channel length and our channel width was varied depending on the flake size from 2 to 15 μm. We also fabricated control device (Au electrodes) with similar device geometry with OFETs with graphene electrodes.
9.3 Characterization of Short-Channel Graphene Electrodes

We measured the current-voltage characteristics of exfoliated graphene film after making contact pads on the flake. Figure 76 (a) shows representative the drain current ($I_D$) vs. drain voltage ($V_D$) curve with zero gate, and Figure 76 (b) shows the drain current vs. gate voltage curve. The transfer curve showed the intrinsic ambipolar behavior of graphene with the field-effect mobility as $\sim 1000 \text{ cm}^2/\text{Vs}$.

![Figure 76](image)

Figure 76. The current-voltage characteristics of pristine graphene film. (a) Output curve at $V_g = 0 \text{V}$ and (b) transfer curve at $V_{ds} = 0.1 \text{V}$.

Figure 77 (a)-(c) shows the optical images of (i) pristine exfoliated graphene, (ii) devices after short-channel defined using Ebem lithography (EBL) process and developing of PMMA layer, and (iii) final resulting sub-100 nm channel graphene electrodes. In order to see the short-channel gap clearly, scanning electron microscopy (SEM) and atomic force microscopy (AFM) images were added to show well-defined graphene electrodes with channel length of 80 nm, as seen in Figure 77 (d) and (e), respectively.

139
Figure 77. Characterization of sub-100nm graphene electrodes. Optical images of (a) pristine exfoliated graphene onto Si/SiO2 substrate, (b) after EBL process to define the channel dimension and developing of PMMA layer, (c) final resulting graphene electrodes with 80nm gap. (d) SEM image and (e) AFM image of well-defined short-channel graphene electrodes.

Figure 78 shows AFM image of our control devices (Au electrodes) fabricated with similar channel geometry with graphene electrodes.
9.4 Characterization of Pentacene Film Deposition in Short-Channel OFETs using Graphene Electrodes

After making short-channel graphene electrodes, pentacene film was thermally deposited under vacuum of $1 \times 10^{-6}$ mbar with rate of 0.1-0.2 Å/sec for 30 nm thickness. The pentacene was deposited under the identical condition for both devices with graphene electrodes and Au electrodes as control devices. Figure 79 shows the morphology of pentacene film onto Si/SiO$_2$ substrate as well as on the electrodes. The typical grain size was found in the range of 150-170 nm. Since our devices was made with sub-100nm, the number of grain boundaries in the channel were reduced compared to longer channel than 100nm.

Figure 79. AFM image of pentacene thin film deposition on the devices using (a) Au electrodes and (b) graphene electrodes. The height analysis shows the average grain size of pentacene film on Si/SiO$_2$ substrate is in the range of 150-170nm.
9.5 Current-Voltage Characteristics of OFETs using Short-Channel Graphene Electrodes

In order to investigate the performance of OFETs using short-channel graphene electrodes, electrical transport measurements were performed. The performance of OFET devices using graphene electrodes were compared with control devices using Au electrodes as shown in Figure 80. Figures 80 (a) show the drain current ($I_d$) vs source-drain bias voltage ($V_{d}$) curves (output characteristics) at different gate-voltages ($V_g$) for representative devices using Au electrodes. The devices shows a short-channel effect phenomena with diode-like behavior with the absence of saturation regime. Also, we found that the OFF state current is high which can lower the current ON/OFF ratio as seen in Figure 80 (b).

Otherwise, Figure 80 (c) shows the representative output characteristics of short-channel OFET devices using graphene electrodes with both linear and saturation regime and complete OFF state current which cannot be found in short-channel OFET devices using Au electrodes (control devices). The mobility of the OFET devices using graphene electrodes was calculated as 0.596 cm$^2$/Vs which is almost six times higher than the devices using control Au electrodes. The current ON/OFF ratio of the devices using graphene electrodes is more than four order of magnitude higher than that using Au control devices. Threshold voltages was found to be closer to zero with the devices using graphene electrodes. We characterized 5 devices for each categorizes and found similar performance. Since the morphology and grain sizes of the devices were found to be similar, the enhanced performance of short-channel OFET devices using
graphene electrodes show that the contact has significant impact on the characteristics of the devices.

Figure 80. The performance comparison of OFET device using Au electrodes (blue) and graphene electrodes (red). Output/transfer characteristics for Au electrodes (a)-(b) and for graphene electrodes (c)-(d). The table shows the mobility, current ON/OFF ratio, and On current, and threshold voltage for both devices.

The enhanced performance of OFETs using short-channel graphene electrodes can be generally attributed to several factors such as reduction of trapped-charges or impurities in the channel, improved contact with gate dielectric, or improved charge injection due to reduced charge injection barrier at electrode/organic interface. Since we deposited the pentacene deposition under identical condition and found similar morphology and grain sizes, the used same gate dielectric layers in this study, we strongly believe that the improvements of short-
channel OFET devices using graphene electrodes may come the better interfacial contact at graphene/organic compared to metal/organic.

9.5 Temperature Dependent Charge Injection and Transport Mechanism

In order to further understand the enhanced performance of OFET devices using graphene electrodes, we performed the temperature dependent study to determine the charge injection barrier height at graphene/organic interface as seen Figure 81.

![Figure 81](image.png)

Figure 81. (a) ln J vs. $V^{1/2}$ plots of short-channel OFET devices at high temperature range of 295K to 230K. The current is strongly depending on the temperature and voltages changes. (b) Arrehnius plot of ln ($J_o/T^2$) vs. 1000/T. The value of $J_o$ was extrapolated from the y-intercept of graph (a). From the extracted slope in high temperature range, the charge injection barrier height at graphene/organic was calculated as 0.235 eV.
Figure 81 (a) shows the current density plot versus square root voltages in logarithium scale which is the indication of thermionic emission with strongly dependence of current as a function of temperature and voltage difference. The strongly dependent curves can be well described by the Richardson-Schottky (RS) model for thermionic emission with the equation of \( J = A^* T^2 \exp[-q(\phi_B-qV/4\pi\varepsilon_0\varepsilon_d)^{1/2})/kT] \). The value of \( J_0 \) was extrapolated from the \( \ln J \) vs. \( V^{1/2} \) curve when \( V=0 \), and the slope of \( \ln (J_0 T^2) \) vs 1000/T in high temperature regime can be extracted. The final charge injection barrier height (\( \phi_B \)) was calculated as 0.235 eV as shown in the Figure 81 (b). We measured three devices and all the devices shows the similar values. The calculated barrier height for the Au/pentacene interface was measured by different groups as 0.5-0.85 eV.[28, 130, 131] This indicates the barrier height of graphene/pentacene interface is much lowered than that of Au/pentacene interface, which can be attributed to the enhanced performance in short-channel OFET devices using graphene electrodes.

### 9.6 Conclusion

Our study have demonstrated that (i) high-performance of short-channel OFETs using graphene as electrodes, and (ii) significantly lowered charge injection barrier at graphene/organic interface which can improve the device performance of OFETs compared to metal electrodes. These improvements can be attributed not only to favorable graphene/organic interface with strong π-π interaction but also reduced barrier height from avoiding a large interfacial dipole formation like metal/organic interface. We found that the interface of graphene/organic can provide more efficient charge injection pathways compared with metal/organic interface. Thus,
we conclude that the performance of the pentacene transistors using short-channel graphene electrodes can be advantageous to fabricate high-performance OFET devices.
CHAPTER 10: CONCLUSION

10.1 Summary

In this thesis, we showed that the performance of nanoelectronic devices such as semiconducting carbon nanotube thin film transistors (s-CNT TFTs) or organic field-effect transistors (OFETs) can be enhanced by improving metal-semiconductor interface using carbon-based material electrodes including carbon nanotubes (CNTs) or graphene. We showed simple and novel fabrication techniques using photolithography, ebeam lithography, plasma etching, metal shadow etch mask as well as direct growth. From the electronic transport measurements, we found that the field-effect mobility, current on-off ratio, and on-current of nanoelectronic devices can be improved. From the temperature dependent studies, we also showed that the charge injection barrier at metal-semiconductor interface can be much lowered compared to bare metal electrodes.

This work is supported by U.S. National Science Foundation (NSF) under Grant ECCS 1102228.

10.2 Future Work

Our study showed that the use of carbon-based materials electrodes can be advantageous for improving the device performance of nanoelectronic devices. The conclusion of our study suggested the way to improve the devices for future electronics. Also, this work will give us a
better understanding of the effect of carbon-based material electrode in terms of the device performance such as charge injection and transport mechanisms. More research can be done by fabricating other applications to evaluate the carbon-based material electrodes such as photodetectors, solar cells, and sensors. This research will provide us a numerical value for the great potential applications that can be commercially available in near future.

Another future work suggestions may be on the fabrication and investigation of device performance on other substrates such as plastic, paper, or clothigs for future applications. Since our study suggests the better interface between electrode and channel semiconductor, further improvements of devices on these substrate can be promisingly expected.
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**APPENDIX B: LIST OF PUBLICATIONS**

*denotes equally contributed authors (co-authors)


APPENDIX C: Curriculum Vitae
Narae Kang  
NanoScience Technology Center and Department of Physics,  
University of Central Florida, 12424 Research Pkwy Suite 400  
Orlando, FL 32826  
E-mail: naraekang@knights.ucf.edu  
Phone: +1 407.607.9091  
URL: www.linkedin.com/in/naraekang

Education

Ph.D. • Department of Physics • University of Central Florida • USA  
Nanophysics and Nanoelectronics Group (GPA 3.75/4.0)  
Advisor: Prof. Saiful I. Khondaker  
Dissertation Title: Nanoelectronic Device using Carbon Nanotubes and Graphene  
Electrodes: Fabrication and Electronic Transport Investigations  
Aug. 2010 – Present (Expected in May)

B.S. • Department of Applied Physics • Hanyang University • Korea  
Surface Science Laboratory (GPA 4.08/4.5)  
Advisor: Prof. Bongjin Simon Mun  
Mar. 2006 – Aug. 2009 (Summa Cum Laude)

Professional Experience

Graduate Research Assistant • University of Central Florida  
Jan. 2011 – Present

NanoScience Technology Center and Department of Physics

- Emerging 2D Materials for Nano Electronics/Optoelectronics  
  • Mastered hands-on expertise in device design, fabrication, and electrical/optical characterization of mechanically exfoliated molybdenum disulfides (MoS2)  
  • Developed the ability to create and manipulate defects for tailoring properties of MoS2  
  • Investigated and characterized electronic/optoelectronic properties of defect-induced bandgap engineering in MoS2 by time-dependent oxygen plasma exposure

- High-Performance Organic Field-Effect Transistors (OFETs) for Organic Electronics  
  Funded by the National Science Foundation (NSF)  
  • Pioneered fabrication techniques of carbon-based electrodes (such as graphene and CNT electrodes) using state-of-art lithography patterning and plasma etching  
  • Designed and fabricated CMOS compatible high-performance OFETs with carbon-based electrodes for enhancing charge injection at electrodes/organic interface to overcome limitations of conventional metal electrodes  
  • Carried out electrical measurements and investigated charge injection mechanism at electrode/organic interface at variable temperature

- Carbon Nanotube Thin Film Transistors (CNT-TFTs) for Nano Electronics  
  Funded by the National Science Foundation (NSF)  
  • Developed assembly techniques of solution-processed single-walled CNTs via dielectrophoresis method  
  • Fabricated tunable density of semiconducting enriched CNT TFTs using metallic CNT electrodes  
  • Performed electronic transport measurements at variable temperature to investigate the charge injection and transport mechanism at electrode/semiconductor interface

- Project Management and Mentorship: 8 Undergraduate and 2 Graduate Students
Graduate Teaching Assistant • University of Central Florida  Aug. 2010 – Aug. 2012

Department of Physics
- Created problem-sets and solutions for quizzes, and provided discussion and instructions to help students for conceptual understanding of physics lab course (PHY2053)
- Assisted faculties with teaching responsibilities including proctoring and grading

Undergraduate Research Assistant • Hanyang University • Korea  Jun. 2008 – Aug. 2009

Department of Applied Physics
- Characterized Ag nanoparticles with X-ray photoelectron spectroscopy (XPS)
- Analyzed the surface segregation in bimetallic alloys with transition metals

- Pohang Accelerator Laboratory (PAL), Pohang University of Science & Technology (POSTECH), Korea
- Lawrence Berkeley National Laboratory (LANL) Advanced Light Source, University of California at Berkeley
- Korea Research Institutes of Standard and Science (KRISS), Korea

Professional Skills

Experimental Skills

- Nano-and Micro-Fabrication: Cleanroom experience, Photolithography, E-beam Lithography (EBL), E-beam Evaporator, Thermal Evaporator, Plasma Etcher, Wire Bonding
- Thin Film Deposition: Thermal deposition, Direct growth, Spin coating/Drop casting, Dielectrophoresis Assembly
- Electronic/Optoelectronic Measurement: Current-voltage Characteristics Measurements at variable temperature, Quantum Efficiency Measurements, Photoresponse Measurements
- Set-up, Maintenance, and Installation: New glovebox system with low oxygen level (<0.5ppm) interfaced LabVIEW probe measurements for electrical measurements and Optics lab for quantum efficiency measurements for organic electronic devices

Application Software
- Proficient in DesignCAD (Pattern layout, simulation, design rule checking for EBL), FlexPDE, Origin, Solidworks, Endnote, and MS Office. Experience in AutoCAD, Adobe Illustrator, LabVIEW, C++, Fortran, Mathematica, and MATLAB.

Other Skills
- Experimental design, Scientific communication, Assisted advisor in writing several NSF research proposals, Multi-disciplinary and multi-tasking skills for handling multi-projects, Strong data analysis and interpretation skills, Excellent written and verbal communication skills for technical reporting and problem solving, Experienced presenter, Excellent interdisciplinary teamwork, Responsibility for operation and maintenance of scientific equipment.
List of Publications (with hyperlinks)

* denotes equally contributed authors (co-author).


Presentations


**Honors and Awards**

- Grand Prize for Poster Presentation, Florida-American Vacuum Society (FLAVS) 2015
- Graduate Research Excellence Fellowship, University of Central Florida 2013-2015
- Graduate Travel Fellowship Award, University of Central Florida 2012-2015
- SGA Travel Expense Award, University of Central Florida 2012-2015
- Honorable Mention for Poster Presentation, Florida-American Vacuum Society (FLAVS) 2013
- Summa Cum Laude, Hanyang University, Korea 2009
- Grand Prize of Contest in Applied Science Technology, Hanyang University, Korea 2008
- Excellence Student Scholarship for Mentor Activities, Hanyang University, Korea 2006-2009

**Professional Memberships and Activities**

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<td>Korean-American Scientists and Engineers Association (KSEA) –YG Chapter President</td>
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[6] "LG’s 77-inch Ultra HD curved OLED TV is the biggest," Available at:

[7] "Samsung Showing Off New Flexible AMOLED Display In Japan.," Available at:


[9] "Nellis Solar Power Plant (Air Force)" Available at:


