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Design and analysis of class AB RF power amplifier for wireless communication applications

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DESIGN AND ANALYSIS OF CLASS AB RF POWER AMPLIFIER FOR WIRELESS COMMUNICATION APPLICATIONS

by

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ABSTRACT

The Power Amplifier is the most power-consuming block among the building blocks of RF transceivers. It is still a difficult problem to design power amplifiers, especially for linear, low voltage operation. Until now power amplifiers for wireless applications is being produced almost in GaAs processes with some exceptions in LDMOS, Si BJT, and SiGe HBT. The submicron CMOS processes for power amplifiers are under research focus since CMOS offers integration for power amplifier with rest of the transceivers blocks due to its high yield. Also CMOS process is cheap.

This thesis report details the design process of a class AB power amplifier for GSM wireless applications using 0.35 μm CMOS process. The transmit frequency for GSM-1800 standard for handset applications is 1710 MHz – 1785 MHz. The power amplifier has been designed to deliver 2 W of minimum output power into a 50 Ω load. The circuit was designed and simulations indicated a peak power added efficiency of 47 %.

ACKNOWLEDGMENTS

Praise is to ALLAH, the lord of the worlds and peace is upon his prophet and last messenger, Muhammad (PBUH). " Glory is to You, have no knowledge except what you have taught us. Verily, it is You, the All-Knower, the All-Wise." Verse 32, Chapter Al-Baqarah, The Noble Qur'AN.

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1 INTRODUCTION

1.1 Motivation

The growth rate for the wireless communications industry is increasing due to the advanced options it offers and adds everyday which led in turn to a big demand from consumers. The annual world wide sales of cellular phones has exceeded $2.5B. With 4.5 million customers, home satellite networks comprise a $2.5B industry. The global positioning system was a $5B market in the year 2000. In Europe, the sales of the equipment and services for mobile communications had reached $30B in 1998 [1]. Some of the criteria that consumers put into their consideration when comparing between different wireless equipment are talk time, price, and size. Talk time can be interpreted to long battery life or less power consumption, which means efficiency in engineering terms. Price and size can be considered to some extent two different sides of a coin as both depend on the technology that is being used. Power Amplifier is the most power-consuming

block of the RF transceiver. Table 1.1 is a summary of some common power amplifiers requirements [2].

Table 1.1 PA standards and summary

	AMPS	IS-54/136 TDMA	CDMA	GSM (Class 4)	DCS1800
Tx Frequency	824-850 MHz	824-850 MHz	824-850 MHz	880-915 MHz	1710-1785 MHz
Eff. Rad. Power	600mW/ 28dBm	600mW/ 28dBm	250mW/ 24dBm	2W/ 33dBm	1W/ 30dBm
PA power	1.4W/ 31.5dBm	1.3W/ 31dBm	600mW/ 28dBm	3W/ 35dBm	1.8W/ 32.5dBm
Duty cycle	100%	33%	100%	12.5%	12.5%
Peak/Ave Power η	0dB >60%	4-6dB >40%	8-10dB >30%	0dB >50%	0dB >40%
Modulation	FM	$\pi/4$ QPSK	BPSK/ QPSK	0.3 GMSK	0.3 GMSK
Envelope	Constant	Varying	Varying	Constant	Constant

1.2 Structure of RF Transceiver System

Refer to figure 1.1 for the transmitter side, I (In-phase) and Q (Quadrature) signals are modulated and then fed to the power amplifier, which drive the antenna

through the BALUN (Balanced. Unbalanced) transformer. For the receiver, the signal received by the antenna is filtered to choose the correct band and fed to the LNA (Low Noise Amplifier) through the BALUN transformer. Then the signal is demodulated to the I & Q components. The circulator is used so that transmitter and receiver can share the same antenna.

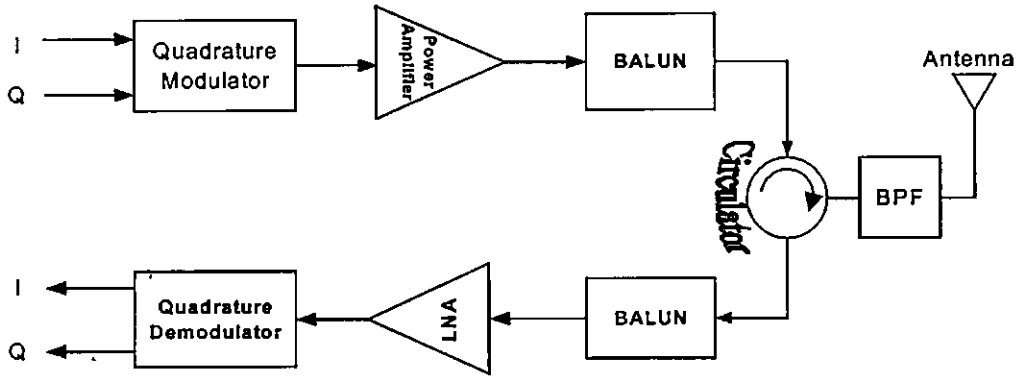


Figure 1.1 The structure of RF system.

1.3 Power Amplifier Design Considerations

1.3.1 Output Power

CMOS process is a good candidate when considering low power requirements around the 1 W range. Especially, with small feature sizes that can

be used which results in smaller stray capacitances and higher ft., which means lower power loss at higher frequencies. But for high power transmission that requires output power of several watts, the use of high power gain microwave devices such as silicon bipolars or especially GaAs MESFETs in the output stage is essential [3]. High output power of the GaAs MESFET is a direct result of the higher critical field, higher saturated drift velocity, and lower stray capacitance.

1.3.2 Power Added Efficiency and Linearity

Many people like to use Power Added Efficiency (PAE) instead of efficiency. The former does refer or include the input RF power and the later just refer to the ratio of the input RF power to DC power drawn from the supply, which is not considered a clear measure or metric of the performance of the power amplifier. High Power Added Efficiency and high linearity are figures of merits for power amplifiers. Unfortunately they are inversely proportional. Trying to increase one will result in decreasing the other and vice versa. For constant envelope applications, which use frequency modulated signals (like FM, FSK,), non-linear amplifiers can be used. And for varying envelope applications, which uses amplitude-modulated signals (like AM, ASK, ...), linear amplifiers can be used. Sometimes a compromise between efficiency and linearity has to be made according to the application.

1.4 Thesis Overview

This thesis report is detailing the design issues related to RF power amplifiers. Chapter 2 reviews definitions and many classes of linear and non-linear power amplifiers. Also it briefly reviews linearization techniques. Chapter 3 discusses the design architecture overview, which details the choice of process, circuit topology, and power amplifier class. Chapter 4 discusses power amplifier circuit design. Chapter 5 discusses the hot-carrier phenomenon and its effect on the power amplifier performance. Finally, chapter 6 is the conclusion.

2 BACKGROUND

2.1 Definitions and Terminology

Power Amplifiers (PAs) are used when the optimum efficiency and output power of an amplifying circuit are important considerations. The efficiency is a measure of the Power Amplifier's performance, the ratio of power delivered to the load, which is the transmitted power to the power consumed by the device. There are three different types of efficiency, which are described here.

The Drain Efficiency

$$\eta_{Drain} = \frac{P_{rf(out)}}{P_{DC}} \tag{2.1}$$

Where $P_{rf(out)}$ is the power delivered to the load at the desired operating frequency, and P_{DC} is the total power taken from the DC supply.

The Power Added Efficiency, or PAE, the most commonly used metric in industry and literature, is defined as:

$$PAE = \frac{P_{rf(out)} - P_{rf(in)}}{P_{DC}} \qquad (2.2)$$

Where $P_{rf(in)}$ is the power needed to drive the input at the frequency of interest.

Finally, the overall Efficiency is defined as:

$$\eta = \frac{P_{rf(out)}}{P_{DC} - P_{rf(in)}} \qquad (2.3)$$

Both the PAE and overall efficiency can give a clear measure of the performance of a power amplifier, since they include input driving power as a measure of the gain of the PA. And thus the overall efficiency can distinguish between two PA's with similar drain efficiencies but different power gains. It is obvious that the PA with the greater power gain will be the more efficient PA overall.

2.2 Power amplifiers configurations

Power Amplifiers can be divided into two main categories, linear and non-linear. The reason behind adopting this classification criterion is that there are mainly two modulation forms, varying envelope (Amplitude Modulation) and constant envelope (Frequency Modulation). For AM Systems, the amplitude of the

signal is of so much concern since the information is carried by the amplitude. That is why the linear power amplifiers types are being used with AM systems. On the other hand, for FM systems or constant envelope systems, the amplitude that is why non-linear PAs are being used with FM systems does not carry the information. Linear PAs are class A, B, AB. Non-linear PAs are class C, E, F, and S. Classes A, B, AB, and C can share the same circuit topology. The only difference is the biasing of the gate of the transistor. Figure 2.1 shows the circuit topology that can be used for class A, B, AB, and C. The RFC (Radio Frequency Choke) is working as a current source assuming it has a sufficiently large inductance.

2.2.1 Linear Classes of Power Amplifiers

2.2.1.1 Class A

Class A PAs is considered completely linear over the input and output range in the expense of low efficiency. So for the applications that the power is not a concern like having unlimited power source which is being used for example for in-the-house equipment. On the other hand, in the case of portable equipment, which uses limited power sources like batteries, the efficiency is an important issue. Since class A power amplifiers' maximum efficiency is 50% then for

example for every 1 Watt output power there is 1 Watt of dissipated power in the MOS transistor. Using other words, the battery power is wasted by 50%.

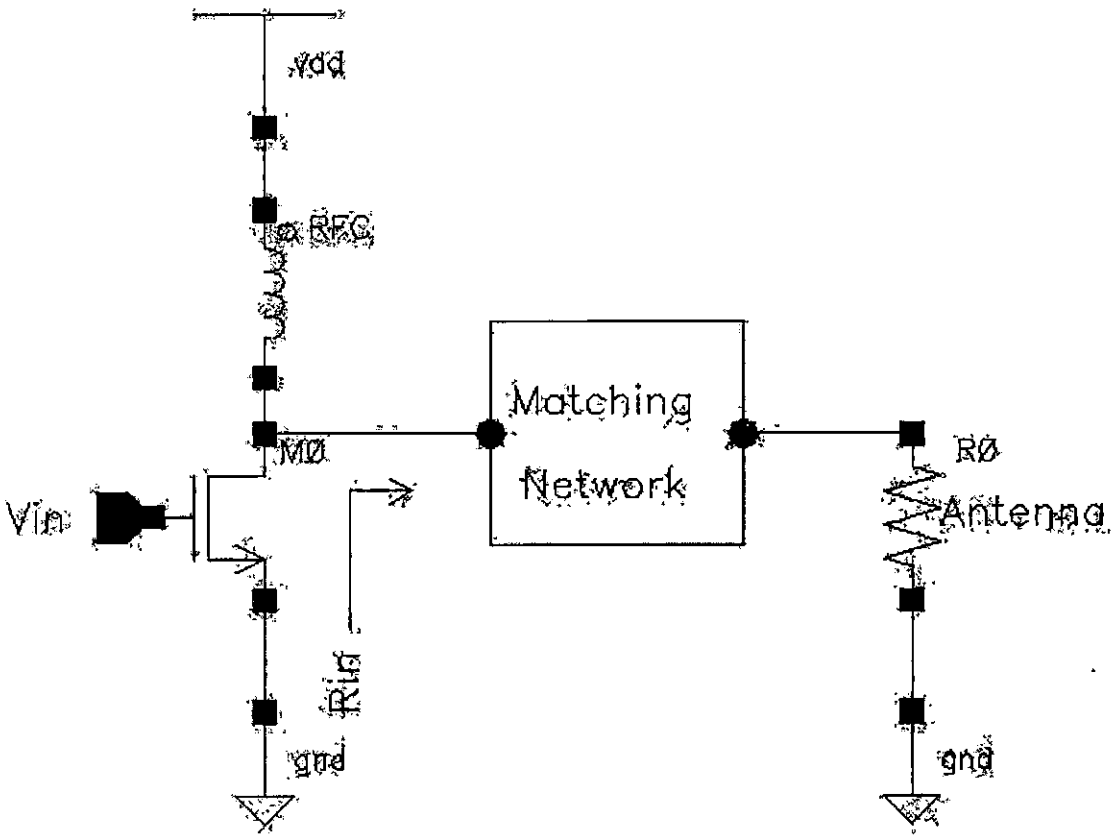
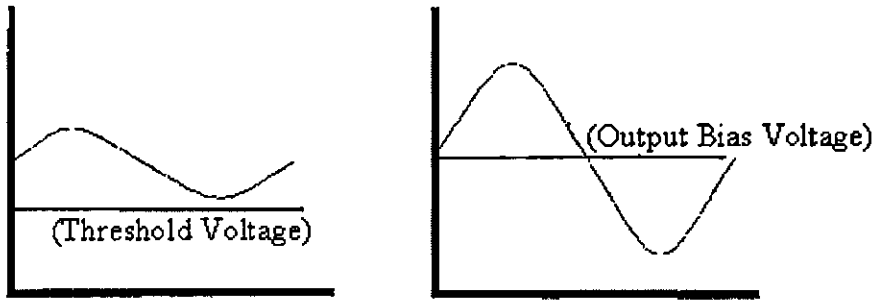


Figure 2.1 General circuit topology suitable for class A, AB, B, and C PAs.

Finally, that is why class A PAs are being used on applications where linearity is a very important factor and/or efficiency is not of a concern as mentioned before in the case of a limitless source. The input signal for class A amplifiers is always above the threshold voltage V_{th} of the MOS transistor enough to make it ON the whole cycle or 360° conduction angle which refers to the portion of the cycle where transistor is conducting and in this case (Class A), the transistor is conducting the whole cycle (see figure 2.2). Then maximum power dissipation occurs and then the lowest efficiency is obtained all classes of PAs. The efficiency of class A PA is given by:

$$\eta = \frac{P_{rf(out)}}{P_{DC}} = \frac{1/2(V_{DD}\hat{I}_o)}{V_{DD}\hat{I}_o} = 1/2 \qquad (2.4)$$

So η = 50% using an inductor connected to the drain of the transistor. If a resistance has been used instead, η = 25% since the voltage swing will be limited to $V_{DD}/2$ instead of V_{DD} in the case of using an inductor. Class A PAs reported in the literature have an efficiency, which is limited to 30% [4].



(a) Input voltage (b) Output voltage

Figure 2.2 Class A waveforms

2.1.1.2 Class B

It was clear that the reason behind low efficiency for class A amplifiers is that the transistor is ON all the time (360° conduction angle). In class B amplifiers, the conduction angle is 180° or the transistor is ON for half of the cycle only. This means that power dissipation through transistor is less. It can be proven that in the ideal case the efficiency of a class B PAs is 78% [5]. Figure 2.3 is showing the waveforms for class B amplifiers. The high efficiency for class B PAs comes with the cost of more distortion in the output. So linearity is sacrificed for increasing the efficiency. Practically, the efficiency of class B PAs may reach 60% using GaAs technology [6].

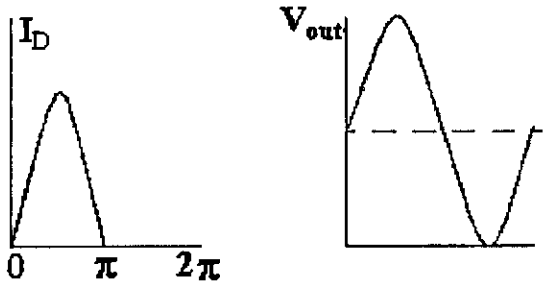


Figure 2.3 Class B waveforms

2.1.1.3 Class AB

Class AB amplifiers are something between classes A and B as its name reveals. By controlling the input bias level to be either close to class A biasing or close to class B biasing, the linearity and efficiency can be controlled. The conduction angle varies from 180° (class B case) to 360° (class A case). If class AB circuit is biased toward class A, more linearity and less efficiency will be achieved and vice versa if it is biased toward class B. This is useful if a compromise between linearity and efficiency is needed. Depending on the desired level of linearity and efficiency, class AB input bias point will be chosen. That is what made class AB popular among linear amplifiers. Several class AB PAs have been reported in the literature, with efficiencies between 30% and 60% [7], [8], [9], [10].

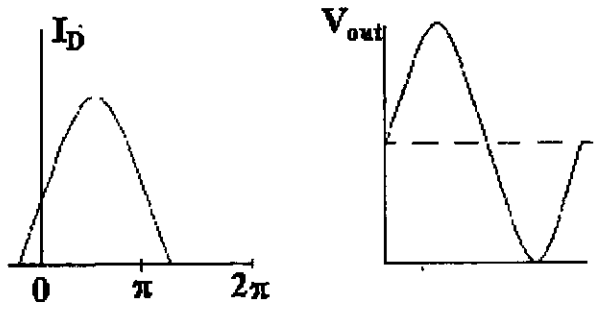


Figure 2.4 Class AB waveforms

2.2.2 Non-linear Classes of Power Amplifiers

The previous three classes A, B, AB are linear classes of Power Amplifiers. We are going to discuss the non-linear classes. In a communication system where the information is not contained in the amplitude, then we do not have to use linear amplifiers. On the other hand, the non-linear PAs offer some merits like efficiency enhancement, which is a very important factor in the PA world.

2.2.2.1 Class C

For class B amplifiers, the transistor conducts for half of the cycle (180° conduction angle). In class C, the transistor conducts for less than half a cycle (conduction angle $<$ 180°). The single transistor configuration that was used with class A, B, AB, can be used. The only difference is that the input bias level for the transistor is negative. By varying this bias level, we can get a conduction angle of 180° to 0° (see figure 2.5 for waveforms). So always for class C PA, the transistor

is conducting less than half a cycle. This will save some of the power dissipated in the transistor and in turn raise the efficiency which can reach 100% theoretically for a corresponding 0° conduction angle. The drain current is always positive or zero. In other words, the drain current is a piece of Sine wave when the transistor is ON, and zero when the transistor is cut off. Another thing about class C PA is that the transistor is assumed to behalf at all times as a current source, i.e. current through the device is independent of the voltage across the drain and source.

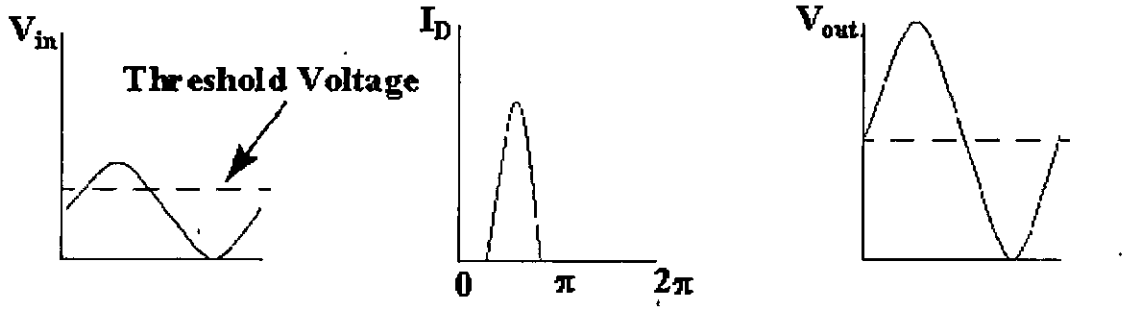


Figure 2.5 Input and output waveforms for class C PA

This means that MOS transistor should remain in its saturation region while it is ON. That is considered a considerable limitation, since V_{DS} of the device must be greater than $V_{GS} - V_T$. Since V_{DS} decreases as V_{GS} increases, this will set a limit on the maximum possible input voltage, which in turn will limit the amount of current swing. That is not good since the trans-conductance of MOS transistors is already

low and the only way to get a reasonable output current is to drive the transistor hard with a reasonable input signal level. Other thing is that by decreasing the input bias level, the efficiency increases and output power decreases till it reaches a point where efficiency is 100% and output power is zero, which is unacceptable (see equations 2.5 and 2.6 below [1]). That made class C not suitable for handset or any portable transceivers since the efficiency at full output power is of great concern [1].

$$\eta = \frac{1}{4}\frac{\theta - Sin\theta}{Sin(\theta/2) - (\theta/2)Cos(\theta/2)} \tag{2.5}$$

$$P_{out} \propto \frac{\theta - Sin\theta}{1 - Cos(\theta/2)} \tag{2.6}$$

There are a lot of harmonics have been generated from class C due to the distortion happened in the output waveform. The matching network resonates all such harmonics and presents the output as pure Sine wave to the load. As mentioned before, the efficiency of the device is less than 100% in the real case. However, the efficiency of class C PA can be 60% or higher which is better than of the linear case [11][12].

2.2.2.2 Class E

Class E stages are non-linear switching amplifiers that achieve efficiencies approaching 100% while delivering full power, which is a very good advantage over class C. In class E amplifier, the transistor works as a switch not like a current source as before. The idea of class E by using a switching transistor is to have current and voltage non-overlapped so there will be no power dissipation. But since the transistor is not ideal which causes some limitations in the turn on and off times and that becomes more of a concern at high frequencies. Figure 2.6 shows a class E stage. The values of C_1, C_2, L_1, L_2, and R_L are chosen such that V_D satisfies three conditions [1]: (1) as the switch turns off, V_D remains long enough for the current to drop to zero, (2) V_D reaches zero just before the switch turns on, and (3) dV_D/dt is also near zero when the switch turns on. The first condition, guaranteed by C_1, resolves the issue of finite fall time at the gate of the transistor. Without C_1, V_D would rise as V_{in} dropped, introducing substantial power loss in the transistor [1]. The second condition ensures that the voltage across and the current through the switch do not overlap in the vicinity of the turn-on point, thus minimizing the power loss in the transistor even with finite input and output transition times. The third condition lowers the sensitivity of the efficiency to violations of the second condition. That is if component or supply voltage introduce some overlap between the voltage and current waveforms, the efficiency

degrades only slightly because $dV_D/dt = 0$ means V_D does not change substantially near the turn-off point [1]. See figure 2.7 for class E waveforms [13]. The design equations are as follows [5]:

$$L = \frac{QR}{\omega} \tag{2.5}$$

$$C_1 = \frac{1}{\omega R(\pi^2/4+1)(\pi/2)} \approx \frac{1}{\omega(5.447R)} \tag{2.6}$$

$$C_2 \approx C_1(\frac{5.447}{Q})(1+\frac{1.42}{Q-2.08}) \tag{2.7}$$

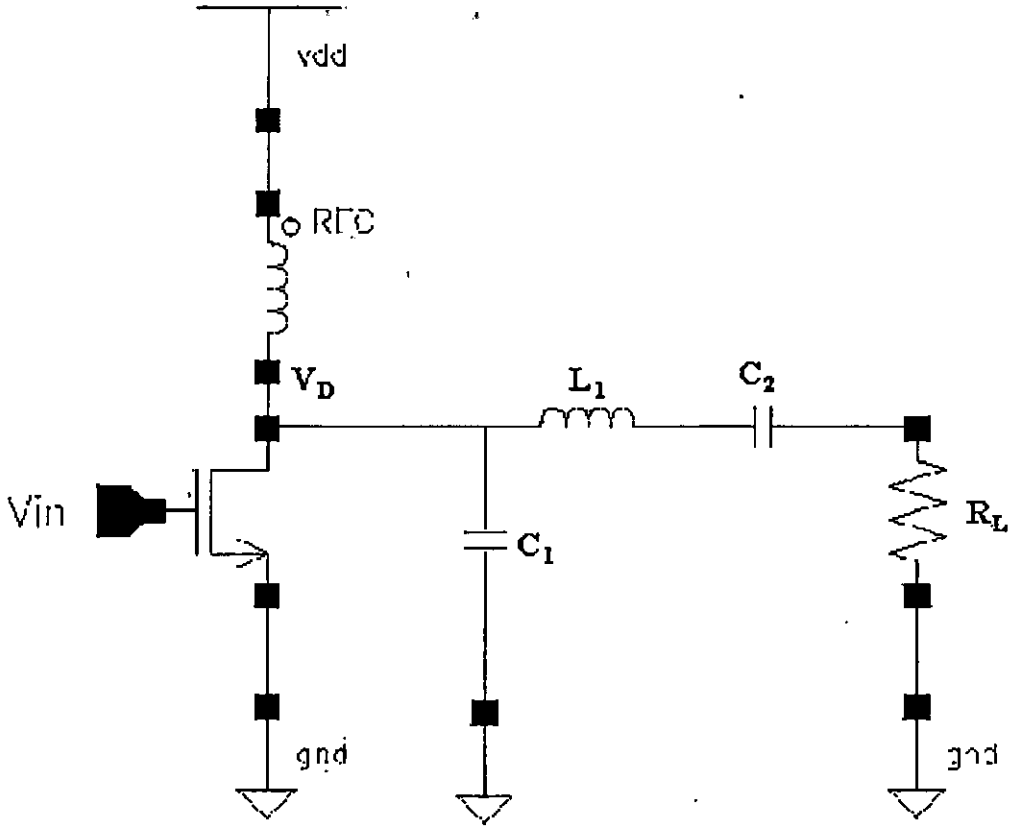


Figure 2.6 A class E stage

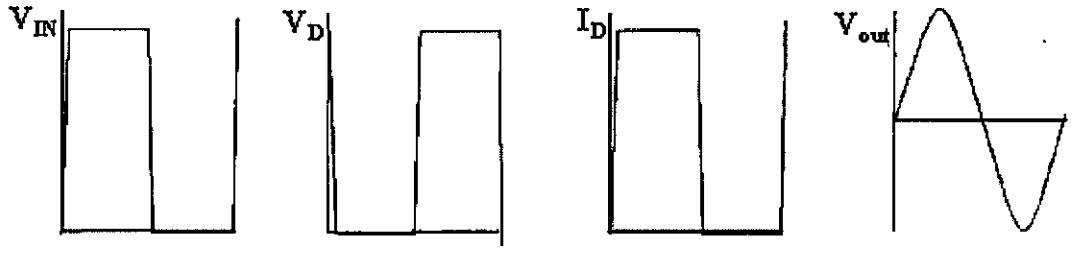


Figure 2.7 Class E waveforms

2.2.2.3 Class F

In class F stages, the output tank is tuned to resonate at the carrier frequency and is assumed to have high Q enough to act as a short circuit at frequencies outside of the desired bandwidth [5]. Figure 2.8 shows a typical class F stage circuit diagram. The L_1 and C_1 tank designed so that it will be tuned to the third harmonic. The L_2 and C_2 tank is tuned to the fundamental. The idea is that, the device will see a non-zero load impedance for both the first and third harmonics, and thus the waveforms at the output of the device will be the sum of the first and third harmonics of the fundamental frequency, which make up the first two terms in the series expansion of a square wave [13]. In this way, the output voltage waveform is closer to zero at the time when the current is flowing, decreasing the power lost through the device [13]. The waveform at the output is still limited to the fundamental frequency, since the impedance at the actual output is tuned to the fundamental. See figure 2.9 for class F waveforms.

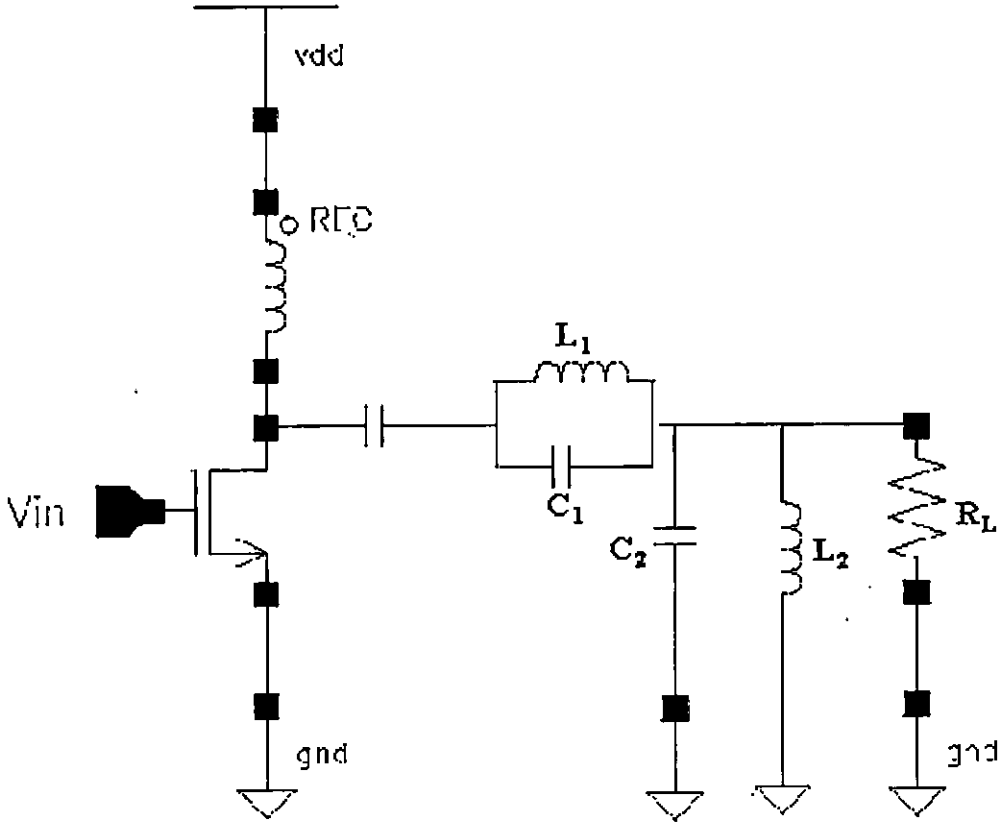


Figure 2.8 A typical class F stage circuit diagram

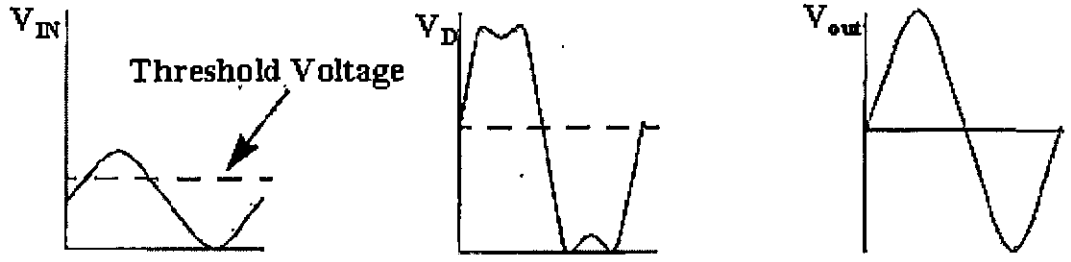


Figure 2.9 Class F waveforms

2.3 Linearization Techniques

Linear power amplifiers are needed in many applications. Specially, the applications that use AM type modulations (varying envelope). Now most linear PAs used in portable devices have class A as the output stage and hence the efficiency is 30-40% [1]. To apply linearization techniques, it is possible to start with a completely non-linear amplifier and use a linearization technique. But that is not possible since most of the linearization techniques require some linearity in the amplifier to build on. The linearization techniques described below have occasionally been utilized in complex, expensive RF and microwave systems, but they have not yet found their way into low-cost portable terminals [1]. This is because such methods complicate the design, require a lot of adjustments, and become less effective as device characteristics change with temperature and output power. But it is beneficial to understand these techniques and their limitations since it aids in the PA design, especially IC technology is offering high level of reproducibility than in discrete circuits.

2.3.1 Cartesian Feedback

Cartesian feedback uses the idea of feeding back the output of the amplifier after translating the signal frequency down to the I & Q signals so it can adjust the signal level for the I & Q in order to provide the correct signal level at the output which is similar to closed loop control system. The only thing that might cause worry is that in this way the forward gain of the amplifier will be less, which is undesirable. Since Cartesian feedback is doing negative feedback at low frequency, so this problem does not exist. As a result, the PA is appearing to operate in an open loop way, so gain reduction with negative feedback will not occur. The standard block diagram for Cartesian feedback is shown in figure 2.10 [13]. As we can see from the block diagram, the linearization works around the entire transmitter, not just the PA, and this is not direct linear feedback at the PA's operating frequency. The baseband signal will go through D/A and then a modulator and up-converter. The RF signal is amplified through the PA. An attenuated version of the PA output is demodulated and down-converted to be subtracted from the analog versions of the I & Q signals. Cartesian feedback in literature have been seen to provide as much as 50 dB of linearization; i.e. the magnitude of undesired spectral components adjacent to the desired signal, due to inter-modulation, spectral re-growth, or other phenomena, has been reduced by 50 dB or more through this technique [14].

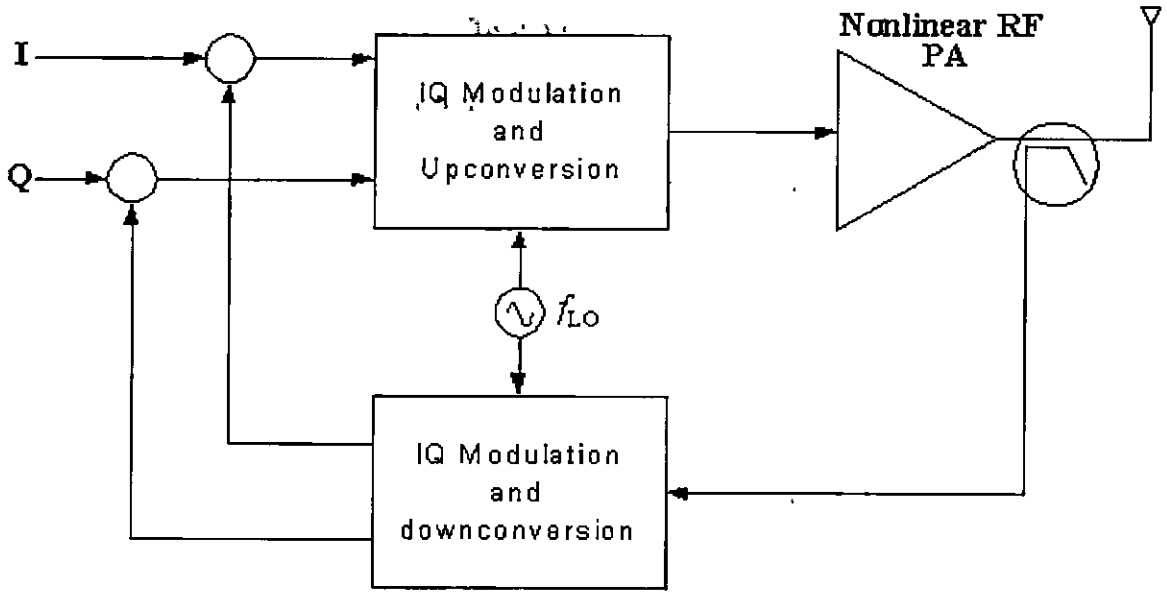


Figure 2.10 A block diagram of cartesian feedback linearization technique

However, there are some limitations to that technique. The linearization is good only when the matching of both gain and phase between the up-converting modulator in the forward path and the down-converting modulator in the feedback path takes place. Moreover, the stability of the loop must be guaranteed, which sets tight requirements on the loop gain and loop bandwidth [14]. Both of these affect the amount of linearization provided as well as the available linearizing bandwidth [13].

2.3.2 Pre-distortion and Adaptive Pre-distortion

The pre-distortion is similar to the cartesian feedback in which it is feeding back the output of the PA but one further step in the transmitter chain. The pre-distortion makes use of a DSP by storing known pre-distortion coefficients in a lookup table, which are then used to pre-distort the input digital bit stream to create a signal that will generate a linear representation of the desired input. The coefficients are generated based on the known distortion characteristics of the PA. Adaptive pre-distortion differs from Cartesian feedback in that it periodically senses the PA's output in order to update the coefficients in the DSP for any time-varying non-linearities in the forward path. Because the feed back loop is only closed at selective times, the linearized transmitter is essentially open loop and can be viewed as unconditionally stable [15]. The block diagram of pre-distortion technique can be seen in figure 2.11 [13]. It can be seen that this method is somewhat similar to the cartesian feedback when in its adaptation mode, but that the signal fed back is converted to a digital representation using an A/D converter and compared to the bit stream in order to update its pre-distorter coefficients. While the linearization is not being updated, the transmitter is strictly an open loop, and thus the stability is not an issue. The digital I and Q channel bits are combined in order to generate an exact 1-to-1 mapping between the digital complex plane and the RF output plane, or possibly combining the I and Q bits to

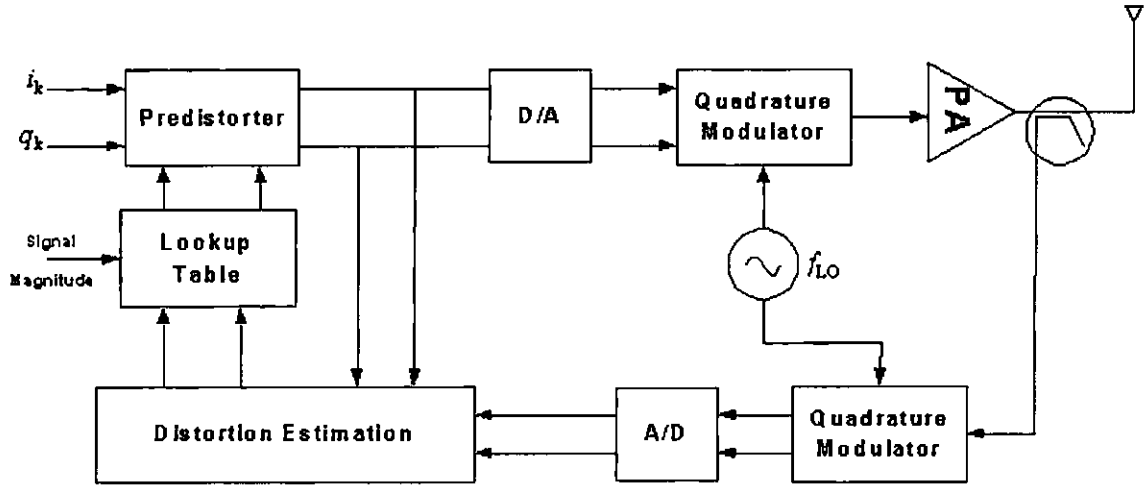


Figure 2.11 Block diagram of pre-distortion technique

generate an effective signal magnitude [16]. The later can give a significant smaller lookup table [13]. Practical considerations can set bounds on the amount of linearization attained through this method. The amount of linearization can be limited by the sampling frequency of the digital input bits. The linearizing bandwidth should nominally be limited by the sampling frequency of the input, due to the Nyquist sampling criterion. Reduction of the sampling frequency can cause limited linearization in higher order products, with the linearizing bandwidth decreasing as the sampling rate decreased [16]. In addition to that, when the feed back loop is active for coefficients adaptation, extremely tight control must be maintained in order to correct adaptation. Clearly since the feed back is periodic and not continuous like in the cartesian feed back case, the amount of errors in the

adaptation loop introduced by the loop components will be reflected directly in the updated coefficients [13]. These techniques have demonstrated reduction in IM components by more than 50 dB for the systems in which they were implemented [15][16]. However, one important disadvantage of this technique is that it uses a DSP, which consumes power reducing the overall efficiency of the system. So a compromise between linearity and efficiency has to be done.

2.3.3 Feed Forward

This method does not use the idea of feedback; it uses a feed forward technique to linearize the PA output. The block diagram is shown in figure 2.12.

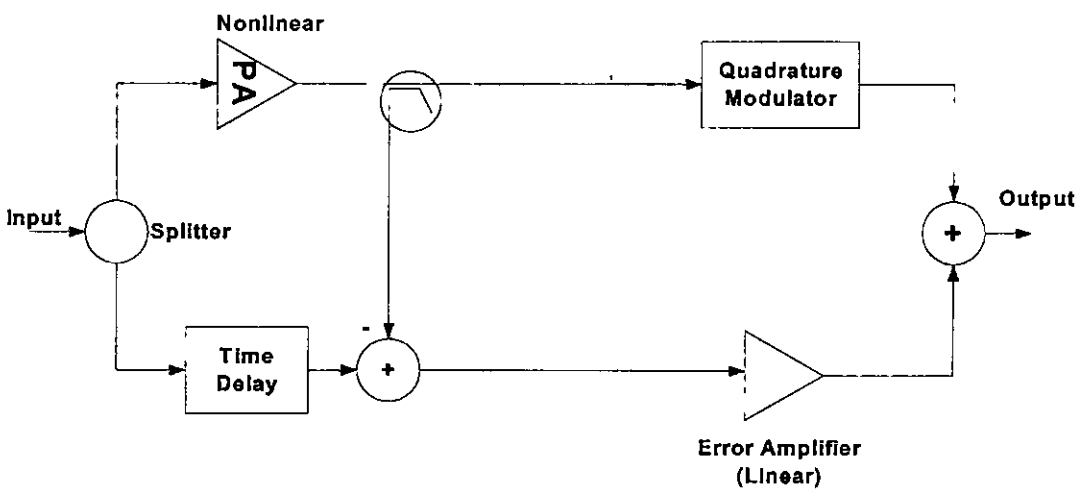


Figure 2.12 Block diagram of feed forward technique

As shown the RF input splits into two paths. The first path contains our PA under linearization. Then an attenuated version of the non-linear amplifier signal subtracted from a delayed version of RF input to obtain the unwanted harmonics, which in turn will be subtracted from a delayed version of the RF amplifier output, to equalize the delay in the error amplifier, to get a nice linear representation of the input. Since feed forward is an open loop technique, so it will never suffer from any stability problems. On the other hand, the delay blocks have to match the corresponding circuit in the other path otherwise poor distortion cancellation can occur. In addition to that, efficiency degradation could be a problem since a linear PA is being used in the feed forward path, which consumes some power, but it is not a lot. Since power gain required to amplify the error signal is not large and thus the power consumed may be small. Still feed forward is a valuable technique. The literature indicated linearization up to 60 dB in a high power system [17].

2.4 Conclusion

The above discussions, while not entirely relevant to the final outcome of thesis report, are of crucial importance in the study of PA's. The different types of PA's and which method might be used to linearize them can be very beneficial in the design process, as meeting the needed specifications with minimum power consumed is a critical consideration.

3 DESIGN ARCHITECHURE OVERVIEW

3.1 Choice of Process

It is very clear that GaAs is dominating the market for Radio Frequency PAs especially on the board level. Since it allows for tuning for maximum output power at the desired frequency. The GaAs process got its advantages from the fact that it allows for higher gain than CMOS for a given frequency and feature size. GaAs also has a good high frequency performance, which means that with a small input signal, a certain output level can be obtained, which increases both the power gain and PAE (Power Added Efficiency), which are key parameters in the PA arena. Also, good high frequency performance means that lower parasitics and in turn lower wasted power in the parasitics since simply f_t is approximately g_m/C_{gs} . Those mentioned reasons above made the GaAs process dominating the PA market even GaAs process is more expensive than CMOS and in a time where the cost is an important factor in judging a product. However, a lot of research is focusing on the CMOS process for PAs. One reason behind that is CMOS is cheaper than GaAs. Also, another important reason is that CMOS offers

integratability with the rest of the transceiver blocks on one chip, which makes it attractive. Especially with the recent advances in wireless communications market. For example the GPRS (General Packet Radio Service), which is dealing mainly with data services, like internet access, data management, and remote access to PC. Another reason that made CMOS under research spotlight is for smaller feature size CMOS gets faster and the high frequency performance gets better (remember f_t dependence on parasitics as mentioned earlier). Finally, when we look at the challenges in the ongoing research for the realization of a fully integrated single-chip transceiver in CMOS, two challenges remain. One is the integration of the power amplifier with the rest of the transceiver blocks and that is because the PA consumes too much power, which degrades the overall efficiency of the system. The efficiency can be improved using non-linear PAs like class E which suffers from serious linearity problems. An evolution of this type of power amplifiers is however inevitable [18]. A second challenge that remains is the coupling via substrate and substrate coupling package between analog and digital circuitry placed on the same die. This is in fact a general problem common to all mixed-signal chip realizations and a lot of research is being done on this topic today [19]. It is however often overlooked that this coupling is not as disturbing for RF applications as it is for other mixed-signal applications. The specific nature of wireless communication (a very small bandwidth signal situated at a high

operating frequency) makes that its analog part is only sensitive to a very small part of the digital switching noise that is coupled in. Problem is that presently no tool is available yet with which the level and spectral distribution of coupled-in digital noise can be predicted. A designer still has to choose the safest solution, the integration of analog and digital circuitry on a different die, while this may not always be necessary for RF applications [18].

3.2 Choice of Power Amplifier Class

There are several factors which go into the class of PA, most of which depend on the communication system for which the PA is being designed. The PA must output a certain level of power. It must also be able to meet the time-domain and frequency-domain transmit masks. In these considerations, the issue of meeting the transmit masks plays an important role in determining the class of PA to use [13]. First, we start with efficiency. To get the highest efficiency we should consider non-linear PAs. But non-linearity can cause the output signal to spread (due to inter-modulation products, in addition to that the input signal might be spread out due to a lot of phase noise in the local oscillator). The spreading of output can cause some problems that contradict with time-domain and frequency-

domain mask requirements. Another point is that the transmitted signal still must meet the spectral mask, which could be difficult for a non-linear amplifier. Since this was first time to try to design a PA, so it was better to be more careful and choose a linear amplifier topology. Another important point that finally confirmed the use of a linear PA is that it was unclear if the existing models is accurate and dependable for modeling switching behavior for high frequency non-linear PA. So a linear PA has been chosen in the sense of security in the models. The next step is to determine which class of linear PAs should be chosen. By reviewing class A, B, AB it can be found that class AB allows for a compromise between linearity and efficiency and actually we can change the class of the PA by just changing the input bias level. Finally class AB has been chosen.

3.3 Choice of Circuit Topology

3.3.1 Multi-Stage Design

Using one stage amplifier will not provide enough gain. The solution is to use multi-stage design. The transistor in first stage has to be sized so it will not load previous stage. Also last stage transistor has to be sized to fulfill output power drive requirement. So we have many stages that are gradually increasing in

size. To determine how many stages should be used, a compromise has to be done. Increasing number of stages will increase DC power drawn from the supply. On the other hand, using small number of stages might not be sufficient to get required overall gain. Most power amplifiers use a two-stage configuration, with matching networks placed at the input, between the two stages, and at the output (see figure 3.1).

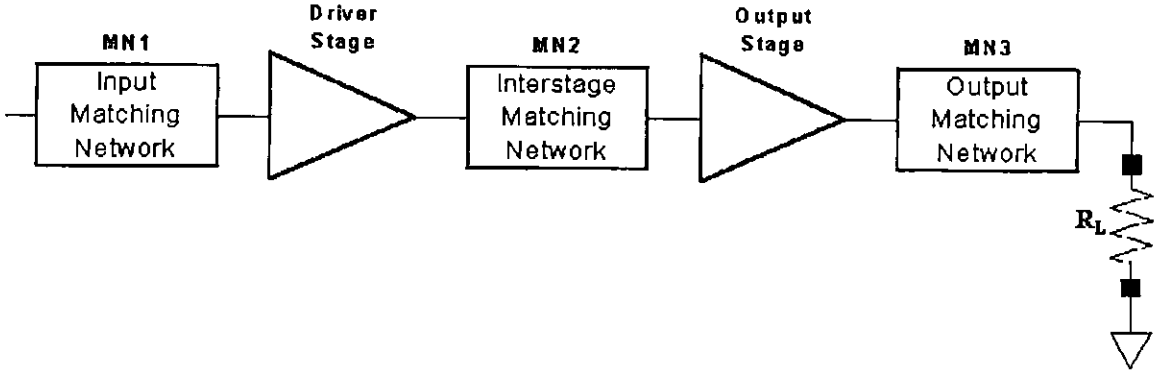


Figure 3.1 Multi-stage power amplifier circuit

The input-matching network (MN1) transfers 50Ω impedance to the input impedance of the driver stage. The output-matching network is designed so as to deliver the required output power from the output stage to the load resistance R_L. First, output stage and output matching network are designed using load-pull techniques. Also input stage and input matching network are designed. Then

comes the inter-stage matching network to match output impedance of first stage (driver stage) to the input impedance of output stage.

3.3.2 Single-Ended Topology

Most Power Amplifiers available are using single-ended topology because most standard antennas need to be driven by a single-ended signal. On the other hand, we have differential topology which is suitable in implementing class AB amplifiers with the cost of doubling number of transistors and the need of transforming differential signal to single-ended as required by most standard antennas as mentioned earlier. Differential topology has some advantages to offer. The voltage swing at every node in the circuit is cut in half. Also differential architecture is immune to common-mode (CM) noise.

Finally, single-ended topology has been chosen since it uses one transistor per stage and the output of the power amplifier will directly drive the antenna. Among the three transistor amplifier configurations, the common-source topology provides the highest efficiency. In common-gate circuits, the output current equally flows to the input network, introducing substantial loss. And in common-drain stages, a bias current in addition to the load current is required, lowering the efficiency by approximately a factor of 2 [1]. Finally, common-source configuration has been chosen.

4 POWER AMPLIFIER CIRCUIT DESIGN

4.1 Introduction

Before starting circuit design for our Power Amplifier, some issues need to be discussed. The first issue is stability. Stability is a very important issue in designing amplifiers generally and RF Amplifiers specifically. It happens due to some feedback from output to input. One famous reason is the feedback occurring due to C_{gd} (Gate to Drain Capacitance), which can be decomposed using Miller method into two separate capacitances at the gate and the drain of the transistor. The capacitance at the gate resulted from the Miller method increases the input capacitance, which makes it more difficult to drive the transistor specially in the case of switching mode PAs where the driving signal is a pulse. Other reasons for instability are the feedback due to external circuit elements. Since the reactance of Cgd decreases as the frequency goes up, the probability of oscillation is more in RF amplifiers [20][21].

The main target of RF Power Amplifier design is to achieve maximum output power with a predictable stability [20]. The first step in RF Power Amplifier design is to determine the stability factor (K) versus frequency. The stability factor (K) is a measure of the stability of the amplifier [21][22]. (K) can be derived basically from simply stability rules, which mention that input and output reflected power must always be less than incident powers. Knowing that the ratios of the reflected power to the incident power at input and output are called input and output reflection coefficients respectively ($S_{11}^{'}$ and $S_{22}^{'}$) represented in terms of the scattering parameters. Scattering parameters has no dimensions and they represent the ratios of powers for matched terminated input and output [21][22].

Input and output reflection coefficients for unknown terminations are defined as:

$$S_{11}^{'} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{12}\Gamma_L} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.1}$$

$$S_{22}^{'} = S_{22}^{'} + \frac{S_{12}^{'}S_{21}^{'}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - D\Gamma_G}{1 - S_{11}\Gamma_G} \tag{4.2}$$

$$D = S_{11}S_{22} - S_{12}S_{21} \tag{4.3}$$

Where Γ_L and Γ_G are respectively the load and generator reflection coefficients.

For unconditional stability, the following condition must occur:

$$\left|S_{11}^{'}\right| < 1, \left|S_{22}^{'}\right| < 1 \tag{4.4}$$

(K) can be obtained by mapping $S_{11}^{'} = 1$ in the Γ_L plane, $S_{22}^{'} = 1$ in the Γ_G plane and algebraic manipulation of equations 4.1, 4.2, and 4.4

$$K = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 - \left|D\right|^2}{2S_{12}} \tag{4.5}$$

For unconditional stability, stability factor (K) should be greater than unity (K>1) [21]. Microwave devices like GaAs MESFET which are generally used in high frequency design are measured for S-parameters thus, gain and stability of a single device are usually known to the designer prior to the design. The measured results however, mainly relate to the small signal S-parameters but for high power, high efficient designs, the large signal parameters of the transistor must be obtained [3]. For class A, B, AB, or C, the small-signal S-parameters become progressively less useful [21].

4.2 Output Stage

4.2.1 Transistor Configuration In The Output Stage

The most important stage of a Power Amplifier is the output stage. This stage should be able to produce enough output power to drive the antenna through a well-designed matching network to minimize reflections and in-turn minimizes power loss. In our design, an open drain output stage was simulated in class AB biased with 1 volt DC input level. As illustrated in figure 2.1, the active device is used in a common-source configuration with an off-Chip RF choke connected to the drain for biasing purposes. The RF choke functions like a current source. The advantage of the RF choke over an active on-chip current source is that it does not impose any limit on the drain voltage swing of the transistor. So the drain voltage can go higher than the supply voltage so achieving higher efficiency. A RF choke is also used instead of a small inductor to minimize the ripples of the current drawn from the supply (RF supply currents) that makes the RF choke works as an ideal current source as possible. Placing the RF choke off-chip helps minimizing losses and chip area since it is easier to build an RF choke using a strip line on the circuit board. This does not violate our need for high integration since the output signal from Power Amplifier will go off-chip to drive the antenna anyways.

The output power of an output stage is lowered by many factors. It is a direct result of lower transconductance g_m of the MOSFETs compared to the microwave devices, lossy substrate, gate poly resistance, and parasitic junction capacitances of the device to the silicon substrate (figure 4.1) [3].

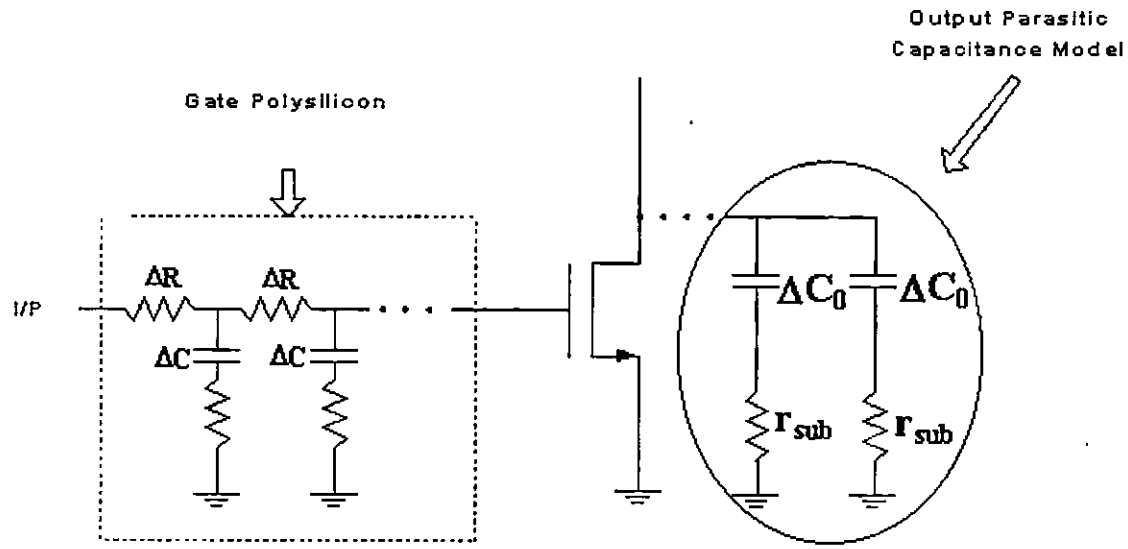


Figure 4.1 Input impedance and output junction capacitance model of device.

In many high frequency circuits, the output capacitance carries a considerable amount of the output current when the transistor is "Off". Putting in mind that the output capacitance is in series with substrate resistance, this results in substantial power dissipation for CMOS. To achieve an output power of 2.0 Watts, a device size of (8 mm X 0.35 μm) was chosen.

4.2.2 Optimum Load Resistance Determination

4.2.2.1 Conjugate match

In conjugate match, a generator, as shown in figure 4.2 below, delivers maximum power into an external load when the load resistance is equal to the real

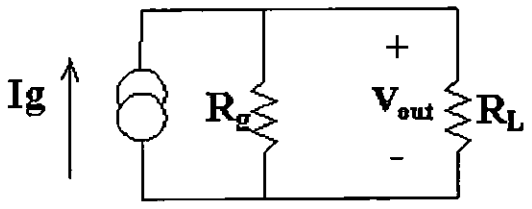


Figure 4.2 Schematic showing generator along with the load

part of the generator impedance, assuming that any reactive component has been resonated out. But there is an important point needs to be considered here. What if a true or real device has replaced the ideal generator specially if it is a transistor? The transistor (can be considered real-world generator) has physical limits, both in terms of the current it can supply and the voltage it can maintain across its terminals [23]. For example, if the current generator can supply a maximum of output current of 1 ampere and has an output resistance of 100 Ω. By applying the conjugate match concept, a load of 100 Ω would lead to maximum power transfer. But the voltage across the generator terminals is 50 Volts. If the current generator

is the output of a transistor, this voltage level exceeded the maximum voltage V_{max} of the device. In addition, the transistor voltage would be limited by the dc supply. On the other hand, the output current of the device will be less than its maximum value I_{max} (see figure 4.3 below) [23].

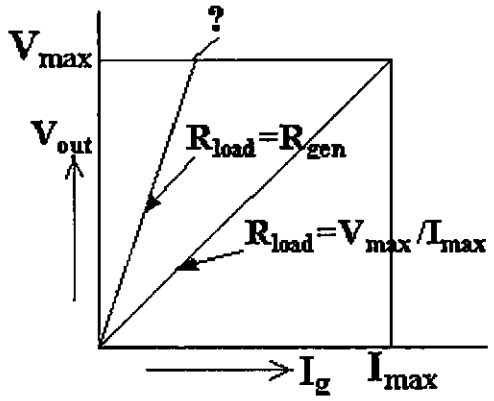


Figure 4.3 Output voltage versus current for a conjugate and load line match.

This means that the transistor is not used to its full capacity. This leads us to another type of match, which is the load line match.

4.2.2.2 Load Line Match

To get the maximum current and voltage swing of a transistor, a lower value of load resistance would need to be selected. This called the load line match or the optimum loading resistance R_{opt} and simply is defined as:

$$R_{opt} = \frac{V_{max}}{I_{max}} \qquad (4.5)$$

The determination of optimum loading at maximum output power becomes more difficult as circuit non-linearities increase [21]. There are several techniques for determining the optimum loading (R_{opt}) of the amplifier, one of them is the load line approach shown in figure 4.4 below.

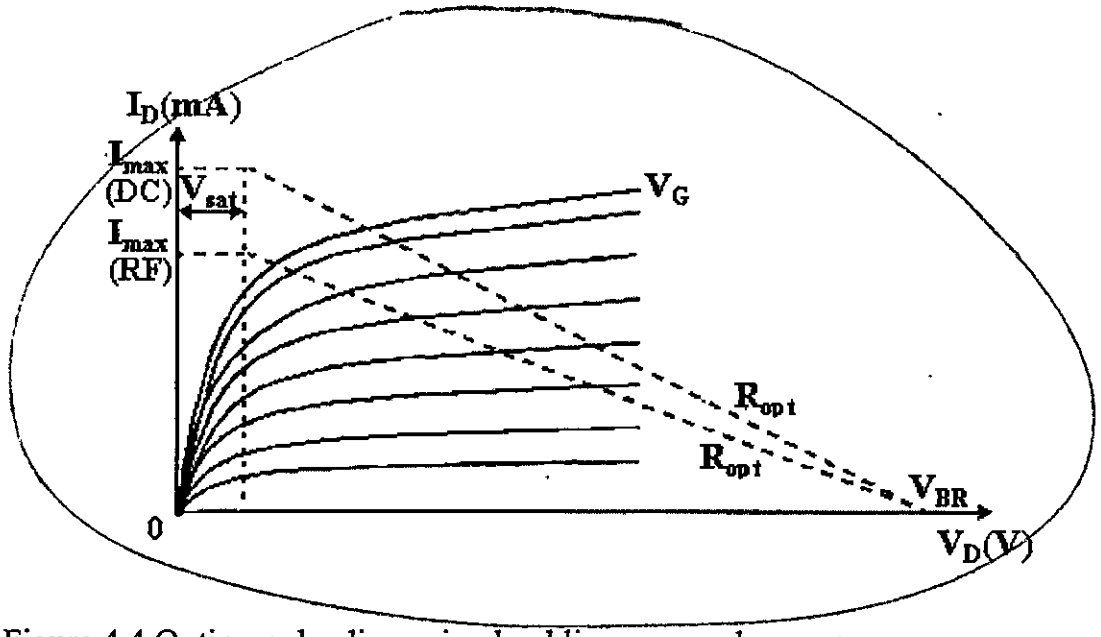


Figure 4.4 Optimum loading using load line approach

In this method, the operating point of the transistor is approximated by a straight line extending from the maximum current point, on the drain current axis, to the maximum voltage point on the drain voltage axis, on the transistor curves as shown in figure 4.5. The slope of the straight line corresponds to the optimum

loading (R_{opt}). The most accurate approach is with the use of a non-linear simulator, provided that the device is properly modeled [21]. In our case, the maximum output power of the output stage transistor can be achieved by terminating the output device with a load equal to the optimum load resistance of the transistor. The easiest method was used to find the optimum load using Cadence SPECTRE simulator. In SPECTRE simulation, the biased output stage was driven using the preamplifier that generates the actual driving signal of the output stage. The average input driving signal was found and later used to calculate the average output impedance, which is the optimum load for the device. The optimum load was found to be 1Ω for a device size 8mm X 0.35μm. The output parasitic capacitance as well as pad capacitance was ignored in this simulation to be absorbed by the matching network later for better efficiency. Consequently, a load equal to the optimum load of the device will allow the highest output power in the load.

4.2.3 Output impedance matching network

The output-matching network mainly should be able to transform the antenna resistive load (for simplicity) to the optimum load of the output transistor to achieve maximum output power. Other functions are to absorb and resonate reactive elements, to block DC, and in the case of input matching network for the

preamplifier stage and inter-stage matching, we add the function of biasing the gate of the transistor. To achieve all the functions mentioned above, a π-matching network has been used a long with a DC blocking capacitor as shown in figure 4.5 below.

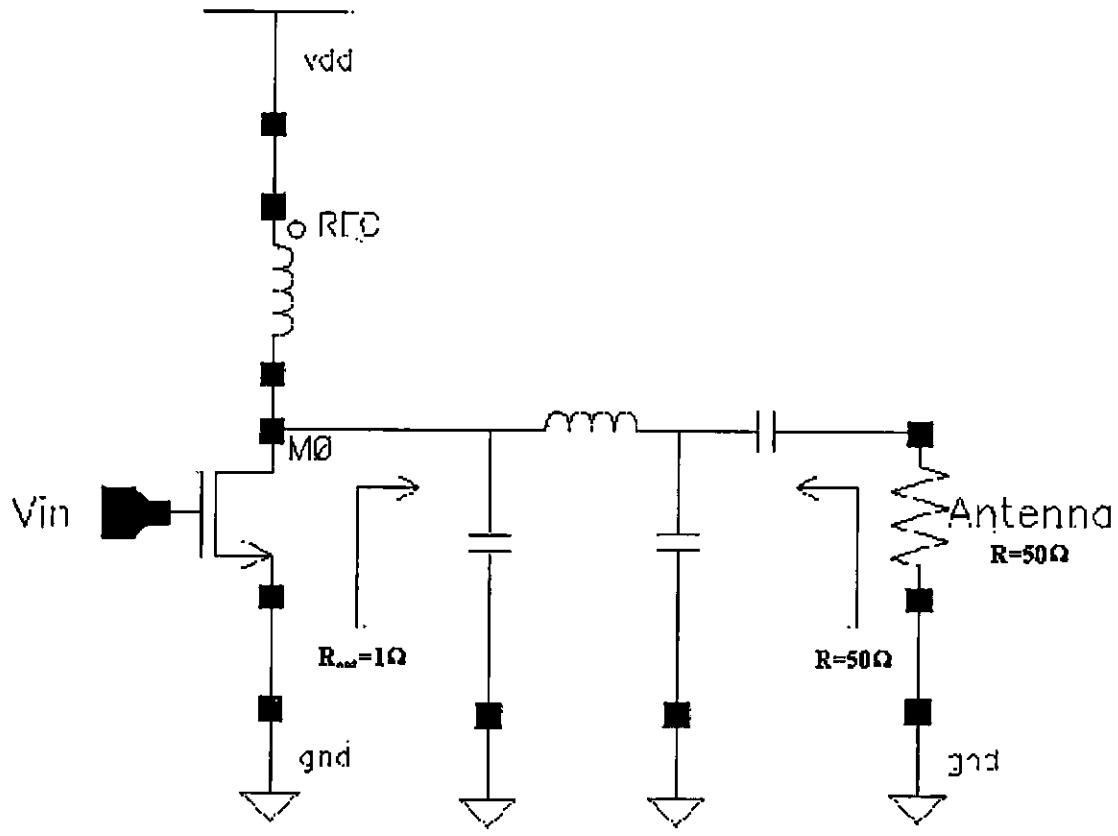


Figure 4.5 Output matching network.

A L-match has been used for input matching for the preamplifier stage and inter-stage matching. One limitation of the L-match is that one can specify only two of

center frequency, impedance transformation ratio, and quality factor (Q) [5]. To acquire a third degree of freedom, a π-match is used in the output-matching network. One important thing of the π-match is that it provides wider bandwidth, which is needed at the output stage due to the spreading of the signal and/or spectrum shifting away from operating frequency. The π-match can be considered as cascade of L-matches as shown in figure 4.6 below.

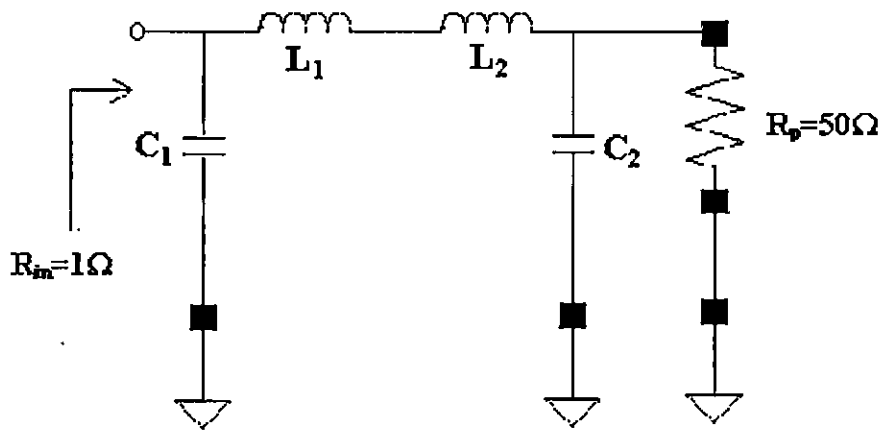


Figure 4.6 π-matching network used in output matching network.

One L-match transforms down and the other one transforms up. The load resistance R_P that is the antenna load (50Ω) in our case is transformed to lower resistance called the image or intermediate resistance R_I at the junction of the two inductances. A second L-match section transforms the image resistance up. The equations used to design our π-match are as follows [5]:

$$R_I = \frac{\left(\sqrt{R_{in}} + \sqrt{R_P}\right)^2}{Q^2} \tag{4.6}$$

$$C_1 = \frac{Q_{left}}{\omega_0 R_{in}} \tag{4.7}$$

$$C_2 = \frac{Q_{right}}{\omega_0 R_P} \tag{4.8}$$

$$L = \frac{QR_I}{\omega_0} \tag{4.9}$$

The values of C_1, C_2, and L are found to be 425pf, 63.9 pf, and 150pH.

4.3 Pre-amplification Stage

Now, the output stage and output-matching network have been designed to get the desired output power level. It is the turn now for the pre-amplification stage to be designed. The previous stages of the PA is either an up-conversion mixer or a transmit filter. The first stage of the PA should be sized reasonably not to load the previous stage and in the mean time get the required or sufficient

power gain to be able to drive the output stage. After doing many simulations, it was found that a 1mm X 0.35μm transistor would suffice.

4.3.1 Optimum Loading

Using SPECTRE simulator to determine the optimum load using load line matching technique, it was found that the optimum loading $R_{opt} = 9.9\ \Omega$.

4.3.2 Design of Input Matching Network

As discussed earlier, the matching network has to satisfy certain criteria. It has to provide impedance transformation to get maximum output power. Also, it provides biasing to the next stage if it is an amplifying stage. In addition to that, it provides DC blocking. Our proposed matching network is a low-pass matching network, which consists of a series capacitor, which will fulfill the criterion of DC blocking and an inductor, which is connected to a bias supply source to bias the gate of the transistor. The inductor works as a biasing element. In the mean time it is (the inductor) a part of the matching network (see figure 4.7 below). In this case smith chart has been used to design the input-matching network. The input-matching network transforms input impedance of the transistor represented by S_{11} or input reflection coefficient to 50Ω source impedance. The values of L and C found to be 4.274nH and 1.016pf.

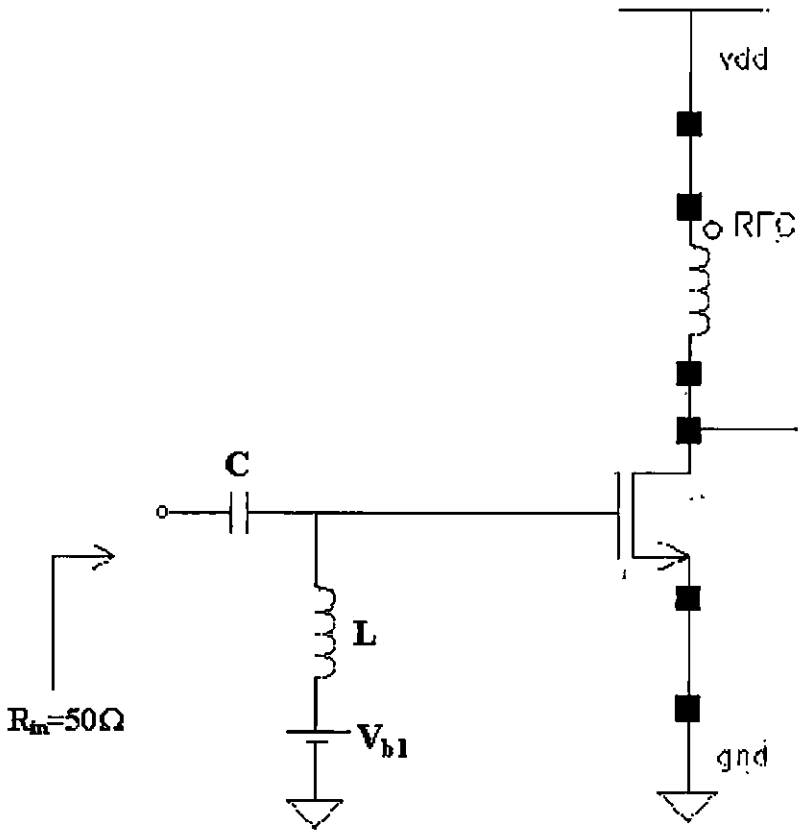


Figure 4.7 Input matching network.

4.4 Inter-stage Matching Network Design

Finally, the last part of the PA to be designed is the inter-stage matching. Without the inter-stage matching, the driver and the output stage must be treated as a single circuit, substantially complicating the design procedure. The L-match or the simple low pass network has been incorporated here for the inter-stage matching. As discussed before, it provides impedance transformation (in our case between input of output stage transistor and output of the driver stage). Also, it provides biasing for output stage through the biased inductor and DC coupling through the series capacitor. Smith chart has been used again to design the inter-stage matching. L and C values were found to be 1.345nH and 9.147pf.

4.5 Final Circuit

The final complete circuit is shown in figure 4.8 including bias levels for each stage, choke values, and matching networks components values.

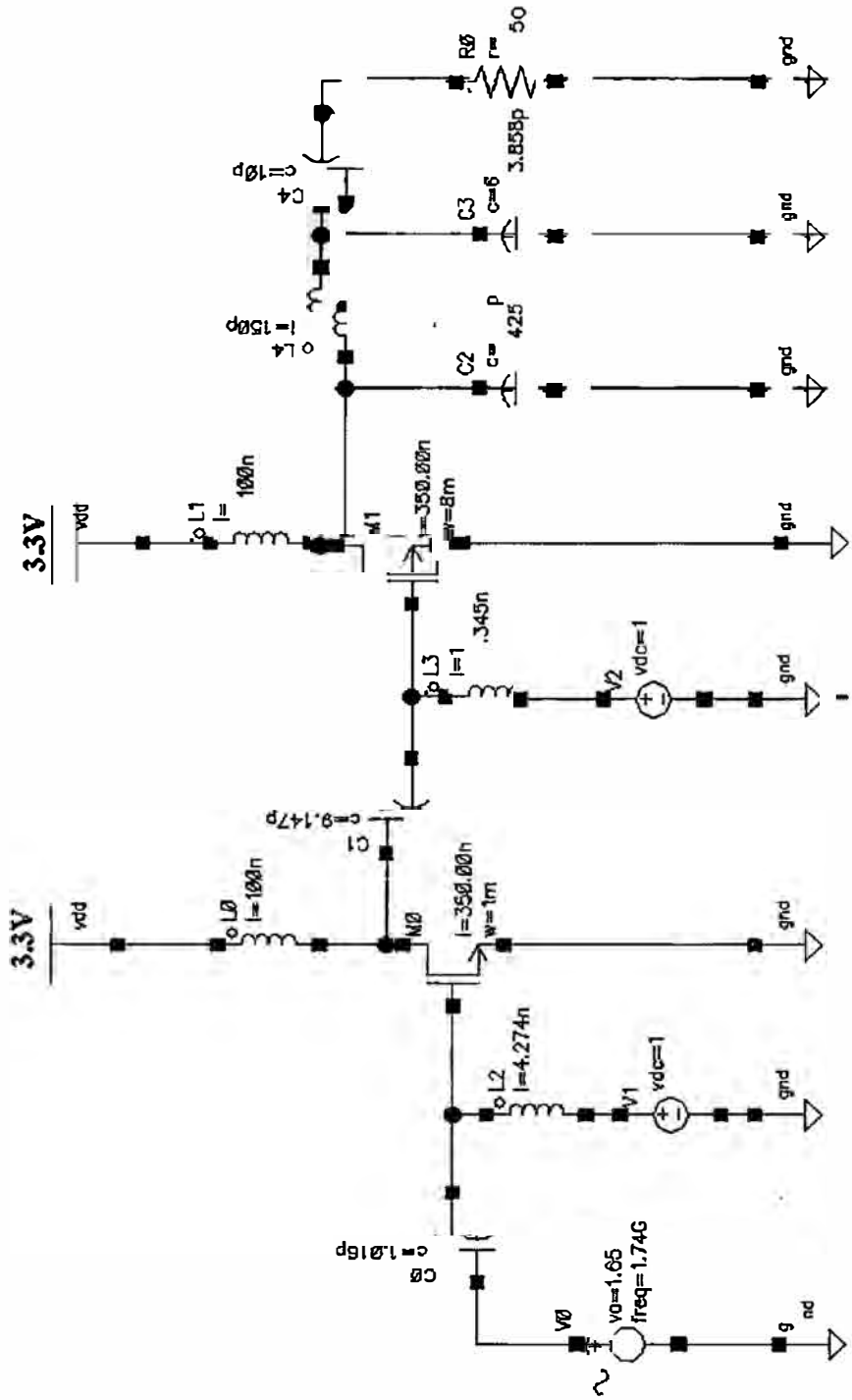


Figure 4.8 Final circuit including all values of components.

4.6 Simulation Results

The circuit simulations were done using SPECTRE circuit simulator (from Cadence Design Systems). The model was used is TSMC 0.35 μm mixed-signal BSIM3V3. The simulations were run on the circuit level. All simulations were run with an input signal at the desired frequency, which is 1.74 GHz. Many simulations were run versus frequency and supply voltage. The maximum output power at 1.74 GHz is 2.3 Watts (33.63 dBm) with a PAE (Power Added Efficiency) of 47% for a bias level of 1 volt for both stages. Below are some of the graphs that show output power and PAE versus frequency and supply voltage. The performance achieved can be considered great even after laying out the circuit, which will contribute to some losses like substrate resistance effect, poly silicon gate resistance loss, passive components loss. Still the power level and PAE achieved looks fine. This circuit can be used in many communication standards especially with GSM standards, which requires 1 Watts of output power for GSM-1800 and 2 Watts of output power for GSM-1900.

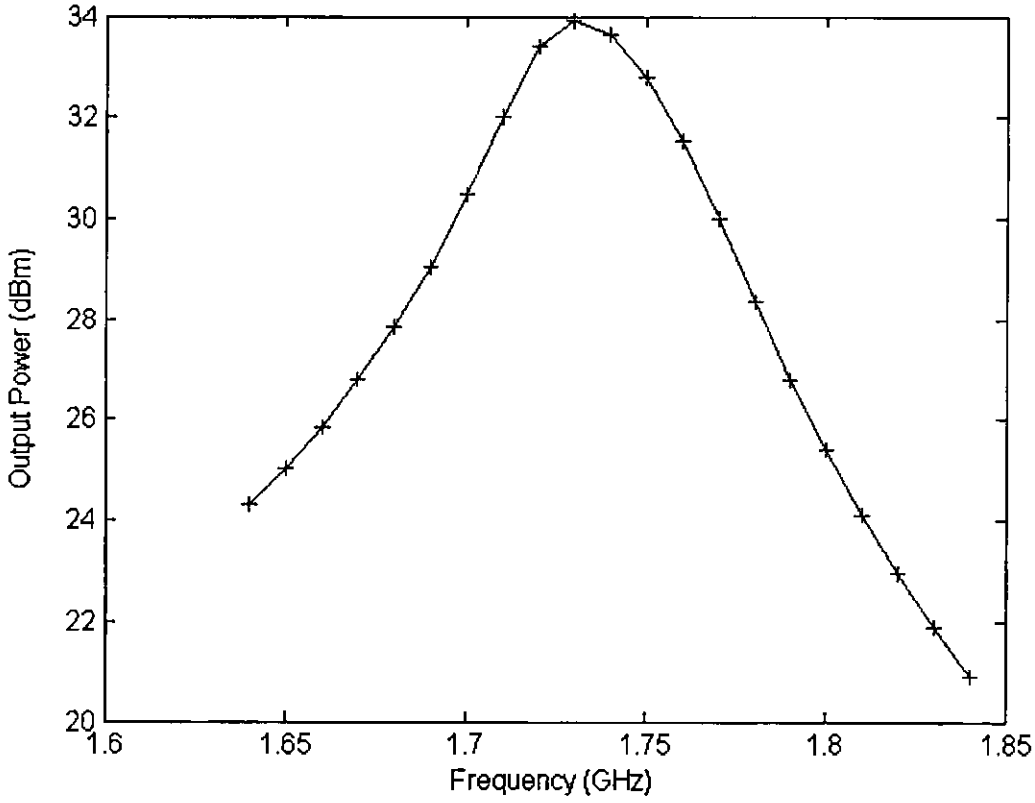


Figure 4.9 Simulated output power versus frequency

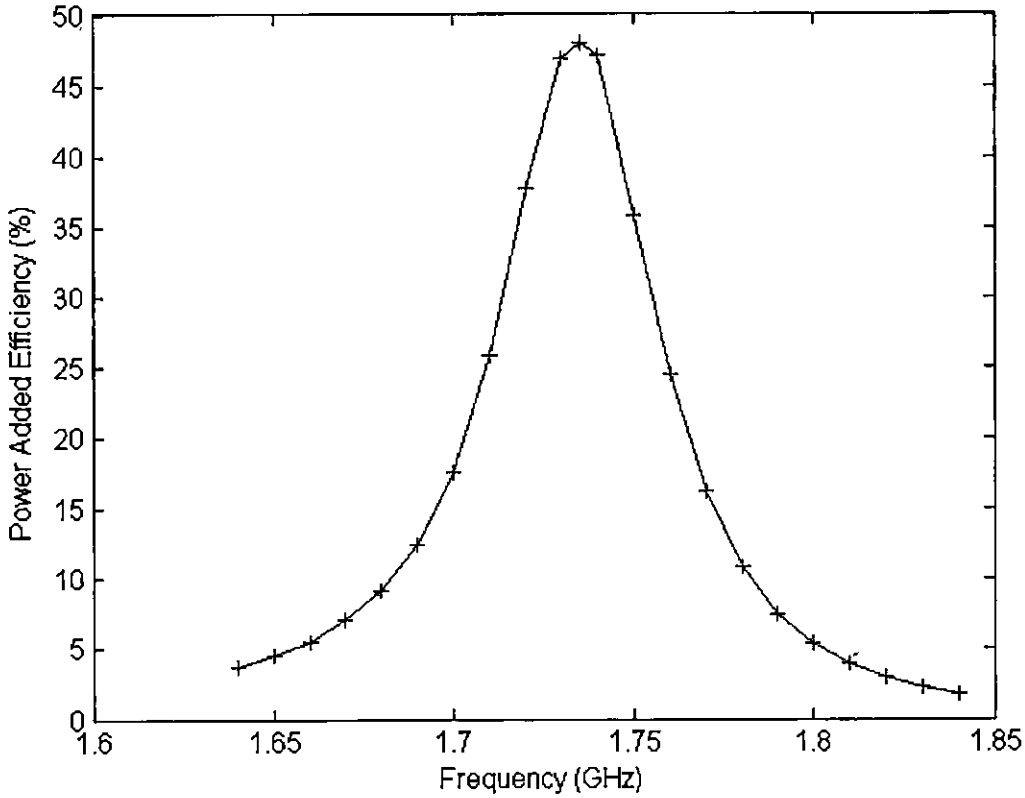


Figure 4.10 Simulated power added efficiency versus frequency

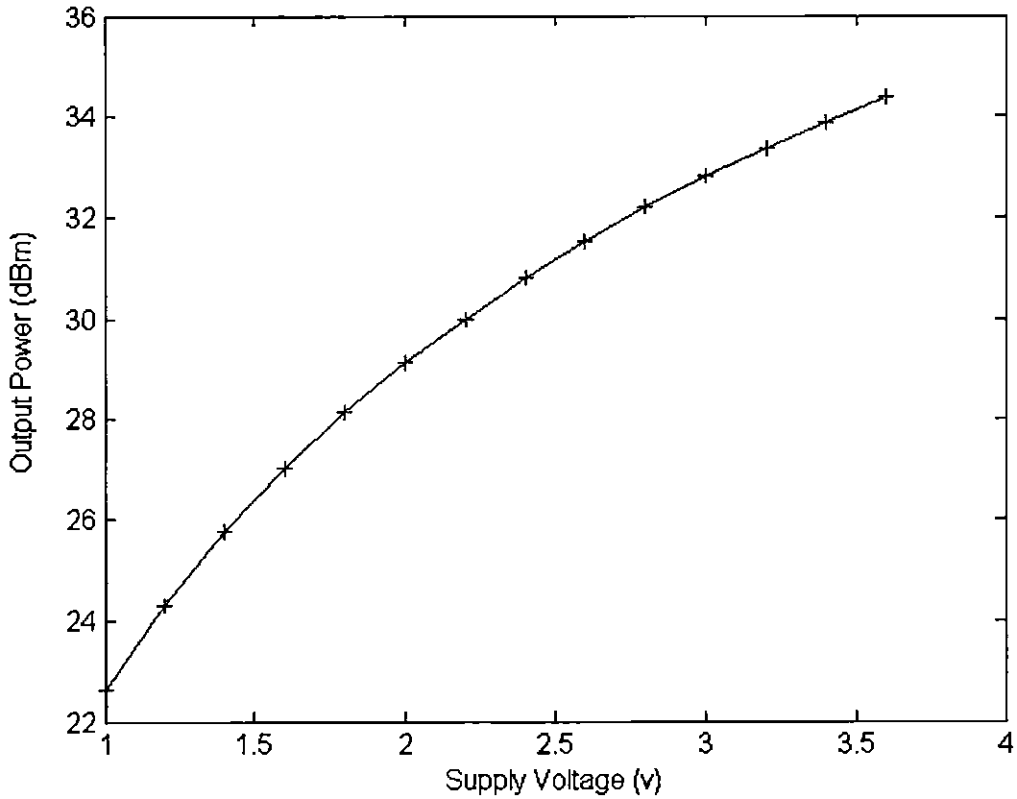


Figure 4.11 Simulated output power versus supply voltage

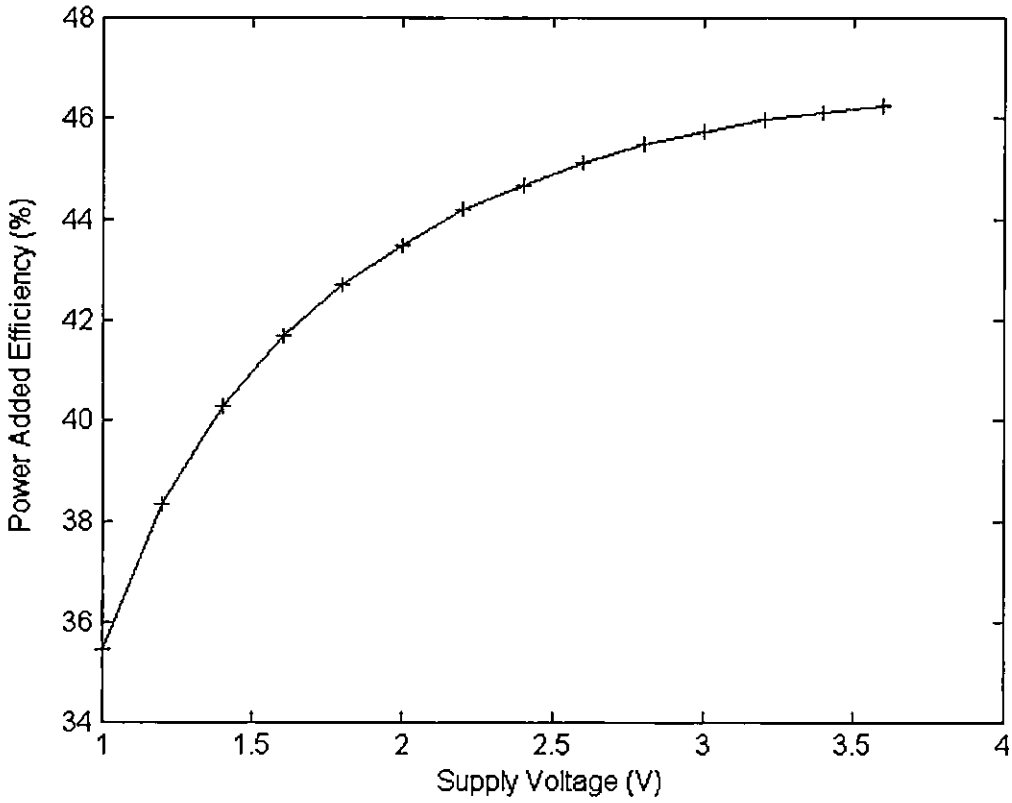


Figure 4.12 Simulated power added efficiency versus supply voltage

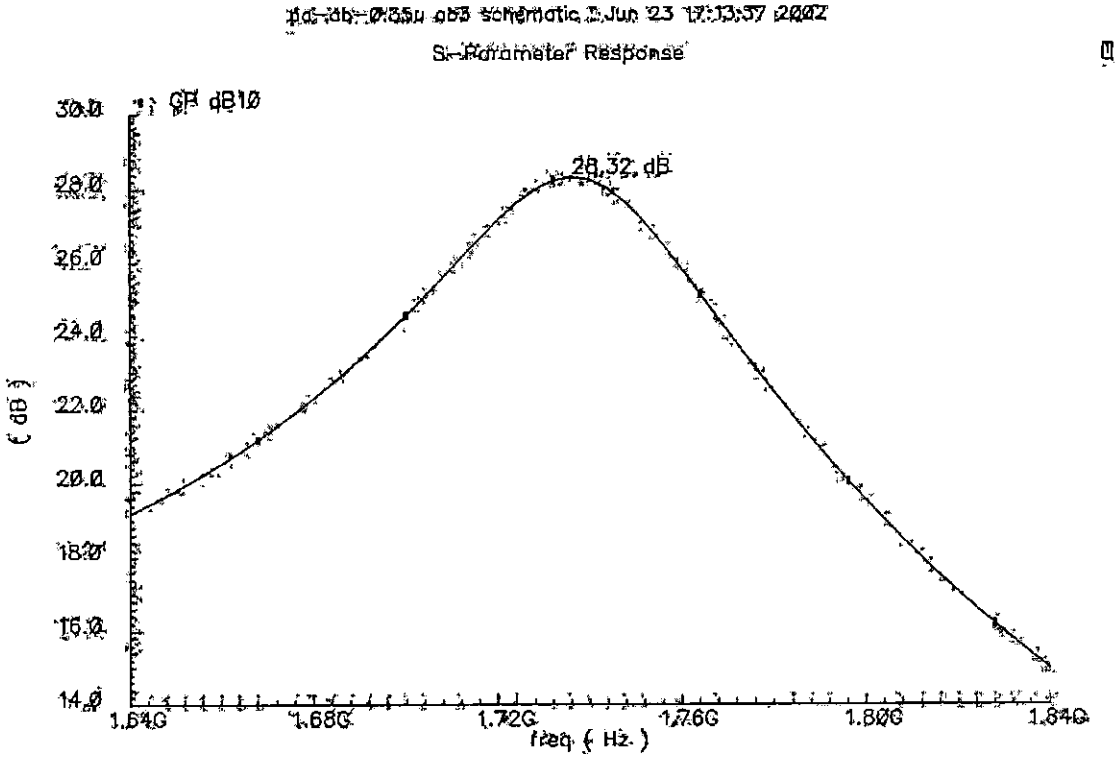


Figure 4.13 Power gain in dB versus frequency

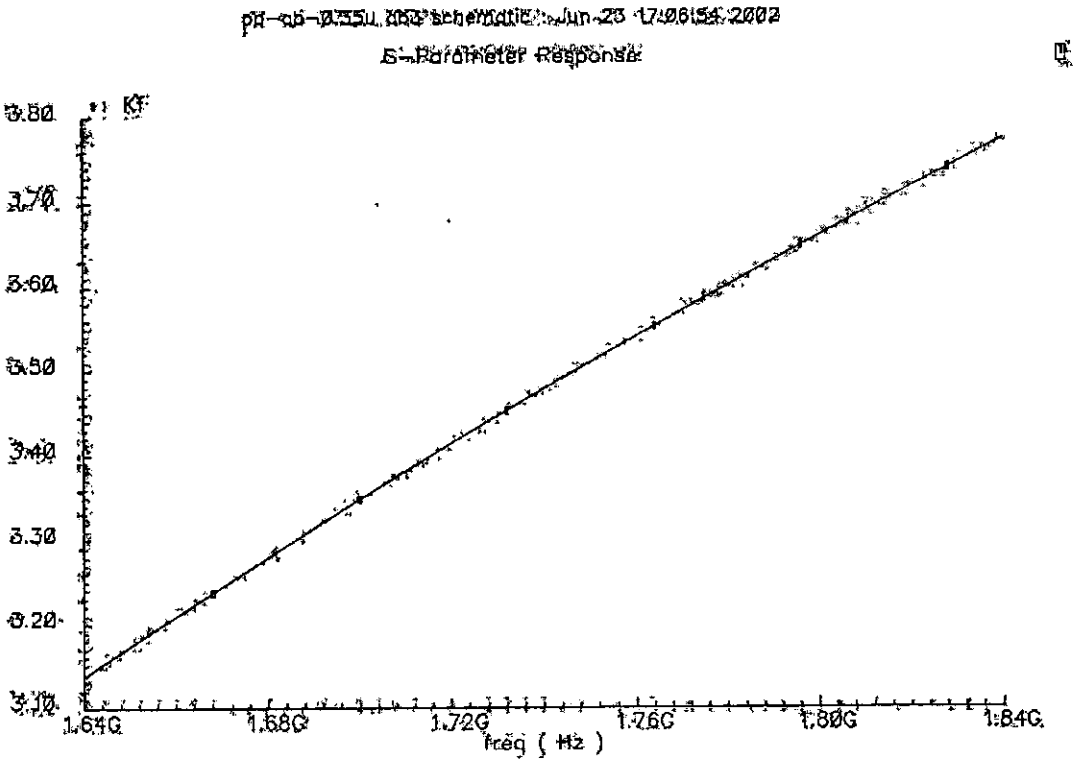


Figure 4.14 Stability factor (K) versus frequency

4.7 Conclusion

In this chapter, the design of class AB Power Amplifier that is suitable for wireless communications handset applications especially GSM was described. The design of individual stages as well as their matching networks was discussed. Finally simulation results was discussed with a maximum output power of 2.3 Watts (33.6 dBm) at 1.74 GHz and with a Power Added Efficiency (PAE) of 47%.

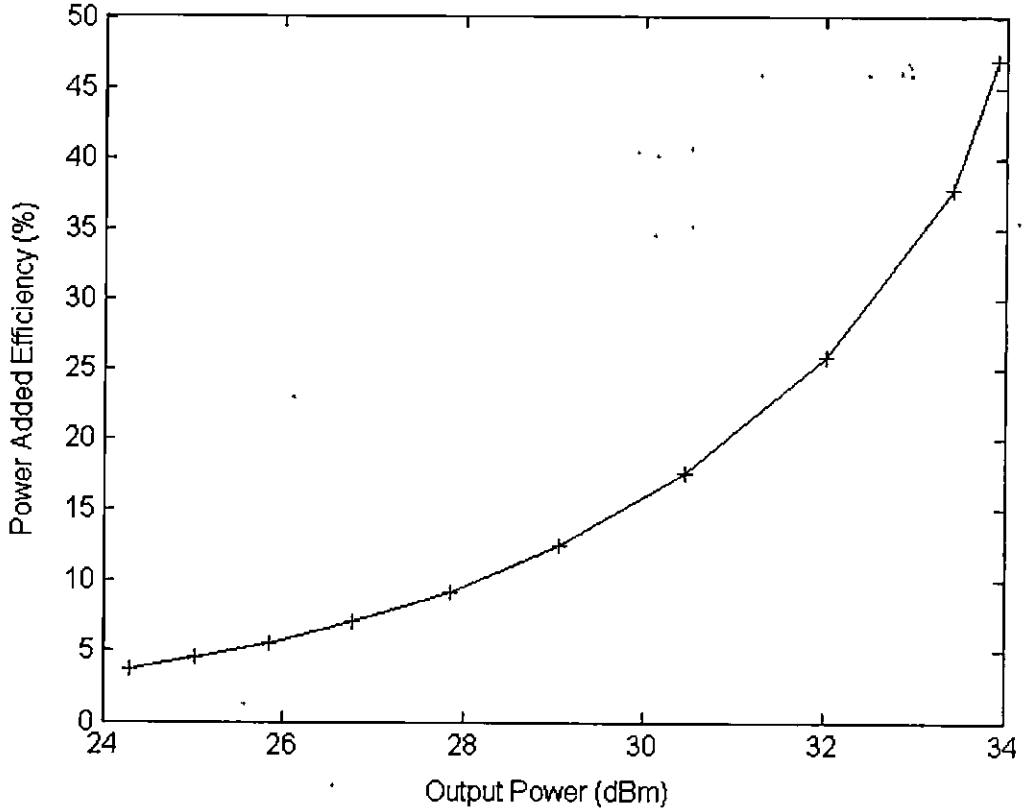


Figure 4.15 A plot of power added efficiency versus output Power

5 HOT-CARRIER EFFECTS ON POWER AMPLIFIER CIRCUIT

5.1 Introduction

5.1.1 Hot-carriers Mechanisms

Hot-carriers at the Si-SiO_2 interface of MOSFET's play an important role in the modeling and characterization of MOSFET devices and systems [24-26]. For 20 years, various research groups have studied the hot-carriers effects in MOSFET, because it is considered one of the stringent limitations in scaling the devices to deep sub-micrometer domain. Hot carrier induced phenomena have attracted research interest [27].

Hot-carrier degradation has its origin in the high electric field in the channel near the drain junction. The high field imparts enough energy to the electrons, through impact ionization, electron-hole pairs. The electrons are swept toward the drain and the holes are attracted to the substrate terminal, resulting in a substrate current I_{sub}, as shown in figure 5.1 [28].

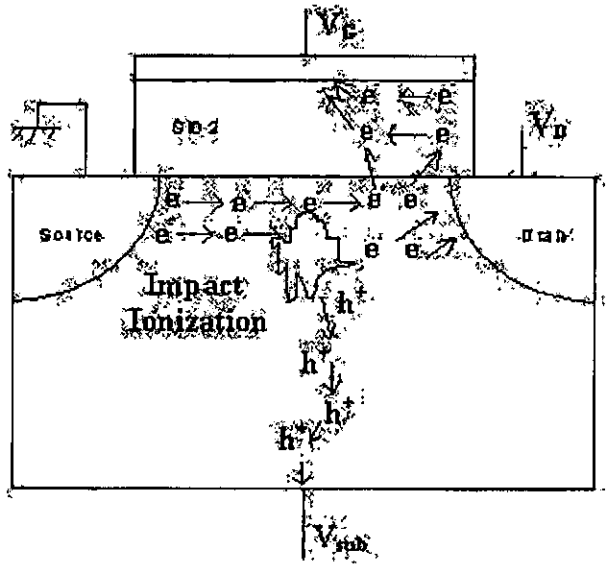


Figure 5.1 A schematic diagram for hot-carrier mechanisms.

Luckier electrons acquire enough energy to reach the Si-SiO_2 interface with a normal component of momentum greater than the value corresponding to the barrier energy. These electrons which surmount the Si-SiO_2 barrier are injected into the oxide, resulting in a gate current I_G . The estimation of the substrate and the gate current is vital to the prediction of the device degradation and the lifetime. A physical model for the degradation of n-MOSFET has been proposed (some modifications is needed for p-MOSFET) [29]. The degradation is dominated by the generation of acceptor-type interface traps, which are located in a narrow band near the drain and reduce local mobile carrier density and mobility. Hot electrons having energies larger than the critical energy, 3.7 eV, generate the interface traps responsible for device degradation. A hot electron could break a silicon-hydrogen bond. If the resultant trivalent silicon recombines with hydrogen, no interface trap is generated. If the hydrogen atom diffuses away from the interface, a new interface trap is generated. The model of hot electrons breaking silicon-hydrogen bonds thus generating interface traps is well established [30]. We assume that Si_SH bonds are formed at the interface during post-metallization anneal [31]. The strength of this bond is about 0.3 eV. This bond energy plus the Si-SiO_2 barrier energy (3.2 eV) are close to 3.7eV. The chemical reaction is given by:

$$Si_S H \xleftrightarrow{hot-e^-} Si^* + Hi \tag{5.1}$$

A hot electron breaks the $Si_S H$ bond to produce Si^*, trivalent silicon atom (i.e. interface trap), and Hi, interstitial hydrogen atom. An exact electric field in the channel can be obtained through 2-dimentional simulations, but it requires a great deal of computer time. Some attempts have been made to obtain analytically the lateral channel field in the vicinity of the drain junction where the phenomenon of hot carriers is mostly observed. Most of the models are based on the two section approach that consists of dividing the channel length into two regions: The source region, in which the gradual channel approximation is valid, extends from the source junction to the point of saturation, while the drain region, in which the quasi-two-dimensional analysis is used, extends from the point of saturation to the drain junction [27].

5.1.2 Hot-Carrier Degradation

When the channel of a MOSFET is switched by a strong electric field, the mobile carriers are accelerated and gain energy. These carriers emit some of their energy into the crystal through carrier-lattice collisions [32]. When the channel field is so strong that the energy gain is greater than that lost in collisions, carrier heating takes place. The energy exchange between the hot carriers and the lattice continues and tends to increase the lattice temperature, especially if the lattice

radiation capability is noticeably small. This provokes stronger lattice vibrations (optical and acoustic phonons) and leads to greater interaction between hot carriers and these vibrations, which decrease the hot carrier mobility. Therefore, the rate at which these carriers gain energy from the channel field and that at which energy is transferred to the lattice are decreased. This process continues until balance is reached between the two rates and the crystal and the carrier temperature attain their steady-state values [27]. Hot electrons injected into the gate oxide increase the gate current, thus enhancing surface state generation and electron trapping at the Si-SiO_2 interface. The interface state and electron trapping cause a distribution of the damaged region along the direction of the channel near the drain junction. The trapped charge in the oxide can shift the flat-band voltage and hereby the threshold voltage. The channel mobility is degraded by the interface state, therefore the drain current, I_D , is degraded. It has been reported that some important circuit parameters such as drain conductance and transconductance are also degraded by hot electron injection. The degradation can cause circuit failure.

5.1.3 Gate-Oxide thickness effect

The gate-oxide thickness is one of the important scaling parameters for device design. A thinner gate-oxide n-MOSFET shows smaller drain current degradation and threshold voltage shift, but larger substrate current [27].

It has been suggested that the mobility degradation is smaller for thinner oxide thickness device in which the damaged interface region moves towards the drain junction [33-35].

5.2 Power Amplifier Performance Degradation due to Hot-Carrier Effect

Here in thesis work, simulating hot-carrier effect was done by changing threshold voltage and mobility in the model file of the MOS transistor. The output power, Power Added Efficiency (PAE), and Stability factor (K) have been plotted below. As we can see the output power and the PAE are decreasing and the same for the (K) factor which can lead to instability problems in any marginally stable amplifier case. That is why it is recommended to do reliability study including hot carriers effect and other effects like Soft Break Down (SBD), not discussed here, after completing the design of the PA circuit or any other electronic circuit to make sure that after certain time the performance will be within its limit. Also reliability study will help in anticipating failure, which will certainly happen so preventive maintenance procedure can be done in the right timing.

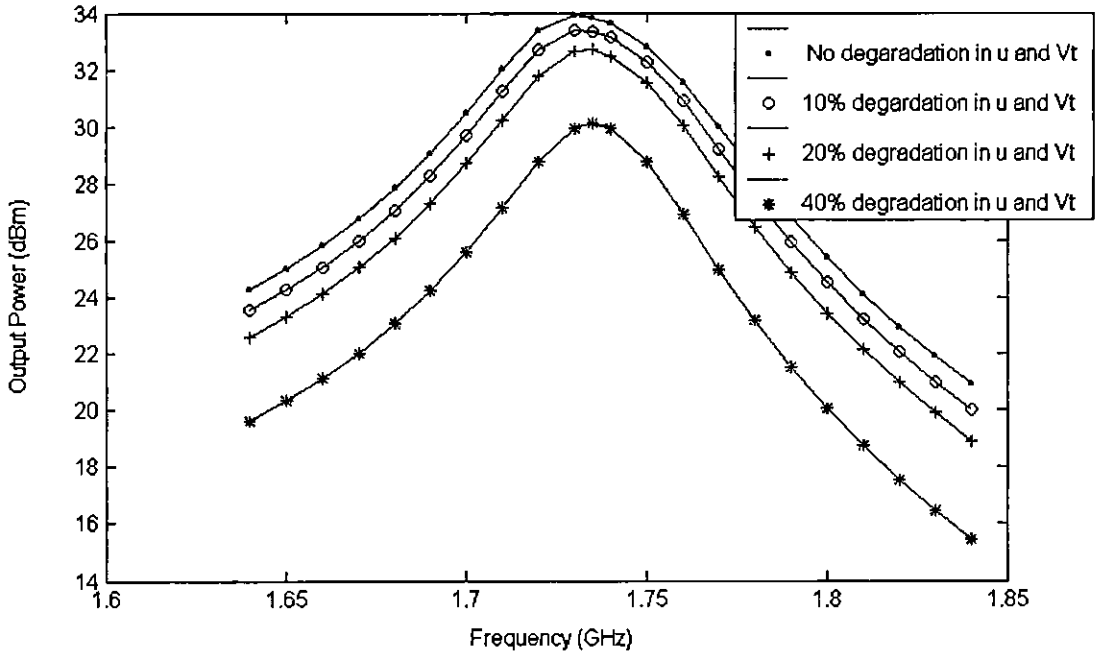


Figure 5.2 Output power degradation due to threshold voltage and mobility degradation

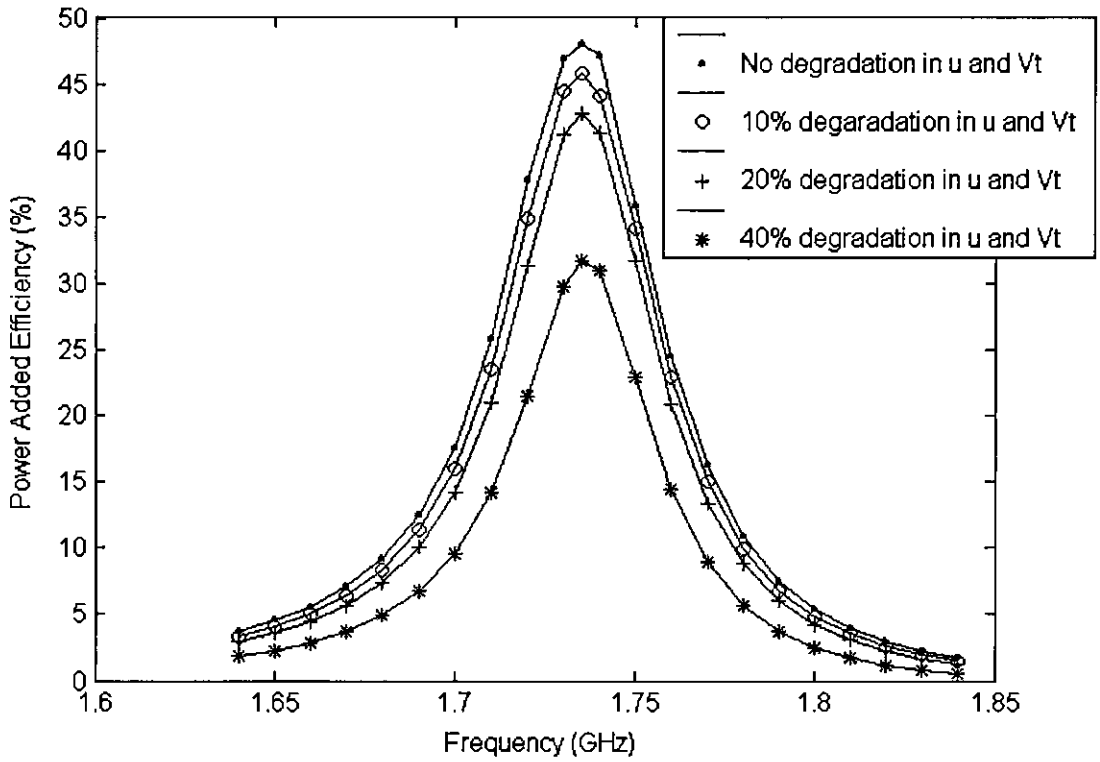


Figure 5.3 Power Added Efficiency degradation due to threshold voltage and mobility degradation

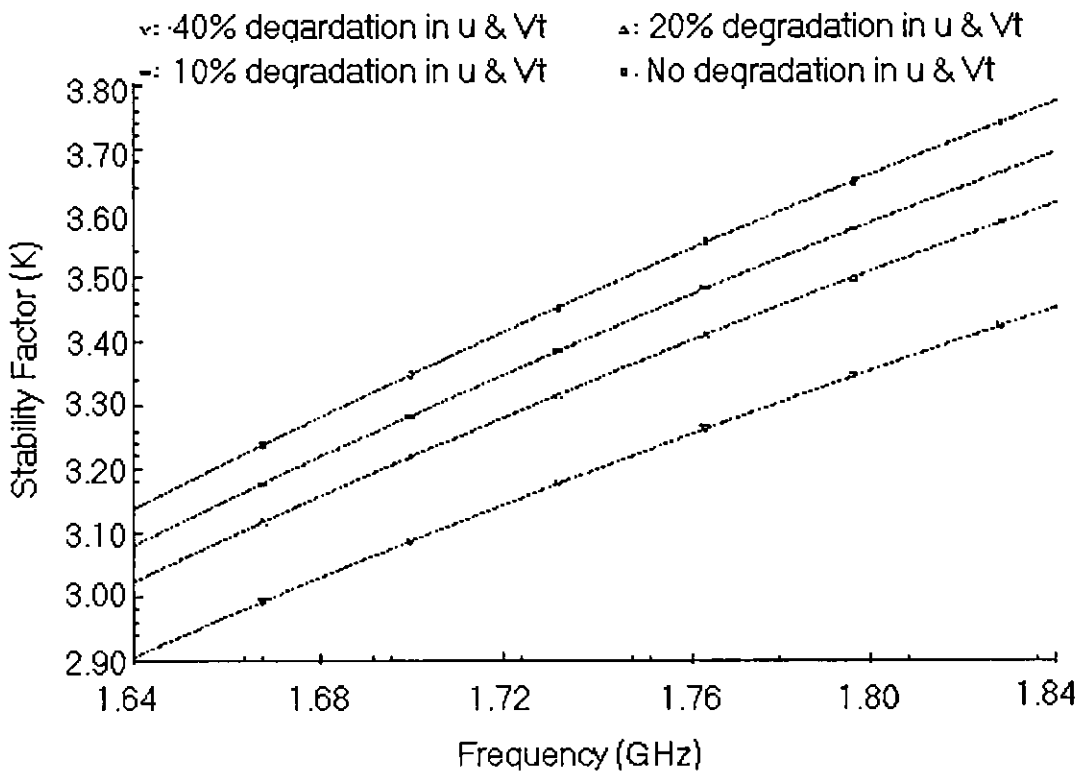


Figure 5.4 Stability factor (K) degradation due to threshold voltage and mobility degradation

6 CONCLUSION

This work attempted to design and simulate a class AB RF Power Amplifier that could be used in a wireless communication system. A host of classes of RF Power Amplifiers was reviewed, as well as methods that could have been used to linearize the non-linear classes of Power Amplifiers. A class AB CMOS Power Amplifier was designed in a 0.35μm CMOS process that delivered greater than 2 watts of peak output power with 47% Power Added Efficiency (PAE) in simulation.

The PA was implemented in a single-ended common source configuration. The design used 2 stages to generate the power needed; a class AB first stage, which controlled output power level, followed by an output stage in class AB also to generate the final power level. Many simulations have been done. Many plots have been included to study the performance of the power amplifier including output power, Power Added Efficiency, and stability factor (K) versus supply voltage and frequency.

A reliability study for hot carriers effects have been done including an introduction about hot carriers effects. Simulations were run to study the performance change due to hot carriers effects, which affects the mobility and the threshold voltage. Many graphs have been plotted including output power, Power Added Efficiency, and stability factor (K).

However, the design process was valuable, in that much was learned about PA's in general as well as the method of designing a PA. While the results obtained from simulations were not verified, as one can see from many of the previous design work that with good layout practices, the performance of an actual chip will not deviate much from the simulated performance.

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