The Relevance Of Time-to-digital Converters To Small Platform Direction Finding Systems

2010

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ABSTRACT

This thesis explores a Time-Difference-of-Arrival (TDOA) approach to radio direction finding, utilizing picosecond-resolution Time-to-Digital Converters (TDCs). By measuring the relative time of arrival of a pulsed RF signal impinging on an antenna array, direction of arrival (DOA) can be ascertained. This technology enables versatile DOA calculation on platforms only several meters in length, and offers various size, weight, power, and cost advantages when compared to present DF technologies. A short baseline S-band TDOA DF system utilizing TDCs is designed, fabricated, and tested in a laboratory environment. This research suggests that such a DF system based on TDCs provides sufficient accuracy and precision to resolve Angle-of-Arrival (AOA) within several degrees.
To Heather, for your love, compassion, and everlasting support.

To my mother Sheryl, father Jeffrey, and sister Jacqueline, for being the best family I could ever hope for.
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<th>Description</th>
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<td>AOA</td>
<td>Angle-of-Arrival</td>
</tr>
<tr>
<td>CW</td>
<td>Continuous Wave</td>
</tr>
<tr>
<td>DF</td>
<td>Direction Finding</td>
</tr>
<tr>
<td>DLVA</td>
<td>Detector Log Video Amplifier</td>
</tr>
<tr>
<td>DOA</td>
<td>Direction-of-Arrival</td>
</tr>
<tr>
<td>LNA</td>
<td>Low-noise Amplifier</td>
</tr>
<tr>
<td>LTCC</td>
<td>Low Temperature Co-fired Ceramic</td>
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<tr>
<td>LVTTL</td>
<td>Low Voltage Transistor-Transistor Logic</td>
</tr>
<tr>
<td>LVPECL</td>
<td>Low Voltage Positive Emitter Coupled Logic</td>
</tr>
<tr>
<td>PRF</td>
<td>Pulse Repetition Frequency</td>
</tr>
<tr>
<td>TDOA</td>
<td>Time-Difference-of-Arrival</td>
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<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
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CHAPTER 1: INTRODUCTION

Assurance of pilot safety and reduced costs are undeniable driving forces behind the impending pervasive UAV deployment across the globe. As reliance on UAVs increases for military and civilian operations, so does the demand for required onboard instrumentation. Integration of ES and ESM equipment used on UAV’s, however, is undoubtedly limited due to size, weight, and power (SWAP) constraints. Current generation direction finding (DF) systems suffer from these confines, so new low-power chip-scale solutions are desirable. Additionally, DF systems that consist of commercial off-the-shelf (COTS) components reduce cost, and are particularly attractive.

The primary function of a passive radio direction finding system is to resolve the location of a radiation source, often referred to as an emitter. DF systems are used in a variety of disciplines, including wide life management, law enforcement, and military operations. Frequent uses include geolocation, navigation, and targeting for weapon systems. With respect to the military, some of the most prevalent applications of passive DF systems include early warning threat detection, targeting homing and jamming, electronics intelligence, and data reduction [1].

Passive DF techniques include the comparison of one or more of the following attributes of a signal: amplitude, phase (interferometry), frequency, and time difference of arrival (TDOA). Due to size, complexity, and high cost, interferometer DF systems are often not ideal for small platforms. Amplitude comparison systems based on the Watson-Watt method and spatially distributed directional antennas are common, but suffer from limited bandwidth [2] and accuracy [1], respectively. TDOA is currently implemented when the distances between antennas are large for localization purposes, such as in the case of mobile phone triangulation, but
utilizing this technique on a small scale has been limited by the ability to resolve the time differences with high accuracy and precision.

This thesis is focused on a feasibility study of a S-band prototype TDOA DF solution using picosecond-resolution time-to-digital converters (TDCs). By measuring the relative time of arrival of a pulsed RF signal impinging on an antenna array, DOA can be ascertained. This technology enables versatile DOA calculation on platforms only several meters in length, and offers many SWAP and cost advantages when compared to current DF technologies. Emitter classification is also possible, based on parameters such as pulse width and pulse repetition frequency. While the technology is intended for integration with small platforms such as UAVs, there is no preclusion to its use elsewhere.

This research began during an internship the author experienced at Pt. Mugu, NAWC in the summer of 2009. One of the assigned tasks during that period was to recommend a low-cost wide-band DF system design, comprised of COTS components. This system, intended for UAV integration, would ideally have an rms AOA error below 10°. Following a literature examination and finding promising (yet immature for deployment) results from ESL Defense, Ltd., the author began to study the approach of using TDCs for determining emitter location. The results of these studies are presented in the subsequent chapters in this thesis.

Chapter 2 provides an overview of the direction finding techniques and concepts that underlie most modern DF systems. It also differentiates the TDOA DF system studied in this thesis from other work. A scenario is introduced in Chapter 3 where a low-cost DF solution is attractive, and presents a block diagram of the proposed TDOA architecture. Each component in the diagram is then discussed in detail. Chapter 4 is focused on the circuit-level design, simulation, and fabrication of key elements within the DF system. Measurement results of DF
performance are discussed in Chapter 5. Conclusions from the research in this thesis are presented in Chapter 6, and finally Chapter 7 includes several topics for further study.
CHAPTER 2: EXISTING DF SYSTEMS

Prior to assessing the feasibility of a short baseline TDOA DF system, it is necessary to understand the fundamental concepts of past and modern radio direction finding. This chapter presents an overview of DF concepts and fundamentals. While many different DF techniques and technologies are available, all resolve AOA based on multiple associations of one or more of the following wave characteristics: amplitude, phase, frequency, or time. To this end, a wide variety of DF systems have been invented, such as rotating vs. non-rotating, single-channel vs. multiple channel, etc. This chapter serves as an introduction to some of the rudimentary concepts that are present in virtually any commercial or military DF system. Additionally, the DF architecture designed and studied in this thesis will be compared to the most similar existing technologies.

2.1 Existing DF Techniques

The following section will describe several fundamental DF configurations and techniques. It is intended to inform the reader of the underlying fundamental principles of various modern DF systems, as well as the advantages as well as disadvantages of each. This serves as a basis to understand how the proposed TDOA method, which will be discussed in chapters 2 and 3, compares to the currently available techniques.

2.1.1 Scanning Beam

The single-channel rotating DF system, or scanning beam, is perhaps the most intuitive configuration. Consider a highly directional antenna (or antenna array) that is mechanically rotated at a designed angular velocity (Figure 2.1). The angle of arrival (AOA), or bearing, of a signal is derived from the received voltage as a function of rotation angle. When a large enough signal is received, the current antenna rotation angle is recorded. Additionally, the received
voltage is compared to the known antenna radiation pattern to yield higher accuracy. The accuracy of a scanning beam DF system is proportional to the antenna beamwidth, so naturally these systems can resolve AOA quite accurately (i.e. 1° or less) with highly directional antennas.

Figure 2.1: Rotating directional antenna DF system (reprinted with permission from [3])

In addition to those discussed above, Table 2.1 summarizes the benefits and drawbacks of a scanning beam DF system [3]. Clearly, a rotating beam DF system would prove to be insufficient for systems where high POI is critical (i.e. early warning threat detection). Nevertheless, scanning beam DF systems still find their uses today due to their inherent high accuracy and sensitivity.

Table 2.1: Scanning beam DF system considerations

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
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<tr>
<td>High accuracy</td>
<td>Low Probability of Intercept (POI)</td>
</tr>
<tr>
<td>High sensitivity</td>
<td>Not ideal for short duration signals with low PRF</td>
</tr>
<tr>
<td>Low-cost</td>
<td>Typically large and cumbersome</td>
</tr>
</tbody>
</table>
2.1.2 Multiple Directional Antennas

In this approach, the relative power received by several directional antennas with different orientations yields AOA. Typically, four or more wideband antennas are placed on a platform to offer full simultaneous 360° coverage, such as in the scenario portrayed by Figure 2.2. The angle of arrival with respect to a heading may be calculated by comparing the received signal power or voltage levels from an antenna pair, \((V_1 \text{ and } V_2)\) in this case.

![Figure 2.2: Idealized DF configuration of four antennas](image)

In contrast to the scanning beam DF system, multiple directional antenna configurations are often utilized in radar warning receiver (RWR) systems. An ideal antenna would have a power gain that decreases linearly (in dB) as the angle from boresight increases (technically, however, as long as the power patterns of the antennas are well characterized and decrease monotonically with increasing angle from boresight, a linear in dB relationship is not necessary).
Other important parameters, mostly specific to RWR systems, include extremely wide bandwidth, almost non-existent back lobes, and radiation patterns that do not vary rapidly across the operating frequency range. Cavity backed spiral antennas can be designed to meet these specifications, and as a result, are used in many modern RWR’s [4]. These DF configurations often cover 2-18 GHz, but only offer 5º - 10º accuracy. [1]

2.1.3 Watson-Watt

The Watson-Watt radio direction finding technique, invented by Sir R. A. Watson-Watt of Great Britain in the 1920s, is one of the earliest methods realizing passive radio direction finding. In short, it uses the difference in the amplitude of an electromagnetic wave incident on multiple antennas to determine the angle of arrival. The simplest case features two omnidirectional antennas are spaced approximately a quarter-wavelength apart, and fed 180º out of phase. A center sense antenna is may be included as well to eliminate the 180º ambiguity in direction that would arise with only a 2-element array. The result is a 3-element linear array, in which a null forms due to the 180º phase imbalance between the outer antennas. AOA in one plane, typically azimuth, is then determined through null tracking the signal by rotating the antenna array on a pedestal.

In practice, however, Watson-Watt based DF systems are not physically rotated. Instead, switched crossed-loop antennas, or more predominantly, Adcock antennas, are used. An example of a modern Adcock DF system is presented in Figure 2.4. In this configuration, two pairs of monopole or dipole antennas take the vector difference of the received signal. Note that the sum signal of the four antennas is used to resolve the 180º ambiguity that would otherwise arise, so a 5th sense antenna is no longer necessary. The idealized patterns produced by such an Adcock array
are presented in Figure 2.3. The NS and EW pair patterns are indicated by blue and green, respectively.

Using array theory, the resulting signals can be expressed as:

\[ V_{NS} = V_N - V_S \]
\[ V_{NS} = e^{j\frac{\pi d}{\lambda} \sin \phi} - e^{-j\frac{\pi d}{\lambda} \sin \phi} = j2\sin\left(\frac{\pi d}{\lambda} \sin \phi\right) \]  

\[ V_{EW} = V_E - V_W \]
\[ V_{EW} = e^{j\frac{\pi d}{\lambda} \cos \phi} - e^{-j\frac{\pi d}{\lambda} \cos \phi} = j2\sin\left(\frac{\pi d}{\lambda} \cos \phi\right) \]

Where \( \lambda \) is the free-space wavelength, \( d \) is the spacing between antenna pairs, and \( \phi \) is the azimuth angle. From the expressions above, we can see that each antenna pair generates a single voltage. Additionally, geometry dictates that the signals are spatially orthogonal to each other. Therefore, AOA can be calculated by taking the arctangent of the ratio of the y-axis voltage to the x-axis voltage:

\[ AOA = \tan^{-1}\left(\frac{V_{NS}}{V_{EW}}\right) \]
One major drawback of the Adcock DF antenna is the limited bandwidth, primarily constrained by the spacing of aerial pairs. As the aerial distance increases, the antenna pattern lobes begin to lose their circularity (i.e. they become elongated). Since the patterns are assumed to be near-sinusoidal in the formation of the AOA equation above, this discrepancy causes bearing errors. According to RDF products, good Adcock designs limit the maximum spacing to 1/3 wavelength at the high end frequency to limit this spacing error [2]. Adcocks typically offer accuracy around 3º.

### 2.1.4 Doppler and Pseudo-Doppler Techniques

The Doppler and pseudo-Doppler DF techniques are perhaps the best known and most widely used within the 2-2000 MHz range [5]. First, a rudimentary Doppler DF system will be presented, followed by a more sensible pseudo-Doppler technique.
Figure 2.5: Simple Doppler DF system

Figure 2.5 indicates an antenna element on a rotating pedestal with a radius $r$. The physical rotation modulates the incoming signal due to the Doppler Effect: if the antenna moves toward the radiation source, the apparent frequency of the source increases, and vice-versa when the antenna moves away from the source. The instantaneous amplitude of the received signal may be modeled as the following [3]:

$$E(t) = A \cos \Phi(t) = A \cos \left( \omega_0 t + \frac{2\pi r}{\lambda_0} \cos(\omega_r t - \alpha) \phi \right)$$

(2.6)

Where the pedestal rotates at frequency $\omega_r$, the frequency of the carrier signal is $\omega_0$, the radius of the pedestal is $r$, the carrier phase offset is $\phi$, and the AOA is $\alpha$. Considering the rate of change of $\Phi(t)$, then blocking the DC component:

$$\frac{d\Phi(t)}{dt} = \omega_0 - \frac{2\pi r}{\lambda_0} \omega_r \sin(\omega_r t - \alpha)$$

(2.7)

$$S_D = \frac{2\pi r}{\lambda_0} \omega_r \sin(\omega_r t - \alpha)$$

(2.8)

$$S_r = -\sin(\omega_r t)$$

(2.9)

The phase of $S_D$ is then be compared to a reference signal $S_r$ derived from the antenna rotation to yield the AOA $\alpha$. 

10
Unfortunately, the discussed Doppler DF technique has practical limitations. First, mechanical systems are often cumbersome, and more erratic when compared to their electronically scanned brethren. Additionally, DF systems require reasonably high signal to noise ratios (and thus high modulation frequencies), which is not feasible for mechanically rotating DF antennas [6]. Instead, electronically switched antenna arrays are used, an example of which is presented in Figure 2.6. It is essentially a single channel, time-sampled interferometer. This method is known as the pseudo-Doppler DF technique.

2.1.5 Array Techniques

DF systems that utilize antenna arrays fall into two categories: parallel beam or steered beam. In parallel beam systems, all beam positions are continuously active, so POI is high. Each beam is composed of one or more antenna elements. Steered beams, on the other hand, use one or more beams that are scanned across a field of view as time progresses. Typically beam forming networks such as Rotman lenses or phase shifters are used in this method. Since the entire field of view is not continuously covered, POI is naturally lower than a parallel DF
antenna array. Since more antenna elements are used to form a beam when compared to a parallel DF system, however, the wider aperture results in higher directivity, and therefore higher accuracy. While the details of array systems and array DF algorithms are outside the scope of this thesis, it is useful to understand that the general tradeoff between these two techniques is accuracy and probability of detection.

2.1.6 Interferometer Techniques

An interferometer is a specific type of antenna array, but the distance between elements is often larger than half a wavelength, creating grating lobes. Additionally, the spacing between receiving antenna elements is generally not uniform, as in the case of many antenna arrays. For high accuracy location of emitters, interferometry is the most commonly used technique [4]. DF systems can be designed to cover very large bandwidths as long as the ambiguity problem is solved, which will be discussed shortly.
A simple single baseline two antenna interferometer is portrayed by Figure 2.6. A plane wave is incident on two antennas at an angle $\theta$. The incident electric fields may be expressed with respect to an incident plane wave $E_0$ as the following:

\begin{align}
E_1 &= E_0 e^{j(\omega t - kr)} \\
E_2 &= E_0 e^{j(\omega t - kr + kd \sin \theta)}
\end{align}

Where $r$ is the propagation distance of the plane wave from the source, $k$ is the wave number, $d$ is the antenna baseline, and $\theta$ is the AOA with respect to the interferometer boresight. It is reasonable to assume that the propagation loss is negligible for the short distance the wave travels between adjacent antennas. Therefore, the incident waves are identical but delayed in time, which manifests as a phase shift. Solving for the differential phase shift:

$\Delta \phi$
\[ \Delta \phi = \angle E_2 - \angle E_1 = kd \sin \theta = \frac{2\pi d}{\lambda} \sin \theta \]  (2.12)

For an unambiguous measurement, the relative phase shift must satisfy: \(0^\circ < \Delta \phi < 360^\circ\) since phase measurement is always modulo 360º. Inspection [of the above equation] indicates that \(d\) must be less than one half-wavelength to avoid ambiguities. As AOA varies between \(\pm 90^\circ\) from boresight (one side of the array is used), \(\Delta \phi\) changes 360º. This phenomenon limits the bandwidth of an interferometer over which a measured AOA is unambiguous. Multiple baseline interferometers, however, may be used to solve the ambiguity problem by calculating all possible AOA’s and checking for maximum correlation [3]. In practice, many interferometers use multiple baselines, often one or more of which are many wavelengths long to improve accuracy. Direction finding through interferometry can achieve very high resolutions by using electrically large baselines; 0.1º to 3º are typical [1], [7].

2.1.7 Time-Difference-of-Arrival (TDOA)

This precise emitter location technique measures the difference in time of arrival of a single pulse-modulated signal at different locations, generally separated by at least several kilometers. Naturally, the technique is useless in determining DOA of a CW emitter due to the reliance on pulse modulated signals. Historically, TDOA has been used on a large scale (i.e. cell-phone geolocation). Reports in the past have explored TDOA-based passive geolocation of emitters through the cooperated efforts of UAV’s and ship/land-based platforms [8].

A TDOA geolocation scenario is presented by Figure 2.7. Consider a signal source (emitter) and various sensors spatially distributed at remote locations. An expression to calculate the location in three dimensions may be deduced (the analysis follows that in [8]). If \(t_n\) represents the time of arrival for a signal to propagate from an emitter to sensor \(n\), the TDOA
between sensor \( n \) and \( n+1 \) may be calculated assuming the propagation velocity of the EM wave is known (here, it is assumed to be that of a vacuum).

\[ \Delta t_{n,n+1} = t_n - t_{n+1} = \frac{1}{c}(d_n - d_{n+1}) \quad (2.13) \]

Where \( n = 1,2,\ldots,N \) \( d_n \) is the distance from the emitter to the \( n \)th sensor, \( c \) is the speed of light, and \( N \) is the total number of sensors. From the distance theorem:

\[ d_n = \sqrt{(x_e - x_n)^2 + (y_e - y_n)^2 + (z_e - z_n)^2} \quad (2.14) \]

where \((x_e, y_e, z_e)\) and \((x_n, y_n, z_n)\) are spatial coordinates representing emitter and the \( n \)th sensor locations, respectively. By combining the above equations, the coordinates can be directly related to the TDOAs:
To solve the three unknowns in the above equation, a minimum of three TDOAs are necessary, requiring a minimum of four sensors. If emitter location is only desired in two dimensions, however, then only three sensors are essential.

2.2 Proposed TDOA Technique

In principle, the technique under study in this thesis is quite similar to the interferometer and TDOA geolocation DF techniques previously discussed. It is essentially an interferometer setup that measures the time of arrival of pulsed RF signals directly, as opposed to a phase measurement. Consider the two element antenna array, separated by a baseline distance $d$, depicted in Figure 2.8. A plane wave is incident on two antennas at an angle $\theta$. The incident electric fields may be expressed with respect to an incident plane wave $E_0$ as the following:

$$c\Delta t_{n,n+1} = \sqrt{(x_e - x_n)^2 + (y_e - y_n)^2 + (z_e - z_n)^2} - \sqrt{(x_e - x_{n+1})^2 + (y_e - y_{n+1})^2 + (z_e - z_{n+1})^2}$$

(2.15)
\begin{align}
E_1 &= E_0 e^{j(ot - kr)} \\
E_2 &= E_0 e^{j((ot - kr + \omega \Delta t_{12})} 
\end{align}

Where \( r \) is the propagation distance of the plane wave from the source, \( k \) is the wave number, \( d \) is the antenna baseline, \( \Delta t_{12} \) is the time difference of arrival of the signal with respect to the two antennas, and \( \theta \) is the AOA with respect to the interferometer boresight. It is reasonable to assume that the propagation loss is negligible for the short distance the wave travels between adjacent antennas. Therefore, the incident waves are identical but delayed in time/phase. Solving for the differential phase shift:

\[ \Delta \phi = \angle E_2 - \angle E_1 = \omega \Delta t_{12} \]

However, we know that the phase shift may also be expressed as the following:
\[ \Delta \phi = \angle E_2 - \angle E_1 = kd \sin \theta \]  

(2.19)

Assuming free-space propagation,

\[ k = \omega \sqrt{\mu \omega} = \frac{\omega}{c} \sqrt{\mu_r \varepsilon_r} = \frac{\omega}{c}, \quad \text{if} \; \mu_r = \varepsilon_r = 1 \]  

(2.20)

Combining the three above equations, and solving for the AOA \( \theta \):

\[ \theta = \sin^{-1} \left( \frac{c \Delta t_{12}}{d} \right) \]  

(2.21)

The results indicate that AOA is only a function of the ability to measure the time difference of arrival and the baseline distance. Unlike with interferometry, ambiguous AOA’s do not exist when the baseline increases beyond half a wavelength. There is, however, a 180° ambiguity with the simple two antenna configuration (as discussed with the interferometer), but this is remedied by using a third antenna/receiver or limiting DF angular coverage to \( \pm 90^\circ \) from boresight by using directional antennas with very small back lobes (i.e. cavity backed spirals).

Table 2.2 outlines some of the potential benefits and drawbacks of the short baseline TDOA DF system. It is worthwhile to emphasize that TDOA is inherently a frequency independent DF technique, only limited by the bandwidth of the antennas, receiver, and time measurement device. Wideband antennas and receivers have been available for decades (i.e. early warning threat receivers), and time measurement devices with sufficient accuracy for short baseline DF systems have been commercially available for several years (this will be discussed in detail in chapter 3. As a result, short baseline TDOA DF systems are well suited for UWB signal direction finding, which has been a topic of interest for both industry and academia for the last decade [9]. Many of the previously discussed DF technologies may not be as effective at detecting UWB signals due to limitations of bandwidth, low POI, and pulse distortion [9], [10].
One of the most glaring drawbacks is the inability to detect AOA of CW signals, since TDOA measurement is achieved by detection and time-stamping the rising and falling edges of a RF pulse envelope. CW waves do not have a reference embedded within the signal, so it is impossible to make any spatial judgments as a function of time. One solution, however, is to use a secondary on-board amplitude comparison system so a UAV or similar platform is not blind to these signals. It will be shown that this functionality can be added with minimal additional hardware in the following chapter.

Table 2.2: Short-baseline TDOA DF System Considerations

<table>
<thead>
<tr>
<th>Benefits</th>
<th>Drawbacks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extremely Broadband</td>
<td>Ineffective with CW</td>
</tr>
<tr>
<td>Low complexity</td>
<td>Calibration may be difficult</td>
</tr>
<tr>
<td>Low Cost – COTS components</td>
<td></td>
</tr>
<tr>
<td>Medium to high accuracy</td>
<td></td>
</tr>
<tr>
<td>Excellent SWAP attributes</td>
<td></td>
</tr>
<tr>
<td>High POI</td>
<td></td>
</tr>
<tr>
<td>Multipath Immunity</td>
<td></td>
</tr>
</tbody>
</table>

The primary challenge of this method is realizing the tremendously accurate and precise time measurements. This hurdle has prevented the practical use of TDOA DF systems being used on platforms where the baselines are only several meters in length. It will be shown that rms time measurement errors on the order of hundreds of picoseconds are often required to yield sufficiently accurate AOA. Additionally, calibration – whether via software post-processing or hardware – may post a significant challenge. Any DF antenna arrays in general require complex calibration schemes [11] as well, so this should not deter exploration of the topic.

2.3 Literature Examination

ESL Defense Ltd. in UK has pioneered the concept of using TDCs for a TDOA DF system in a laboratory and outdoor environment; unclassified results are presented in conference
proceedings [12], [13], [14], and [15]. Their results are promising, but their DF system is still immature for deployment. The work of [16] studies the concept of a single channel model for TDOA direction finding, specific to UWB signals, but the receiver architecture is quite different from that in this thesis, and the paper mostly explores mathematical models.

Several key differences exist when comparing the research in this thesis to the work of other individuals and companies previously mentioned. Firstly, as indicated in the following chapter, a demodulating logarithmic amplifier is employed rather than a simple wideband square law detecting diode [15], which increases the dynamic range of the receiver. Secondly, the mechanism for threshold detection is not thoroughly explained in the previous works of ESL Defense. The threshold logic and signal conditioning circuitry was custom designed for the DF prototype assessed this thesis, so variation is expected. Thirdly, a VGA is incorporated in the presented DF system, which is not included in previous works. Measurements of TDOA performance with the VGA configured in automatic gain control loop will be compared to manual VGA control. Finally, and perhaps most importantly, a rudimentary software-based calibration scheme is explored in this thesis as a means to enhance measurement accuracy. Of the four papers produced from ESL Defense Ltd., a calibration method – whether based on hardware or software – is not utilized.
CHAPTER 3: PROPOSED ARCHITECTURE

3.1 Problem Description

Figure 3.1 illustrates the TDOA concept on a UAV. A pulse modulated RF signal from an emitter is received by two matched antenna/receiver channels, which are separated by a baseline distance. From measurement of the relative time delay of the signals impinging on the antennas, the angle of arrival (AOA) in a single plane can be calculated using the method described beneath Figure 2.8. The study in this thesis focuses on the above hypothetical situation, and assumes that directional antennas such as cavity backed spirals are employed. While AOA in one plane can be determined from a single TDOA measurement between two sensors, it will be shown later that bearing error may be reduced, if AOA is estimated based on a series of TDOA measurements.
A deployed UAV would likely contain an on-board GPS and altimeter to permit accurate spatial positioning in three dimensions. The information necessary to geolocate an emitter can then be retrieved over a brief period of flight. The geolocation process is similar to that described in [8].

3.2 Proposed Hardware Solution

Figure 3.2: S-band prototype TDOA DF architecture

A block diagram of the proposed short baseline TDOA DF system is presented in Figure 3.2. It features two matched crystal video receivers for wideband high dynamic range signal reception with high POI. RF pre-amplification is included to increase sensitivity. The flow of a signal through the each component of the DF system will now be described, beginning with the path a signal takes through one receiver.

1. A pulse-modulated RF signal is received by the antenna
2. The RF limiter blocks high-power signals that may illuminate the receiver (i.e. under jamming conditions), thereby protecting the LNA
3. The low-noise amplifier acts as a preamplifier to boost DLVA sensitivity
4. A low-pass RF filter helps suppress unwanted out of band signals.

5. The detector log video amplifier (also known as demodulating logarithmic amplifier) demodulates the pulse-modulating RF signal directly over a wide dynamic range. The demodulated signal has a bandwidth below 150 MHz.

6. The variable gain amplifier post-amplifies and conditions the demodulated signal. The VGA may be configured in an automatic gain control (AGC) loop.

7. The signal is split five ways.

8. Four of these signals are further conditioned and passed into threshold detection logic. High speed comparators trigger at specific adjustable voltage thresholds and output LVTTL logic. Refer to these signals as channels 1-4 and 5-8 for receivers A and B, respectively.

9. The fifth signal (output of the VGA) from receivers A and B are feed into high speed comparators with low thresholds voltages. The output signal feeds into an OR gate, which has LVTTL output. Let us refer to the output of the OR gate as the start timer signal.

10. The start timer signal is connected to T_start on the ATMD-GPX module. Outputs from the high speed comparators (CH 1-8) are connected to T_stop 1–8 on the ATMD-GPX module, respectively.

11. The ATMD-GPX system accepts a rising or falling pulse on any input to indicate a start or stop time. In simplest case above, a rising edge on T_start will start an accurate internal timer. When a rising edge reaches each T_stop input, the stop times with respect to the start time are recorded to registers within the GPX.
12. The stop times are retrieved from the registers using one of the methods discussed later in this thesis.

13. Assuming the signal voltage is high enough, each receiver will have four stop times that correspond to various thresholds. The stop times that correspond to the identical threshold voltages between receiver A and B are subtracted to yield TDOA.

It is worth noting that while this prototype is designed to cover S-band, a LPF with a corner frequency of 4 GHz is included to suppress out of band noise. Technically, one would want to use a 2-4 GHz band-pass RF filter if only S-band is desired. The purchased wideband preamplifier, however, operates from 20 MHz to 4 GHz, so this prototype can actually accept signals within this frequency span.

An earlier discussion pointed out that one of the pitfalls of TDOA DF techniques is their inability to estimate DOA or AOA for CW signals. A secondary on-board amplitude comparison system would allow DF estimation (albeit, with lower accuracy) for CW signals. Such a system could also serve as a second reference when estimating AOA. The proposed architecture includes demodulating logarithmic amplifiers in both receiver channels. As we will see shortly, the output voltage of a logarithmic amplifier is proportional to the input power. Thus, a common function of the logarithmic amplifier is to detect the power of incoming signals. A simple analog to digital converter would provide the necessary signal to calculate AOA based on amplitude alone. High speed ADC’s can be found in compact packages, so adding this functionality would not significantly increase board real estate. Additionally, emitter classification is a vital function of modern DF systems, so an ADC is obligatory to digitize the demodulated signal in a deployed unit.

Each component in the block diagram will now be discussed in detail in the following subsections.
3.2.1 Antennas

A practical short baseline TDOA DF system requires antennas that are extremely wideband and have reasonably broad beamwidths that do not vary extensively with frequency. Cavity-backed spiral antennas are a good solution as the technology is mature, designs are straightforward, and they are commercially available. Another nice attribute of these self-complementary structures is they are circularly polarized, which is a highly desirable characteristic for direction finding. A circularly polarized antenna has the capability to receive horizontal, vertical, and the matched sense of circular polarization. The polarization mismatch loss to receive linear polarizations is only 3 dB, which is extremely desirable. While the opposite sense of circular polarization cannot be received, dual-polarized antenna configurations exist that eliminate this shortcoming. It is for these reasons that cavity-backed spirals are one of the most useful and popular antennas for microwave direction finding [1]. An examples of spiral antennas are shown in Figure 3.3 and Figure 3.4.

Figure 3.3: 2-18 GHz Equiangular spiral antenna (reprinted with permission [17])

Figure 3.4: 18-42 GHz spiral antenna with radome (reprinted with permission [17])
A viable alternative to spiral antennas is the four-arm sinuous antenna, which lends itself well to dual circular-polarized operation. The feeding network of the sinuous antenna, however, is slightly more complex when compared to two-arm spiral antennas. Horn antennas are another possible solution, but they are more bulky, generally less broadband, and the narrower beamwidth patterns are more suited for DF antenna arrays.

Since this thesis is a preliminary feasibility study, antennas were not included in any lab-bench measurements. Instead, signals are directly injected into the receiver channels. This eliminates unnecessary variables (i.e. distortion effects) caused by antennas, and allows the attention to be focused on other fundamental aspects.

3.2.2 RF Limiter

The purpose of a limiter, as the name indicates, is to protect sensitive components from high power signals. RF limiters are often placed early within a receiver chain to prevent low-noise amplifier burnout. A number of limiter technologies exist, but those of the solid state variety are arguably the most common, including PIN diodes, Schottky diodes, and FET’s. The broadband (2-18 GHz) limiters selected for this design were purchased from Krytar, model KSL2018. They come in a coaxial package with a SMA interface.

3.2.3 Low Noise Amplifier

The purpose of a low noise amplifier (LNA) is to amplify weak signals, thereby allowing further processing by the receiver. They can be found in nearly all RF and microwave receivers in commercial and military applications. To minimize noise that may be added to the received signal, LNA’s are designed to have a small noise figure and moderate to high gain. To understand the usefulness of a LNA, we first define noise factor as the ratio of the signal to noise ratio going into a device, divided by the signal to noise ratio leaving that same device:
\[
F = \frac{\left( \frac{S}{N} \right)_{\text{in}}}{\left( \frac{S}{N} \right)_{\text{out}}}
\]

(3.1)

And the noise figure as the dB value of the noise factor:

\[
NF = 10 \log_{10} (F) = 10 \log_{10} \left( \frac{\left( \frac{S}{N} \right)_{\text{in}}}{\left( \frac{S}{N} \right)_{\text{out}}} \right)
\]

(3.2)

From cascade analysis, following the well known Friis equations [18]:

\[
F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots
\]

(3.3)

where \( F_n \) and \( G_n \) denote the noise factor and gain of the nth device in the amplifier chain. We can conclude that the total noise figure of a receiver is dominated by the first stage, given that the gain of the first stage is sufficiently large, and the noise figure of the second stage isn’t unusually high.

In the case of logarithmic amplifiers, discussed in more detail later, noise figure is not always the most appropriate measure of performance since they do not generally require low noise figures to be useful [19]. A more useful metric is the “measurement floor”, which indicates the minimum power level of a received signal to maintain accuracy.

The wide-band pre-amplifier selected is the Minicircuits ZX60-4016E-S+ [20]. While the typical noise figure of 3.9 is not particularly low, it is cost efficient at less than $50 per amplifier, and sufficient for evaluation of the TDOA concept. It effective in reducing the overall noise figure of the receiver and increasing sensitivity, and comes in a convenient coaxial package with a SMA interface.
3.2.4 Low-pass Filter

RF low-pass and band-pass filters are implemented in receivers to suppress unwanted out of band signals. Filter concepts we well known so an in-depth discussion regarding their behavior is not necessary. The low-pass filter selected for this design is the Mini-Circuits LFTC-4000+ [21]. These low-temperature co-fired ceramic (LTCC) surface mount filters are compact, low-cost, and offer good performance. In addition, two TB-233 evaluation boards were ordered to assess performance and reduce design time.

3.2.5 Demodulating Logarithmic Amplifier

Before continuing, it is sensible to briefly discuss square law - the property that gives logarithmic amplifiers their wide dynamic range. From undergraduate courses in semiconductor theory, we know that the I-V characteristics of an ideal diode may be modeled by an exponential function in the following form:

\[
I = I_S \left( \exp \left( \frac{V_D}{nV_T} \right) - 1 \right) = I_S \left( \exp \left( \frac{qV_D}{nkT} \right) - 1 \right)
\]

(3.4)

where \(I\) is the diode current, \(I_S\) is the reverse bias saturation current, \(V_D\) is the voltage across the diode, \(V_D\) is the voltage across the diode, \(V_T\) is the thermal voltage, and \(n\) is the ideality factor. The I-V curve of a typical semiconductor diode is plotted in Figure 3.5. The forward bias region can be broken into three regions: the square law, transition, and linear. Within the bounds of the square law region the cut-in voltage of the diode has not been reached, and the voltage across a diode is proportional to the input voltage squared. Since power is proportional to voltage squared, the output power is proportional to the input voltage:

\[
V_o = kV_i^2 = kP_i
\]

(3.5)
Note that $k$ and $k'$ are not constants, but functions of input voltage or power level, respectfully. As a result, diodes need to be well characterized since the slope in mV/dB changes with input level. Nevertheless, diodes operated within the square law region may be used as a power measurement device over a reasonable dynamic range, and have high sensitivity.

Figure 3.5: Diode electrical characteristics
There are many instances; however, when higher dynamic range and a linear output voltage slope in mV/dB is desired. Logarithmic amplifiers can meet this requirement by cascading amplifier chains. Each amplifier output has a diode detector, of which each stage feeds into a summing junction. In addition, the amplifiers have linear-in-dB gains and are designed to clip or limit the voltage of a signal to a designed value (on the order of 1 V is common). Thus, a signal at the input will propagate through the chain of amplifiers, eventually clipping as long as the power level of the input signal is above the “measurement floor” mentioned earlier in the low-noise amplifier discussion.

A plot of the input and output voltage characteristics of a typical log amp is presented in Figure 3.8. Notice that the x and y axes are in log and linear scales, respectively, showing the multiple-decade linear-in-dB relationship between $V_{OUT}$ and $V_{IN}$, which can be expressed as:

$$V_{OUT} = V_Y \log_{10} \left( \frac{V_{IN}}{V_X} \right)$$  \hspace{1cm} (3.6)
where \( V_Y \) is the slope, \( V_X \) is the x-axis intercept voltage, and \( V_{IN} \) and \( V_{OUT} \) are the input and output voltages, respectively. The x-axis intercept voltage is generally not reached within the dynamic range of the log amp; rather, it is the intercept if the linear response were extended.

![Logarithmic amplifier transfer function](image)

**Figure 3.7:** Logarithmic amplifier transfer function (reprinted with authorization from [22]. Copyright Analog Devices)

The demodulating logarithmic amplifier selected for the TDOA DF system is the AD8319, manufactured by Analog Devices [23]. The evaluation board version was procured to reduce design time and promptly evaluate performance. Some of the most noteworthy features include a wide bandwidth from 1 MHz to 10 GHz, ±1.0 dB accuracy, 45 dB dynamic range, and a pulse rise/fall time 10 ns/6 ns, respectively. Since it is a demodulating logarithmic amplifier, a RF pulse present at the input will yield the envelope at the output. Note that the signal at the output has a DC offset and is inverted for the AD8319. The signal inversion is due to the negative in dB relationship between input and output voltages, in contrast with the positive slope indicated in Figure 3.8. The DC offset results from the transfer function of the system; as the
input voltage approaches zero, the output voltage approaches a set point of approximately 1.5 V. Thus, increased input voltages cause the signal to deviate from this set point, causing the output voltage to drop.

3.2.6 VGA/AGC

The Analog Devices AD8367 was selected for this design. Some of the most noteworthy features include a 3-dB cutoff frequency of 500 MHz, voltage controlled gain (linear-in-dB) across a range of -2.5 dB to +42.5 dB, an on-chip square law detector for automatic gain control capability, and nominal input and output impedances of 200 Ω. Manual VGA and AGC functionality can be easily changed by incorporating switches into the PCB design.

3.2.7 Threshold Detection

The design, fabrication, and debugging of the threshold detection logic circuitry was one of the most time consuming and challenging aspects of the TDOA study. While the principle of operation is straightforward, numerous complications were encountered in development.

A block diagram of the threshold detection mechanism is illustrated in Figure 3.9. Note that each receiver integrates threshold detection, but only one circuit is shown to illustrate the concept. The ideal waveforms characteristics are drawn as the signal passes through the network, and are indicated by the numbers (1) through (4). A pulse modulated carrier is received and propagates through the RF front end at (1), and passes into a demodulating logarithmic amplifier. The output of the DLVA (2) is the negative envelope of the RF signal, offset by a DC voltage. The signal is then AC coupled via a capacitor and fed into an inverting amplifier, which inverts the envelope to a positive sense and provides a modest amount of gain (3). This signal is then split across five channels and parallel-fed into five high-speed threshold detection circuits. Each threshold detection unit is a 1-bit analog to digital converter (ADC), and outputs a logical “1”
(assuming an active-high system) once the threshold is reached. Four of the threshold detectors are connected to the stop timer inputs of the ACAM ATMD-GPX time to digital converter (which will be discussed in more detail later). The fifth is set to a low threshold voltage (approximately 100 mV) and compared to its counterpart in receiver B via a high-speed OR gate.

The sub-circuit including low-threshold comparators is necessary because it is unknown as to which receiver a signal enters first, and the start timer must be activated before the stop timers, otherwise the rising edge of the pulse will not be measured properly. Another alternative is to introduce a delay within one receiver that is longer than the maximum differential time delay a signal could experience in this DF system. This delay, perhaps produced with a coaxial cable of specific length, could be precisely measured and calibrated out via software post-processing. The maximum possible delay occurs when a signal arrives 90° off boresight of the two antenna array, and propagates parallel to the baseline length.
3.2.8 ACAM Time-to-Digital Converter

Time-to-digital converters (TDCs) are devices that calculate the time interval between infrequent, aperiodic square wave pulses, and produce the measurement data in a digital format. They are used in applications where useful information can be obtained from event timing. Several common applications of TDCs include laser distance meters, pressure sensors, ultrasonic flow meters, and high-speed physics calculations [24]. At the time of writing this thesis, ACAM
is the only company known to the author that offers commercially available TDCs, even though there are abundant academic papers demonstrating high resolution TDCs.

ACAM currently offers three different time-to-digital converters: the GP1, GP2, and GPX. The most significant specifications for these parts are summarized in Table 3.1. Moreover, GPX supports four operating modes, summarized in Table 3.2, which is reproduced from the ATMD-GPX datasheet.

![ACAM GP1](image1.png) ![ACAM GP2](image2.png) ![ACAM GPX](image3.png)

Figure 3.9: ACAM TDC Chips

**Table 3.1: ACAM TDC product comparison**

<table>
<thead>
<tr>
<th>Model</th>
<th>Number of Stop Channels</th>
<th>Resolution</th>
<th>Maximum Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP1</td>
<td>1</td>
<td>125 ps</td>
<td>200 ms</td>
<td>TQFP44</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>250 ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP2</td>
<td>1,2</td>
<td>65 ps</td>
<td>4 ms</td>
<td>QFN32</td>
</tr>
<tr>
<td>GPX</td>
<td>2</td>
<td>10 ps</td>
<td>10 μs</td>
<td>TQFP100</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>81 ps</td>
<td>unlimited*</td>
<td></td>
</tr>
</tbody>
</table>

Technically, if a sufficiently long delay line is used in one receiver channel in the proposed TDOA DF system, only one stop-channel is necessary to measure the relative time of arrival. It is beneficial, however, to sample and average the relative time of arrival of two pulses from adjustable threshold voltages, as this may reduce measurement error when the signal to noise ratio of the pulse is low. This assertion will be tested in Chapter 5. Since the GPX TDC offers more features and flexibility, it was selected over the competitors. Furthermore, ACAM
offers the ACAM Time Measuring Device (ATMD) Evaluation System for its customers, which facilitates learning and decreases development time by giving customers the ability to become familiar with their products. It was due to these benefits that the ATMD Evaluation System for the GPX TDC was procured.

![Figure 3.10: ATMD-GPX Evaluation System (reprinted with permission from ACAM)](image1)

Figure 3.10: ATMD-GPX Evaluation System (reprinted with permission from ACAM)

![Figure 3.11: ATMD-GPX Register Communication (reprinted from [25] with permission. Copyright ACAM)](image2)

Figure 3.11: ATMD-GPX Register Communication (reprinted from [25] with permission. Copyright ACAM)
An image of the ATMD-GPX evaluation kit is presented in Figure 3.10. The metal case houses a motherboard with the AM-GPX plug-in module. The ATMD-GPX offers nine Low Voltage Transistor-Transistor Logic (LVTTL) inputs via SMB jacks and three Low Voltage Positive Emitter-Coupled Logic (LVPECL) inputs via Molex. The GPX is connected to a PCI card via a SCSI cable (although a SCSI protocol is not used). Communication between a PC and the GPX is accomplished through a number of registers on the motherboard FPGA and the AM-GPX module’s FPGA, indicated by the block diagram in Figure 3.11. Data can be read from the ATMD-GPX system via two modes:

1. **Direct Read Mode:** The contents of registers DRA and DR are read periodically. The TDC must be reinitialized after each read by sending a partial or master reset. This mode allows up to 300k continuous measurements per second.

2. **Burst Mode:** The FPGA module controls the measurement, in which the TDC writes data into the motherboard FIFO and reinitializes the TDC automatically. The user reads the data from the motherboard FIFOs. This mode allows a peak of 1 million measurements per second, 300k continuous measurements per second.

While direct read mode is a slightly more natural way to obtain data from the TDC, using burst mode is not particularly difficult, and the speed increase over short measurement intervals is worthwhile. ACAM supplies example C++ code for each mode of operation for its customers, significantly reducing development time. Communication is also possible using LabVIEW, but ACAM admits that there are significant speed advantages to using compiled C++ code over LabVIEW’s graphical “G” language. ACAM also includes with the evaluation kit a LabVIEW-based ATMD-GPX measurement software. While this software is rudimentary and doesn’t offer
any customization, it was sufficient enough for the TDOA study in this thesis. Eventually, however, a custom C++ code interfaced with MATLAB would be extremely beneficial.

Table 3.2: ATMD-GPX Features [25]

<table>
<thead>
<tr>
<th>Mode</th>
<th>Channels</th>
<th>Resolution</th>
<th>Additional Features</th>
</tr>
</thead>
</table>
| I-Mode | 8 | 81 ps | 5.6 ns pulse-pair resolution with 32-fold multi-hit capability  
LVTTL inputs |
| G-Mode | 2 | 40 ps | Measuring falling and rising edge, minimum pulse width 1.8 ns  
5.6 ns pulse-pair resolution with 32-fold multi-hit capability  
Differential LVPECL inputs, LVTTL inputs for testing  
Optional quiet mode |
| R-Mode | 2 | 27 ps | Measuring falling or rising edge  
5.6 ns pulse-pair resolution with 32-fold multi-hit capability  
Differential LVPECL inputs, LVTTL inputs for testing  
Optional quiet mode |
| M-Mode | 2 | 10 ps | Measuring falling or rising edge  
Single stop pulse  
Differential LVPECL inputs, LVTTL inputs for testing  
Quiet mode |
Figure 3.12: Measurement timings (reprinted from [26] with permission. Copyright ACAM)

Measuring the time between pulses with the GPX is actually fairly straightforward. A start pulse with minimum width is indicated in Figure 3.12. When this pulse reaches the GPX, it begins counting an internal timer until a second pulse impinges on a stop channel. The timing data is then recorded to several registers for user retrieval.

<table>
<thead>
<tr>
<th>Par.</th>
<th>Time (Condition)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>$t_{ph}$</td>
<td>1.5 ns</td>
<td></td>
</tr>
<tr>
<td>$t_{pl}$</td>
<td>1.5 ns</td>
<td></td>
</tr>
<tr>
<td>$t_{ss}$</td>
<td>0 ns min</td>
<td>9.4 $\mu$s</td>
</tr>
<tr>
<td></td>
<td>***5.2 ns</td>
<td>*unlimited</td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>5.5 ns typ.</td>
<td>6.9 ns max.*</td>
</tr>
<tr>
<td>$t_{rf}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*with int. start retrigger * *with StopDisStart = 1
CHAPTER 4: DESIGN, SIMULATION, AND FABRICATION

The previous chapter focuses on a high-level design of the TDOA DF system under study in this thesis. The next logical step is to select commercially available IC’s, design circuits, and simulate their performance. Designs include the variable gain amplifier with optional automatic gain control, as well as the threshold logic board that interfaces with the ATMD-GPX evaluation kit. The other components in the TDOA block diagram were obtained from commercial vendors such as Mini-Circuits.

4.1 Threshold Logic

4.1.1 Design and Simulation

Part of the design process of the threshold logic circuitry was to assess performance of selected IC’s using a software tool. Normally Agilent ADS would be used for RF designs, but since the maximum frequency of the signal is below 200 MHz, a more appropriate tool would be a SPICE simulator. A plethora of SPICE software is available on the market, but Linear Technology offers a free version named LTspice. LTspice is a sensible option since LT parts were employed in this design, and LT SPICE models are optimized for the LTspice simulator. The design is very closely modeled after the block diagram in Figure 3.9, so readers should use this as a reference.

A schematic of a threshold logic board from one receiver is shown in Figure 4.1. The Analog Devices AD8319 log amp does not a SPICE model available; instead it is modeled as an inverted pulse train with a DC offset. The pulse train has the characteristics indicated in Table 4.1. Note that a white noise source of ±50 mV was added to account for real-world performance. The added noise is more than sufficient, as ±50 mV is at least one order of magnitude greater.
than the noise generated by the AD8319, assuming a $90\,\text{nV/\sqrt{Hz}}$ noise spectral density and an output bandwidth of 140 MHz.

Table 4.1: Simulated AD8319 pulse characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse width</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Period</td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td>Rise time</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>Fall time</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>DC offset</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>Amplitude</td>
<td>-0.4</td>
<td>V</td>
</tr>
<tr>
<td>White Noise</td>
<td>±50</td>
<td>mV</td>
</tr>
</tbody>
</table>

To add supplementary gain to the post-demodulated signal and perform to signal inversion, the AD8058 voltage feedback operational amplifier was selected. The specifications of this part exceed the application requirements. A textbook inverting amplifier configuration is used, where the gain is controlled through the ratio of the feedback to the series input resistors. It is worth noting that later on, this sub-circuit was removed in favor of the previously discussed VGA with AGC capabilities.

The selection of the type of comparator to achieve threshold detection is a critical design decision. They must be high-speed and reliably trigger at predetermined threshold voltages to accurately compute TDOA. These devices should also have low propagation delay, low variation in propagation delay between parts, low timing jitter, high slew rates (short rise/fall times), and be capable of LVTTL output. Linear Technology LT1721 quad high-speed (4.5 ns) comparators were chosen in a 16-lead SOIC package to perform threshold detection for threshold logic detection. Due to their importance, a few significant timing parameters of these comparators are summarized in Table 4.2.
Table 4.2: Notable LT1720/1721 timing specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation Delay</td>
<td>4.5</td>
<td>ns</td>
</tr>
<tr>
<td>Differential Propagation Delay</td>
<td>0.3</td>
<td>ns</td>
</tr>
<tr>
<td>Rise time</td>
<td>2.5</td>
<td>ns</td>
</tr>
<tr>
<td>Fall time</td>
<td>2.2</td>
<td>ns</td>
</tr>
<tr>
<td>Timing Jitter (Low→High)</td>
<td>15</td>
<td>ps$_{RMS}$</td>
</tr>
<tr>
<td>Timing Jitter (High→Low)</td>
<td>11</td>
<td>ps$_{RMS}$</td>
</tr>
<tr>
<td>White Noise</td>
<td>±50</td>
<td>mV</td>
</tr>
</tbody>
</table>

Finally, it is worth mentioning that stable DC power is supplied to the circuits, and comparators for threshold detection. Common LM317 voltage regulators were used for this task. For threshold detection, extremely stable voltages below 100 mV may be necessary, however, and the LM317 can provide variable DC supply down to only ~1.25 V. It is for this reason that resistive dividers were used. Care was taken to place sufficiently large capacitors at input of each non-inverting comparator input to filter out noise that may be introduced. Each IC was also properly bypassed with ceramic and tantalum capacitors to mitigate noise.
Figure 4.1: Threshold logic schematic (single receiver)
Figure 4.2: LTspice results - \( T_{\text{stop}} \) threshold voltages
A transient simulation from zero to 200 ns was executed. The results in Figure 4.2 indicate that the $T_{\text{stop}}$ threshold voltages are free of noise, presumably due to the use of the LM317 voltage regulator and proper use of filtering capacitors. Figure 4.3 present the waveform outputs at different stages of the circuit. $V_{\text{in}}$ represents the simulated noisy output of the logarithmic amplifier. $V_{\text{opamp}}$ shows the output after the coupling capacitor and inverting amplifier, set to a gain of magnitude 2.5. $V_{\text{out1}}$ through $V_{\text{out4}}$ indicate the waveform output from the LT1721 quad comparator. Fortunately, performance is simulated to be in-line with predictions.

The simulation results above do not take into account the circuitry necessary to generate the start timer pulse ($T_{\text{start}}$). Recall from Figure 3.12 that the GPX requires a pulse on the $T_{\text{start}}$ input to tell the unit to begin counting, and then pulses on the $T_{\text{stop}}$ channels to measure time. This signal is obtained by using two comparators with very low threshold values and performing an OR operation, as indicated in Figure 3.9. The sub-circuit to fulfill this operation is shown in Figure 4.4. Note that the circuitry for both receivers, while not shown, is identical to Figure 4.1.
The LT1720 comparators used for this “start timer” circuit share the same core design as the ones previously used, but the LT1720 package houses two comparators versus the LT1721’s four. LM317’s were placed where highly regulated DC supplies were necessary. To perform the OR function, a high-speed OR gate (TC7SZ32F in a SSOP-5 package, produced by Toshiba) was selected. A SPICE model for this part was unable to be procured, but a user-defined model was created that matches the specifications such as $t_{\text{PLH}}, t_{\text{PHL}}, V_{\text{OH}},$ and $V_{\text{OL}}$ found in the datasheet.

A transient simulation from zero to 200 ns was performed to assess the performance of the start timer sub-circuit. The purpose of the simulation is to ensure that $T_{\text{start}}$ occurs before $T_{\text{stop}}$ 1 through 8. The simulation setup is identical the analysis of the single receiver $T_{\text{stop}}$ threshold.

Figure 4.4: Threshold logic (start timer sub-circuit)
detection performed previously, but the following adjustments were made to the circuit’s characteristics:

1. The $T_{\text{stop}}$ threshold voltages were adjusted to 400, 600, 800, and 1000 mV by adjusting the voltage division resistors. This broadens the timing window between $T_{\text{start}}$ and $T_{\text{stop1}}/T_{\text{stop5}}$.

2. The $T_{\text{start}}$ threshold was set to 100 mV.

3. The magnitude of gain for the inverting amplifier was increased from 2.5 to 3, resulting in a pulse amplitude of approximately 1.2 V.

4. The input signal characteristics are unchanged, with the exception that receiver B’s signal was delayed by 200 ns to simulate an emitter off boresight.

The results in Figure 4.5 demonstrate stable threshold voltages, owing to proper capacitor placement, supply bypassing, and tight voltage regulation. Also shown is the output of the inverting amplifier from receiver confirming a gain magnitude of 3.

![Figure 4.5: New $T_{\text{start}}$ and $T_{\text{stop}}$ threshold voltages and inverting amplifier output.](image-url)
The output of the start timer and lowest threshold stop timers are plotted in Figure 4.6. The results indicate that $T_{\text{start}}$ does indeed occur before $T_{\text{stop1}}$ and $T_{\text{stop2}}$, and that the stop timers are separated by 200 ps.

4.1.2 PCB Board Layout

After successful simulation, schematics for the start timer and stop timer PCBs were created using Cadsoft EAGLE. EAGLE is a powerful tool for designing PCBs that has a small learning curve when compared to other commercially available layout editor software. Additionally, EAGLE is available as freeware, only restricting the board size to 100 x 80 mm, which is more than sufficient for the threshold logic PCBs. The full schematic and board layouts are available in Appendix A.

Astute observation of the LTspice and EAGLE schematics indicate that several static resistors were replaced with 25-turn trimming potentiometers. While bulky, these devices add precise adjustment capability to threshold voltages, inverting amplifier gain, and DC supply to
important IC’s. Additionally, the input and output cable interfaces are now defined. While bulky, BNC was chosen because the ATMD-GPX system is supplied with 9 male BNC to SMB plug cables. While SMA or SMB cables would further miniaturize the board, the cost of purchasing 9 new cables of near equal length is unjustifiable for the study in this thesis.

For convenience, downscaled top and bottom layouts for the threshold logic PCBs are displayed above. Note that the bottom side layouts are mirrored so all components appear aligned when the layers are stacked; this is the standard for PCB layout editors.

The PCBs are dual-sided with through-hole components on the top layer, and surface-mount on the bottom. While as many surface mount components were used as possible to minimize board size, chip capacitors were not on-hand at the time of fabrication, so through-hole
were substituted. A wide selection of chip capacitors were procured at a later date and used in subsequent designs and when making minor modifications when debugging the circuit.

4.1.3 Fabrication

The threshold logic boards were fabricated on 0.062” thick FR4 using a LPKF ProtoMat S100, a high performance PCB rapid prototyping machine. The sequences of steps from the initial design to a finished product are enumerated in Table 4.3. Photos of the finished boards are presented in Figure 4.11 and Figure 4.12.

Table 4.3: Design and fabrication process summary

<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Design</td>
<td>The circuits were designed and verified with LTspice simulation software</td>
</tr>
<tr>
<td>2</td>
<td>Layout</td>
<td>Cadsoft Eagle was used for the schematic entry and board layout. The CAM processor was then used to export the necessary Gerber files.</td>
</tr>
<tr>
<td>3</td>
<td>Tool</td>
<td>The Gerber files were imported into LPKF CircuitCAM 6.1, a software interface to CAD/EDA systems. The isolation, drilling, and contour routing</td>
</tr>
<tr>
<td></td>
<td>Routing</td>
<td>paths were set, and the result was exported as a LMD file.</td>
</tr>
<tr>
<td>4</td>
<td>Milling</td>
<td>The LMD file was imported into LPKF Boardmaster, which actively controls the LPKF ProtoMat S100. The PCB was then milled.</td>
</tr>
<tr>
<td>5</td>
<td>Tinning</td>
<td>To prevent copper corrosion and facilitate soldering, board was cleaned, scrubbed, and tinned via an electro-less tin plating solution named</td>
</tr>
<tr>
<td></td>
<td></td>
<td>“Tin It”.</td>
</tr>
<tr>
<td>6</td>
<td>Soldering</td>
<td>Components were hand soldered via a Weller WES51 temperature controlled soldering station.</td>
</tr>
<tr>
<td>7</td>
<td>Testing</td>
<td>The boards were tested and debugged.</td>
</tr>
</tbody>
</table>
4.2 Variable Gain Amplifier

4.2.1 Component Selection and Design

The AC component of the signal output of the AD8319 log amp may vary from several tens of millivolts to 1.5 volts, depending on the received power. Attractive features such as linear-in-dB gain over a wide dynamic range and integrated AGC capability are compared for
two high performance Analog Devices VGAs in Table 4.4. The data was retrieved from the part’s respective datasheets [27] and [28].

Table 4.4: Comparison between high performance analog VGAs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AD8367</th>
<th>AD8368</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Variable Gain Range</td>
<td>-2.5 dB to +42.5 dB</td>
<td>-12 dB to +22 dB</td>
</tr>
<tr>
<td>Gain Accuracy</td>
<td>±0.2 dB</td>
<td>±0.4 dB</td>
</tr>
<tr>
<td>3 dB Bandwidth</td>
<td>500 MHz</td>
<td>800 MHz</td>
</tr>
<tr>
<td>Integrated RMS Detector</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Input/output Impedance</td>
<td>200 Ω</td>
<td>50 Ω</td>
</tr>
<tr>
<td>Package</td>
<td>14-lead TSSOP</td>
<td>24-lead LFCSP</td>
</tr>
<tr>
<td>Adjustable AGC setpoint</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

The data in the table suggests that either VGA is suitable, but the AD8368 was initially selected due to the flexibility of adjusting the AGC setpoint. Analog Devices was also kind enough to provide an evaluation board of the AD8368 through their university program. Unfortunately, the AD8368 on the evaluation board began to behave erratically for unknown reasons several days into testing; the signal would “bounce” back and forth between the VGA setpoint and the input signal voltage level. A custom schematic and layout based on the evaluation board were created using EAGLE, and the circuit was fabricated. Regrettably after four fabrications, these designs also failed to operate correctly, exhibiting similar bouncing effects until the ICs failed to function. The culprit is thought to have been thermal damage as the AD8368 was hot to the touch, but nine thermal vias were installed and soldered to the exposed pad beneath the LFCSP package to reduce thermal and electrical impedance. Another possibility is failure to properly solder the 0.5 mm pitch 4 mm x 4 mm LFCSP 24 package, causing a contact failure or short. Various soldering methods were attempted; however, including temperature monitored reflow, hot air, and traditional iron.
Alas, the prudent decision was to switch to the AD8367, which shares a very similar architecture with the AD8368, accelerating the design process. Like the AD8368, design was based off the information provided in the datasheet as SPICE models were not available for these parts at the time of writing this thesis. The circuit was designed so VGA and AGC operation could be switched by swapping two resistors and removing a capacitor. Input and output signal interfaces are female SMA end-launch connectors to enable easy device characterization, testing, and prototype integration. Additionally, high-performance surface-mount components were used for all resistors and capacitors. The full schematic is available in Appendix A.

4.2.2 PCB Board Layout

As with all PCB designs in this thesis, schematics and layouts for the VGA circuit were created with Cadsoft EAGLE. For convenience, downscaled top and bottom layouts for the threshold logic PCBs are displayed in Figure 4.14 and Figure 4.15; enlarged diagrams are available in Appendix A.

![Figure 4.14: EAGLE layout of VGA in AGC loop (top)](image)

![Figure 4.15: EAGLE layout of VGA in AGC loop (bottom)](image)

4.2.3 Fabrication

The variable gain amplifiers were fabricated on 0.062” thick FR4 using a LPKF ProtoMat S100 milling machine. The sequences of steps from the initial design to a finished product are
listed in Table 4.3, with the exception of that a reflow soldering approach was used for all SMD components.

Figure 4.16: Fabricated VGA with optional AGC functionality
CHAPTER 5: SETUP AND MEASUREMENTS

In this chapter, real-world performance of the TDOA DF system is simulated through several tests in a laboratory environment. A signal delay, which would normally manifest due to off-boresight alignment with an emitter, can be realized through the insertion of a coaxial cable in one receiver channel. The propagation delay of such a coaxial cable, presumably having a SMA interface, can be accurately characterized using a vector network analyzer (VNA). This approach enables study of the system in a stable laboratory environment, mitigating outside interference. While evaluation of the proposed TDOA DF system outdoors or within a large anechoic chamber is undoubtedly a necessary step in the research and development process, it is critical to first assess the feasibility of such a system in a more controlled fashion.

5.1 Cable Delay Characterization

Accurate characterization of cable propagation delay is of utmost importance as it serves as a basis for evaluating the TDOA DF system’s performance. One way to perform this measurement is to use a time-domain transform function on a VNA. When using this method, however, the user must consider the Fourier transform relationship between the bandwidth over which a calibration is carried out and time-domain resolution. Recall that the Fourier transform of a rectangular function results in a sinc function (albeit with different amplitude), and that the width of this sinc function is inversely proportional to the width of the rectangular function. Thus, as calibration bandwidth increases, time-domain resolution increases as well since smaller fluctuations in the signal become more discernable. Another important factor to consider is the number of points, as this affects the maximum record length in time that can be attained before aliasing occurs.
To ensure maximum accuracy and sufficient record length, a 1-port calibration was performed using the settings in Table 5.1. Measurements of $S_{11}$ were recorded with an Agilent N5230A 40 GHz VNA. Two cables were selected for characterization: a 1.5 ft black cable, and a 10 ft blue cable.

Table 5.1: VNA 1-port calibration settings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Frequency</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Stop Frequency</td>
<td>18 GHz</td>
</tr>
<tr>
<td>IF Bandwidth</td>
<td>15 kHz</td>
</tr>
<tr>
<td>Number of points</td>
<td>16,001</td>
</tr>
</tbody>
</table>

Figure 5.1: Round-trip propagation delay of 1.5 ft black cable
Figure 5.1 and Figure 5.2 present the plots of $S_{11}$ for the 1.5 ft black cable and 10 ft blue cable, indicating a round-trip propagation delay of 7.657 ns and 29.08 ns, respectively.

To ensure that these measurements are accurate, the cables were re-measured over a 1-port and 2-port calibration. A SMA female-female adapter was added to each cable. This was done to ensure that the reference plane was correct in the 2-port calibration (otherwise, a “through” connector would be required, causing the reference planes to shift to the center of the through standard). Results are presented in Table 5.2 and Table 5.3, concluding that the difference is only 1.7 ps and 9 ps, respectively – well below the GPX resolution in I-mode.

Table 5.2: 1.5 ft black cable with SMA F-F adapter

<table>
<thead>
<tr>
<th>Calibration</th>
<th>One-way Propagation Delay [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>One Port</td>
<td>3.8613</td>
</tr>
<tr>
<td>Two Port</td>
<td>3.8630</td>
</tr>
<tr>
<td>Delta</td>
<td>0.0017</td>
</tr>
</tbody>
</table>

Table 5.3: 10 ft blue cable with SMA F-F adapter

<table>
<thead>
<tr>
<th>Calibration</th>
<th>One-way Propagation Delay [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>One Port</td>
<td>14.5769</td>
</tr>
<tr>
<td>Two Port</td>
<td>14.5778</td>
</tr>
<tr>
<td>Delta</td>
<td>0.0009</td>
</tr>
</tbody>
</table>
5.2 Preliminary Assessment of TDC Accuracy

To mitigate errors and unknown variables that may be introduced in a receiver, the ATMD-GPX system was independently evaluated using the test setup discussed below. The video output of a pulsed RF signal (the envelope) is fed into a 3 dB power splitter. The output of the power splitter is then connected to the $T_{\text{start}}$ and $T_{\text{stop}}$ inputs of the ATMD-GPX interface. A slightly longer cable was connected to the $T_{\text{stop}}$ input to ensure $T_{\text{start}}$ occurs first.

![Measurement setup (calibration)](image)

Due to inherent mismatch in propagation delay along signal paths, a calibration step is necessary (Figure 5.3). The stop time measurements were taken using the ATMD GPX 4.0 software and recorded to a data file. A pre-characterized delay cable was then inserted in the $T_{\text{stop}}$ signal path, and new stop times were recorded (Figure 5.4). A MATLAB script was then written to post-process the data. Since only one stop timer is used, TDOA is calculated by simply subtracting the calibration stop time from the measurement stop time.
Figure 5.4: Measurement setup (delay)

Measurements were taken by inserting the previously characterized 1.5 ft black cable and 10 ft blue cable in the $T_{stop}$ signal path. Results of 1024 samples are presented in Figure 5.5 and Figure 5.6, and indicate an excellent measurement error that is below 100 ps when compared to the VNA measurements.

Figure 5.5: Measured propagation delay for a 36” cable
Figure 5.6: Measured propagation delay for a 10 ft cable

It was hypothesized that signal attenuation would cause a shift in TDOA for a given rise time. Naturally, as frequency increases, a signal will become more attenuated as it passes through a cable of fixed length. TDOA should not vary significantly for low frequency signals when cable runs are electrically short. The RF pulse envelope from the E8257D signal generator was measured with a 16 GHz digitizing Tektronix oscilloscope, and the rise/fall times were determined to be approximately 2.5 ns. Assuming a Gaussian response, the time-bandwidth product is approximately equal to 0.34, which yields a signal 3 dB bandwidth of approximately 136 MHz. Signal attenuation at these frequencies was measured to be less than a tenth of a dB, which would have a very small effect on TDOA.
To verify the adverse effect of larger attenuation on TDOA, a 6 dB RF attenuator was inserted in the T\textit{stop} channel after the delay line. The total propagation delay of the cable and attenuator were measured as well. Results are presented in Figure 5.7 and Figure 5.8.

Figure 5.7: Measured propagation delay for a 36” cable with a 6 dB attenuator

Figure 5.8: Error in time measurement (VNA - TDC) for a 1.5 ft black cable and 6 dB attenuator

TDOA error
Figure 5.8: Measured propagation delay for a 10 ft cable with a 6 dB attenuator

Clearly, a 6 dB mismatch between the signal paths has an adverse effect on TDOA performance. The reason for the high degree of error in rms error (the measurements “spike” continuously) is most likely attributed to the attenuated signal now being below ideal LVTTL operating voltages. In the future, it would be better feed the envelope signals into high-speed comparators so the output is properly conditioned to LVTTL logic. This study, however, was conducted early on, before the threshold logic boards were fabricated. Nevertheless, one can still conclude that amplitude mismatch between channels must be accounted for when desiring accurate TDOA measurements.

5.3 TDOA performance with AGC

A block diagram of the measurement setup is presented by Figure 5.9. The RF front end before the demodulating logarithmic amplifier is removed for this study. Note that the VGA is
configured in an automatic gain control loop with a $V_{\text{rms}}$ setpoint of 354 mV, as long as the crest factor is less than 5 [27]. The AGC operation requires that the AD8367 is operated in “LO” mode, yielding a decreasing linear-in-dB gain function with respect to voltage applied to the GAIN pin. The negative slope results in signal inversion, the AD8058 inverting amplifier is no longer needed and bypassed using a short jumper wire. The E8257D signal generator settings are listed in Table 5.5. The threshold voltages were set to 400, 600, 800, and 1000 mV for $T_{\text{start}}$.

Table 5.4: Threshold voltage values

<table>
<thead>
<tr>
<th>Threshold Voltage</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{thA}}$, $V_{\text{thB}}$</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{\text{th1}}$, $V_{\text{th5}}$</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{\text{th2}}$, $V_{\text{th6}}$</td>
<td>600</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{\text{th3}}$, $V_{\text{th7}}$</td>
<td>800</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{\text{th4}}$, $V_{\text{th8}}$</td>
<td>1000</td>
<td>mV</td>
</tr>
</tbody>
</table>

Table 5.5: Signal Generator Settings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>-10</td>
<td>dBm</td>
</tr>
<tr>
<td>Frequency</td>
<td>4</td>
<td>GHz</td>
</tr>
<tr>
<td>Modulation Type</td>
<td>Pulse</td>
<td></td>
</tr>
<tr>
<td>Period</td>
<td>5</td>
<td>µs</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>1</td>
<td>µs</td>
</tr>
</tbody>
</table>

Figure 5.9: Measurement setup
As mentioned previously, the AGC setpoint of the AD8367 cannot be adjusted, unless external circuitry is used. This hindrance requires a custom AGC loop or post-AGC amplification. Consider a square-wave with a constant rms voltage and fixed period: as the pulse width decreases, the amplitude must increase in order for the signal to retain the same RMS voltage. When the crest factor is small, the 354 mV rms setpoint does not produce a square wave that with large enough amplitude to trigger all of the preset threshold voltages. Before designing a custom AGC loop or adding a post-amplifier, it seemed prudent to assess TDOA performance, even if not all $T_{stop}$ channels are triggered.

The measurement procedure closely resembled that in section 5.2. The stop times for 1024 samples were recorded using the ATMD GPX 4.0 software prior to adding a delay line. A coaxial cable was then inserted in receiver “A” after demodulation. The reasoning for inserting the delay after the DLVA is signal attenuation was proven to be negligible post-demodulation,
having little effect on TDOA. The following explanation legitimizes this study. In a real-world scenario, two antennas would receive a signal that has traveled over, at minimum, several kilometers. The additional attenuation a signal would incur over a short baseline of 2 meters is also negligible. In other words, a DF system designer would not need to consider attenuation due to free-space propagation.

Figure 5.11: TDOA results (1.5 ft black cable) with AGC
Figure 5.12: TDOA results (10 ft black cable) with AGC

Calculation of TDOA, following calibration, for the 1.5 ft black cable and 10 ft blue cable are presented in Figure 5.11 and Figure 5.12. The signal amplitude was strong enough to trigger only the first two thresholds in each receiver. The mean of the TDOA signals was calculated and plotted against the raw measurements, alongside the cable propagation delay measured with a VNA. While the error is tolerable for the 1.5 ft black cable, the 10 ft cable...
measurements were quite erratic, with a mean error that varies over 1.5 ns across 1024 samples. Subsequent measurements (not shown) did not produce improved results. It is thought that the response time of the AGC circuit, which is on the order of microseconds, causes unwanted fluctuations in the signal.

5.4 TDOA performance without AGC

Following uninspiring results, the automatic gain control loop was disabled. The VGA is controlled by a stable DC source that varies from 50 mV to 950 mV. To this end, a simple voltage regulator circuit with two trimmer potentiometers was fabricated on a mini project board. The VGA was operated in “LO” mode, yielding a linear-in-dB gain with respect to the voltage applied to the GAIN pin. The negative slope results in signal inversion, the AD8058 inverting amplifier is no longer needed and bypassed.

Figure 5.13 is a picture taken of the updated setup. Tests resumed with the signal generator settings outlined in Table 5.6. The threshold voltages were not modified. Two measurements were taken and analyzed, and will be discussed next.

Table 5.6: Signal Generator Settings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Power</td>
<td>-20</td>
<td>dBm</td>
</tr>
<tr>
<td>Frequency</td>
<td>3</td>
<td>GHz</td>
</tr>
<tr>
<td>Modulation Type</td>
<td>Pulse</td>
<td></td>
</tr>
<tr>
<td>Period</td>
<td>5</td>
<td>µs</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>1</td>
<td>µs</td>
</tr>
</tbody>
</table>
5.4.1 Measurement 1

The stop times in absence of a delay cable, which are used for calibration, are plotted in Figure 5.14. The solid and dashed lines indicate samples retrieved from receivers A and B, respectively. Also note that matching line colors refer to identical threshold trigger voltages. The threshold values remain unchanged from the measurement with the VGA in an AGC configuration. Similar to before, a MATLAB script was created to generate the plots and apply error correction.
Figure 5.14: Stop time calibration data

TDOA results following calibration for both the 1.5 ft (Figure 5.15) and 10 ft (Figure 5.16) delays are favorable. For reasons not yet known, the 800 mV threshold seems to perform well for both the black and blue cables. In a second measurement, we will see whether or not a pattern forms. The source of the rapid fluctuation in (CH 3 – CH 7) is currently unknown, but subsequent measurements indicate this is most likely an anomaly.

In addition to calculating TDOA for the paired thresholds across receivers A and B, an average was taken of the calculated TDOA curves to assess whether or not averaging reduces error. Results from measurements of the 1.5 ft black cable indicate an error less than 100 ps for the averaged TDOA (magenta). Likewise, the averaged TDOA for the 10 ft blue cable is quite encouraging – near 50 ps.
Figure 5.15: TDOA results (1.5 ft black cable)
Figure 5.16: TDOA results (10 ft blue cable)

- Difference in stop time with 10 ft blue cable

- Error in time measurement (VNA - TDC) with 10 ft blue cable

Data for Sample Numbers 0 to 1000.
5.4.2 Measurement 2

Prior to taking a second measurement, it was discovered that several of the BNC connectors on the PCB were becoming loose. To avoid potential issues, bonding posts were strengthened and extra solder was added to the signal lines (they were not disconnected, but becoming weak). Additionally, the LM317’s were beginning to get quite hot, so the supply was switched from +12 V to +5V, reducing thermal load. Finally, the threshold voltages were retuned to their nominal values, as they had drifted since the PCBs were fabricated (or quite possibly the potentiometers were bumped in the process of mounting). Following these adjustments, data was gathered for post processing matching the procedure in the first measurement. The results are presented in Figure 5.17 and Figure 5.18.

The 800 mV threshold pairs have again produced accurate TDOA for the 1.5 ft and 10 ft cables. The reason is not clear from these two simple tests, and prompts further investigation. From the two measurements, it seems reasonable to conclude that averaging the TDOA results for different threshold voltages yields a more accurate estimation of true TDOA.
Figure 5.17: TDOA results (1.5 ft black cable)
Figure 5.18: TDOA results (10 ft blue cable)
CHAPTER 6: CONCLUSIONS

The work presented in this thesis studied the feasibility of using picosecond-resolution Time-to-Digital converters in short baseline Time-Difference-of-Arrival direction finding systems. An inexpensive and potentially versatile prototype DF system has been designed, fabricated, and tested in a laboratory environment. Measurements indicate that through calibration and averaging the stop time data from threshold pairs between two receivers, measurement accuracy on the order of 100 ps to 200 ps can be expected. For short baseline systems, this is theoretically enough to ascertain AOA within several degrees.

This research suggests a practical low-cost short baseline TDOA DF system based off COTS components could be developed. While the hardware designed in this thesis is certainly too bulky for a UAV payload, nearly all components can be replaced with low-power surface mount devices, reducing all hardware to a single multi-layer PCB (except for the antennas). Such a refined system would certainly hold SWAP advantages over current technologies. For these reasons the author believes that continued research and development to realize a deployable system is beneficial to commercial and military applications.
CHAPTER 7: FURTHER RESEARCH

Pending more time, the system could have been further developed in many aspects. It was initially planned to develop C++ code to retrieve data automatically from the ATMD-GPX module, and to use MATLAB MEX files to display retrieved data in real time. MATLAB could be used to demonstrate emitter sorting capability by measuring pulse width, pulse repetition frequency, rise/fall time, and other attributes. In a real-world scenario, it isn’t necessary for the post-processing to be performed on the UAV; timing measurements could be controlled by a FPGA and sent to a remote location for analysis. The following long-term plan was conceived by the author during his internship at Pt. Mugu NAWCWD, if the research were to persist in the future.

Figure 7.1: Long-term task progression
APPENDIX A: SCHEMATICS AND LAYOUTS
Figure A.1: EAGLE schematic of stop timer threshold logic circuit
Figure A.2: EAGLE layout of stop timer threshold logic board circuit (top)
Figure A.3: EAGLE layout of stop timer threshold logic board (bottom)
Figure A.4: EAGLE schematic of start timer board
Figure A.5: EAGLE layout of start timer board (top)

Figure A.6: EAGLE layout of start timer board (bottom)
Figure A.7: EAGLE schematic of VGA in AGC configuration
Figure A.8: EAGLE layout of VGA in AGC loop (top)
Figure A.9: EAGLE layout of VGA in AGC loop (bottom)
APPENDIX B: COPYRIGHT PERMISSION LETTERS
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C: 513-720-7597
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Figure 27 from AD8319 Datasheet
Figure 2 from MT-077 Tutorial: Log Amp Basics
Gain chain figure (p.2 on the left) from: Ask the Applications Engineer - 28: Logarithmic Amplifiers Explained

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--

Kind regards,

Julian Robbins
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Fax +44 (0) 1568 616373

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