Design Of Silicon Controlled Rectifiers Sic] For Robust Electrostatic Discharge Protection Applications

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ABSTRACT

Electrostatic Discharge (ESD) phenomenon happens everywhere in our daily life. And it can occur through the whole lifespan of an Integrated Circuit (IC), from the early wafer fabrication process, extending to assembly operation, and finally ending at the user's site. It has been reported that up to 35% of total IC field failures are ESD-induced, with estimated annual costs to the IC industry running to several billion dollars. The most straightforward way to avoid the ICs suffering from the threatening of ESD damages is to develop on-chip ESD protection circuits which can afford a robust, low-impedance bypassing path to divert the ESD current to the ground.

There are three different types of popular ESD protection devices widely used in the industry, and they are diodes or diodes string, Grounded-gate NMOS (GGNMOS) and Silicon Controlled Rectifier (SCR). Among these different protection solutions, SCR devices have the highest ESD current conduction capability due to the conductivity modulation effect. But SCR devices also have several shortcomings such as the higher triggering point, the lower clamping voltage etc, which will become obstacles for SCR to be widely used as an ESD protection solutions in most of the industry IC products.

At first, in some applications with pin voltage goes below ground or above the VDD, dual directional protection between each two pins are desired. The traditional dual-directional SCR structures will consume a larger silicon area or lead to big leakage current issue due to the happening of punch-through effect. A new and improved SCR structure for low-triggering ESD
applications has been proposed in this dissertation and successfully realized in a BiCMOS process. Such a structure possesses the desirable characteristics of a dual-polarity conduction, low trigger voltage, small leakage current, large failing current, adjustable holding voltage, and compact size.

Another issue with SCR devices is its deep snapback or lower holding voltage, which normally will lead to the latch-up happen. To make SCR devices be immunity with latch-up, it is required to elevate its holding voltage to be larger than the circuits operational voltage, which can be several tens volts in modern power electronic circuits. Two possible solutions have been proposed to resolve this issue. One solution is accomplished by using a segmented emitter topology based on the concept that the holding voltage can be increased by reducing the emitter injection efficiency. Experimental data show that the new SCR can posses a holding voltage that is larger than 40V and a failure current It2 that is higher than 28mA/um. The other solution is accomplished by stacking several low triggering voltage high holding voltage SCR cells together. The TLP measurement results show that this novel SCR stacking structure has an extremely high holding voltage, very small snapback, and acceptable failure current. The High Holding Voltage Figure of Merit (HHVFOM) has been proposed to be a criterion for different high holding voltage solutions. The HHVFOM comparison of our proposed structures and the existing high holding voltage solutions also show the advantages of our work.
To my my parents Qingsheng Liu and Xuemei Zeng
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CHAPTER 1. INTRODUCTION

1.1. ESD and It’s Threatening to Semiconductor Devices

Electrostatic discharge (ESD) is defined as the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field [1]. ESD phenomenon happens everywhere in our daily life. The problem of ESD is also well known. From merely receiving a mild shock after crossing a room and touching a metal object, to sending a shock into electronic equipment, nearly everyone has experienced an ESD problem at some time [2]. The most dramatic affection from ESD we can watch is the lightning [3].

ESD can occur throughout an integrated circuit (IC) lifespan, from early wafer fabrication process, extending to assembly operation, and finally ending at the user’s site. When the ESD pulse happens on the PAD of a silicon chip, it will flow to the ground through the internal circuits. Normally this ESD pulse is possible to damage the internal circuits due to its high peak voltage or high peak current characteristic if there is no ESD protection scheme for the IC or electronic products. It is reported that up to 35% of total IC field failures are ESD-induced, with estimated annual costs to the IC industry running to several billion dollars [4][5][6].

Figure 1.1 (a) to (c) shows the ESD induced damages found in a bulk MOSFET, FinFET [7], and nanowire FET [8], respectively. It is obviously to see the ESD damage can occur at the traditional CMOS technology or even the advanced and prominent technology (Nanowire FET). It is very desirable to conduct more deep investigations on the ESD damage schemes for
semiconductor devices and provide effective on-chip or off-chip solutions to prevent these damages happen to reduce the cost loss during the manufacture.

Figure 1.1 ESD induced damages in (a) 130 nm bulk MOSFET, (b) FinFET [7], and (c) Nanowire FET[8].

1.2. ESD Models and TLP Test

To provide the ESD protection for a silicon chip, it is necessary to characterization the ESD events which happened during the fabrication or shipping procedures. These ESD events can be simulated by different ESD test models categorized according to its origins, upon which on-chip ESD protection circuits can be tested and rated [6]. Based on the different ESD events generation situation, four different kinds of ESD models have been proposed to simulate these different cases, and they are Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM) and IEC model.

HBM: HBM is the most popular ESD event model and widely used as a basic ESD protection criteria for the semiconductor products at industry. It can simulate the discharge procedure of a charged human body directly into a device. A simple equivalent circuit model described in Figure 1.2 is used as HBM ESD test. In the circuits, a 100pF capacitor represents
the charged human body and the 1500ohm resistor is used to model the discharging resistance of human body [6][9][10].

![RLC network reflecting normal human body effect](image)

Figure 1.2 A HBM ESD model circuit, where the RLC network reflecting normal human body effect [6].

MM: Machine model is an ESD test standard method originated from Japan. And it is intended to model ESD stress produced by charge metallic machinery making contact with IC components. Such can happen in an IC manufacturing environment during device bonding, assembly or during ATE (automatic test equipment) test. The MM equivalent circuit model is similar as HBM model shown in Figure 1.2, however with different parameters: $C_{ESD} = 200\text{pF}$ and negligible $R_{ESD}$ and $L_{ESD}$ [6][11][12].

CDM: Charged Device Model is different from the HBM and MM. The CDM ESD event is a one pin self-discharge event resulting in gate oxide breakdown or metal burn-out inside the IC. These failures are related to the voltage build-up across the elements of the discharge path in the chip [6][13]-[15].

IEC: IEC model is intended to model the discharge from a person holding a metallic object in a hand to an electronic system. It will produce extremely short rise time, and very high current peaks. IEC was initially developed as a system ESD model. However it is being used for
IC chip ESD characterization recently to reflect tougher ESD protection demands. The sub-ns rise time ESD pulse property makes IEC ESD protection design very challenging in practical IC design [6][16].

All of the above introduced ESD test model are destructive and they are used to check the failure threshold of an ESD sensitive device but do not give an insight on the possible failure mechanisms. To overcome the common disadvantageous feature shared by all existing ESD test models, a testing method with the name of Transmission Line Pulse (TLP) test method was introduced by Tim Maloney in 1985 [17]. The principle of the TLP measurements is that a piece of a transmission line cable is used to produce a stable square waveform and then discharge into a DUT to simulate ESD stressing events. TLP model is critical to conducting ESD simulation and predictive ESD protection design [6].

1.3. ESD Design Window Introduction

The ESD design window is defined as the solution space in which ESD clamping devices must operate [18]. The protection devices’ I-V characteristic should be restricted in this design window, or they will not act as an efficient protection. To provide full chip ESD protection solution for a specific IC, the understanding of its ESD design window will be the first priority work.

1.3.1. I-V Characteristic for Two Kinds of ESD Protection Devices

Basically there are two kinds of on-chip ESD protection devices to realize the ESD protection purpose. The first one functions as a simple turn-on characteristic as in Figure 1.3 (a),
and it will turn on at the threshold point (Vt1, It1). Before this turn on point, it works at a high-impedance state and there is no current flow through. After it has been turned on, a low-impedance discharge path will be formed to divert the ESD current. The second one has an I-V characteristic with snapback shape as in Figure 1.3 (b). It works as similar as a turn-on characteristic device before the triggering point (Vt1, It1). After that, it will be driven into the snap-back region with a low clamping voltage, and then a low impedance discharge path will be formed at this low clamping voltage point. Both these two kinds of protection devices will be damaged after the second breakdown point (Vt2, It2).

![Graph](https://via.placeholder.com/150)

**Figure 1.3** Typical ESD protection devices with (a) turn-on characteristic (b) snapback characteristic.

The parameters in the above figures are defined as below:

Vt1 --- Triggering voltage or turn on voltage,

It1 --- triggering current or turn on current

(Vt1, It1) --- Triggering point
Vt2 --- second breakdown voltage
It2 --- second breakdown current
(Vt2, It2) --- second breakdown point
Vh --- holding voltage or clamping voltage
Ih --- holding current
(Vh, Ih) – snapback point or holding point
Ron --- turn on resistance

1.3.2. The Description of ESD Design Window

For the two different kinds of ESD protection devices mentioned in the section 1.3.1, the design windows for each of them are listed in the Figure 1.4 (a) and (b) respectively. Different colors are used to differentiate three regions: the internal circuits operational region (blue color), internal circuits failure region (red color) and ESD devices failure region (yellow region) respectively.

The ESD design window is highlighted by three solid green lines. A good ESD protection should have the devices I-V characteristic located in the region with the boundaries of these three solid green lines. Left boundary is the internal circuits’ operational voltage. ESD protection devices should keep at the off state under the normal operational status since we do not wish the internal circuits function will be affected by the ESD protection. For the ESD devices with snapback characteristic, its holding voltage are also be restricted by this left boundary, i.e., it should have a higher holding voltage than the operational voltage. The restriction of holding voltage is used to avoid the potential latch-up issue when the ESD devices are mis-triggered by
external noise at the normal operational situation [19]. The right boundary (VMax) is the minimum damage voltage of internal circuits. It can be the MOSFET’s gate oxide breakdown voltage or drain substrate junction breakdown voltage. ESD protection devices should have a lower triggered voltage or turn on voltage than VMax, or the internal circuits will be damaged before ESD devices response. The top boundary is defined by the required ESD protection level (For HBM model ESD protection, the HBM protection voltage can be converted to the equivalent second breakdown current It2 with this equation: HBM Level = 1500 x It2). In order to satisfy the required ESD protection capability, ESD protection devices’ second breakdown current should be higher than the top boundary.
In the above ESD design window, the devices with snapback characteristic should have a holding voltage higher than the operational voltage to avoid the possible latch-up issue. But there is an exception for the high holding current SCR (HHI-SCR) device which has been reported in the paper [20]. By adopting a SCR with an increased holding current above the minimum latchup threshold current (I_LU), HHI-SCR can still be latch-up immunity no matter the situation that its holding voltage is lower than the operational voltage. The reason is that the external noise current is not large enough to exceed the HHI-SCR’s holding current value and make it run into the latch-up state.
1.3.3. The Ideal ESD Protection Devices

Basically an ideal ESD protection device should be transparent during the normal operational condition and have zero resistance to conduct all of the ESD current when ESD events happen. In the design window of Figure 1.4, the red solid line is used to demonstrate the characteristic of an ideal ESD protection device. We can summary the conditions for an idea ESD protection as below [21]:

Zero on resistance – It will allow the device to shunt large amount of ESD current with no ohm voltage drop.
Finite clamping voltage – The clamping voltage should be lower enough to conduct more ESD current. To avoid unintentional triggering of the protection device, the clamping voltage of the protection device should be higher than the supply voltage with a safety margin.

Minimum silicon area occupied – Smaller device area will lower the chip fabrication cost.

Instantaneous turn-on time and infinite energy absorption – Before the IC chip fails, protection device has to absorb full ESD induced energy as soon as ESD events occurs.

Transparent to circuit operation (i.e., no parasitic) – The protection devices should active only under ESD conditions and cause no parasitic effects on the function of IC chip (leakage current, parasitic capacitance).

Easy fabrication – It can be fabricated compatible with the internal circuits and do not need to add extra mask or fabrication procedure.

1.4. On Chip ESD Protection

1.4.1. On Chip ESD protection Development Flow

A general on-chip ESD protection development flow is described in Figure 1.6. ESD protection design window needs to be defined at first since it will setup the ESD protection goals and design specification. Once the proposed candidate devices for protection have been fabricated, the TLP measurement will be conducted to check these devices’ quasi-static I-V characteristic. Only if its characteristic is located at the pre-defined ESD design window, we can start to combine the ESD protection devices with the core internal circuits together. The final design with ESD protection need to be tested under different ESD test models to make sure that it will pass the expected ESD protection requirements before this product’s mass production.
This development flow is based on the traditional trial-and-error method. As we all know, the semiconductor fabrication is time consuming and expensive especially for those processes under 90nm. Some advanced technology such as TCAD simulation or devices modeling methods have been proposed for semiconductor devices development [22]. But this trial-and-error development flow is still very popular in the industry. Only very few companies have adopted
today’s advanced TCAD simulation and ESD protection device modeling methods for some of their products’ ESD protection developments [23]-[25]. Several issues still need to be resolved before these advanced ESD protection development methods can be widely used in the industry, and they are:

1) TCAD simulation consumes lots of computing resource and memory capacitance, especially for 3D devices simulation.

2) Only after taking a very careful calibration for the parameters in process and devices simulation models, TCAD simulation results can be comparable with the measurement results.

3) The TCAD simulation for snapback type devices is possible to face converging issue during the calculation.

4) Devices physics after avalanche breakdown is very complex, and there are no standard models available for the typical ESD protection devices, such as GGNMOS or SCR. It will be very time and labor consuming for building a group of ESD protection device model on a specific process.

1.4.2. On Chip ESD Protection Devices

Based on our knowledge, the most popular devices frequently used as the working horses for on-chip ESD protection are diode or diodes string, GGNMOS or LDNMOS and SCR. The cross section structures for these three type devices are given in Figure 1.7 and they are built on 0.6um BiCMOS process.
Figure 1.7 The cross section view for three kinds of typical ESD protection devices: (a) Diode (b) GGNMOS (c) SCR.
**Diode and diodes string:**

Diode is simple and widely used as ESD protection. Both its forward and reverse operational mode can be used to conduct ESD current. For diodes working under reverse direction, it has smaller current conduction capability and need to consume large silicon area to reach the expected protection specification. For forward biased diode, it is always combined with power supply clamping devices together to realize a rail based protection. The rail based protection schemes are mostly used for RF ESD protection. Lots of research works have been conducted to optimize diode’s layout topology, diffusion, metal routing etc. to find the structure with the less parasitic capacitance and highest ESD protection capability by consuming the same silicon area[26][27].

Several forward diodes can also be connected serially as diode string. Diode string can be used as power supply clamping, but the Darlington effect existed in the diode string with large number of diodes will lead to a huge leakage current at normal operation which will exceed the highest allowable leakage current specified in the product datasheet[28].

**GGNMOS:**

GGNMOS structure is made from the normal NMOS structure by grounding the gate terminal. It will stay at the blocking state when the applied voltage is lower than its breakdown voltage. More and more leakage current will generate after the triggering voltage and the potential drop at P-Well resistor will help to turn on the Emitter-Base junction of parasitic BJT. A lower turn on resistance will be formed due to the current injection effect after the BJT turn on [29]. Then the ESD current will be diverted through the lateral parasitic BJT in GGNMOS structure.
In all different ESD protection structures, GGNMOS is the most frequently used in the industry. No matter the ESD protection for the IC chips or the standard ESD protection library afforded by foundry, GGNMOS is always been chosen firstly. Even for the advanced process technology lower than 90nm, GGNMOS is still very popular [30]. The reasons can be summarized as: (1) GGNMOS has similar structure as the internal core devices in today’s CMOS technology, and it can be easily layout and fabricated without adding any extra mask. (2) By adjusting its’ channel length or applying gate-coupled structures, its’ triggering voltage can be decreased to be lower than the internal NMOS or PMOS devices’ drain substrate breakdown voltage to act as a protection function.

There are still several issues existed for the development of GGNMOS structures: 1) large protection area is required due to its poor protection capability. 2) Its turn on uniformity needs to be improved to realize a high ESD protection through multi-finger GGNMOS structures. 3) Intrinsic reliability issue and high lath-up risk existed in HV LDMOS devices [31].

**SCR:**

SCR type devices have a low turn on resistance. This merit is attributed to its double injection modulation effect [29]. It can conduct 10 times more current than the normal GGNMOS type devices. But SCR type devices have the following shortcomings: 1) larger trigger voltage, 2) small holding voltage (possible causing latchup effect happen) and 3) low turn on speed (causing overshoot under fast ESD pulse zapping and damage the internal devices under a safe triggering voltage situation).

In this dissertation, most of the work will focus on how to optimize SCR structure for different ESD protection applications.
1.4.3. Full Chip ESD Protection

The ESD events can happen between the combinations of any two pins in a silicon chip with positive or negative polarity. To realize a full chip ESD protection, it is necessary to build ESD current bypassing paths between any two pins with dual direction conducting characteristic. Eight different protection modes have been summarized in [19] and they are listed as below:

1. PS mode: ESD stress at an I/O pin with positive voltage polarity to VSS bus when VDD bus is floating;

2. NS mode: ESD stress at an I/O pin with negative voltage polarity to VSS bus when VDD bus is floating;

3. PD mode: ESD stress at an I/O pin with positive voltage polarity to VDD bus when VSS bus is floating;

4. ND mode: ESD stress at an I/O pin with negative voltage polarity to VDD bus when VSS bus is floating.

5. Positive VDD to VSS ESD stress mode: ESD stress at VDD pin with positive voltage polarity to VSS bus when all the other I/O pins are floating;

6. Negative VDD to VSS ESD stress mode: ESD stress at VDD pin with negative voltage polarity to VSS bus when all the other I/O pins are floating;

7. Positive pin to pin stress mode: ESD stress at one I/O pin with positive voltage polarity to all other I/O pins when the VDD and VSS pins are floating;

8. Negative pin to pin stress mode: ESD stress at one I/O pin with negative voltage polarity to all other I/O pins when the VDD and VSS pins are floating.
Typically there are three full-chip ESD protection topology which can be used to realize the above different protection modes and they are demonstrated in Figure 1.8 (a) to (c). The common power supply clamping unit in these three topologies functions as the positive and negative protection between VDD and VSS.

(a)

(b)
Figure 1.8 Different schematics for full chip ESD protection a) PAD based b) power-rail based c) the combination of power-rail based and PAD based protection d) ESD protection between different I/O pins e) ESD protection for IC with mixed power domains.

The working mechanism of PAD based protection is very straightforward. Six different ESD conducting paths are placed between each two pins to resist different ESD stress mode from (1) to (6).

The power-rail based full chip ESD protection is composed by a power supply clamping unit and two diodes Dp and Dn. The forward working mode of Dp and Dn are used to realize the NS and PD mode protection, but their reverse working mode can’t function as ESD protection between I/O pin and VDD or VSS due to the poor protection capability of reverse diode. In the Figure 1.8 (a), the PS mode protection is realized by the combination of forward conducting of Dp and power supply clamp, and ND mode protection can be realized by the combination of forward conducting of power supply clamp and Dn.
Comparing with PAD based protection, the power-rail based protection will save lots of silicon area since its PS and ND mode are realize by the reusing of the other ESD current paths. The second advantage of this protection scheme is that it can reduce the design complexity since the diodes have been choose as protection unit which is the most simple protection cell. The disadvantage of power-rail based topology is that it can’t be used in the application where a high ESD protection is desired. The reason is the diode structure is not very efficient as an ESD protection unit.

To realize a high ESD protection with the possible less silicon area, the protection topology which combines the power-rail based and PAD-based protection is described in Figure 1.8 (c). In this topology, two conduction paths (1) and (2) are placed between I/O and VSS and they will function as PS and NS protection respectively. The PD and ND mode protections are realized by reusing the ESD path (1) or (2) and power supply clamp. In which, we can choose SCR type structure to work as the ESD conducting path of (1) and (2) and they will make this chip to resist high ESD level easily without causing a large silicon area consuming.

As for the ESD protection of stress mode (7) and (8), they are normally realized by the reusing of the above ESD conduction paths placed at different I/O pin and the power supply clamp. Figure 1.8 (d) demonstrates the ESD current conducting path when a positive ESD stress zaps on I/O1 pin with I/O2 pin grounded.

With the increasing complexity of current IC development technology, some silicon chips adopt multiple power domains. A traditional protection topology for multi power domain is described in Figure 1.8 (e). Back-to-back diodes are placed between different VSS bus lines. For
demonstration, the ESD current conducting path between I/O1 and VDD2 is indicated by blue solid line in Figure 1.8 (e) [25].

1.5. Off-Chip ESD Protection

Except the on-chip ESD protection introduced in the above section, the other type ESD protection method is off-chip ESD protection, for which the ESD unit is fabricated separately and connected with the to-be-protected integrated circuits on PCB board. For today’s electronic products, both on-chip and off-chip protections are required to satisfy the application requirements. There are severe reasons for the necessary of off-chip protection [33]:

1) In the race to provide more and faster functionality, on-chip ESD protection is often sacrificed in favor of chip performance. According to the ESD Association, the ICs of tomorrow will not sustain the current levels (2kV) of on-chip ESD protection. In fact, there is a proposal to lower on-chip ESD stress target levels by more than half. At the system level, as on-chip protection is reduced, ICs will be more sensitive to transients such as cable discharge events and ESD from the human body. With increased ESD sensitivity of current and future ICs, the need to protect systems with more robust off-chip transient voltage suppression is greater than ever.

2) In future high speed applications, a mix of off-chip and on-chip protection may be required to reduce the capacitance loading effect. The off-chip protection can be present in the electrical cables, connectors, ceramic carriers, or on the circuit boards. As the frequency increases, or the material change, the ESD protection may shift to only off-chip protection [33].

3) Additionally, there are a number of present and future technologies where on-chip ESD protection is not feasible from a material perspective. For example, magnetic recording
industry devices, such as magneto-resistor (MR) heads, giant magneto-resistor (GMR) heads, and tunneling magneto-resistor (TMR) heads are formed on nonsilicon substrates [33].
CHAPTER 2. AN IMPROVED BI-DIRECTIONAL SCR STRUCTURE FOR LOW-TRIGGERING ESD PROTECTION APPLICATIONS

2.1. Introduction

Providing adequate electrostatic discharge (ESD) protection solutions to modern and future microchips is becoming more difficult and challenging because of the increasing complexity of the IC’s and continuing scale down of device dimensions. Adding to this complexity is the requirement for some circuits to have pin voltage requirements to go below ground. Normal ESD protection provides a clamp in the forward direction (pin positive) and relies on the body diode for the reverse direction (pin negative). For pins that are required to go below ground, new protection schemes are required.

A straightforward application to demonstrate the above situation is the ESD protection for the transceiver or receiver pins of RS485 interface circuits. RS485 or EIA-485 is a standard defining the electrical characteristics of drivers and receivers for use in balanced digital multipoint systems [34]. It specify the voltage level on the transmission line at the range of [-7V, 12V]. The typical products support RS485 transceivers is ISL317xE serial ICs made by Intersil Incorporation, and it works under the operational voltage of 5V [35]. That means the I/O voltages have exceeded both the power supply voltage and the ground voltage level.

The circuits for RS485 I/O ports (A and B) are given in the Figure 2.1. The traditional ESD protection cell, such as GGNMOS or SCR can be used to protect the ESD pulse from A or B to ground. Regarding the ESD protection from ground to pin A or B, the parasitic body diode
will not work since it will form a direct current flowing path from ground to pin A or B under the normal working condition (the voltage on the I/O pin goes below the ground). As we all known, the ESD protection unit should not have interference to the internal circuits normal operation. To resolve this issue, ESD protection devices or circuits with bi-directional protection capability are desired.

Figure 2.1 I/O circuits for the pin A and B in a typical RS485 transceiver product.

2.2. Prior Arts for Bi-Directional ESD Protection

Regarding the situation mentioned in the above section, a clamping element for both polarities is required. As most ESD devices can only snapback in one direction, more than one ESD devices will be needed at every I/O pin to provide a bi-directional path to discharge the current associated with the ESD event [36]. In the paper [36], a novel dual-polarity device is
composed by two separate SCR structures described in Figure 2.2. The left SCR’s cathode and the right SCR’s anode are connected with the PAD to be protected. The left SCR’s anode and the right SCR’s cathode are connected with the GND pin. Once the positive ESD pulse zapped on the PAD, the right SCR will turn on and conducts the ESD current from PAD to GND. If there is a negative ESD pulse zapped on the PAD, the left SCR will turn on and conducts the ESD current from GND to PAD.

To realize the dual directional ESD protection with two separate SCRs, two important things need to be considered. The first one is that the N+ tap in N-Tub region is disconnected with the Anode in each SCR. By this engineering work, the SCR’s reverse direction will function as a reverse diode instead of a forward body diode in the traditional SCR structure. The second thing is that the SCR’s forward blocking junction’s breakdown voltage should be higher that the breakdown voltage of its reverse parasitic diode. These two conditions guarantee the proposed structure will always work at SCR’s forward conducting mode no matter the polarity of ESD pulse zapped on the PAD. The current paths under different ESD polarity are indicated by red solid line in Figure 2.2.
To reduce the die area and parasitic effect, a single ESD device that snapback in both the positive and negative directions is more desirable. A bi-directional SCR device has been developed recently [37]. The device is capable of dual-polarity snapback, has a trigger voltage higher than 15 V, and a relatively small leakage current. The trigger voltage of such an SCR device could be reduced, but doing so will result in a significant increase in the leakage current [37].

Figure 2.3 Conventional bi-directional SCR device using the NPNPN structure
In this chapter, we are going to develop an improved bi-directional SCR structure for ESD applications that require a dual-polarity protection, low trigger voltage, small leakage current, and adjustable holding voltage.

2.3. Operation Principles of the Novel Bi-Directional SCR

The cross-sectional view of a conventional bi-directional SCR structure is given in Figure 2.3 [37]. Two SCRs, namely SCR1 and SCR2, are imbedded in the structure, as indicated in the figure. When Terminal 1 is subject to a positive ESD stress related to Terminal 2, the N-P-N-P SCR1 will turn on, and there will be a conducting path from Terminal 1 to Terminal 2. Likewise, the P-N-P-N SCR2 will turn on to discharge the ESD current from Terminal 2 to Terminal 1 when Terminal 1 is subject to a negative ESD stress relative to Terminal 2. Thus, it provides a bi-directional ESD protection and possesses an S-shape current-voltage (I-V) characteristic in both the positive and negative directions.

In general, the trigger voltage of an SCR structure is determined by the avalanche breakdown mechanism at the forward blocking junction (FBJ). The FBJ’s of SCR1 and SCR2 are marked as FBJ1 and FBJ2 in Figure 2.3 respectively, which are formed by the N-well/P-well junction with a reverse breakdown voltage around 20 V. This trigger voltage is too high for most modern MOS-based integrated circuits. To reduce the trigger voltage of the bi-directional SCR, a smaller dimension of D4 in Figure 2.3 has been recommended. Using this approach, the SCR triggering will be controlled by the punch through mechanism in the P-well region (i.e., D4 region) sandwiched between the N+ and N-well regions, instead of the avalanche breakdown at
the FBJ. As D4 is reduced, the overlap of the depletion regions associated with the N+/P-well and P-well/N-well increases, and consequently the trigger voltage decreases. Unfortunately, punch through gives rise to a much larger leakage current.

To alleviate this drawback, we propose a new SCR structure aiming at producing a trigger voltage of less than 15 V while keeping the leakage current in the nano-Ampere range. The schematic of such a bi-directional device is shown in Figure 2.4. It is constructed by adding two extra P+ doping regions BP1 and BP2 in the conventional bi-directional SCR device, a concept similar to that proposed by Chatterjee and Polgreeen for one-directional SCRs [38]. With these two P+ regions, FBJ will be the P+/N-well instead of P-well/N-well junction. As a result, a lower trigger voltage for both the positive and negative directions can be obtained. Alternately, the P+ regions could be replaced with N+ regions and the blocking junction would be N+/P-well. For the process we are using, the P+/N-well junction has a lower breakdown than the N+/P-well because the P-well is lighter doped than the N-well. To get the lowest trigger voltage it was chosen to use the P+/N-well configuration shown in Figure 2.4.

![Figure 2.4 Proposed bi-directional low-triggering SCR device with two P+ regions (BP1 and BP2) added in the conventional SCR in Figure 2.3.](image)

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2.4. TLP Measurement Results and Discussions

We first consider the I/O ESD protection of a data communication transceiver. The operating voltage range for this type of pin is +/- 8 V. The ESD protection for this application is required to be bi-directional with a trigger voltage between 10 to 15 V and a leakage current no more than a few nanoamps. Both the conventional and new bi-directional SCR structures have been fabricated using the IBM 0.6-μm BiCMOS process. The TLP measurement results of these two devices are plotted in Figure 2.5 and Figure 2.6, respectively.

TLP current-voltage characteristics, as well as the leakage currents, of the conventional bi-directional SCR devices having three different D4 are shown in Figure 2.5. For the cases of D4 = 1.0 and 1.2 μm, the trigger voltage is around 20 V and the leakage current is about 10^-9 A. This relatively high trigger voltage results from the fact that the triggering is governed by the avalanche breakdown at the N-well/P-well junction. When D4 is decreased to 0.6 μm, punch through mechanism in the region of D4 takes over, and the trigger voltage drops to about 12 V but the leakage current is increased significantly to the level of milliamps (see Figure 2.5).
Figure 2.5 TLP measurement results for the conventional bi-directional SCR devices having three different D4.

The holding voltage is another important parameter when the ESD device is used as a supply clamp connected between two supply rails [29]. The holding voltage of the conventional SCR is insensitive to D4 variation, and the relatively small holding voltage (i.e., about 4 V) makes the conventional SCR susceptible to the latch-up condition. The width of the conventional SCR’s is 50 μm, and the failing current It2 of the devices is around 70 mA/μm.

Figure 2.6 shows the TLP current-voltage and leakage current results of the new bi-directional SCR devices having four different D4. Like the conventional bi-directional SCR, decreasing D4 reduces the trigger voltage. For the case of D4 = 0.7 μm, the trigger voltage is about 12 V and holding voltage about 3 V. But this where the similarity ends, as the leakage
current of the new SCR devices maintains at a few nanoamps even when D4 is reduced. In contrast with the conventional SCR structures, adjusting D4 in the new SCR affects more on the holding voltage and less on the trigger voltage (see Figure 2.6). This is because the addition of the P+ regions has altered the functionality of D4 region from controlling the triggering mechanism to the holding mechanism. As D4 increases, the current gain of the parasitic bipolar transistor is decreased, and hence the increased holding voltage. For the case of D4 = 6.4 μm, the holding voltage of the new SCR is 7.5 V, making it very suitable as a supply clamp for the data communication transceiver having a 5 V to 0 supply voltage. To a lesser extent, increasing D2 (the length of P+ region) can also increase the holding voltage. The width of the new SCR’s is 200 μm, giving rise to an It2 of about 75 mA/μm for these devices.

Thus it has been demonstrated that the proposed bi-directional SCR can fulfill the ESD protection requirements of the data communication transceiver considered of a trigger voltage in the range of 10 to 15 V, a leakage current of several nanoamps, a small holding voltage for I/O pad (i.e., 3 to 4 V) and a large holding voltage for supply clamp (i.e., 7.5 V).

The bi-directional SCR device proposed is more compact comparing to the conventional approach of combining two unidirectional SCR devices to achieve the dual-snapback behavior. Generally speaking, for the same ESD protection level and robustness, the die size saving of using the bi-directional device is between 30 to 40%.
Figure 2.6 TLP measurement results for the new bi-directional SCR devices having four different D4

2.5. Summary of This Chapter

A new and improved SCR structure for low-triggering ESD applications has been proposed and successfully realized in a BiCMOS process. Such a structure possesses the desirable characteristics of a dual-polarity conduction, low trigger voltage, small leakage current, large failing current, adjustable holding voltage, and compact size. Example of ESD protection for a data communication transceiver has been considered, and measurement data have been presented to support the new SCR development.
CHAPTER 3.  SCR DEVICES HOLDING VOLTAGE MODULATION

3.1. Existed Latch-Up Issue for SCR Type ESD Protection Devices

Silicon controlled rectifier (SCR) is an attractive device for electrostatic discharge (ESD) protection applications. Its inherent bipolar conductivity modulation effect makes it exhibit a deep snapback characteristic, i.e. the holding voltage in the range of 1V to 2V, and have a smaller on resistance of several ohms [29]. The smaller holding voltage and on resistance will help it to conduct more ESD current with the same silicon area. Thus SCR type devices have a stronger current handling ability comparing with the other ESD protection devices, such as diodes or GGNMOS [39]. But this deep snapback or lower holding voltage characteristic will lead it to be more sensitive to latchup issue.

When a silicon chip is working under the normal operational status with the VDD pad connected with the power supply, the SCR type ESD protection cell is possible to be mis-triggered by the external noise signal if the noise has a higher peak voltage than SCR’s triggering voltage value or has a higher peak current level than the SCR’s triggering current value. Normally SCR’s holding voltage is very small and lower than the power supply voltage value. The mis-triggered SCR device is going to clamp at its holding voltage level if the power supply is still connected with the IC. In such a case, the SCR’s low clamping voltage will make it to be damaged by the high energy from the power supply since the power supply is trying to sustain a stable operational voltage and driving more and more current to the SCR protection device.
Typically when a SCR is triggered, the power to the SCR must be lowered below the holding voltage or completely removed from the device to reset it back to an off state [40].

To adopt SCR as the ESD protection unit and benefit its’ high ESD current conduction capability, we need to conduct some engineering work on its’ structure and make it to be immunity to latch-up effect under the normal power on status. Two effective solutions to resolve SCR-based device latch-up issue are summarized in the paper [19]. The first one is to increase its triggering current value, but the triggering voltage and holding voltage are kept the same. A SCR device with higher triggering current threshold (i.e. larger than 200mA, the normal maximum noise current level) will prevent it to be turned on by the external noise. The second solution is to increase SCR device’s holding voltage to be higher than the IC’s operational voltage. With a higher holding voltage value, the SCR will return to off state even if it has been mis-triggered by the external noise signal. The reason is that the operational voltage is lower than SCR’s holding voltage and can’t keep the SCR at turn on status once the noise signal disappears.

In this chapter, we studied the SCR devices working principle and analyzed the basic components of SCR’s holding voltage at first, and proposed several solutions to increase its holding voltage. Test devices have been fabricated and their TLP measurement results showed that all the proposed solutions can increase the holding voltage efficiently. Finally, we can combine these different methods together to adjust the holding voltage of SCR devices from several volts to close to the triggering point. The SCR structure with a holding voltage close to triggering point is prominent to be used as the ESD protection devices in high voltage applications with latch-up immunity.
3.2. SCR Holding Voltage Modulation Based On Physical Analyzing

A traditional SCR structure with a twin-well structure is shown in Figure 3.1 (a), and its equivalent circuit composing of two parasitic bipolar transistors (BJT1 and BJT2) and two resistors (\(R_{n\text{Ext}}\) and \(R_{p\text{well}}\)) is given in Figure 3.1 (b). It should be noticed that a blocking junction of N-Ext/P-Well is chose for high voltage ESD protection instead of the typical N-Well/P-Well. This N-Ext/P-Well blocking junction will lead to SCR’s triggering voltage to be as high as 45V. SCR can also be simplified as a one dimension (1D) structure plotted in Figure 3.1 (c). In this 1D structure, there are four doping layers P1, N1, P2 and N2 which form three different PN junctions J1, J2 and J3 [41].

![Figure 3.1](image_url)

**Figure 3.1** (a) Cross section view of a traditional SCR structure (b) its equivalent circuits and (c) 1D equivalent structure for a typical SCR device.
At normal forward working mode, junction J2 with a reverse bias voltage blocks the current flow through the device. If the potential drop between Anode and Cathode $V_{AK}$ continues increasing and reaches the avalanche breakdown voltage of junction J2, electrons and holes generated by impact ionization will be swept into N1 region and P2 region respectively. Then positive bias voltages will be formed between the emitter and base junctions (EB) of parasitic BJTs (BJT1 and BJT2 in the Figure 3.1 (b)). If these bias voltages are larger than the build-in voltage of EB junctions, the BJTs will turn on and make SCR work at forward conduction mode [41].

Once SCR is turned on, tons of electrons injected from N2 region and holes injected from P1 region will occupy the N1 and P2 doping regions, which will lead to junction J2 disappear and the N1, P2 doping regions become highly conductivity or low resistivity. At this time, SCR works like a PiN diode. This effect is called as conductivity modulation [41]. The required voltage drop between Anode and Cathode to sustain the conductivity modulation is SCR devices’ holding voltage ($V_H$).

Indicated in Figure 3.1 (c), the holding voltage is composed by three parts ($V_1$, $V_2$ and $V_3$). $V_1$ and $V_3$ are the potential drops required to apply on the parasitic BJTs’ EB junctions for sustaining enough carriers to be injected from parasitic BJTs’ emitter region to the base region. $V_2$ are the potential drop between the junctions J1 and J3. To realize a high holding voltage SCR device, we can elevate the voltage $V_1$, $V_2$ and $V_3$ separately.

Normally $V_2$ is very small since N1 and P1 region will become highly conductivity modulated and crowded with electrons or holes when SCR is turned on. The possible solution to increase $V_2$ is increasing the equal resistance value between junction J1 and J3. A normal
resistor value can be calculated by Equation 3.1, where \( \rho \) is the resistivity, \( l \) is the resistor length and \( A \) is the cross section area. Assuming that the resistivity of region N1 and P2 after the SCR’s turning on will be a constant value affected by the fabrication process only and has no relationship with the initial doping concentrations, there are two possible ways to elevate \( V_2 \):

1) Increase the length of \( L_B \).

2) Decrease the device junctions’ cross section area. A smaller junction cross section area can be realized by choosing a smaller device width.

\[
R = \rho \times \frac{l}{A}
\]  

(3.1)

\( V_1 \) and \( V_3 \) are a little higher than the EB junctions’ build in voltages of parasitic BJTs, which are about 0.7V. They can be elevated by decreasing the parasitic BJTs’ emitter injection efficiency factors. With smaller emitter injection efficiency, more voltage drops needed to apply on the junction J1 and J3 to sustain enough carriers being injected into N1 and P2 regions for conductivity modulation [29]. The emitter injection efficiency factor can be expressed as Equation 3.2,

\[
\gamma \approx \frac{1}{1 + \frac{N_B}{N_E} \times \frac{D_E}{D_B} \times \frac{x_B}{x_E}}
\]  

(3.2)

Where \( N_B \) is the base doping concentration, \( N_E \) is the emitter doping concentration, \( D_E \) and \( D_B \) are the minority carrier diffusion coefficients in emitter and base regions, respectively, \( x_B \) is the width of neutral base region, and \( x_E \) is the width of neutral emitter region [41].
Based on Equation 3.2, there are several ways to control the emitter injection efficiency for parasitic BJTs (BJT1 and BJT2) in SCR:

1) Increasing the parasitic BJTs’ base length or decreasing their emitter length

2) Reducing the emitter area. The reduction of parasitic BJTs’ emitter area will have the same effect as the reduction of emitter length in the 1D structure analyzing.

3) Increasing the parasitic BJTs’ base doping concentration or decreasing their emitter doping concentration. For most ESD protection designs, they are required to protect the ICs on an indicated process, which means we can’t change the doping concentration of N+ or P+ region. What’s more, the adjustment on parasitic BJTs’ base doping concentration will affect the FBJ J2’s avalanche breakdown voltage, and the triggering voltage will be changed consequently. So this solution is not applicable for current ESD protection application.
3.3. Experiments for Elevating SCR Holding Voltage

With the above comprehensive physical analyzing on SCR devices holding voltage components, several design rules have been proposed for a high holding voltage SCR design. In this section, four groups of experiments have been setup to verify these design rules and the TLP measurement results shows that all of them are effective methods on holding voltage modulation.

3.3.1. Decreasing the Devices Width

Normally we use semiconductor devices’ 2D cross section to analyze their I-V characteristic. Regarding the SCR’s triggering voltage and holding voltage, we suppose they are determined by the dimensions in the cross section and process parameters. But through the physics analyzing in the above section, SCR type devices’ holding voltage values can also be affected by its devices width and a small SCR device width will lead to a higher holding voltage. In this group experiment, three SCR devices with the same structure as Figure 3.1 (a) have been fabricated. They have the same dimensions for the cross section structures, which are listed as below: D1=1.6um, D2=0.6um, D3=1.6um, D4=1.5um, D5=8.0um, D6=8.0um, but they have different device widths as 50um, 100u and 200um. The TLP measurement results in Figure 3.2 confirms that a SCR device will have a bigger holding voltage value if its device width decreasing.
Figure 3.2 TLP I-V characteristic for SCR devices with different device widths.

3.3.2. Increasing the Parasitic BJTs’ Base Length

From the analyzing in section 3.2, a bigger base length for the parasitic BJTs in SCR structure will make the voltage drop of V2 in the conductivity modulation region N1P2 become larger due to the increased resistance between junction J1 and J2 region. What’s more, the increasing of base length can also lower the emitter injection efficiency, which will lead to the
holding voltage elevating for some degree. A group of devices have been fabricated to investigate this conclusion. These devices are fabricated based on the SCR structure described in Figure 3.1 (a) with the same dimensions as D1=1.6um, D2=0.6um, D3=1.6um, D4=1.5um and the same device width of 50 um, but they have different base lengths for parasitic BJT1 (D5) and BJT2 (D6) which are denoted in Figure 3.3. From TLP measurement results, it is obviously to see that the SCR’s holding voltage will increase with the increasing of parasitic BJTs’ base lengths (D5 and D6).

![Figure 3.3 TLP I-V characteristic for SCR devices with different base length in the parasitic BJTs.](image)

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For the high voltage application, an even higher holding voltage is required. To implement such a device with holding voltage around 40V, the parasitic BJTs’ base length needs to be increased even more. Two similar SCR devices with parasitic BJTs’ base length (D5 and D6) of 16.0um and 20.0um have also been fabricated. The TLP measurement results showed that both these devices are damaged before the snapback happens. In fact, the longer parasitic BJTs’ base length in SCR structure will result in the increasing of both the turn on time and trigger current [42]. For the parasitic p type BJT device, it never produces similar deep S-shape I-V characteristics due to the isothermal avalanche-injection effect unless other parasitic NPN structure or different thermal effects are involved [43]. In this special case, the longer base length will make both PNP and NPN need a longer time to accumulate enough current for turning on, the PNP is most possible be damaged before the whole SCR turns on. So the SCR devices with a very big parasitic BJTs’ base length (larger than 12um in this 0.6um BiCMOS process) will not be conducted.

3.3.3. Reducing the Parasitic BJTs’ Emitter Area

A strip topology shown in Figure 3.4 (a) is used for the conventional SCR. In this configuration, the N+ blocks in the cathode (emitters of BJT2) and P+ blocks (emitters of BJT1) in the anode are continuous. To reduce the effective emitter areas of BJT1 and BJT2, a novel segmented topology is proposed and shown in Figure 3.4 (b). In this case, the N+ and P+ blocks are not continuous and are separated by the well-tie blocks. For the segmented topology shown, about 50% of the P+ emitter of BJT1 is replaced with the N+ well-tie, and similarly for the
emitter topology of BJT2. Thus, the segment ratio for this SCR is referred as 1:1 (one emitter block vs. one well-tie block).

![SCR Topology Diagram]

**Figure 3.4** SCR with (a) a traditional strip topology (left) and (b) novel segmented topology (right)

Figure 3.5 shows the TLP I-V curves of the two SCR devices having the same areas (a width of 186 μm) but different topologies (strip and 1:1 segmented topologies). Clearly, the holding voltage has been increased from 4 V to about 40 V when the segmented topology is used. The failure current, It2, is also increased in the segmented version (5.3 amps vs. 3.4 amps) as shown by the leakage current. This can be attributed to the reduced well resistance and more uniform field distribution near the emitter regions.
Except for the elevated holding voltage, the other differences between the I-V characteristic of these two SCR devices with different layout topology are their triggering voltages and triggering currents, which are highlighted in the inner plot of Figure 3.5. SCR with new layout style has smaller well tie resistances $R_{nExt}$ and $R_{pwell}$, comparing with the conventional strip layout. With the decreased well tie resistance, more triggering currents are expected to build the turn on potential between the Emitter Base junctions of parasitic BJTs in this new SCR. Consequently, the increased triggering current will also lead to a higher potential drop at the FBJ (i.e., a higher triggering voltage). This effect is not good for the high voltage application which requires a narrow ESD design window. To satisfy the narrow ESD protection design window, some other assistant methods are needed to overcome this problem.

![Figure 3.5 TLP I-V characteristic for two SCR devices with different the strip and segmented layout topology.](image)
The preceding study focused on the SCR with a 1:1 segment ratio. Intuitively, one would expect different segment ratios would affect the SCR’s holding voltage. Two group experiments have been set up to verify how the SCR’s holding voltage vary with different segment ratios. Both of them include 5 devices, which have different emitter segment ratios which are demonstrated in Figure 3.6 (i.e., a 3:1 segment ratio has three emitter blocks versus one well-tie block). They have the same cross section view as Figure 3.1 (a), and the same devices dimension except D5 and D6. The D5 and D6 value for the first group are 8.0um and 8.0um, and they have been reduced to 4.0um and 4.0um for the second group.

The TLP measurement results for these two group experiments are plotted in Figure 3.7. Both of these two group experiments showed that the SCR’s holding voltage can be modulated from 5V to 40V by adjusting the segmentation ratio from 3:1 to 1:1. However, decreasing the segment ratio further does not increase the holding voltage any more. Another important observation is that the failure current It2 decreases with decreasing segment ratio, as the current crowding resulting from the smaller emitter area, together with the increased holding voltage, leads to lower It2 results. Nonetheless, a reasonably high It2 of 5.3A (or 28mA/um) is still obtainable for the case of 1:1 segment ratio having a holding voltage of 40V.
Figure 3.6 Several SCR devices with novel layout topology having different segment ratio a) 3:1 b) 2:1 c) 1:1 d) 1:2 e) 1:3.
Figure 3.7 TLP measurement results for the group of SCR devices with the layout topology shown in Figure 3.6 and the same cross section view as Figure 3.1(a) (a) D5=D6=8.0um (b) D5=D6=4.0um. (Their other cross section dimensions are listed as: D1=1.6um, D2=0.6um, D3=1.6um, D4=1.5um)

The segmentation structures mentioned above are all symmetrical. In the following a group of asymmetrical segmented SCR is proposed. Two types of such devices are shown in Figure 3.8 and Figure 3.9. For the first group in Figure 3.8, the topology on the anode is not segmented (i.e., conventional topology) and the topology on the cathode side is segmented. The segmented ratios of the 3 devices in Figure 3.8 are 0/1:2 (0 denotes non-segmented topology on the anode, and 1:2 indicates that there are one N+ region for every two P+ regions on the cathode side), 0/1:1, and 0/2:1. In these devices, the emitter injection efficiency in the NPN BJT is
modulated to change the holding voltage. For the second group in Figure 3.9, the topology on the cathode is not segmented and the topology on the anode is segmented, and the ratios of these devices are 1:2/0, 1:1/0, and 2:1/0.

Figure 3.8 Asymmetric segmented SCR with a segmented ratio of (a) 0/1:2, (b) 0/1:1, and (c) 0/2:1

Figure 3.9 Asymmetric segmented SCR with a segmented ratio of (a) 1:2/0, (b) 1:1/0, and (c) 2:1/0
TLP measurement results for the above devices are plotted in Figure 3.10. It can be suggested from the results that segmentation in the PNP BJT on the anode side has little effect on the holding voltage, but the holding voltage can be changed quite significantly when the cathode topology is segmented. For the latter, the SCR’s holding voltage can be increased from 10 to 36V.
Figure 3.10(a) TLP measurement results for asymmetric segmented SCR’s in Figure 3.8 and (b) TLP measurement results for asymmetric segmented SCR’s in Figure 3.9.

Besides the holding voltage, the SCR’s failure current It2 is also affected by the topology segmentation. For example, It2 decreases as the segmented ratio is increased from 0/1:2 to 0/1:1 to 0/2:1. Such a trade-off needs to be considered when using the proposed devices for high voltage ESD applications.

3.3.4. Holding Voltage Modulation by Applying Multiple Methods Mentioned Above

The previous experiments results are consistent with the physical analyzing in section 3.2 very well. It showed that there are several ways to elevate the SCR devices holding voltage: 1) decreasing the devices width, 2) increasing the parasitic BJTs’ base length, 3) reducing efficient emitter area by the novel segmentation layout topology. In fact, these high voltage modulation
methods can be combined together to realize a more efficient way on high holding voltage SCR solutions. For example, in the Figure 3.3, we can increase the device’s holding voltage to 8V by using a SCR with parasitic BJTs’ base length as large as 12um. The method is not efficient to reach a holding voltage as high as 40V. A big base width will make the SCR devices to be damaged easily after the triggering point, and it also make the devices consume large die area. We can combine the base length modulation with emitter injection efficient modulation methods together.

In this group experiments, several SCR devices with the same layout topology as Figure 3.4 (b) have been fabricated. The difference for these devices is their parasitic BJT base length (D5 and D6), which is varied from 2.0um to 8.0um. When D5=D6 is changed from 2.0um to 8.0um, the holding voltage is increased from 10V to 45V. And the results show that the limitation for holding voltage modulation through different base length has been resolved through this new method.
Figure 3.11 TLP measurement results for the SCR devices with the symmetrical segmented layout topology and the segmentation ratio is 1:1. (Their cross section dimensions are listed as below: D1=1.6um, D2=0.6um, D3=1.6um, D4=1.5um. Different D5 and D6 dimensions are depicted in the above figure.)
3.4. Summary of This Chapter

In this paper, based on the theory analyzing of SCR devices working principle, several new methods have been proposed to modulate SCR type devices’ holding voltage to satisfy the high holding voltage requirement in high voltage application. These methods have also been verified by the TLP measurement results of the fabricated test devices on IBM 0.60 BiCMOS process. By combining several holding voltage modulation methods together, a SCR device with holding voltage about 40V has been realized. It has a higher It2 as 4.3A with the devices width of 186um, which is very prominent to be applied in high voltage applications.
CHAPTER 4. STACKED SILICON CONTROLLED RECTIFIER STRUCTURE FOR HIGH-HOLDING VOLTAGE ESD PROTECTION APPLICATIONS

4.1. Introduction the Latch-up Issue in the ESD Protection for High Voltage Applications

Power ICs or high voltage ICs are widely used in the application of LCD driver circuits, telecommunication, power management switches, motor control systems, automotive electronics, medical applications, etc. [44][45]. With the power supply voltage over ten volts or even higher, harsh operating environment, huge noise generated from large switching current, the latchup issue has become one of the main concerns for the ESD protection of high voltage ICs [46].

To avoid the snapback type ESD protection devices’ potential latchup issue in high voltage application, there are two possible solutions: the first one is to increase its triggering current and keep the triggering voltage and holding voltage as the same, and the second one is to increase its’ holding voltage value [19]. Normally the high holding voltage solution will be used for the power supply clamping since the ESD protection with a high holding voltage larger than operational voltage will keep it always latchup immunization no matter the maximum current driving capability of power supply.

Several high holding voltage solutions have been published for high voltage power supply clamping applications [47][29][48]. In [47], an accurate physical analysis of the mechanisms encountered during ESD stresses drives to define the parameters controlling the snapback at first. Based on the conclusion from physical analyzing, the PNP type structures include PLDMOS and self-biased PNP structures have been optimized and realized. Both of them demonstrate no snapback characteristic. In [29], an LVTSCR with a high holding voltage
based on reducing the parasitic BJT emitter area was proposed, but the increase of the holding voltage was not sufficiently large for high-voltage IC applications. By adopting the theory summarized in [29] that the SCR devices holding voltage can be elevated by the reducing of parasitic BJT emitter area, a novel segmented SCR device with a holding voltage of more than 40V has been proposed in [48].

All of the solutions mentioned above [47][29][48] tried to realize the high holding voltage ESD protection by the engineering or optimization work on a basic ESD protection cell. In fact, the holding voltage value can also be increased a lot by stacking several basic ESD protection cells together [49][50][51][40]. In this chapter, the high holding voltage designs with different stacking structures will be introduced at first. Then a novel stacking SCR structure with an extremely high holding voltage, very small snapback, and acceptable failure current was proposed and realized in 0.6um BiCMOS process. The new and existing high-holding voltage ESD devices are also compared to demonstrate the advancement of this work.

4.2. Prior Arts for High Holding Voltage Design with Stacking Structures

To realize a high holding voltage ESD protection device with snapback characteristic, a simple way is to stack several snapback devices together. Figure 4.1 demonstrates that the triggering voltage and holding voltage value will become double or triple when two or three of the same structures have been stacked together. Several papers or patents have been published to disclose how to stack different type snapback devices to develop high holding voltage ESD protection [49][50][51][40].
Figure 4.1 IV characteristic for the stacking ESD structure with different stacking numbers.

In the paper [49], the low voltage NMOS and PMOS devices have been stacked together to make the holding voltage become several times of the one of single low voltage NMOS or PMOS unit. The TLP measurement results for the stacking structure with different stacking numbers are plotted in Figure 4.2. It is obviously to see that the holding voltage values will scale linearly with the stacking numbers for both low voltage NMOS and PMOS structures. What’s more, the low voltage PMOS device and stacking low voltage PMOS devices have no-snapback characteristic, which will make them to be very good candidates for the high voltage application with the requirement of narrow ESD design window. For example, in a real application reported in paper [31], a display driver chip works under the maximum power supply voltage of 43V and the output driver NMOS device breakdown voltage with floating gate (undefined potential at the gate during ESD) is 54V. The ESD design window of this application is limited between 47V (the maximum operational voltage plus 10% safety margin) and 54V. For such a narrow ESD
design window, it is better to choose the stacked PMOS structures with no snapback characteristic as ESD protection candidate.

Figure 4.2 TLP measurement results for (a) stacked low voltage NMOS devices and (b) stacked low voltage PMOS devices [49].

Besides the LV NMOS or PMOS devices introduced above, the Field-Oxide-Devices (FOD) has also been reported to be used as a basic stacking unit. With two basic FOD devices stacked together, its triggering voltage and holding voltage will be doubled. Some further measurements have also been conducted to approve that this stacking structure can be used in 40V application without causing any latchup issue [50].
The above reported results show that the holding voltage of low voltage NMOS or PMOS and FOD devices’ holding voltage value will scale with different numbers of stacking units. Two general principles for making a stackable structure for high holding voltage propose successfully can be summarized as below:

1) The basic stacking cell should have a holding voltage close to its triggering voltage. The above mentioned basic stacking cells include NMOS and PMOS and FOD. All of them use avalanche-injection conductivity modulation that is realized due to positive feedback between the avalanche multiplication in the anode (collector, drain) junction and the injection from the cathode (emitter, drain). Due to the avalanche injection mode of operation, they can produce rather high holding voltage suitable for power clamps and nonlatch-up operation [29].

2) PNP type FOD or MOSFET structures will be more easily for stacking since they can produce higher holding voltages than NPN type structures. The reason is that PNP
type structures have a lower current gain and avalanche multiplication factors, comparing with the NPN type [47].

In fact, there are three kinds of popular snapback ESD protection devices: BJT, MOSFET and SCR. The building block of all of the above devices was either the BJT or MOSFET, taking advantage of the relatively high holding voltage in these devices. Nonetheless, the BJT and MOSFET based ESD devices are not sufficiently robust and prone to ESD-induced damages. Regarding the SCR type structures, after the initial breakdown of the blocking junction, produce double-injection or injection at both the anode and the cathode regions at relatively low build-in electric fields. Due to both the low peak electric field as well as the electric field distribution deeper in the Si under the double bipolar effect, these types of structures deliver ~10 times more specific power than the structures that use parasitic bipolar effect [29]. However, the relatively low holding voltage for SCR makes it as high voltage protection solution difficult.

Recently a new patent has been released to show that the stacking SCR can also be used as nonlatch-up solution in high voltage ICs [40]. The cross section view of new stacking SCR structures is given at Figure 4.4 (a). Comparing with the traditional stacking structures, the new stacking SCR does not have a very good isolation between each stacking unit. What’s more, a common N+ buried layer (NPBL) has been diffused under the NW and PW regions of each SCR. This NPBL functions as a resistor to connect both SCR’s NW region together. The equivalent circuit of this new stacking structure is described in Figure 4.4 (b), in which the R3 resistor is used to represent the common NPBL across two SCR structures. The R3 resistor in this new stacking structure is will change the triggering voltage of the stacking structure from two NW/PW blocking junction to one NW/PW blocking junction in SCR2. The advantage of this
improvement is reflected in Figure 4.5. Comparing the I-V curve of traditional stacking SCR structure and the new stacking SCR structure, we can see that the new structure have overcome the larger triggering voltage issue existed in the traditional one and make stacking SCRs can be used as high holding voltage purpose without damage the internal circuits due to the large triggering voltage.

Figure 4.4(a) The cross section view and (b) the equivalent circuits of a new stacking SCR structure disclosed in the patent [40].
Figure 4.5 The I-V characteristic for (a) one single SCR device (b) traditional two SCR stacking structure and (c) improved two SCR stacking structure.

In the above improved stacking SCR structure, an extra mask NPBL is required for reducing the triggering voltage. In the following section, a new stacking SCR structure is proposed and it has a better figure of merit by comparing with the previous high holding voltage ESD protection solutions.

4.3. The Development of Stacking SCR Structure with High Holding Voltage

To stack several basic SCR cells together and get a very high holding voltage structure, we need to lower the normal SCR structure’s triggering voltage at first since the stacked structure’s triggering voltage should not exceed the high voltage CMOS devices’ drain breakdown voltage in the internal circuits, or it will fail to act as ESD protection purpose.

A modified lateral SCR (MLSCR) device has been proposed in [52] to realize the low voltage triggering and its cross section is demonstrated in Figure 4.6 (a). Comparing with the
traditional SCR structure, MLSCR has an extra P+ diffusion region which was inserted across the edge of N-well and P-Well region. The extra P+ diffusion is indicated as BP (bridge P+) in Figure 4.6 (a). With this extra BP diffusion, SCR devices’ forward blocking junction (FBJ) will be changed from N-Well/P-Well to N-Well/P+. The FBJ for the conventional SCR and the low triggering voltage SCR is indicated in Figure 4.6 (b) and Figure 4.6 (c). Due to the higher P+ doping concentration in the FBJ of MLSCR, it’s triggering voltage will be decreased from around 20V to about 10-12V [53].

![Diagram of MLSCR structure](image)

Figure 4.6(a) The cross section view for MLSCR devices (b) the FBJ of conventional SCR devices (c) the FBJ of MLSCR devices.

The biggest barrier to stack the above MSCR structure for high voltage application is SCR’s deep snapback characteristic due to the conductivity modulation effect happened after its turning on [29]. In A. Chatterjee’s paper, the holding voltage model was presented and it predicted that the SCR’s holding voltage will scale with its Anode to Cathode spacing under the same epitaxial layer thickness [54]. Based on this principle, a high holding voltage SCR design can be realized through the engineering on MLSCR’s Anode to Cathode spacing.
As shown in Figure 4.6 (a), the anode to cathode spacing is composed of the anode P+ diffusion length (D1), the cathode N+ diffusion length (D1), the spacing between anode and BP (D2), the spacing between cathode and BP (D2), and the length of BP (2xD3). The anode P+ diffusion and cathode N+ diffusion are mainly for ohm contacts, and changing its dimensions does not alter notably the holding voltage. So D1 should be made just large enough to facilitate the current conduction and minimize the on-state resistance. The spacing between anode and BP or cathode and BP can be increased to increase the holding voltage, but doing so will adversely increase the triggering voltage due to a larger voltage drop in the regions. Thus, to design an ESD structure with a very small snapback (i.e., trigger and holding voltages are very close to each other), the most effective way to adjust the MLSCR’s holding voltage is to change the length of BP region (i.e., D3 length).

With the near no-snapback low-triggering voltage SCR device ready, the stacked SCR structure can be realized by connecting any two adjacent SCR devices together, which is demonstrated in Figure 4.7. Figure 4.7 (a) described the cross section view of two connected adjacent SCR devices, and Figure 4.7 (b) is the top view for the layout of these stacked two SCR structures. Both N type guard ring (N-Ring) and P-type guard ring (P-Ring) have been adopted for isolation between two adjacent SCR structures. The N-Ring surrounds the devices with N-Tub doping concentration, and it will be floating. The P-Ring surrounds the N-Ring with P-Substrate material, and it is connected to the ground. The spacing for N-Ring and P-Ring should follow the basic design rule in the specific process. A good isolation will help the triggering voltage value and holding voltage value of stacked structure can be stacked linearly.
Figure 4.7(a) The cross section view and (b) the layout top view for two stacked SCR devices with N-Ring and P-Ring as isolation.

On the 0.6um BiCMOS process, high-holding-voltage (HHV) MLSCRs have been realized through larger D3 dimension, and a structure with the holding voltage of 44V can be developed by stacking 4 single HHV-MLSCRs together. The experiment results and related discussion are presented in the next section.
4.4. TLP Measurement Results and Discussions

Figure 4.8 presents the Transmission Line Pulse (TLP) measurement results for one group of MLSCR devices which have the same structure (D2=0.6um and D1=1.6um) as Figure 4.6 (a) with different D3 values. Clearly, the holding voltage can be elevated from 3 to 11.5 V by increasing the D3 dimension from 1.2 to 6.0 µm, while the trigger voltage is kept the same. Naturally, the failure current It2 decreases with increasing D3 due to the larger holding voltage. For the device with D3 = 4 µm, It2 is still at an acceptable level of 2 A, or 3000 V human body model.

Figure 4.8 TLP measurement results for MLSCR devices with different BP diffusion length (the device width is 50um)
With the above low triggering voltage and HHV-MLSCR structures ready, a very high holding voltage SCR can be constructed by stacking several same HHV-MLSCR devices together. Each MLSCR structure’s Anode to Cathode spacing, the stacking unit number are two important parameters for adjusting the final stacking structure’s holding voltage value to satisfy the latchup immunity requirements in different operational voltage applications. A group of stacking MLSCR devices has been fabricated based on different SCR stacking numbers. The basic SCR unit for stacking is chose from the experiment devices in Figure 4.8, which has a devices width of 50um and D3 dimension of 4.0um. The TLP measurement results are demonstrated in Figure 4.9. Finally the stacked SCR structure’s holding voltage can reach 44V if the stacking number is 4.

![Figure 4.9 TLP measurement results for stacked MLSCR structure with different stacking unit numbers (D3 dimension in each MLSCR cell is 4.0um, and device width is 50um).](image)
The above stacking MLSCR structures have two advantages for HHV required applications. One is that it can provide flexible holding voltage modulation by adjusting the D3 dimension and the stacking numbers. The second advantage is the stacked SCR structure has a higher ESD protection capability than the stacked BJT or MOSFET with the same silicon area. To compare the ESD robustness among different high holding voltage solutions, the figure of merit for high holding voltage ESD protection structures (HHVFOM) can be described as:

\[ HHVFOM = \frac{I_{t2} \times V_H}{W \times n} \]

where \( I_{t2} \) is the second breakdown current, \( W \) is the total device width, \( n \) is the stacking cells’ number if the structure is realized by stacking several basic units together, \( V_H \) is the holding voltage value. Considering that different processes will have different minimum design rule for the lateral structure, we will ignore the area difference due to the lateral structure lengths and only choose the equivalent device width for HHVFOM calculation instead of the real device area. What’s more, \( V_H \) value will affect the devices’ \( I_{t2} \) and it varies in different published high holding voltage solutions, so \( I_{t2} \times V_H \) has been adopted in \( HHVFOM \) to measure the real protection capability. Table 4.1 gives a summary of the published high holding voltage solutions performance and the stacking SCR structure of this work. It is clear that the proposed stacked SCR structure has a very good HHVFOM.
Table 4.1 Comparison of HHVFOM for different high holding voltage solutions

<table>
<thead>
<tr>
<th>High Holding Voltage Solutions</th>
<th>( V_H ) (V)</th>
<th>( W ) (( \mu )m)</th>
<th>( n )</th>
<th>( I_{t_h} ) (A)</th>
<th>HHVFOM (( \frac{A \times V}{\mu \text{m}} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>pLDMOS [47]</td>
<td>47</td>
<td>800</td>
<td>1</td>
<td>1.75</td>
<td>0.103</td>
</tr>
<tr>
<td>Self-Biased PNP BJT [47]</td>
<td>24.3</td>
<td>1700</td>
<td>1</td>
<td>4.0</td>
<td>0.057</td>
</tr>
<tr>
<td>Segmented SCR [48]</td>
<td>35</td>
<td>186</td>
<td>1</td>
<td>5.2</td>
<td>0.978</td>
</tr>
<tr>
<td>Stacked Field-Oxide Device (FOD) [50]</td>
<td>35</td>
<td>800</td>
<td>2</td>
<td>1.55</td>
<td>0.034</td>
</tr>
<tr>
<td>Stacked LV-MOS [49]</td>
<td>40</td>
<td>770</td>
<td>4</td>
<td>3.5</td>
<td>0.045</td>
</tr>
<tr>
<td>Stacked MLSCR (this work)</td>
<td>44</td>
<td>50</td>
<td>4</td>
<td>2.3</td>
<td>0.506</td>
</tr>
</tbody>
</table>

4.5. Summary of This Chapter

A silicon controlled rectifier (SCR) based structure with a very high holding voltage of 44 V and good ESD robustness has been realized in a 0.6-\( \mu \)m BiCMOS process. The structure was built by stacking four high-holding, low-triggering SCR’s. The holding voltage can be adjusted to meet different ESD requirements by changing the stacking unit number and/or the dimension in the unit cell. Comparison of the ESD figures of merit of the proposed structure and existing ESD devices was also presented to illustrate the usefulness of this work.
CHAPTER 5. CONCLUSIONS

The semiconductor devices are facing more and more serious threaten from ESD damage since the transistor size are scaling towards several tens or even several nanometer level with the advanced semiconductor fabrication technology nowadays. It is estimated that up to 35% of total IC field failures are ESD-induced and the annual costs to the IC industry running to several billion dollars. The development of on-chip ESD protection devices can function as an effective way to divert the ESD current to the ground and make the internal circuits to be safe.

A general on-chip ESD protection flow widely used at industry is described at the introduction section. ESD design window need to be defined at first. All of the proposed ESD protection candidate should be tested by TLP to make sure that they satisfy the pre-defined ESD design window. Then the devices with I-V characteristic located into the ESD design window can be choose to be integrated with the internal functional circuits. The final chip with on-chip ESD protection solution should be tested by different ESD models to check their real ESD protection capability.

There are three different kinds of popular ESD protection devices and they are diodes or diodes string, GGNMOS and SCR. Of these three different protection structures, SCR has the highest ESD protection capability with the silicon area due to the conductivity modulation effect after its turning on. But SCR devices also have several shortcomings such as the higher triggering point, the lower clamping voltage and the lower turning on speed etc, which will become obstacle for SCR to be widely used as an ESD protection solution in most of the industry
IC products. The main contribution of our work is to resolve the SCR devices’ potential shortcomings and realize high ESD protection solutions with the less silicon area.

The first part of our work is to develop an improved dual-direction SCR type device for low-triggering ESD applications. In some specific applications, such as the interface circuits for RS 232/RS485 standard, the pins are required to go below ground or go above the VDD. To protect the IC for these applications, new protection schemes with a clamping element for both polarities are required. Our proposed new bi-direction SCR device is more compact when compared of the conventional approach of combining two one-direction SCR devices to achieve the dual-snapback behaviors. What’s more, by including the bridge P+ region, the proposed SCR’s triggering voltage could be reduced to 12V without causing a significant increase in the leakage current which normally exists in the traditional NPNPN five layer bi-directional structures. Its holding voltage can be adjustable for the applications which require a higher clamping voltage due to latch-up immunity requirement.

The second part of our work is to overcome SCR’s low holding voltage issue and make it useable for high voltage application. To eliminate the SCR structure’s potential latch-up risk, it is required to increase its holding voltage value to be larger than the power supply voltage. The proposed novel structure is developed based on the use of a segmented topology to reduce the emitter injection efficiency of the parasitic BJTs in the SCR. The advantages of the new SCR over the existing ESD devices are larger holding voltage for latchup immunity and high failure current for ESD robustness. Test devices have been fabricated in the BiCMOS 0.6um technology, and TLP measurements have illustrated that such an SCR device is viable for realizing latchup immune ESD supply clamps in the voltage range of 30 to 40V.
The third part of our work is also to resolve SCR’s latch-up issue. In this section, we adopted stacking SCR structure to realize the high holding voltage purpose. Both the stacked FOD and stacked GGNMOS structures have already been reported for realizing high holding voltage devices. But SCR is always been excluded for stacking due to its deep snapback characteristic. In our work, a close no-snapback low triggering voltage SCR has been made at first by some holding voltage engineering work on a MLSCR structures. Based on this high holding voltage low-triggering voltage SCR, it is easy to realize a stacking SCR device with a very high holding voltage by adjusting different stacking numbers. Comparison of the ESD figures of merit of the proposed structure and existing ESD devices was also presented to illustrate the usefulness of this work.
LIST OF REFERENCES


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