High Linearity 5.8 Ghz Power Amplifier With An Internal Linearizer

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High Linearity 5.8 GHz Power Amplifier
with an Internal Linearizer

by

YIHENG WANG

M.S. Beihang University, 2009

A thesis submitted in partial fulfillment of the requirements
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Major Professor: Jiann.S.Yuan
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ABSTRACT

A 5.8 GHz RF Power Amplifier (PA) is designed and fabricated in this work, which has very high linearity through a built-in linearizer. The PA is designed, post-layout simulated by Agilent Advanced Design System (ADS) software and fabricated by Win-Semiconductors 0.15µm pHEMT process technology. The post-layout simulation results illustrate the power amplifier can obtained an output power of 23.98 dBm, a power gain of 32.28 dB and a power added efficiency (PAE) of 29% at saturation region, the 3rd intermodulation distortion (IMD3) of -37.7 dBc at 0 dBm input power is attained when operation frequency is 5.8 GHz. We finally obtain that the output power of 17.97 dBm and power gain of 27.97 dB at input power of -10 dBm, PAE of 11.65% at input power of 0 dBm and the IMD3 of -25.66 dBc at -20 dBm input power by measurement, when operation frequency is 5.2 GHz. So the overall RF performance of the PA demonstrates high power, high efficiency and high linearity.
ACKNOWLEDGMENTS

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<th>Abbreviation</th>
<th>Description</th>
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<tr>
<td>ADS</td>
<td>Agilent Advance Design System</td>
</tr>
<tr>
<td>CDMA2000</td>
<td>IMT Multi-Carrier</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communication</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input Third Order Intercept Point</td>
</tr>
<tr>
<td>IMD3</td>
<td>3rd Intermodulation Distortion</td>
</tr>
<tr>
<td>OIP3</td>
<td>Output Third Order Intercept Point</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>PHEMT</td>
<td>Pseudomorphic High Electron Mobility Transistor</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>---------</td>
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<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wideband Code Division Multiple Access</td>
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CHAPTER ONE: INTRODUCTION

In modern communication application field, the new wireless communication technology is developing very fast at recent years, the 2 generation wireless communication technology for instance Global System for Mobile Communication (GSM) has been almost completely upgraded to 3 generation wireless communication technology [1] [2] which emphasize the high data transmission rate for example the Wideband Code Division Multiple Access (WCDMA) and IMT Multi-Carrier (CDMA2000) wireless communication system. The power amplifier (PA) [3] are widely used in the wireless communication base station and portable mobile termination equipment of 3rd generation wireless communication technology, for instance the power amplifier is indispensable part for wireless transceiver, Figure 1 is a black diagram of conventional wireless transceiver and the wireless transceiver is the core part of wireless communication system which is used to transmit and receive wireless signal.
Figure 1: Block Diagram of Conventional Wireless Transceiver

Compare to 2nd generation wireless communication system, the 3rd generation wireless technology transmit and receive data at much higher rate, so the high data rate raises higher request for power efficiency and linearity of the power amplifier. Based on these requirements, the new kind of InGaAs pHEMT [4] technology is a good choice. High electron mobility transistor (HEMT) is a field effect transistor incorporating a junction between two materials with different band gaps as the channel instead of a doped region, as is generally the case for MOSFET [5] [6]. To allow conduction, the complementary metal–oxide–semiconductor (CMOS) is doped with impurities which donate mobile electrons or holes. However, these electrons are slowed down through collisions with the impurities (dopants) used to generate them in the first place. HEMTs avoid this through the use of high mobility electrons generated using the heterojunction of a
highly-doped wide-bandgap n-type donor-supply layer and a non-doped narrow-bandgap channel layer with no dopant impurities. A HEMT where this rule is violated is called a pHETM or pseudomorphic HEMT. This is achieved by using an extremely thin layer of one of the materials – so thin that the crystal lattice simply stretches to fit the other material. This technique allows the construction of transistors with larger bandgap differences than otherwise possible, giving them better performance. Based on above reasons, the InGaAs pHETM technology can provide higher output power and lower power consumption compared to conventional CMOS technology.

In normally power amplifier design, the amplifier’s circuit includes an active FET device and matching circuit which consist the passive components like inductors, capacitors and resistors which exhibits favorable RF characteristics. The RF characteristics such as insertion loss, high power, high efficiency and high linearity are very important for power amplifier. Power amplifier’s linearity is also a very important factor for new generation communication systems besides above power performances of PA [7]-[10]. The circuit’s passive components such as inductors, capacitors and resistors could affect the PA’s linearity. Indeed, the linearity and efficiency is a trade-off issue for power amplifier. If the linearity of PA increases, the power efficiency performance would reduce and vice versa. So, find out a new PA architecture to improve the linearity and do not affect the efficiency strongly at the same time, is a valuable topic that is worth to study. Finally, we design a power amplifier circuit associate with a built-in linearizer circuit to improve the PA’s total linearity, and make it have better power performance such as output power, power gain and power added efficiency at the same time.
This literature is divided into six sections, the first section is introduction which has been indicted above. The second section demonstrates how to design the circuit and pre-layout simulation results. The third section shows that the layout and post-layout simulation results. The measurement information and measurement results are explained in fourth section. The fifth section is the work’s conclusion. We also demonstrate the future research direction in final section.
CHAPTER TWO: CIRCUIT DESIGN

This chapter is divided into two sections. The first section explains the power amplifier circuit design and the second section describes the built-in linearizer circuit design.

**Power Amplifier Design**

Power amplifier is a dispensable part for modern wireless communication system. It is used in signal transmitting and receiving part of wireless communication equipment. The power amplifier is a device for increasing the power of a signal, it is required to amplify the input signal and do not induct too much insertion loss and noise simultaneously. The PA’s performance is measured by followed criteria, such as output power, power gain and power added efficiency (PAE). The unit of output power is dBm, defined as

\[
P_{out}(dBm) = 10 \times \log_{10} P_{in}(W) - 30
\]  

where \(P_{in}(W)\) is input signal power, unit is Watt. The power gain defined as

\[
\text{Powe gain} = P_{out}(dBm) - P_{in}(dBm)
\]

where \(P_{out}\) (dBm) is output signal power and \(P_{in}\) (dBm) is input signal power, the unit of these two parameters is dBm. The power added efficiency (PAE) is defined as

\[
\text{PAE} = \frac{P_{out}(W) - P_{in}(W)}{P_{dc}(W)}
\]
where $P_{out}(W)$ is output power, $P_{in}(W)$ is input power and $P_{dc}(W)$ is direct current power, their unit is Watt.

Power amplifier circuits are classified as A, B, AB and C for analog design [11], and D and E for switch design according to the conduction angle $\Theta$. In communication system, the classes A to D power amplifier are commonly used. Conduction angle $\Theta$ reflects how many portion of input signal can be conducted through amplifying device. For class A power amplifier, the conduction angle is $360^\circ$ so 100% input signal can be conducted, class A PA has more linearity but its efficiency is very low. For class B power amplifier, the conduction angle is $180^\circ$, it determines 50% input signal is used, its efficiency better than class A but linearity is worse at the same time. For class AB power amplifier, the conduction angle is greater than $180^\circ$ and less than $360^\circ$, so it could have the advantages of class A and class B, high linearity and high efficiency. The class C power amplifier’s conduction angle is less than $180^\circ$, its efficiency is very high and disadvantage is high distortion. Base on above considerations, we choose the class AB PA to realize the work, because of its high linearity and high efficiency features.

Beside the classification, PA also has many kinds of architectures, for instances one stage PA, two stages PA and multi-stages PA. The advantage of one stage PA is simple architecture but its power gain is low. Multi-stages PA although could attain very high power gain, but its construction is too complex. So we choose the two stages PA architecture finally. This kind of architecture has the high power gain and easy to design features. The basic two stages PA architecture is showed as Figure 2.
In this figure, M1 is driver stage transistor, M2 is power stage transistor. The power stage is the most important part is two stages PA design, because this stage can determine the PA’s power performances like output power and PAE.

The PA circuit design phase is divided into two steps, the first step is load and source pull simulation, the second step is matching network design. Each of them will be detailedly explained at the following sections.

Load Pull and Source Pull Simulation

Because the power stage will determine the power performance of PA, in order to exploit the power stage transistor’s potential, we make the load pull and source pull simulation when design the power stage circuit [12]. Load pull simulation will use the Win-Semiconductors nonlinear device model to find out this device’s optimal output power and efficiency. In our
work, the load pull simulation is realized by Agilent Advanced Design System (ADS). Advanced Design System is the leading electronic design automation software for RF, microwave, and high speed digital applications. ADS pioneers the most innovative and commercially successful technologies, such as X-parameters and 3D EM simulators, used by leading companies in the wireless communication & networking and aerospace & defense industries. For WiMAX, LTE, multi-gigabit per second data links, radar, & satellite applications, ADS provides full, standards-based design and verification with Wireless Libraries and circuit-system-EM co-simulation in an integrated platform. The ADS has the key features of Complete schematic capture and layout environment, innovative and industry leading circuit and system simulators, direct, native access to 3D planar and full 3D EM field solvers, largest number of process design kits (PDKs) developed and maintained by leading foundry and industry partners, EDA and Design Flow Integration with companies such as Cadence, Mentor, and Zuken, Optimization Cockpit for real-time feedback and control when using any of 12 powerful optimizers, X-parameter model generation from circuit schematic and Agilent's NVNA for nonlinear high-frequency design, up-to-date Wireless Libraries enable design and verification of the latest emerging wireless standards. The load pull simulation’s procedure is described below. First of all, choose the transistor size and DC biasing condition. For this design, we choose two paralleled 4x75µm transistors as power stage device, although the bigger size transistor can provide higher output power, this design has fabrication dimension limitation (the limitation is 1mm x 2mm), so we decide to use this size finally. After making decision of transistor size, we determine the 5V Vds and -1V Vgs as DC biasing supply, because we need the transistor to work under class AB condition. Secondly, we put the transistors, power supply, RF choke and DC block into circuit,
and run the circuit under ADS load pull design kit. We set the operation frequency at 5.8 GHz, terminal impedance as 50Ω, characteristic impedance as 50Ω and source impedance as (10+j*0) Ω before running the simulation. Finally, we can achieve the transistors’ optimal load impedance which could get best power and efficiency from the load pull simulation result. This result is showed as Figure 3.

![Simulated Load Impedances and Input Reflection Coefficients](figure.png)

**Figure 3: Load Pull Simulation Result**

The function of source pull simulation is same as load pull simulation, but it will exploit the even better potential of the power stage transistor base on the result of load pull simulation. The procedure of source pull simulation is also similar to load pull simulation. The most of parameters are same as load pull simulation. For example, operation frequency is 5.8 GHz, characteristic impedance is 50 Ω. The only exception is that the load impedance should use the (45.326+j*4.105) Ω which is obtained from load pull simulation result, the load impedance value is also the optimal load impedance for the power stage transistor. After setting all of parameters,
we use the ADS source pull design kit to run the source pull simulation. We attain that the two paralleled 4x75\(\mu\)m Win-Semiconductors pHEMT transistors’ optimal power performance is output power of 25.55 dBm and PAE of 33.32% at input signal power of 0 dBm from the source pull simulation result. Figure 4 shows the result.

![Simulated Source Impedances and Input Reflection Coefficients](image)

**Figure 4: Source Pull Simulation Result**

### Matching Network Design

We have known the transistors’ optimal load and source impedance from the load and source pull simulation. The next step is to design the two stage PA’s matching network according to the impedances which are achieved before. In fact, the power amplifier’s matching network could be separated three sections [13]. The first section is driver stage matching network, the second section is power stage matching network and the third section is inter-stage matching
network. After completing all of the marching networks, we pack the DC bias network, transistor and matching networks together, and power amplifier circuit is finished finally. Figure 5 is the power amplifier circuit’s schematic diagram.

Figure 5: Power Amplifier Circuit Diagram

The power stage matching network is designed firstly, because the power stage is the most important part in power amplifier. The power stage’s output matching network is to make the power stage device’s output impedance to match the 50Ω terminal impedance. The output impedance is the conjugate value of load impedance which is obtained from load pull simulation. The theoretical reason is to make the output impedance and load impedance conjugate match. In Figure 5, the series L5 and C7, parallel C6 compose the output matching network. The input matching network of power stage is similar to output matching network design. According to the source impedance attained from source pull simulation, to use its conjugate value as input impedance. The difference is make input impedance to match driver stage output impedance not 50Ω terminal impedance, this step is also the inter-stage matching network design, the
destination of inter-stage matching network is to transfer the signal from driver stage to power stage with very low loss. The C3, C4, L3 and C5 construct the inter-stage matching network in Figure 4.

For the driver stage design, only using the basic amplifier design process could satisfy the requirement of driver stage and do not need to run load pull and source pull simulation for this stage transistor. The reason is that the function of driver stage is to transfer the input signal to next stage with low loss and low noise. It is not requested to provide very high power gain. The driver stage input matching network is composed by C1, C2 and L1.

Beside the matching network components, we can see some other components too from the circuit schematic diagram Figure 5. L2 and L4 are the RF choke to block the RF signal between matching network and voltage supply. Although R1, R2 and R3 could degrade the noise and efficiency performance, they can improve the circuit’s stability significantly, so the reason of use resistor is to improve stability [14] [15]. The value of these three resistors is compromised result, to lead the power amplifier very stable and do not reduce efficiency significantly.

**Linearizer Design**

General speaking, the power amplifier exhibits gain compression at the time of high input power level, so the conventional power amplifier need to be operated at low power level to satisfy the linearity request, but the output power is the most important performance for power amplifier [16]. Therefore, in order to make power amplifier works at best available power level and satisfy the linearity requirement meanwhile, the linearization technology is developed to
decrease the amount of power trade-off issue. Number of literatures about linearization technology have been published, for instance the predistortion linearizer solution, it can improve the circuit linearity obviously and has advantages of smaller size, lower complexity and lower cost, but the predistortion linearizer can cause higher insertion loss which would reduce the power amplifier overall power gain performance finally, the cost is a little higher for power amplifier. Therefore, the attempt is being done for linearization technology with low complexity, small size, low cost and low insertion loss such as this work [17]–[19]. The principle of our linearizer is showed in Figure.6, in order to achieve the satisfaction linearity under high power level, the gain compression effect should be compensated by the linearizer, so the linearizer must have gain extension characteristic opposite to conventional power amplifier, the total gain of the circuit is maintained finally like the Figure.5 shows.

![Figure 6: Principle of Gain Compensation](image)

In order to achieve the gain extension characteristic, the linearizer’s real-part resistance should increase along with power amplifier’s input power signal that means the gain is extended. The equivalent circuit of linearizer is showed in Figure.7.
Base on above analysis, the resistance of $R_{off}$ and $R_{ds}$ should increase along with power amplifier’s RF signal. At the beginning, the linearizer works at linear region which it is biased at $V_{\text{linearizer}} = -1.8\,\text{V}$, and transistor’s size is $4\times75\,\mu\text{m}$, so its resistance is maintain as a constant. When the power amplifier’s input RF signal’s power increases, the linearizer’s operation point will swing into the I-V dynamic load line’s nonlinear region which result in the increased $R_{ds}$, because the $R_{ds}$ is inverse proportion to the derivative of the drain current $I_{ds}$ divided by drain voltage $V_{ds}$, $R_{ds} = 1/(\frac{\partial I_{ds}}{\partial V_{ds}})$. The variation of $R_{ds}$ is much larger than the variation of $R_{off}$ and $C_{off}$, so the variation of $R_{off}$ and $C_{off}$ can be ignored and assume that the resistance of $R_{off}$ and $C_{off}$ is a constant at any work region. For the size choice of linearizer’s transistor, it is proportional to gain extension and inverse proportional to insertion loss, so we should to find out a balance value of linearizer’s transistor, the size of $4\times75\,\mu\text{m}$ is the optimized value which is achieved through simulation. The final circuit of linearizer is showed in Figure 8. The driver
stage and power stage belong to power amplifier circuit which we mentioned before. The drain of the linearizer transistor is supplied by RF signal, so the Rds will become larger through the power of RF signal increasing as mentioned before. The result is that the linearizer circuit will have the gain extension feature, and the linearity of power amplifier become better.

Figure 8: Linearizer Circuit Diagram

Final Circuit

Figure 9 is the final circuit diagram which includes a power amplifier and a built-in linearizer. The M1 is driver stage transistor, M2 is power stage transistor and M3 is linearizer transistor in Figure 9. C1 and C7 have two functions, one is used to matching network, another one is DC block to protect RF terminal. L2 and L4 are RF choke which is used to block the RF signal. The DC bias scheme is VDD of 5V, VGG of -1V and VLIN of -1.8V.
Figure 9: Final Circuit of High Linearity Power Amplifier
Pre-Layout Simulation

In order to verify our circuit design scheme, we need to make simulation before layout in term of pre-layout simulation. We can know whether the circuit is matched well, whether the power and linearity performance could meet design requirement through the pre-layout simulation results. The pre-layout simulation results are showed as Figure 10 to Figure 13

![Figure 10: S Parameter Results of Pre-Layout Simulation](image-url)
Figure 11: Stability Result of Pre-Layout Simulation
Figure 12: Power Performances of Pre-Layout Simulation

Figure 13: Linearity Result (IP3) of Pre-Layout Simulation
From the pre-layout simulation result, we get S11 of -25.3 dB, S22 of -21.7 dB and S21 of 29.5 dB, the S parameters demonstrate that the circuit has been well matched; the circuit stability is very good because of 5.7 stable factor at 5.8 GHz; for power performance, the saturation output power of 26 dBm, power gain of 29 dB and PAE of 32%, these value demonstrate the power performance of the power amplifier is nice; the OIP3 is 48 dBm and IIP3 is 15 dBm which indicate our power amplifier has high linearity. In order to evaluate the effect of linearizer, we compare the simulation results between with linearizer and without linearizer through 3rd inter-modulation (IMD3) value, the result is showed as Figure 14. The result indicates linearity of power amplifier with linearizer is approved significantly.

![Figure 14: Linearity Comparison With Linearizer to Without Linearizer](image-url)
CHAPTER THREE: LAYOUT AND POST-LAYOUT SIMULATION

Layout Design

We choose the Cadence Virtuoso Layout Suite to make the layout design after circuit design. All of the components such as inductor, capacitor and transistor, wire and via are obtained from Win-Semiconductors pHEMT 0.15μm layout library. The Cadence Virtuoso Layout Suite is the high-end custom block authoring physical layout tool. It could deliver an unparalleled set of features—from Quick Cell parameterized cell definition to design rule-driven support. More advanced capabilities such as constraint-based connectivity-driven design, floor planning, and design optimization further help to achieve better yield. Connectivity-driven layout provides a proven 4-10xproductivity boost over manual layout editing, while design rule-driven support ensures correct-by-construction layout, which is especially important at advanced design geometries. Also included are automated custom placement and automated custom routing capabilities, which not only follow the technology file but also the design constraints entered by the front-end designer. For users who prefer fully automated layout of blocks, Virtuoso accelerated layout also supports constraint based layout synthesis. Beside these features, Virtuoso also provides the high accurate analysis function. For RF design at 0.18 micron and below, high accuracy parasitic extraction, analog IR-drop analysis, and power grid electro migration analysis become critical for both circuit design and full chip electrical verification. Virtuoso high accurate analysis function combines all of these capabilities with design rule checking (DRC) and layout-versus-schematic checking (LVS). For high-frequency designs like
this work (5.8 GHz), Virtuoso analysis includes inductance extraction, signal-wire electro migration analysis, and a fast field solver for capacitance extraction. These capabilities enable design teams to perform silicon-accurate analysis quickly and avoid extremely expensive unplanned re-spins.

The Cadence Layout Suite tool is just a layout platform, in order to finish the layout, we must have the layout library which is provided by IC chip foundry. So beside the Virtuoso, Win-Semiconductors Corp provided their 0.15µm pHEMT process technology layout library to us. The layout library includes the different lays metal material, vias and many pre-defined components such as components, inductors and transistors, all of these metal and components are indispensable for layout design procedure.

The basic requirement of layout is to try our best to make the layout circuit as symmetry as possible. Because generally inductor is the biggest component in layout, inductor position should be determined firstly in layout procedure. RF signal input and output pads and DC supply pads are determined after the inductor position. The rough arrangement is built up through the two steps. The following step is to locate those smaller components such as resistor, capacitor and transistor and connect them with metal wires and vias. Beside the layout symmetry issue, the RF signal path design should also be especially cared. Some problems should be avoided such as the RF signal is accumulated at some certain location, if the signal is accumulated at some certain location, these area will be burned out much earlier than other parts of the RF chip because of power accumulation. So we should try our best to make RF signal path as smooth as possible. The final layout is showed in Figure 15.
Figure 15: Final Layout of Power Amplifier With Linearizer
We make the design rule check (DRC) as this work’s layout analysis. For Win-Semiconductors pHEMT process, the design rule check includes air bridge check, basic rule check, gate direction check and label layer check. Figure 16 to Figure 19 demonstrate every check rules’ result. These figures indicate that all of design rules have been passed without any error.

Figure 16: Air Bridge Rule Check Result (Total Error Found: 0)
Figure 17: Basic Rule Check Result (Total Error Found: 0)

Figure 18: Gate Direction Rule Check Result (Total Error Found: 0)
After finishing the layout, in order to get more accurate simulation result, we need to make post-layout simulation. The post-layout simulation will extract the parasitic effect of all components and metal layers such as inductor, capacitor, transistor and metal, via from the circuit layout, and composed these extracted parasitic effect with ideal circuit to achieve the more accurate physical simulation result. The physical simulation result includes metal’s impedance, capacitance between different metal layers and electrical and magnetic field effect and so on.

We use the Agilent Advanced Design System (ADS) Momentum as post-layout simulation tool. In fact, Momentum is a part of Advanced Design System, it can provide the simulation tools engineers need to evaluate and design modern communications systems products. Momentum is an electromagnetic simulator that computes S-parameters for general
planar circuits, including microstrip, slotline, stripline, coplanar waveguide, and other topologies, such as Vias and airbridges connect topologies between layers. So we can simulate multilayer RF/microwave printed circuit boards, hybrids, multichip modules, and integrated circuits. Momentum gives us a complete tool set to predict the performance of high-frequency circuit boards, antennas, and ICs. Beside the basic functions, Momentum also has some extended capability, like Momentum Optimization and Momentum Visualization. Momentum Optimization extends Momentum capability to a true design automation tool. The Momentum Optimization process varies geometry parameters automatically to help us achieve the optimal structure that meets the circuit or device performance goals. By using (parameterized) layout components we can also perform Momentum optimizations from the schematic page. And Momentum Visualization is an option that gives users a 3-dimensional perspective of simulation results, enabling us to view and animate current flow in conductors and slots, and view both 2D and 3D representations of far-field radiation patterns. On the basis of the above mentions, Momentum could enable us to simulate when a circuit model range is exceeded or the model does not exist, identify parasitic coupling between components, go beyond simple analysis and verification to design automation of circuit performance, visualize current flow and 3-dimensional displays of far-field radiation. Momentum has the key advantages of an electromagnetic simulator using the method of moments, adaptive frequency sampling for fast, accurate, simulation results, optimization tools that alter geometric dimensions of a design to achieve performance specifications, comprehensive data display tools for viewing results, equation and expression capability for performing calculations on simulated data, full integration
in the ADS circuit simulation environment allowing EM/Circuit co-simulation and co-
optimization.

There are four steps in process of post-layout simulation. The first step is to extract the
layout file from Cadence Virtuoso. The second step is to add the metal layer and substrate files to
Momentum, and open the extracted layout file in Momentum. The metal layer and substrate files
are provided by Win-Semiconductors, which include the metal and substrate information in Win-
Semiconductors pHEMT process technology. These information must be used by Momentum to
locate the layout’s layer and substrate position and extract the parasitic effect information. The
Figure 20 is the layout file which is opened by Momentum.

Figure 20: Layout Opened by Momentum

Third step is to select the critical path and extract the parasitic information from the path. The
criteria of critical path selection is to choose the section from RF signal path, because the RF
signal path is more sensitive to parasitic effect. And for the RF signal path, we should select the
metal wire which is too wide, too narrow, too long or has too many corners. Because long and narrow metal wire has more impedance effect, long and wide metal wire has more capacitance effect, if the metal wire has many turns, it will have the inductance effect and every corner would accumulate power which affect the RF signal. Base on above criteria, the selected critical path is showed as Figure 21, where all of critical path are marked as red color.

Figure 21: Layout Simulation Critical Path Selection

In order to extract the parasitic information of every critical path, we need to use Momentum to add input and output port on every critical path, this is software usage requirement. The fourth step is to achieve every critical path parasitic information data and put all of the parasitic data into schematic circuit to run simulation again. The parasitic data file is S parameter simulation result file. The result of this simulation is post layout simulation result, because it has included parasitic effect of layout. Figure 22 to Figure 25 are the post-layout simulation results. And the
RF performance comparison between pre-layout simulation and post-layout simulation are showed as Table 1 to Table 4.

![Figure 22: S Parameter Result of Post-Layout Simulation](image)

<table>
<thead>
<tr>
<th></th>
<th>S11</th>
<th>S22</th>
<th>S21</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pre-Layout</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulation Results at 5.8 GHz</td>
<td>-25.30 dB</td>
<td>-21.67 dB</td>
<td>29.54 dB</td>
</tr>
<tr>
<td><strong>Post-Layout</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulation Results at 5.8 GHz</td>
<td>-20.41 dB</td>
<td>-16.42 dB</td>
<td>27.10 dB</td>
</tr>
</tbody>
</table>
Figure 23: Stability Result of Post Layout Simulation
Table 2: Pre-Layout Simulation and Post-Layout Simulation Stability Comparison Table

<table>
<thead>
<tr>
<th>Stable Factor</th>
<th>Pre-Layout Simulation Result at 5.8 GHz</th>
<th>5.73</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Post-Layout Simulation Result at 5.8 GHz</td>
<td>7.96</td>
</tr>
</tbody>
</table>

Figure 24: Power Performance Results of Post Layout Simulation
Table 3: Pre-Layout Simulation and Post-Layout Simulation Power Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Output Signal Power</th>
<th>Power Gain</th>
<th>PAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-Layout Simulation Saturation Result at 5.8 GHz</td>
<td>26 dBm</td>
<td>29 dB</td>
<td>32%</td>
</tr>
<tr>
<td>Post-Layout Simulation Saturation Result at 5.8 GHz</td>
<td>23 dBm</td>
<td>28 dB</td>
<td>29%</td>
</tr>
</tbody>
</table>

Figure 25: Linearity Result (IP3) of Post Layout Simulation
Table 4: Pre-Layout Simulation and Post-Layout Simulation Linearity Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>IIP3</th>
<th>OIP3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-Layout Simulation Result</td>
<td>18 dBm</td>
<td>49.5 dBm</td>
</tr>
<tr>
<td>Post-Layout Simulation Result</td>
<td>17 dBm</td>
<td>45.6 dBm</td>
</tr>
</tbody>
</table>

Because the chip fabrication will meet fabrication variation, we need to evaluate the fabrication variation effect, to make sure that the PA can normally work under different condition. Based on above consideration, we run different temperature simulation and different voltage supply simulation to evaluate the fabrication variation effect, and set four conditions which is 0°C temperature, 85°C temperature, increasing 10% voltage supply and reducing 10% voltage supply respectively. The post-layout simulation results under different condition are showed as Figure 26 to Figure 29. These results indicate the power amplifier is not very sensitive to fabrication variation and could normally work under different fabrication condition.
Figure 26: Power Performance Simulation Result at 0°C

Table 5: 0°C and Normal Condition Power Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Output Signal Power</th>
<th>Power Gain</th>
<th>PAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation Saturation Result Under Normal Condition</td>
<td>23 dBm</td>
<td>28 dB</td>
<td>29%</td>
</tr>
<tr>
<td>Simulation Saturation Result at 0°C</td>
<td>23.5 dBm</td>
<td>30 dB</td>
<td>29.5%</td>
</tr>
</tbody>
</table>
Figure 27: Power Performance Simulation Result at 85°C

Table 6: 85°C and Normal Condition Power Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Output Signal Power</th>
<th>Power Gain</th>
<th>FAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation Saturation Result under Normal Condition</td>
<td>23 dBm</td>
<td>28 dB</td>
<td>29%</td>
</tr>
<tr>
<td>Simulation Saturation Result at 85°C</td>
<td>22.5 dBm</td>
<td>27 dB</td>
<td>27.7%</td>
</tr>
</tbody>
</table>
Figure 28: Power Performance Simulation Result at Voltage Increasing 10%

Table 7: Normal Voltage and 10% Increasing Voltage Power Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Output Signal Power</th>
<th>Power Gain</th>
<th>FAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation Saturation</td>
<td>23 dBm</td>
<td>28 dB</td>
<td>29%</td>
</tr>
<tr>
<td>Result under Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Condition</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulation Saturation</td>
<td>24.5 dBm</td>
<td>28 dB</td>
<td>28.5%</td>
</tr>
<tr>
<td>Result at Voltage Increasing 10%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 29: Power Performance Simulation Result at Voltage Reducing 10%

Table 8: Normal Voltage and 10% Reducing Voltage Power Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Output Signal Power</th>
<th>Power Gain</th>
<th>FAE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation Saturation Result under Normal Condition</td>
<td>23 dBm</td>
<td>28 dB</td>
<td>29%</td>
</tr>
<tr>
<td>Simulation Saturation Result at Voltage Increasing 10%</td>
<td>22.7 dBm</td>
<td>28.3 dB</td>
<td>29.5%</td>
</tr>
</tbody>
</table>
CHAPTER FOUR: MEASUREMENT

We make S parameter measurement, power performance measurement and linearity measurement in the measurement section. This chapter will explain the measurement procedure, include measurement equipment requirement, measurement environment construction and measurement results. We will also discuss the measurement results at the end of this chapter. The chip’s photo is showed as Figure 30.

![Figure 30: Photo of Power Amplifier Chip](image)

Measurement Environment Setting Up

Measurement Instrument

The measurement instruments are required in chip measurement include RF probe station, RF and DC probe, probe positioner, network analyzer, signal generator, spectrum analyzer,
isolator, attenuator. Probe station, probe and probe postioner are used to connect the fabricated power amplifier die chip; network analyzer is used to make S parameter measurement; signal generator and spectrum analyzer are used to make power and linearity measurement; isolator is used to isolate RF signal and attenuator is used to attenuate signal power, they are protection component in measurement environment.

Chip Connection

There are two types of scheme for RF chip measurement, one is on board measurement, another one is on wafer measurement. The on board measurement is used for RF chip without DC bias network and DC block, because there are not DC bias and DC block, the engineer must to design a printed circuit board (PCB) independently, and solder the DC bias, DC block and RF chip on PCB later. If the operation frequency is high, we must consider the transmission line effect when design the measurement PCB, and could use the ADS line calculation kit to estimate the length and width of the connection line. Because the pads of RF chip are too tiny, it is imposable to manually solder the connection wires to chip pad, we can only bond the wire to pad through wire bonding machine. Because there are many uncertain issues for on board measurement, such as bonding wire insertion loss, PCB and component insertion loss, bonding quality, components soldering quality and static electricity protection, compare to on wafer measurement the on board measurement is not the best choice for RF chip experiment and the on wafer measurement is preferable one. The on wafer measurement requires RF chip ingrates DC bias network and DC block, it means the RF chip does not need the external components to start work when it is measured. This kind of measurement need probe station and RF DC probe to
connect the RF chip. Compare to on board measurement’s PCB, component, wire bonding and so on, the probe station connection’s insertion loss and uncertainty are much better. Because we have integrated the DC bias and DC block at the phase of circuit design, the PA could be measured by high reliable on wafer measurement at this time.

Measurement Environment

S-Parameter Measurement

The instruments are required by S-parameter measurement consist probe station and network analyzer. In order to get more accurate result, before making the S-parameter measurement, the network analyzer should be calibrated and calibration method includes thru-reflect-line TRL and open-shot-load-thru SOLT calibration. And we select the SOLT calibration for this work because we have the agilent SOLT calibration kit. The S parameter measurement environment is showed as Figure 31. The reason of using attenuator is protect the network analyzer because of very high small signal gain of power amplifier.
Power Performance Measurement

The power performance measurement requires instruments such as signal generator, isolator, attenuator and spectrum analyzer. Figure 32 indicates the final power performance measurement environment. The signal generator is used to generate input RF signal which is transferred to power amplifier. The spectrum analyzer is used to capture the output RF signal which is amplified by power amplifier. The function of isolator is to block the signal reflected by power amplifier, because if the chip’s matching network is not good after fabrication, the power amplifier will reflect high power signal to signal generator and have the risk of damaging the signal generator. The reason of using attenuator is similar to S parameter measurement, to protect the spectrum analyzer.
In order to measure the power amplifier’s linearity, we require two adjacent input signals which means of two signal generators and use spectrum analyzer to capture fundamental frequency output signal and 3rd frequency output signal, and judge the power amplifier’s linearity through the difference between these two output signals in term of 3rd inter-modulation (IMD3) value. The reason of using isolator and attenuator is same as power performance measurement mentioned above. The final linearity measurement scheme is showed as Figure 33.
Figure 33: Linearity Measurement Environment
Measurement Results

S-Parameter Measurement Results

S11 Measurement Result

The S11 measurement result is showed as Figure 34.

![Figure 34: S11 Measurement Result](image)

From Figure 34, the best value S11 is achieved at 5.3 GHz, which of -35.01 dB.

Table 9 shows the difference between measurement and post layout simulation, S11 of -19.23 dB at 5.8 GHz indicates the circuit’s input matching has met the design requirement.
Table 9: Measurement and Post-Layout Simulation S11 Comparison Table

<table>
<thead>
<tr>
<th>S11</th>
<th>Measurement at 5.8 GHz</th>
<th>Post-Layout Simulation at 5.8 GHz</th>
<th>Measurement at 5.3 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-19.23 dB</td>
<td>-20.41 dB</td>
<td>-35.01 dB</td>
</tr>
</tbody>
</table>

S22 Measurement Result

S22 measurement result is showed as Figure 35.

![Figure 35: S22 Measurement Result](image)

The best value of S22 is obtained at 5.4 GHz and it is -11.2 dB from Figure 35.
Table 10 shows the difference between measurement and post layout simulation, S22 of -8.54 dB at 5.8 GHz indicates the circuit’s output matching is good but much worse than post layout simulation result because of more parasitic effect.

Table 10: Measurement and Post-Layout Simulation S22 Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Measurement at 5.8 GHz</th>
<th>Post-Layout Simulation at 5.8 GHz</th>
<th>Measurement at 5.4 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>S22</td>
<td>-8.54 dB</td>
<td>-16.42 dB</td>
<td>-11.2 dB</td>
</tr>
</tbody>
</table>

S21 Measurement Result

S22 measurement result is showed as Figure 36.

Figure 36: S21 Measurement Result
The best S21 of 29.85 dB is achieved at 5.0 GHz from Figure 36.

Table 11 shows the difference between measurement and post layout simulation, S21 of 21.13 dB at 5.8 GHz which is a little lower than post layout simulation result.

<table>
<thead>
<tr>
<th></th>
<th>Measurement at 5.8 GHz</th>
<th>Post-Layout Simulation at 5.8 GHz</th>
<th>Measurement at 5.0 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>S21</td>
<td>21.13 dB</td>
<td>27.30 dB</td>
<td>29.85 dB</td>
</tr>
</tbody>
</table>

**Power Performance Measurement Result**

Base on the S parameter measurement results, we know that the best match frequency is around 5.2 GHz, so we make power measurement at two different frequencies, one at 5.8 GHz, another one at 5.2 GHz.

**Output Power Measurement Result**

Figure 37 is output signal power measurement result at 5.8 GHz and Figure 38 is result at 5.2 GHz. The output signal power at 5.2 GHz is better than at 5.8 GHz from comparing the two figures.
Figure 37: Output Signal Power Measurement Result at 5.8 GHz

Figure 38: Output Signal Power Measurement Result at 5.2 GHz
The comparison between output signal power’s measurement result and simulation result is showed as Table 12, which indicates the measurement result at 5.2 GHz is very close to simulation result.

Table 12: Measurement and Simulation Output signal Power Result Comparison Table

<table>
<thead>
<tr>
<th>Pin (dBm)</th>
<th>P_{\text{out}} \text{ Measurement Result at 5.2 GHz}</th>
<th>P_{\text{out}} \text{ Measurement Result at 5.8 GHz}</th>
<th>P_{\text{out}} \text{ Simulation Result at 5.8 GHz}</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>-13.71 dBm</td>
<td>-20.04 dBm</td>
<td>-11.83 dBm</td>
</tr>
<tr>
<td>-30</td>
<td>-3.54 dBm</td>
<td>-10.02 dBm</td>
<td>-1.83 dBm</td>
</tr>
<tr>
<td>-20</td>
<td>8.02 dBm</td>
<td>0.14 dBm</td>
<td>8.18 dBm</td>
</tr>
<tr>
<td>-10</td>
<td>17.97 dBm</td>
<td>11.25 dBm</td>
<td>17.48 dBm</td>
</tr>
<tr>
<td>0</td>
<td>20.7 dBm</td>
<td>18.56 dBm</td>
<td>21.73 dBm</td>
</tr>
</tbody>
</table>

Power Gain Measurement Result

The power gain measurement results at 5.8 GHz and 5.2 GHz are showed respectively as Figure 39 and Figure 40.
Figure 39: Power Gain Measurement Result at 5.8 GHz

Figure 40: Power Gain Measurement Result at 5.2 GHz
Table 13 is the comparison table among power gain measurement result and simulation result. From the result, we get that the power gain at 5.2 GHz is better than at 5.8 GHz and is more close to simulation result.

Table 13: Power Gain Measurement and Simulation Results Comparison Table

<table>
<thead>
<tr>
<th>Pin</th>
<th>Power Gain Measurement Result at 5.2 GHz</th>
<th>Power Gain Measurement Result at 5.8 GHz</th>
<th>Power Gain Simulation Result at 5.8 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin = -40 dBm</td>
<td>26.29 dB</td>
<td>19.96 dB</td>
<td>28.17 dB</td>
</tr>
<tr>
<td>Pin = -30 dBm</td>
<td>26.46 dB</td>
<td>19.98 dB</td>
<td>28.17 dB</td>
</tr>
<tr>
<td>Pin = -20 dBm</td>
<td>28.02 dB</td>
<td>20.14 dB</td>
<td>28.18 dB</td>
</tr>
<tr>
<td>Pin = -10 dBm</td>
<td>27.97 dB</td>
<td>21.25 dB</td>
<td>27.48 dB</td>
</tr>
<tr>
<td>Pin = 0 dBm</td>
<td>20.7 dB</td>
<td>18.56 dB</td>
<td>21.73 dB</td>
</tr>
</tbody>
</table>

PAE Measurement Result

PAE at 5.8 GHz measurement result is showed as Figure 41 and 5.2 GHz result is showed as Figure 42. The DC power dissipation is changed slightly for different input signal power at the stage of measurement.
Figure 41: PAE Measurement Result at 5.8 GHz

Figure 42: PAE Measurement Result at 5.2 GHz
The PAE measurement and simulation result comparison table is showed as Table 14, it indicates that the PAE at 5.2 GHz is much better than 5.8 GHz, but still has big gap compare to simulation result. We know the output power and power gain measurement results at 5.2 GHz is very close to simulation result from above two sections, so the reason of big PAE gap between measurement and simulation is much more DC power dissipation of real PA chip.

Table 14: PAE Measurement Result and Simulation Result Comparison Table

<table>
<thead>
<tr>
<th>Pin</th>
<th>PAE Measurement Result at 5.2 GHz</th>
<th>PAE Measurement Result at 5.8 GHz</th>
<th>PAE Simulation Result at 5.8 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40 dBm</td>
<td>0.004%</td>
<td>0.0009%</td>
<td>0.01%</td>
</tr>
<tr>
<td>-30 dBm</td>
<td>0.04%</td>
<td>0.009%</td>
<td>0.10%</td>
</tr>
<tr>
<td>-20 dBm</td>
<td>0.63%</td>
<td>0.10%</td>
<td>1.04%</td>
</tr>
<tr>
<td>-10 dBm</td>
<td>6.26%</td>
<td>1.17%</td>
<td>7.76%</td>
</tr>
<tr>
<td>0 dBm</td>
<td>11.65%</td>
<td>5.30%</td>
<td>23.20%</td>
</tr>
</tbody>
</table>

Linearity Measurement Result

The linearity measurement results at 5.8 GHz and 5.2 GHz are showed from Figure 43 to Figure 46. For 5.8 GHz measurement, we choose f1=5.8 GHz and f2=5.801 GHz, Figure 43 and Figure 44 indicate the frequency of f1 and 2*f1-f2 measurement result. For 5.2 GHz measurement, we select f1=5.2 GHz and f2=5.201 GHz, Figure 45 and Figure 46 demonstrate the frequency of f1 and 2*f1-f2 measurement result too.
Figure 43: Fundamental Output Signal Power and 3rd Output Signal Power Measurement Result at 5.8 GHz

Figure 44: IMD3 Measurement Result at 5.8 GHz
Figure 45: Fundamental Output Signal Power and 3rd Output Signal Power Measurement Result at 5.2 GHz

Figure 46: IMD3 Measurement Result at 5.2 GHz
Table 15 shows the comparison between IMD3 measurement result and simulation result. From the data, we get that although the match and power performance at 5.2 GHz is much better than 5.8 GHz, the result is different for linearity measurement. The linearity at 5.8 GHz is better than 5.2 GHz, but also worse than simulation result.

<table>
<thead>
<tr>
<th>Pin (dBm)</th>
<th>IMD3 Measurement at 5.2 GHz</th>
<th>IMD3 Measurement at 5.8 GHz</th>
<th>IMD3 Simulation at 5.8 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>-30</td>
<td>-30.8 dBc</td>
<td>-49.41 dBc</td>
<td>-168.76 dBc</td>
</tr>
<tr>
<td>-20</td>
<td>-25.66 dBc</td>
<td>-32.84 dBc</td>
<td>-130.04 dBc</td>
</tr>
<tr>
<td>-10</td>
<td>-13.92 dBc</td>
<td>-28.23 dBc</td>
<td>-92.972 dBc</td>
</tr>
<tr>
<td>0</td>
<td>-12.39 dBc</td>
<td>-12.5 dBc</td>
<td>-37.7 dBc</td>
</tr>
</tbody>
</table>

Result Discussion

All of above results illustrate some inconsistency between the simulated and measured performance, such as the S parameter measurement result at 5.2 GHz is better than 5.8 GHz, the power performance at 5.2 GHz is much better than 5.8 GHz and more close to simulation results. These results may be caused by the reasons explained as follows. First reason is that the ADS device model has some deviation from the real fabricated device, especially for high order simulation result. Second reason should be the fabrication variation for instance the elimination of thinning polish, via hole process and so on, these fabrication variation could cause the weak power dissipation performance of the chip. Third reason is that we did not consider all of the
possible conditions when use Momentum to make post layout simulation, the chip must have more parasitic effect than our anticipation, and when we make the measurement, the RF probe must introduce more parasitic effect and the resistance of RF probe could affect the circuit match result, similarly the linearizer circuit also would associate with resistors and cause mis-match in the PA circuit.
CHAPTER FIVE: CONCLUSION

This article describes a two stage power amplifier using a built-in linearizer which base on predistortion theory, the power amplifier consists a driver stage with class AB and a power stage with class AB. The power amplifier circuit is realized with 0.15 µm pHEMT technology, and fabricated by Win-Semiconductors Corp. The fabricated chip shows appropriate RF performance at 5.2 GHz, although our design is made base on 5.8 GHz, the reason is explained by above chapters. The circuit is designed and simulated through ADS, layout is done by Cadence Virtuoso. The measurement results demonstrate good small signal performance at 5.2 GHz for example S11 of -23.23 dB, S22 of -9.78 dB and S21 of 28.67 dB; and good power performance at 5.2 GHz such as output power of 20.7 dBm, power gain of 20.7 dB and PAE of 11.65% when the input signal power is 0 dBm. The linearity performance is evaluated though IMD3 value and the measurement result shows the IMD3 of -12.39 dBc at 5.2 GHz and input power is 0 dBm. In summary, the overall power characterization exhibits high gain and linearity, with favorable RF characteristics and is very suitable for 5.2 GHz microwave integrated circuit power transmission application.
CHAPTER SIX: FUTURE WORK

Although we know that the InGaAs pHEMT technology has many advantages compared to conventional CMOS technology from this work, it still has to face the reliability issues, like hot electron effect and self heating effect. So the reliable issue is another valuable research direction. Some of research about hot electron effect and self heating effect are done in recent years, but they are mainly focused on device self. Beside the device own reliability issues, these reliability issues how to affect the power amplifier circuit’s power and linearity performance and how to compensate these effects through circuit design are very attractive research topics.

Base on above considerations, we plan to research at two directions in the future. One is the pHEMT circuit reliability study which base on the power amplifier chip of this work, such as hot electron effect and self heating effect research. The hot electron effect is a phenomenon that often occurs in semiconductor devices. The hot electrons are such electrons which get excited to energy levels higher than those associated with the semiconductor’s conduction band. These hot electrons can tunnel out of the semiconductor material—instead of recombining with a hole. For the pHEMT semiconductor device, when it works under high RF drive and high DC voltage supply, a high impact ionization gate current would be generated because the transistor is supplied high electric field. Under this situation, some electrons will receive sufficient energy to escape from the device’s channel and be trapped in the passivation layer, and some electrons will gain big enough energy to pass through the passivation layer and generate gate current at the same time. These electrons could make the reduction of channel current, and degrade the circuit’s output power further. The output power degradation would adversely affect the power
performance of PA. Because of these reasons, to study the power degradation of PA under hot electron effect for modern communication system becomes very important, because communication companies must to warrant that the system still provide enough power for proper operation by the end of life. In fact, the self heating effect is generated from hot electron. The electrons become hot when their temperature is higher than the temperature of the crystal which they will drift through. And such hot electron is the physical origin of self heating effect. The self heating effect contains of heat generation in the transistor channel which is caused by the energy transfer from the hot electrons to the lattice. This effect could reduce the channel electron velocity in term of an increase of phonon scattering processes. The reduction of electron velocity will generate the degradation of carrier mobility and the reduction of transistor drain current further. So the pHEMT device may demonstrate a negative slope of drain current with respect to drain-source voltage when the self heating effect becomes more and more significant. The negative slope will be enhanced with self heating effect increasing. The heating process cause a degradation of drain current and transconductance due to reduction of carrier mobility and velocity. So base on the conditions, when the heat is accumulated for long time, it will affect the power performance of power amplifier circuit significantly and cause the circuit to out of service eventually. Other one is trying to design a compensation circuit to compensate the hot electron effect, self heating effect and fabrication variation on power amplifier circuit. Because the hot electron, self heating and fabrication variation will degrade the RF performance of power amplifier, we need to find some way to improve the circuit and could compensate the performance degradation further.
LIST OF REFERENCES


