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HIGH PERFORMANCE LOW VOLTAGE POWER MOSFET FOR HIGH-FREQUENCY SYNCHRONOUS BUCK CONVERTERS

by

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A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the School of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

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ABSTRACT

Power management solutions such as voltage regulator (VR) mandate DC-DC converters with high power density, high switching frequency and high efficiency to meet the needs of future computers and telecom equipment. The trend towards DC-DC converters with higher switching frequency presents significant challenges to power MOSFET technology. Optimization of the MOSFETs plays an important role in improving low-voltage DC-DC converter performance. This dissertation focuses on developing and optimizing high performance low voltage power MOSFETs for high frequency applications.

With an inherently large gate charge, the trench MOSFET suffers significant switching power losses and cannot continue to provide sufficient performance in high frequency applications. Moreover, the influence of parasitic impedance introduced by device packaging and PCB assembly in board level power supply designs becomes more pronounced as the output voltage continues to decrease and the nominal current continues to increase. This eventually raises the need for highly integrated solutions such as power supply in package (PSiP) or on chip (PSoC). However, it is often more desirable in some PSiP architectures to reverse the source/drain electrodes from electrical and/or thermal point of view. In this dissertation, a stacked-die Power Block PSiP architecture is first introduced to enable DC-DC buck converters with a current rating up to 40 A and a switching frequency in the MHz range. New high- and low-side NexFETs are specially designed and optimized for the new PSiP architecture to maximize its efficiency and power density. In particular, a new NexFET structure with
its source electrode on the bottom side of the die (source-down) is designed to enable
the innovative stacked-die PSiP technology with significantly reduced parasitic
inductance and package footprint.

It is also observed that in synchronous buck converter very fast switching of
power MOSFETs sometimes leads to high voltage oscillations at the phase node of the
buck converter, which may introduce additional power loss and cause EMI related
problems and undesirable electrical stress to the power MOSFET. At the same time, the
synchronous MOSFET plays an important role in determining the performance of the
synchronous buck converter. The reverse recovery of its body diode and the \( C_{dv/dt} \)
induced false trigger-on are two major mechanisms that impact the performance of the
SyncFET. This dissertation introduces a new approach to effectively overcome the
aforementioned challenges associated with the state-of-art technology. The threshold
voltage of the low-side NexFET is intentionally reduced to minimize the conduction and
body diode related power losses. Meanwhile, a monolithically integrated gate voltage
pull-down circuitry is proposed to overcome the possible \( C_{dv/dt} \) induced turn-on issue
inadvertently induced by the low \( V_{TH} \) SynFET.

Through extensive modeling and simulation, all these innovative concepts are
integrated together in a power module and fabricated with a 0.35µm process. With all
these novel device technology improvements, the new power module delivers a
significant improvement in efficiency and offers an excellent solution for future high
frequency, high current density DC-DC converters. Megahertz operation of a Power
Block incorporating these new device techniques is demonstrated with an excellent efficiency observed.
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CHAPTER 1   INTRODUCTION

1.1   Research Background

The development of low voltage power electronics industry is motivated by the evolution of the energy consumption of CPUs (Central Process Units). Recent innovations in low voltage semiconductor technology, integration, packaging, control approaches and system architectures have been enormously conditioned by the energy requirements of the microprocessor and related solutions for conversion and transfer of power.

From the power supply standpoint, high-end computer microprocessors are one of the most demanding electronic loads, since a combination of stringent performance requirements have to be simultaneously met. To be exact, CPU power delivery solutions must critically comply with large conversion ratios, low output voltage ripple, high current operation, high power density, high efficiency and wide bandwidth response to rapid load changes all in one design. The level of sophistication demanded to energize power hungry CPUs have rapidly increased over the past decades.

1.1.1   Evolution of Microprocessors

With the astonishing advances in integration technology, the minimum feature size of transistors in state of the art CPU microprocessors has shrunk from 10 um to 22 nm in the past 40 years, and appears to continue to decrease down to the 5 nm scale by year 2020. Ever since the release of the first microprocessor back in 1971, Moore’s law, which states “transistor density doubles every eighteen months”, has successfully
predicted the evolution of integrated circuits. Moore’s empirical observation combined with the miniaturization trend and the increasing operation clock frequency has resulted in a progressive increase of the power density, currently approaching $100\text{W/cm}^2$.

![Figure 1.1](image)

**Figure 1.1** Voltage supply and current supply evolution of Intel® microprocessors [1]

Because of its square proportionality to switching losses, the reduction of CPU’s supply voltage has undoubtedly been one of the key measures to slow down the increase of heat generation. The reduction of the supply voltage further helps to mitigate reliability issues concerning short-channel effects like punch-through breakdown and oxide breakdown, which become increasingly relevant as processing geometry shrinks and processor speed increases. As shown in Figure 1.1, the supply voltage has dropped from over 10 Volts to below 1 Volt in the last 40 years. However, for the reasons of signal integrity and device performance, it’s hard to expect the supply voltage drop below 0.5V in the next few years according to the present slow scaling pace.
The continuous rise of transistor count and clock frequency has generally been accompanied by the demand of higher current operation. In the last two decades, the current supply has prominently increased by two orders of magnitude, as depicted in Figure 1.1. The forecast indicates a continuous increase in the next few years, with the possibility to reach 200 A peaks soon. Negative impacts associated with the distribution of high current throughout the CPU chip area include heat generation, metal migration, and system malfunction due to voltage fluctuations.

1.1.2 Microprocessor Power Supply – Voltage Regulator

A power supply is a device that supplies electric power to an electrical load. Most generally, it refers to electric power converters that convert electrical energy from the form supplied by a source to the form required by an electric load. The input source of dedicated microprocessor power supplies may typically be of the form of a DC voltage (typically around 19 V for laptops and 12 V for servers and desktops), which must be converted to lower DC voltage levels. Because of its primary ability to maintain the output voltage compliant to the load requirements, these power supplies commonly receive the name of voltage regulators.

The voltage regulator is broadly used nearly in every electronic system. At the very beginning, the inexpensive linear regulator based solutions were the primary choice for the low power consumption microprocessors. However, because of the imperative need of high power consumption and high efficient energy conversion, modern microprocessor must employ Switched Mode Power Supply (SMPS) based voltage regulator. The linear power supply regulates the output voltage by continually
dissipating power in the transistor. Unlike a linear power supply, the transistor of a switching-mode supply continually switches between low-dissipation, full-on and full-off states, and spends very little time in the high dissipation transitions (which minimizes power loss). Ideally, a switched-mode power supply dissipates no power. Voltage regulation is achieved by varying the ratio of transistor on-to-off time.

The most extended SMPS topology used to perform the required DC–DC step-down conversion function is the synchronous buck converter. A detailed analysis of this voltage regulator will be present in Chapter 2.

The evolution of voltage regulators is highly influenced by the power delivery architecture of the computer system. Centralized power system, which consists of a single power supply residing in a particular location and powering all system’s elements, is widely used at first. With the demands of high current operation, since the parasitic elements of the interconnections can excessively increase power loss and compromise the signal integrity of the intended power delivery form, this centralized power delivery architecture has been replaced by Distributed Power Architectures (DPA). This new concept essentially bringing power processing closer to where energy is used gives rise to a special class of power supplies known as Point-of-Load converters (PoL). The PoL approach has proven to effectively increase power conversion density while improving efficiency, forming the basis for the power supply-in-package (PwrSiP) and power supply-on-chip (PwrSoC) concepts that have recently gained more attention in the power management industry.
1.1.3 Semiconductor Power Devices

Power switched device is the key element of the VR since its associated power loss usually accounts for a significant portion of the overall generated heat. The power loss contribution from power devices often represents the main barrier to achieve higher system efficiency and operating frequency. Therefore, meeting the stringent VR specifications requirement highly relies on performance improvements in the semiconductor power device.

Among all transistor structures, the power MOSFET is the preferred implementation for the low voltage applications. It is compatible with the demands of high switching frequency due to its inherent fast switching speed capabilities, low conduction resistance and high input gate impedance. Power MOSFET can be used as electric switches for high frequency pulse width modulation (PWM) applications and load switches in power applications. When used as load switches, where switching times are usually long, cost, size and on-resistance of the switches are the prevailing design considerations. When used in PWM applications, the MOSFET must exhibit small power loss during switching, which imposes an additional requirement of small internal capacitances, making the MOSFET design challenging and usually more expensive.

The in-depth analysis and design of power MOSFET will be presented in the following chapters.
1.2 Dissertation Outline

This dissertation is devoted to the design, developing and optimizing next generation high performance power MOSFET for high frequency synchronous DC-DC buck converters. There are eight chapters in total including an introduction.

Chapter 2 describes the background information about the synchronous buck converter and its power loss. An in-depth analysis of power MOSFETs’ switching behavior and related loss mechanisms will be provided. The state of art power MOSFETs are also introduced in this chapter, where the advantages and the remaining issues are highlighted in here with details.

Chapter 3 gives the objective of this dissertation and the research methodology in details.

Chapter 4 introduces the source-down structure NexFET. This new configuration of MOSFET enables the innovative stack-die packaging technology and achieves very impressive performance together with the new packaging comparing to the state of art technologies.

Chapter 5 investigates the influence of implementing low threshold voltage MOSFET as the synchronous MOSFET. The body diode reverse recovery loss is expected to be lowered by utilizing low $V_{TH}$ MOSFET in low side, and the switch node voltage ringing is predicted to be lower than before as well. However, this could exacerbate the shoot-through risk.

The design concept of the integrated pull-down circuit as a protection of low threshold voltage MOSFET implementation is extensively analyzed in Chapter 6. This
integrated circuit can effectively prevent the shoot-through during high $du/dt$ events, even in the high input and high temperature application.

After investigation of the theory of gate pull-down circuitry, the experimental performance of the integrated power module is presented in Chapter 7. This power module achieves high efficiency, high power density and low switch node ringing at high output current rating and high operation frequency applications.

Finally, conclusions of this work and suggestions for future work are exposed in Chapter 8.
CHAPTER 2  OVERVIEW OF POWER MOSFET AND BUCK CONVERTER TECHNOLOGIES

In low voltage application, the most commonly used SMPS (Switched Mode Power Supply) topology to perform the required DC-DC step-down conversion function is the synchronous rectifier buck converter (SRBC). A Synchronous Buck converter is a modified version of the basic buck converter circuit topology in which the diode on the low-side is replaced by a second power MOSFET. As the output current in computing power supplies keeps increasing, the diode conduction loss is easily the largest source of power loss. Unfortunately, the diode junction contact potential limits what can be done to reduce the forward voltage drop of diodes. The solution of replacing the diodes with MOSFETs operated as synchronous rectifiers is a tradeoff between higher cost and better efficiency. The MOSFETs switch can effectively reduce the conduction power loss, but also typically cost more than the freewheeling diode, let alone the extra need on switch driver circuit. Due to the broadly adoption of synchronous buck topology in low voltage SMPS system, the operation of a Synchronous Buck converter (sync buck) and power losses analysis will be discussed below.

As mentioned in introduction chapter, power switch devices are pivotal components in the voltage regulator (VR) because the related switching power losses usually account for a significant portion of the overall heat generated [2]. Therefore, meeting the future VR requirement highly depends on the semiconductor switching device performance improvement.
A power MOSFET is a specific type of metal oxide semiconductor field-effect transistor (MOSFET) designed for handling large power. Among all power switch structures, with the inherent fast switching speed capability, high input gate impedance and low conduction resistance, power MOSFET is considered as the most suitable semiconductor power switching device in VR for the low voltage range of interest. An ideal power MOSFET should have zero switching losses and zero conduction resistance. Since the beginning of the 1980s, various power MOSFETs structures had been explored to approach the ideal, and every new MOSFET generation in the past continuously improved the FOM (Figure-Of-Merit). Currently, the arguments for which structure of the MOSFET can be best adapted to the targeted application are subject to nonstop debate. The advantages and the remaining issues involved in these two MOSFETs will be discussed in detail in this chapter as well.

2.1 Overview of Synchronous Buck Converter

2.1.1 Principle of the Synchronous Buck Converter

Basic topology of Synchronous buck converter is shown in Figure 2.1. This half-bridge configuration comprises two power metal oxide semiconductor field effect transistors2 (MOSFETs). The high-side and low-side devices are named as control MOSFET (CtrlFET) and synchronous MOSFET (SyncFET), respectively.
The SRBC is an advanced version of the basic buck converter topology, where the rectifying diode is replaced by an active switch (SyncFET) which is controlled to conduct or block current in synchronism with the CtrlFET. This additional active device and associated control complexity represents the most effective and feasible alternative solution to mitigate the principal efficiency limitation of the diode’s forward voltage in low-voltage applications. The SyncFET works in the 3rd quadrant at a negative drain bias. If a negative bias is applied to the SyncFET gate, the current flows through the body diode. As soon as the MOSFET is turned-on, the current flows mainly through the MOSFET channel. This additional switch and associated control complexity mitigates the efficiency limitation of the diode’s forward voltage in low-voltage applications.

Basic operation of the synchronous buck converter is shown in Figure 2.2. Controller and the gate driver IC defines the duty cycle (D) based on the feedback signal monitoring the output voltage. In the “On” phase, the control FET is turned-on while synchronous FET is turned-off and the input energy is stored in the output inductor.
The output inductor is supplying the current to the output load and charging the output capacitor to the desired output voltage during the same time period.

Figure 2.2 Basic operation principle of synchronous buck converter

Figure 2.3 Gate driver timing in a synchronous buck converter
During the “Off” phase when the control FET is turned-off while synchronous FET is turned-on, the inductor current is decaying eventually and the output capacitor provide the missing portion of the current demand. To enable a fast response of the controller to instantly change the power demand of the load, the value of the output inductance has to be small. On the other side, smaller output inductance leads to a larger amplitude of the current ripple. Therefore, for fast output regulation ability, high switching frequency is required to keeping the switching period short. At the same time, high switching frequency allows a reduction of the output inductance saving the real estate occupied in board and making the converter less expensive.

The gate driver circuit implements duty cycle defined by PWM clock signal, and is responsible for the right timing of the gate signals introducing a proper delay time between the operation of the high-side and low-side switches. This delay time also called dead-time is required to avoid a simultaneous turn-on of both switches leading to a spontaneous cross current and destruction of the circuit, which is called shoot-through. The sequence of the events in the synchronous buck converter can be described following the illustration shown in Figure 2.3:

i. PWM clock signal sends the turn-off signal to low-side switch gate;

ii. Low-side switch turns off after the delay time \( t_{D,OFF} \) which depends on the size of the transistor;

iii. Low-side switch internal body diode is conducting during the dead-time when both transistors are in off state (Low-side MOSFET works in the 3rd quadrant);
iv. The high-side gate receive the turn-on signal when the low-side gate voltage potential goes below a pre-defined value;

v. High-side switch turns-on after the inherent delay time of the HS transistor \( t_{D,ON} \);

vi. Switch node voltage potential \( V_{SW} \) has a high over-shoot and followed oscillations as soon as the high-side switch starts to conduct;

vii. During the high \( \frac{dV}{dt} \) ringing of the switch node, the low-side switch gate voltage potential bounces up which may result in a shoot-through events (will be explained in 6.1);

viii. High-side switch remains turned-on while low-side switch remains turned-off during the “ON” time of the duty cycle;

ix. PWM sends signal to turn off the high-side switch;

x. After a short delay time \( t_{D,OFF} \) the high-side switch starts to turn off and the body diode of the low-side transistor conducts the output current during the dead-time;

xi. Gate driver circuit implements a short delay time \( t_{D,ON} \) before the low-side gate is turned-on;

xii. Low-side gate is turned-on to allow the low-side MOSFET to conduct for the rest of the period time.

2.1.2 Power Loss Analysis of the Synchronous Buck Converter

Except the power loss in parasitic components in package, the total power loss in silicon power MOSFETs in a switching application consists of conduction and switching
power loss. An example of a simple power loss breakdown for a synchronous buck operating is presented and can be roughly calculated in below. This first order power loss approximation is not accurate enough to offer precise power loss calculation, but can provide us a basic knowledge of the relationship between different power losses and MOSFET parameters and a guideline to improve the MOSFET performance. It has to be noticed that following parameters are interrelated:

- The ratio of $V_{OUT}$ to $V_{IN}$ determines the required duty cycle ($D$)
- $R_{LOAD}$ determines the required output current $I_{OUT}$
- $I_{rms}$, D and output inductor L determine the ripple current described by low and high current peak values $I_{SW(ON)}$ and $I_{SW(OFF)}$

For the purpose of a first order approximation the power loss can be roughly calculated as follows:

High-side switch total power loss can be simply divided into 4 parts: conduction loss, switching loss, gate driver loss and output capacitance $C_{OSS}$ loss; whereas the low-side switch total power loss comprises conduction loss, switching loss, gate driver loss, body diode conduction loss and body diode reverse recovery loss [3].

The conduction loss is related to the output current and the on-resistance of the switch:

$$High\text{ }side:\quad P_{CON} = I_{rms}^2 \cdot R_{DS(ON)} \cdot D \quad (2.1)$$

$$Low\text{ }side:\quad P_{CON} = I_{rms}^2 \cdot R_{DS(ON)} \cdot (1 - D) \quad (2.2)$$

where $I_{rms}$ means root-mean-square drain current of high-side and low-side switch.
Turn-on switching loss in high-side switch is:

\[
P_{SW, \text{turn-on}} = \frac{I_{SW(ON)} \cdot R_{\text{driver}}}{2(V_{GS} - V_{TH})} \cdot V_{IN} \cdot (Q_{GS} + Q_{GD} - Q_{GS(TH)}) \cdot f_s \quad (2.3)
\]

Turn-off switching loss in high-side switch is:

\[
P_{SW, \text{turn-off}} = \frac{I_{SW(OFF)} \cdot R_{\text{driver}}}{2V_{TH}} \cdot V_{IN} \cdot (Q_{GS} + Q_{GD} - Q_{GS(TH)}) \cdot f_s \quad (2.4)
\]

Note that in some datasheet, the \(Q_{GD} + Q_{GS}\) portion above \(V_{TH}\) is also called \(Q_{SW}\).

Turn-on switching loss in low-side switch is:

\[
P_{SW, \text{turn-on}} = \frac{I_{SW(ON)} \cdot R_{\text{driver}}}{2(V_{GS} - V_{TH})} \cdot V_{OUT} \cdot (Q_{GS} + Q_{GD} - Q_{GS(TH)}) \cdot f_s \quad (2.5)
\]

Turn-off switching loss in low-side switch is:

\[
P_{SW, \text{turn-off}} = \frac{I_{SW(OFF)} \cdot R_{\text{driver}}}{2V_{TH}} \cdot V_{OUT} \cdot (Q_{GS} + Q_{GD} - Q_{GS(TH)}) \cdot f_s \quad (2.6)
\]

Power losses due to charging of the high-side and low-side output capacitances are:

\[
P_{OSS} = \frac{1}{2} \cdot V_{IN} \cdot Q_{OSS} \cdot f_s \quad (2.7)
\]

The gate drive losses in high-side and low-side switches are:

\[
P_{GATE\text{DRIVER}} = V_G \cdot Q_G \cdot f_s \quad (2.8)
\]

Body diode reverse recovery loss manifesting as \(I_{rr}\) flowing through high-side switch:

\[
P_{Body\ Diode} = V_{IN} \cdot Q_{rr} \cdot f_s \quad (2.9)
\]

The conduction loss of the body diode is:

\[
P_{CON,\ diode} = (I_{SW(ON)} \cdot V_f \cdot t_{DT(on)} + I_{SW(OFF)} \cdot V_f \cdot t_{DT(off)}) \cdot f_s \quad (2.10)
\]
where \( V_f \) is the forward voltage drop of the body diode of low-side switch, \( t_{DT(on)} \) is the dead time at the rising edge of the switch node voltage and , \( t_{DT(off)} \) is the dead time at the falling edge of the switch node voltage

### 2.2 Overview of Lateral Power MOSFETs

Lateral Double Diffused MOSFET (LDMOSFET) was the first power MOSFET structure which is still employed to build output power stages in power management integrated circuits. Over the past 30 years, although the lateral structure of power MOSFET is not adequate for high current switch, it’s still preferred by monolithic smart power applications in recent years because of the compatibility with advanced VLSI technologies [4,5].

A typical N-Channel LDMOSFET structure is shown in Figure 2.4. Compared to the basic MOSFET structure, LDMOS has an additional lightly doped drain (LDD) region between the body region and heavily doped drain region. The LDD region, instead of the body region, supports most of the voltage applied on the drain terminal. Therefore, the LDMOS can withstand higher voltage without any compromise on thicker gate oxide and longer channel length. At the same time, LOCOS (LOCal Oxidation of Silicon) technology is also employed to reduce the high electric field occurred at the corner of the gate. The junction of \( p\)-type body and \( n^+ \) source is short circuited by overlapping the source electrode to suppress the parasitic bipolar transistor. Sometimes, an additional \( p\)-type implantation is added to increase the doping concentration
underneath the source region, which will further reduce the resistance of the base region of the parasitic bipolar transistor [3].

![Figure 2.4 Schematic cross-section of a LDMOS](image)

Over the past three decades, publications have paid a lot of attention to the REduced SURface Field (RESURF) high voltage thin epitaxial layer technologies, which consecutively improved the performance of LDMOS [6,7,8]. In 1979, Philips Research Lab in Eindhoven first proposed the novel high voltage devices (RESURF devices) which gives the best trade-off between the on resistance and breakdown voltage of a lateral device [9]. Figure 2.5 explains the basic principle of the RESURF effect. The basic device structure consists of a high resistivity $p^-$ substrate with a lightly $n$-type doped epitaxial layer on it, which is laterally bounded by a heavily doped $p$ region. In Figure
2.5(a), the $n^-$ epitaxial layer is too thick to be fully depleted, so that the critical electric field is at the surface of $p^+/n^-$ junction. For a much thinner epitaxial layer in Figure 2.5(b), the lateral depletion layer around $p^+/n^-$ junction will interact with the depletion layer of the vertical $p^-/n^-$ junction, and the total effect is that the depletion edge moves towards the $n$-region, leading to a strong reduction in the surface electric field. When a higher voltage is applied, two electric field peaks occur at the surface, one originating from the $p^+/n^-$ junction and another just around the curvature of the $n^+/n^-$ high-low junction, with a moderate electric field in between. Thus in the vertical $p^-/n^-$ junction the ideal bulk breakdown can be achieved if the length of the $n^-$ drift region is sufficient. This makes it possible for lateral power devices to withstand a high voltage only with a thin epitaxial layer.

![Figure 2.5 Schematic of Distribution of Electric Field and Depletion Region for Different Epi-Layer Thickness](image-url)
To be able to carry high currents, many of these individual unit cells are connected in parallel and arranged in a silicon die. The MOSFET cell pitch determines the density of cells per unit area; moreover, the required current handling capability and the density of cells per unit area together determine the total semiconductor area. Minimizing the total area is critical to reduce manufacturing costs, which is one of the most important driving aspects to decide which solution is the most suitable one. However, regarding to the area occupancy, the planar structure LDMOS is unsatisfactory. In order to achieve a high breakdown voltage, even with the RESURF technology, the drain to source spacing has to be increased in comparison to low power MOSFETs. This feature will reduce the utilization of effective area to form the active region. Moreover all three terminal electrodes have to be formed from the upper of the die. Although this feature will be welcomed by the monolithic integration application, it complicates the interconnection in a single discrete device package [1].

2.3 Overview of Trench Power MOSFETs

In the early 1990s, a new power MOSFET technology, the trench power MOSFET, was introduced by Siliconix and became the preferred implementation because the improved conduction resistance [10,11,12,13,14]. The Structure of Trench power MOSFET is shown in Figure 2.6. As can be easily observed, the fundamental difference between the Trench MOSFET and LDMOS is, unlike the planar arrangement, the Trench MOSFET vertical structure employs the substrate material as the drain terminal. Trench MOSFET mitigate the cell density problem by forming the MOS channels along
the vertical walls of a trench, which is etched into the semiconductor material and filled with dielectric as the gate electrode, thus allowing closer cell spacing and increased current density. Consequently, Trench MOSFETs can offer much lower specific-$R_{DS(ON)}$ than LDMOS and is adopted by the majority of semiconductor manufactures progressively.

Figure 2.6 Schematic cross-section of Trench power MOSFET

After Trench MOSFET has been introduced, it evolved at a much faster pace than any other structures [15]. In the last decade, the trend towards DC/DC Converters with higher switching frequencies ignited a demand to minimize MOSFET related switching losses. At the same time, further scaling down the cell pitch of conventional Trench
MOSFET makes the inherent high Gate-Drain capacitor even worse. With the development of switching power converters, an emphasis shift took place toward improving the $R_{DS(ON)} \times Q_{GD}$ Figure of Merit, where $Q_{GD}$ is the gate-to drain switching charge defined in the field of power FETs. The main driver has been primarily directed at producing the lowest possible specific-$R_{DS(ON)}$ for an acceptable switching performance.

Figure 2.7 TEM Cross-section of the Trench MOSFET with labeling

Figure 2.7 shows a main cross-section of a low voltage trench power MOSFET. As the process technology continues improving, the cell pitch of the trench MOSFET can be
scaled down to sub-micron dimension, which can significantly improve the specific on-resistance of the switch. Besides the contribution from etching technology, another improvement over the traditional trench technology is the introduction of vertical trenched tungsten plug contacts to the source/body areas. The inclusion of the tungsten plug contacts allows the Trench MOSFET cell pitch to continue shrinking. Without the plug contacts, the scaling of the cell to less than 1μm would have been impossible due to the intrusion of the p+ region dopant in the channel through lateral diffusion, therefore increasing the threshold voltage and on-resistance.

In addition, this plug contact also helps the p+ body regions, which are implanted through open trenches, to be lowered closer to the drain. In this context, the advantage of the relatively deep body junctions is two-fold: firstly, it forces a desirable avalanche breakdown in the bulk region instead of the channel area near the bottom corner of the trench gate; and secondly, the gate-to-drain capacitance $C_{GD}$ is reduced because the area for the gate-to-drain capacitive interaction is reduced without the complication of more advanced processes. Several advanced techniques can help trench MOSFET to obtain such a deep body junction. One possibility is a double vertical implant into the open trench of the tungsten plugs, with a first high-energy implant for the lower portion of the profile (the p-body region) followed by a shallow, low-energy implant (the p+ region). Another possibility is arsenic implantation at the bottom of the gate trench to prevent the merging of the body regions from the sides of the trench [16].

On the other hand, allowing the body junction to go deeper results in longer channels and implicitly to higher on-resistance $R_{ON}$. However, one should keep in mind
the asymmetric, double-diffused nature of these transistors makes the total length of the channel less relevant to the drive capability of the transistor: it is the small length of the threshold portion of the channel around the peak doping of the body region that contributes primarily the total resistance of the channel, while the main, longer part of it makes up a normally-on transistor with a smaller contribution [17].

Another major improvement on Trench MOSFET towards reducing the Miller capacitance ($C_{GD}$) value incorporated a thick oxide layer at the gate trench bottom [18,19]. Figure 2.8 shows the TEM cross-section picture of a state of art thick-bottom trench MOSFET, with labeling of the transistor elements.

![Figure 2.8 TEM Cross-section of a Thick-bottom Trench MOSFET with labeling](image)
The new structure utilizes a normal thin gate oxide along the vertical trench walls and a thicker oxide at the bottom of the trench. Recently, as the development of the processing technology, the thick bottom oxide is created by a deposition process rather than by LOCOS or SACVD process. Therefore, the thickness of the trench bottom oxide layer can be further increased and now is normally 20%~30% of the trench total depth. In addition, the thick bottom oxide can further help to improve the long term reliability of Trench MOSFET brought by the avalanche breakdown occurring at the bottom corner of the trench. As a result, this structure allows further increase in cell density for lower specific on-resistance and achieves relatively low $C_{GD}$ at the same time.

Figure 2.9 TEM Cross-section of a Split Gate Trench MOSFET with labeling
A more advanced approach to improve the FOM of modern Trench MOSFETs is using the split polysilicon gate structure [20], as shown in the main cross-section of the device in Figure 2.9. In this case the polysilicon in the gate trench is split into two parts: the top segment acting as the control gate, and the bottom segment capacitively shielding the top gate from the drain region. The shield gate, being connected to the source outside the cross-section plane at both ends of the trench stripes, has double functions: firstly, it screening the top poly gate from the drain influence in A.C. and transient conditions; secondly, it shapes the electric field to avoid surface breakdown in D.C. and electrostatic conditions. The depletion region in Figure 2.9 shows how the bottom shield gate helps moving the breakdown location away from the gate surface: when a high voltage applied on the drain region, the capacitor of the shield gate operates in deep depletion and breaks down at its bottom when the avalanche condition is reached [21].

A simplified schematic representation of the integrate shielding principle is shown in Figure 2.10. It illustrates a fundamental problem of the shield-game architecture. In order to form a more effective shield gate, i.e., to deflect to ground the A.C. current coming from drain to gate, the drain to shield-gate capacitance has to be large in comparison with other inter-electrode capacitances, such as drain to FET-gate capacitance and FET-gate to shield-gate capacitance. This can be done by thinning the dielectric of the shield gate or by making the shield trench deeper. Unfortunately, thinning the shield-gate dielectric layer is limited by the requirement for it to support the large drain-to gate voltage. The thickness of the shield-gate oxide usually is around
1000Å, which is double of the thickness of FET-gate oxide. Therefore, the only remained solution is deepening the shield trench, which has its own limitation: if the shield trench is too deep, it substantially enters the heavily doped substrate region, reducing the breakdown voltage of the device. As a result, the shield-gate technique is efficiently applicable only to low-voltage power MOSFET.

Figure 2.10 A simplified schematic representation of the integrated shielding principle

The shielding gate is very effective in reducing $C_{GD}$, but such technique has been able to bring only incremental performance improvements at the cost of substantially increased process complexity. Simply just using narrow trenches with minimum area of the trench bottom may be an alternative approach. Also, because of the bad control of
the gate extension overlap length beyond body region, $C_{GD}$ is still relatively high no matter whether shielding gate or narrow trench approach is used. Trying to use short channel approach, the dopant concentration in the body region has to increase what leads to a high threshold voltage of the transistor. In other words there are design limitations inherent to the Trench MOSFET structure which can’t be removed easily. Thus, Trench-FET development is in a matured stage of technology optimization and further development can be expected to bring an incremental improvement only [3].

2.4 Overview of the NexFET$^\text{TM}$

![Potential Applications for NexFET](image)

Figure 2.11 Possible Frequency and Current Range for Different MOSFET [22]
Recently, a new generation power MOSFET, NexFET, was introduced to reduce associated parasitic capacitances while achieving a similar specific $R_{DS(ON)}$ to the Trench MOSFET technology [23]. NexFET has its roots in an LDMOS based transistor optimized for RF applications in a frequency range up to 2GHz. It takes the advantage of short gate from RF-LDMOS, which has a minimum overlap with source and drain regions. The reduced capacitances result in lower gate charges ($Q_G$ and $Q_{GD}$) required by switching the device at higher frequency. As shown in Figure 2.11, the new coming NexFET fill the application gap between Trench MOSFET and LDMOS [22].

![Figure 2.12 Schematic cross-section of NexFET](image)

The device structure is shown in Figure 2.12. Figure 2.13 shows a TEM picture of a NexFET manufactured with 0.35μm technology. The source metal creates a large area top electrode, and the current flow is diverted from the lateral channel, through a
heavily doped sinker region, into the substrate to reach the drain electrode at the back of the die. The heavily doped sinker region directs the current flow to the back side of the die, thus removing the scaling limitations of conventional LDMOS Transistor. Comparing to the conventional LDMOSFET, this vertical current flow makes this device suitable for carrying high current density.

Figure 2.13 TEM Cross-section picture of NexFET with junction and depletion region labeling

As the drain voltage increases, the depletion region shown in Figure 2.12 expands inwardly into the p-type body area until it hits the heavily doped p+ region and bulk breakdown occurs. This is the intended effect of the built-in diode clamping, i.e., the
location of the avalanche breakdown has been carefully chosen underneath the source contact by a built-in $p^+\text{-}p^-\text{-}n^-$ clamping diode. The diode has a breakdown voltage lower than the lateral breakdown in LDD region by 2V, which makes the device quite rugged in terms of absorption of a large amount of avalanche energy. This diode diverts avalanche breakdown away from the surface, where it would naturally occur and cause hot-electron oxide charging [24].

Unlike the conventional field oxide, the thinner oxide layer on top of LDD region is designed to be the dielectric of the grounded field plate above it. The field plate, created by portion of source metallization, stretches the electric field distribution away from the gate and reduces the critical electric field spike at the gate corner. By doing so, the hot carrier effects of creating reliability issues in the conventional LDMOS devices are avoided. Additionally, the unique topology of the source metal wrapping the polycide gate stack electrode makes an effective electrostatic shield between the gate and the drain potential appearing in the vertical current plug $n^+$ region.

The doping of the n-type LDD region follows the design guideline of charge balance, which is similar to the RESURF or super-junction approach. This two-dimensional charge balancing allows a given breakdown voltage to be sustained by a more heavily doped LDD region (a.k.a drift region) and a shorter pitch of the cell, thus minimize the specific on-resistance of the transistor. The gate to drain overlap is not determined by lithography, like in conventional LDMOS power FETs, but by the diffusion of a self-aligned LDD implantation. This feature minimizes the gate-to-drain
overlap, substantially reducing the gate-to-drain capacitance $C_{GD}$ and the gate-to-drain charge $Q_{GD}$.

The package of this device is also unique. Its most striking feature is the Dual-Cool involving metal plates on both the bottom face (standard) and top face (unusual) of the package, with portions of the top copper plate not overlapping the bottom one to make room for the gate connection to an external pin [25]. In a traditional QFN package the power device is usually over molded with low thermal conductivity mold compound making the thermal resistance to the top of the device high. Using this new package technology the thermal resistances to the top of the device are comparable to thermal resistance junction to case, so similar amounts of heat can be dissipated to the environment by using an appropriate heat sink attached to the top of the device.

The Specific $R_{DS(ON)}$ of NexFET Devices, taking advantage of the short MOS channel and short length of the LDD region, is competitive to Trench MOSFET Technology. The essential advantage of the NexFET comes from the low-input gate charge and very low $Q_{GD}$ values, which is not achievable with the state-of-art Trench FET device. The substantial improvement in $Q_{GD}$ comes from the integrated screening of the gate from the undesirable capacitive feedback from the drain, which is more efficiently done with the type of screening architecture used in NexFET (virtually total enclosing of the gate inside the dielectric shield) than with the split gate (only a portion of the gate covered by the shield) used in the other advanced trench power MOSFETs. With the significant reduced gate charges and competitive specific $R_{DS(ON)}$, the figure of
merit (FOM) values of NexFET are over 2-times better than the cutting edge Trench MOSFET [23] [26], as shown in Figure 2.14.

![Figure 2.14 Comparison of FOM for leading edge trench-FET parts vs. NexFET](image)

**Figure 2.14** Comparison of FOM for leading edge trench-FET parts vs. NexFET [27] [28] [29] [30] [31]
CHAPTER 3  OBJECTIVES AND METHODOLOGY

3.1 Objectives

As processor based systems, such as laptops or smart mobile devices, become more complex, more power is consumed in the new generation systems. Consequently, efficient power management solution for such systems ignites new challenges for next generation energy management, especially for improved power conversion efficiency or extended battery life. With the increasing emphasis of saving energy and increasing demand for more energy efficient power management and distribution, it is necessary to revisit the currently employed power architectures, which may no longer be the right solution to meet future needs.

The aggressive roadmaps for the future generations of microprocessors and their chipsets from Intel have imposed a number of challenges on the issues of power delivery and power management, such as the voltage regulation, thermal management, power density, efficiency, reliability and cost. In the present solutions, to maximize the conversion efficiency, the voltage regulators are typically operated at somewhat low frequencies, such as 300 kHz to 500 kHz. As discussed in Chapter 1.1, future voltage regulators, not only for serving the microprocessors but also for serving the other various loads, must be designed with significantly increased output current, lower output voltage, faster transient response and more accurate output voltage regulation. To meet these stringent requirements, following today’s low frequency approach, the number of the output capacitors and decoupling capacitors demands a significant increase. Currently, the output capacitance already occupied large real estates of the
mother board and cost over half of the whole voltage regulator module. With the large increased amount volume, it will be unrealistic to fit them into the limited space, let alone the significant cost inflation.

![Pie charts showing power loss breakdown for different switching frequencies](image)

**Figure 3.1** Power loss breakdown of a synchronous buck converter in different switching frequencies

Higher switching frequency is an applicable solution of the bulky and expensive output capacitors. However, the main bottleneck is that the voltage regulator suffers significant power losses at high frequency operations. A power loss breakdown of a synchronous buck converter is shown in Figure 3.1 [32]. In 500 kHz frequency application, conduction power losses are major power losses of the total power loss, thus on-resistance is always required to keep improving. However in higher frequency applications, because switching power loss increases proportionally to the switching
frequency, the total power loss increases significantly. Conduction losses remain nearly constant independent of frequency change, and contribute only a small percentage of the total power loss in the MHz frequency range. Switching power loss, substituting the conduction power loss, dominates the total power loss and draws more attention for further improvement.

Since reducing switching power loss became the primary design consideration, current power management solutions can no longer satisfy future requirements. The objective of this dissertation is to find a new solution to reduce the converter power loss and improve the voltage regulator efficiency in the future high frequency applications. The research will mainly focus on the design and development of next generation high performance low voltage power MOSFETs. Specific $R_{DS\,(ON)}$ is no longer the most important factor in the MOSFET to improve its performance. Parameters like $Q_G$, $Q_{GD}$ and $Q_{RR}$ related to switching power loss attract more attention now. Besides the consideration on silicon device, the excessive interconnection parasitic components between high-side and low-side MOSFET limit the transient performance and efficiency as well.

In this dissertation, firstly, a novel “source-down” structure NexFET is designed and developed to enable the innovative stack-die packaging technology which can effectively lower power loss brought by the parasitic components. At the same time, with its inherent lateral channel structure, the optimized “source-down” NexFET provide minimized $Q_G$ and $Q_{GD}$. Moreover, the MOSFET with intentional lower threshold voltage will be implemented in the low-side for the minimization of body diode reverse recovery
loss. An integrated “gate pull-down” circuit is designed as a protection for the employment of low $V_{TH}$ MOSFET which may introduce shoot-through issue and suffer efficiency degradation. In the meantime, dead-time can also be minimized without shoot-through risk, which could further effectively reduce the switching loss. All these aforementioned new technologies will be integrated together in one power module to increase the voltage regulator’s efficiency and power density in high frequency applications.

3.2 Methodology

The research approach flow of this work is illustrated in Figure 3.2. It starts with the TCAD manufacture process simulation. Process flow and process parameter need to be wisely designed to build the “virtual” power MOSFETs. The process models have to be carefully and iteratively calibrated for accurately matching the experimental data. TCAD device simulation and simulated characterization process is followed to provide evaluation of the virtual power MOSFETs. Afterwards, the virtual power MOSFETs will be placed into synchronous buck converter system for mixed-mode device/circuit simulation. TCAD tools will numerically solve Possion’s equation and the continuity equations of electron and hole currents self-consistently, using various specific physical models. At the same time, a set of measurements from which to characterize the existing system performance is required to determine the parameters of the circuit models. The accuracy of the measurements will be influential on generating meaningful simulations that can reproduce the performance of current solutions. Based on the market input (i.e.,
server or laptop specifications), such circuit simulations will primarily consist of parameter variations and sensitivity analysis to translate the load requirements into clear roadmap targets for the voltage regulator system. Any modifications in the power MOSFET that allow meeting the roadmap targets will be defined as improvement options. At last the most suitable and effective improvement will be implemented in the technology platform.

Figure 3.2 The proposed design approach
The critical aspect of the proposed methodology approach is to iteratively identify the most appropriated improvement options by means of active simulations. This raises the concept called virtual design loop, where numerical computations replace the usually enormous experimental or empirical effort to clarify the pathway toward the most effective solutions. Therefore the ability of the models to accurately predict performance trends as function of process, device or circuit parameters is of extreme importance for a successful technology development. Mixed-mode simulation not only can provide prediction of the electrical characteristics of arbitrary semiconductor structures under user-specified operating conditions, but also can offer SPICE-like circuit simulation capability combined with device numerical modeling capability. Moreover, unlike SPICE models of power MOSFETs, the numerical device model relying little on approximations or simplifications, faithfully represents the behaviors of a realistic power MOSFET, and therefore proves to be a very powerful tool for the investigation of power MOSFET.

The virtual design loop utilizes the device physics models to accurately predict the impact of new structures and/or topologies in the application. Therefore, it is essential that the characterization process be compatible with both experimental (real devices) and simulated (virtual devices) data. Only after enough virtual loop iterations have been run and the most suitable solution has been chosen, the prototype device will be worked out. The design process flow will begin once again after the new device performance being tested and more improvement being proposed.
4.1 Stack-Die Package Technology Configuration

As explained by various publications [33], parasitic inductances, introduced by the assembly of the push-pull stage, have a serious impact on the performance of the converter. Specifically, the total inductance in the main current path from $V_{IN}$ to ground (inductance number 3, 8, 9 and 10 shown in Figure 4.1) determines the voltage ringing on the switched node and the resulting power loss. In the conventional approaches, high-side and low-side MOSFETs are packaged discretely by LFPAK or SO-8 package. The package-related power loss is always larger than or at least equal to silicon-related power loss, no matter which packaging approach is chosen [34].

![Figure 4.1 Schematics of Synchronous Buck Converter assembly with related parasitic components](image-url)
In some recent new approaches, such as DrMOS, the two power MOSFETs and the corresponding gate driver circuits are integrated into a power module as shown in Figure 4.2 [35]. By integrating these components, it is possible to place the two MOSFETs close enough to minimize the current loop and the packaging-related power loss is no longer a dominant part of the total power loss. However, the wire bonding connection between the two switches, as well as to the output terminals, still introduce significant inductance in to the power converter.

![Image](image-url)

**Figure 4.2 Integrated Powertrains: MCM approach adopted by Intel for DrMOS**

Another more advanced system-in-package (SiP) module is shown in Figure 4.3 [36]. In this module assembly, copper (Cu) leads are used instead of the Au bonding wires to connect the topside electrodes of the MOSFETs to lead frames. Because of the wide copper plates, the current is uniformly distributed in the electrodes and minimum parasitic inductance is introduced. However, there is always a need to connect the front metal on the high side switch (source electrode) to the lead frame of the low side
MOSFET (drain electrode) (shown in Figure 4.3 (b)), when the package is used with power MOSFET devices with vertical current flow. This approach consumes more area and increases the footprint of the module.

Figure 4.3 Schematics of advanced power system in package with copper leads

Therefore, a new configuration for power switches is desired that does not introduce significant inductance, has minimum footprint area and low manufacturing cost.

An innovative three-dimensional stacking packaging approach is introduced by Texas Instruments recently [37], [38], where the MOSFETs are actually stacked on a grounded lead frame with two copper clips. In this stack-die packaging arrangement, which is illustrated in Figure 4.4, both high-side MOSFET die and low-side MOSFET die
are needed to be configured as MOSFET with vertical current flow and backside source electrodes. Because the dies are stacked, the backside source electrode of the high-side die can be directly connected to the top drain electrode of the low side die. A thick copper clip constituting the switching node ($V_{SW}$) of the synchronous buck converter is used between the two MOSFETs to provide the external phase node pins. The topside drain metal of high-side MOSFET is connected by another thick copper clip to the external input pins ($V_{IN}$ of the synchronous buck converter). The low-side MOSFET, which also has the source electrode on the backside of the die, is soldered to the main pad of the lead frame, providing the ground connection of the Power Block PSiP module.

Both top and bottom dies’ gate connections are made by gold wire-bonding ($T_G$ and $B_G$ in Figure 4.4). Pin $T_{GR}$ provides a sense signal of the switching voltage node which returns to IC driver and allows it to properly bias the gate of the high-side MOSFET.

**Figure 4.4 Stack-die packaging technology configuration**

As shown in cross-section view in Figure 4.5, the stacked-die configuration virtually eliminates the parasitic inductance and resistance between high-side and low-
side MOSFETs, especially the loop inductance shown in Figure 4.6, which is critical for the switching power loss. Using thick copper clips for high current connections ($V_{IN}$ and $V_{SW}$), substantially reduces the interconnect resistance of the power block in comparison to wire bonding solutions. Both of these unique packaging approaches contribute to the excellent electrical performance and help to achieve higher efficiency at higher switching frequency.

![Figure 4.5 A SEM Cross-section View of the Stack-die PSiP Module](image)

**Figure 4.5** A SEM Cross-section View of the Stack-die PSiP Module

![Figure 4.6 Stack-Die configuration virtually eliminates parasitic inductance and resistance between HS and LS MOSFETs](image)

**Figure 4.6** Stack-Die configuration virtually eliminates parasitic inductance and resistance between HS and LS MOSFETs
In this power system in package configuration, the two power MOSFETs must have a device structure providing a vertical current flow and a source electrode on the backside of the die. This setup allows for two device terminals at the output switching node to be placed in intimate contact that introduces minimal parasitic inductance.

Therefore, there remains a need to design an advanced power MOSFET structure with good device performance, vertical current flow and source terminal on the backside of the die.

4.2 Structure of the Source-Down NexFET™

In Chapter 2.4, a drain down version NexFET was introduced to reduce inherent parasitic capacitances while achieving similar specific $R_{DS\ (ON)}$ to the trench-gate MOSFET technology. However, the preferred power MOSFET devices that may be used in the stacked-die packaging technology are needed to have vertical current flow and backside source electrode. To meet this requirement, in this dissertation, an innovative source-down structure NexFET is designed, developed and fabricated [39] [40] [41].

Figure 4.7 is an illustration of a source-down NexFET device, specifically an n-channel MOSFET. This transistor structure includes a highly doped p-type silicon wafer substrate. The source electrode comprising conductive material such as Ti/Ni/Ag is coupled to the bottom surface of the substrate during packaging of the device. A p-type lightly doped silicon epitaxial layer is formed over the substrate. Comprising a doped polysilicon layer with an upper silicide layer, a conductive gate overlies the upper surface of the epitaxial layer.
The Lightly Doped Drain (LDD) region, completely formed within epitaxial layer, forms an enhanced drift region adjacent to heavily doped drain implant region. This enhanced drain drift region increases the lateral drain-to-source breakdown voltage, though it also contributes a lot for the on-resistance. The p-type doped body region is also formed in epitaxial layer and forms the channel region between source and enhanced drain region. A conductive source contact plug, also known as a sinker, is deposited in a shallow trench region formed adjacent to the sidewalls of the n+ source implant region and p-body region. A highly doped body contact p+ region is formed
under the contact plug and shorts the body region and the contact plug to the substrate, where the source electrode is coupled. The conductive source contact plug shorts the $n+$ source implant region, $p$-body region and the highly doped body region to source ground potential.

An insulation layer is formed over the conductive gate sidewalls and upper surface of the gate, as well as over the LDD region. The source contact plug conductive layer extends over the insulation layer, gate electrode and portion of the LDD region, working as gate shield and field plate at the same time. After the formation of the field plate layer and the insulation layer, the drain contact opening is etched and filled by a metal deposition. Excess of the metal deposition can be removed by CMP (Chemical-Mechanical Polish) process. Finally, the top drain metal is patterned to form a drain electrode that substantially covers on the active area of the device.

In this source down NexFET topology design, electrons flows from the source terminal on the substrate, through the low resistance, vertical sinker and metallization layer, into $n+$ source region, then is forwarded to drain terminal through the LDD region. All the active cells of the device are connected in parallel to allow handling of large currents. Comparing with the conventional LDMOSFET design with an interdigit type of layout of the drain electrode, the source-down NexFET device takes full advantage of a device with a vertical current flow and is free from drain metal contact de-biasing effect.
4.3 Device Design Considerations

A TEM cross-section picture of the source-down structure NexFET is shown in Figure 4.8. One of the design problems with this structure relates to the resistive contribution of the $p$-type doped substrate. The substrate can be grinded or etched to a desired thickness for minimizing the contribution of the substrate to the on-resistance of the MOSFET, which typically be finished toward the end of the fabrication processing of the substrate wafer.

Figure 4.8 TEM cross-section picture of source-down structure NexFET with junction and depletion region labeling
The doping level of the $p$-epitaxial layer is closely related to the vertical breakdown voltage and the on-resistance trade-off. Usually the doping of the epitaxial layer is chosen to be low enough and the thickness of the epitaxial layer is chose to be thick enough to meet the targeted breakdown voltage of the MOSFET which happened at the vertical $n$-LDD / $p$-epi junction. On the other hand, the thickness of the epitaxial layer is preferably as thin as possible in order to reduce the on-resistance between the drain and source along the vertical current. With this consideration, a highly doped $p$-type contact implant region is then formed under the source contact plug. Thus, the doping concentration of the epitaxial layer can be kept very low to withhold high breakdown voltage and the high doped $p$-type contact implant region will help to reduce the on-resistance.

At the same time, the highly doped $p$-type contact implant region also connects the $p$-body region to the substrate, which helps avoid the turn-on of the parasitic NPN bipolar transistor. This event can occur when generated or stored minority carriers have to flow through the body region to the source contact plug [42]. If the flow of the minority carriers results in a lateral voltage drop greater than 0.7V underneath the $n+$ source region, the $p$-body region / $n+$ source region PN junction would be forward bias and the NPN bipolar transistor would turn on. This normally will results in excessive heat dissipation and leads to a destruction of the device. Conventional approach to protect the transistor against this parasitic bipolar turn-on problem is to ensure a low resistance of the $p$-body region underneath the $n+$ source implantation and to make the lateral extension of the $p$-body region as short as possible. In this new device, because
the highly doped $p$-type contact implant region shorts the $p$-body to ground potential, the minority carriers flowing into the $p$-body region will flow the least resistive path to the substrate through the highly doped $p$-type contact implant region, which will result in significant lower voltage drop.

The doping concentration and location of the LDD region is carefully chosen to pin the location of the avalanche breakdown at the vertical $n$-LDD / $p$-epi junction instead of the lateral $n$-LDD / $p$-body junction. By doing so it is secured that no hot carriers are generated near the corner of the gate oxide and guarantees that the internal bipolar transistor will not be triggered up to very high avalanche current densities, which can limit the long term reliability of the MOSFET. In other words, the location of the electric breakdown at the vertical junction beneath the drain contact region substantially improves the reliability of this transistor. It allows the MOSFET to operate even under avalanche breakdown conditions, which is an important feature for some power applications.

The ratio of the gate-to-drain capacitance ($C_{GD}$) to the gate-to-source capacitance ($C_{GS}$) can be adjusted simply by the selection of the thickness of the insulation layer surrounding the gate electrode. Minimization of the $C_{GD}$ is always a consideration in conventional power MOSFET. Not only because larger $C_{GD}$ introduces higher switching loss, but also the large $C_{GD}/C_{GS}$ ratio is critical to the $C_{dv}/dt$ induced turn-on issue (will be described in Chapter 6.1) which happens in many power electronics applications. In the present device, the coupling between the gate electrode and the drain electrode is cut out by the field plate metal layer. Therefore, the ratio of $C_{GD}/C_{GS}$ is inherently small and
can be further adjusted by a reduction of the thickness of the insulating layer which could increase the value of $C_{GS}$.

The formation of a single and continuous conductive layer of source contact plug greatly simplifies the fabrication of the source-down NexFET, as the source contact, gate shield and field plate can be formed using the same fabrication step. As a result, there is no need to form a separate gate shield of field plate nor is there a requirement to separately connect the gate shield to the source. Thereby, the manufacturability of the source-down NexFET is greatly improved.

### 4.4 Effect of the MOSFET Design Parameters on Performance

Numerical TCAD manufacture process simulation is used to design the MOSFET and study the effects of the power MOSFET design parameters on final performance. As addressed in CHAPTER 2, the switching loss is mainly determined by $Q_{GD}$, the gate driver loss by $Q_G$ and the conduction loss by $R_{DS\ (on)}$. The effects of numerous design parameters on these device performances are studied.

**a) Poly Gate Length ($L_G$)**

Because gate length ($L_G$) has a close relationship with the channel on-resistance and gate charge, obviously, it plays a very important role in device performance. Usually, shorter gate length can provide small channel on-resistance and smaller gate charge at the same time. Therefore, a number of advanced process techniques are studied to achieve shorter gate length. As shown in Figure 4.9, adjusting $n+$ source, $p$-body and
LDD implantation dosage and thermal budget can be used as an effective way to shrink the gate channel avoiding the requirement of increasing the complex of fabrication.

Figure 4.9 Doping profiles of the channel region with different channel length

Figure 4.10 Simulated leakage current curves of the MOSFETs with different gate length

However, as the scaling down of gate length, the characteristics of the MOSFET change due to short-channel effects. As shown in Figure 4.10, the leakage current is increased with the shrinking of gate length. At short gate lengths, transistors also will
suffer threshold voltage shift. If the gate length is too small, the switch is more susceptible to lateral junction breakdown or punch-through breakdown in the n+ source / p-body / n-LDD junction.

As a result, the channel length cannot be reduced too much. Meanwhile, adjusting body implantation conditions is necessary. The doping profile in the body region along the interface with the gate should be made as flat as possible which allows a reduction of the channel length while avoiding $V_{TH}$ shift.

b) *Gate Oxide Thickness ($t_{ox}$)*

![Graph showing the effects of gate oxide thickness on $Q_{GD}$ and on-resistance](image)

**Figure 4.11** The effects of gate oxide thickness on $Q_{GD}$ and on-resistance

The effects of gate oxide thickness on $Q_{GD}$ and on-resistance are shown in Figure 4.11. As expected, thicker $t_{ox}$ leads to higher on-resistance and lower $Q_{GD}$. This
parameter influences the trade-off between the conduction loss and switching loss. The overall effect on the $Q_{GD} \times R_{DS(ON)}$ Figure-of-Merit is that the FOM has a slight reduction with the decrease of the $t_{OX}$ in the range of 100Å to 300Å. However, the gate oxide cannot be too thin, since it needs to support the gate-to-source voltage.

c) LDD Region Length and Doping Level

The lightly doped drain (LDD) region length and doping level are critical in the trade-off between breakdown voltage and on-resistance. Each power MOSFET structure contains an internal diode created by the PN junction between body and drain regions. In the case of the source-down NexFET, the blocking diode structure is created by $p$-body, $n$-LDD and $n^+$ drain regions. Since the slope of the electric field distribution is proportional to the doping concentration, if the doping of the LDD region is lighter, the electric field inside the LDD region will be lower, therefore, the diode breakdown voltage will be larger. As shown in Figure 4.12, if the doping of the LDD region is too high, breakdown voltage is limited by the electric field spike at the LDD / $p$-body junction. In opposite, if the doping concentration is lower, the LDD / $p$-body junction breakdown will be increased. The vertical junction breakdown occurs prior to the lateral LDD / $p$-body junction breakdown. It’s always a better design to move the avalanche breakdown far from the gate oxide, which can avoid hot carrier generated during the avalanche breakdown injecting into the gate oxide.
Figure 4.12 Simulated impact ionization distribution of Source-Down NexFETs with heavy (left) and light (right) LDD doping level.

Figure 4.13 LDD length impact on the trade-off between breakdown voltage and on-resistance.
In general, the LDD region has to be made longer to withhold high enough breakdown voltage, although this will result in an increase of the specific on-resistance of the device. Figure 4.13 shows the effect of the LDD length on both lateral breakdown voltage and specific on-resistance. The selection of the LDD length should be mainly based on the requirement of the avalanche breakdown voltage.

\textit{d) Epitaxial Layer Thickness}

The epitaxial layer thickness is another important factor related to the trade-off between breakdown voltage and on-resistance. On one hand, the thickness of the epitaxial layer need to be large enough to withhold the breakdown voltage; on the other hand, it is preferably as thin as possible in order to reduce the on-resistance between the drain and source along the vertical current.

Take the 30V MOSFET design as an example. As shown in Figure 4.14, when the epitaxial layer is unnecessary thick, the vertical junction has a higher breakdown voltage and the device breakdown is limited by the lateral junction. As a result, the unnecessary thick epitaxial layer cannot provide any extra benefits on device breakdown voltage, but only brings a large on-resistance. In this situation, the epi-layer can be reduced to the optimized value which is in the red circle in Figure 4.14. The on-resistance can be improve a lot but still keeps a high breakdown voltage. Figure 4.15 shows how the avalanche breakdown location changes from the corner of gate oxide to the bulk junction when the epi-layer thickness is reduced.
Figure 4.14 The relationship between breakdown voltage and epitaxial layer thickness

Figure 4.15 Simulated impact ionization distribution in Source-Down NexFET with various epitaxial layer thickness

e) Die Size of Transistor

The die size of the power MOSFET is always a compromise. For design and optimizing the power MOSFET regarding efficiency, a well-balanced ratio between switching losses and conduction losses has to be found. If the die size is too small, the resulting $R_{DS(ON)}$ of the switch is too large, and the respective conduction loss is too high. On the other hand, if the die size is too large, transistor capacitances are large leading to
excessive switching loss. At the same time, at which load current should the MOSFET be optimized is another question to be considered. Large chip set with smaller conduction losses shows advantage in efficiency in heavy load condition, whereas small chip set with smaller switching power loss is always used for light load optimization.

![Power Loss vs. High-Side Area](image)

*Figure 4.16 Optimization of die size for high-side transistors*

Therefore, the die size optimization always focuses on an known operating condition. Figure 4.16 and Figure 4.17 illustrate the power loss as a function of active area of the high-side and low-side switches. In this case, the synchronous buck converter is working in the conditions of 12V input voltage, 1.8V output voltage, 25A output current and 1MHz frequency. The duty cycle of this case is small and low-side switch has to conduct much longer than the high-side transistor. Meanwhile, the high-side switch is switching against the full input voltage under a high frequency resulting in
large switching power loss. Therefore, the high-side switch has to be made much smaller than the low-side switch.

Figure 4.17 Optimization of die size for low-side transistors

### 4.5 Device Performance

The improved source-down structure NexFET device is fabricated by a 0.35µm process and packaged with stacked-die technology for power applications such as DC/DC voltage regulators. The aforementioned transistor provides the advantageous switching performance of a power LDMOSFET while introducing a large current handling capability due to the vertical current flow and continuous drain and source electrodes on top and bottom side of the die. At the same time, the implementation of
the continuous source contact on the back-side of die also can minimize the cell pitch of the device, which provides higher channel density, and smaller specific $R_{DS(ON)}$.

The measured voltage blocking capability of the source-down NexFET is presented in Figure 4.18. As addressed previously, in order to fulfill all kinds of requirements in low voltage power applications, the length of the LDD region can be adjusted to acquire various devices with different breakdown voltage ratings. In Figure 4.18, the voltage blocking performance of NexFET switches with 25V and 30V breakdown voltage rating is shown. The actual breakdown voltage of the device is usually higher than the voltage rating by 5% ~ 10% margins depends on the location of the avalanche breakdown within the device.

![Source Down NexFET I-V Curves](image)

Figure 4.18  Experiment results of 25V and 30V Source-Down NexFET breakdown characteristics
The measured forward $I_D$-$V_{DS}$ curves of the source-down NexFET are shown in Figure 4.19 [43]. The on-resistance of a 30V packaged device with an active area of 8.5 mm$^2$ is approximately 2.2 mΩ at $V_{GS}$ of 4.5 V and 2.0 mΩ at $V_{GS}$ of 8.0 V. The corresponding specific $R_{DS(ON)}$ of the source down NexFET die is 18.7 mΩ·mm$^2$ at $V_{GS}$ of 4.5 V and 17 mΩ·mm$^2$ at $V_{GS}$ of 8.0 V. Table 4.1 compares the experimental and simulation results of 25V and 30V MOSFETs. The difference between the simulation and experiment is reasonable.

![Figure 4.19 Measured forward $I_D$-$V_{DS}$ curves of the source-down NexFET at different $V_{GS}$](image)

SMPS (Switched Mode Power Supply) applications demand power MOSFETs with minimum power losses under hard switching conditions. Low switching losses can be achieved by minimization of the internal capacitances associated with the structure of the device. As discussed in chapter 2.1.2, two device parameters are critical to allow high
frequency switching with low switching power losses: low $Q_G$ reducing gate driver power loss and low $Q_{GD}$ being responsible for fast voltage transients.

Table 4.1 Comparison of the Experimental and Simulation Result

<table>
<thead>
<tr>
<th>Breakdown Voltage</th>
<th>Threshold Voltage</th>
<th>Specific $R_{DS(ON)}$ ($V_{GS}=4.5V$)</th>
<th>$C_{RSS}$</th>
<th>$C_{ISS}$</th>
<th>$C_{OSS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>30V NMOS (Experiment)</td>
<td>32.2 V</td>
<td>1.1 V</td>
<td>18.7 mΩ-mm$^2$</td>
<td>5.6 pF/mm$^2$</td>
<td>236 pF/mm$^2$</td>
</tr>
<tr>
<td>30V NMOS (Simulation)</td>
<td>31.5 V</td>
<td>1.0 V</td>
<td>17.1 mΩ-mm$^2$</td>
<td>4.9 pF/mm$^2$</td>
<td>214 pF/mm$^2$</td>
</tr>
<tr>
<td>25V NMOS (Experiment)</td>
<td>27.6 V</td>
<td>1.1 V</td>
<td>12.3 mΩ-mm$^2$</td>
<td>7.8 pF/mm$^2$</td>
<td>293 pF/mm$^2$</td>
</tr>
<tr>
<td>25V NMOS (Simulation)</td>
<td>26.7 V</td>
<td>1.0 V</td>
<td>11.0 mΩ-mm$^2$</td>
<td>7.4 pF/mm$^2$</td>
<td>267 pF/mm$^2$</td>
</tr>
</tbody>
</table>

Figure 4.20 Measured Qg curve of Source-Down structure NexFET

Figure 4.20 shows a measured gate charge curve of a 30V source-down structure NexFET with a 2.2mΩ on-resistance at $V_{GS}$ of 4.5 V. The total gate charge ($Q_G$) is 20 nC at $V_{GS}$ of 4.5 V and the gate-to-drain charge ($Q_{GD}$) is 3.6 nC.
4.6 Discussion on Power Block Performance

While remains the similar on-resistance of the state of the art Trench technology, source-down configuration NexFET combined with innovative integrated stacked-die package technology (which is called “Power Block”) reduces the switching losses and delivers a significant efficiency improvement for SPMS systems. Figure 4.21 illustrates the efficiency and power loss of power block in a typical synchronous buck converter under different switching frequency converting the 12V input voltage to 1.3V output voltage.

![Figure 4.21](image)

Figure 4.21 Power loss and efficiency of the NexFET power block in various switching frequency applications

As known in previous chapters, switching power loss is significantly magnified in high frequency application. However, with the outstanding low gate charge and innovative stacked-die packaging technology, when the frequency increases to 3MHz,
the power block only suffers 6W power loss at 25A output current and the efficiency still can remain above 85%.

**Table 4.2 Comparison of electrical parameters of NexFET power block and leading competing trench dual MOSFET**

<table>
<thead>
<tr>
<th></th>
<th>TI NexFET Power Block 5mm × 6mm</th>
<th>Competing Trench Dual MOSFET 5mm × 6mm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CtrlFET</td>
<td>SyncFET</td>
</tr>
<tr>
<td>( V_{BR} )</td>
<td>25 V</td>
<td>25 V</td>
</tr>
<tr>
<td>Current Rating</td>
<td>40 A</td>
<td>40 A</td>
</tr>
<tr>
<td>( R_{DS(ON)} ) @4.5V</td>
<td>5 mΩ</td>
<td>2 mΩ</td>
</tr>
<tr>
<td>( Q_{G} ) @4.5V</td>
<td>8.2 nC</td>
<td>19.4 nC</td>
</tr>
<tr>
<td>( Q_{GD} )</td>
<td>1 nC</td>
<td>2.5 nC</td>
</tr>
<tr>
<td>( Q_{GS} )</td>
<td>3.2 nC</td>
<td>5.1 nC</td>
</tr>
</tbody>
</table>

As discussion in chapter 2.3, although trench power MOSFET is optimized by various ways to improve the parasitic gate capacitances, such as thick gate oxide in the trench bottom, it still suffers large switching power loss at higher switch frequency operations. A leading competing dual trench MOSFETs product in market is chose to have a performance comparison with the NexFET Power Block. Table 4.2 demonstrates a comparison of the key electrical parameters of these two devices. Both of these two devices have high-side switch and low-side switch integrated together in a 5mm×6mm package. With 25V breakdown voltage and 40A current rating, these two similar devices are suitable for the low voltage high current computing applications, such as in server.

Figure 4.22 shows a power loss comparison to a leading competing Trench technology dual MOSFET product. The slopes of trench power loss curves slopes are obviously sharper than NexFET power block, which means switching loss and body-
diode loss dominate the total power loss in MHz frequency range and Trench MOSFET has more efficiency degradation. Figure 4.23 shows the overall efficiency comparison between NexFET power block and competitor’s dual trench MOSFET with 15A and 25A output current at various switching frequencies. While NexFET power block initially demonstrates 1% higher efficiency at 500 kHz, the efficiency improvement increases with rising switching frequency and can be beyond 2% at 3 MHz.

![Graph showing power loss and efficiency comparison](image)

**Figure 4.22** Power loss and efficiency comparison with competing dual trench MOSFET
Figure 4.23  Power loss and efficiency comparison with competing dual trench MOSFET in various switching frequency applications

Besides the great improvement in silicon, the innovative stack-die packaging technology also optimized the high frequency performance of the DC/DC power converter by avoiding the presence of unwanted parasitic interconnecting inductances and resistances. As widely known, the common source inductance (CSI), which is the inductance shared by the main current path and the gate driver loop in a converter, greatly impedes the switching characteristics of the MOSFET which in turn increases switching losses and reduces system efficiency [44] [45]. Any voltage induced on CSI changes the effective gate-source voltage of the MOSFET. Because of the importance of gate-source voltage on the switching performance of power MOSFETs, CSI has a significant impact on the system performance, especially on HS MOSFET switching loss.
In order to illustrate the improved performance brought by the innovative stack-die packaging technology, two converters are given here: one is conventional synchronous buck converter with two discrete MOSFETs as the high-side and low-side switches; the other is a synchronous buck converter using Power Block devices as switches. The Table 4.3 lists the main device electrical parameters of the NexFET power block device and two conventional discrete power MOSFETs. Both power block and discrete MOSFETs adopt the NexFET technology and have a similar excellent figure of merits. For this comparison, the same gate driver ICs are used in both converters, as well as the same output inductor, similar PCB layout designs and the same test conditions: $V_{IN} = 12V$, $V_{DRIVER} = 5V$, $V_{OUT} = 1.3V$, $I_{OUT} = 25A$. Figure 4.24 compares the efficiency and power loss performance versus output current curves under 500 kHz and 2 MHz switching frequency of the two cases. The power block obviously has less power loss and higher efficiency than the traditional discrete power MOSFETs as it virtually eliminates the undesired parasitic loop inductance. Since all the package parasitic components are frequency dependent, the difference in efficiency between the two circuits is magnified while the switching frequency increases from 500 kHz to 2MHz, especially operating under heavy load current conditions. This result reflects the power block has much more higher-current and high-frequency handling capability than the traditional discrete approach.
Table 4.3 Comparison of Electrical Parameters of NexFET Power Block and NexFET Discrete MOSFET

<table>
<thead>
<tr>
<th></th>
<th>NexFET Power Block 5x6</th>
<th>NexFET Discrete MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CtrlFET</td>
<td>SyncFET</td>
</tr>
<tr>
<td>V_{BR}</td>
<td>25V</td>
<td>25V</td>
</tr>
<tr>
<td>R_{DS(ON)} @4.5V</td>
<td>5 mΩ</td>
<td>2 mΩ</td>
</tr>
<tr>
<td>Q_{G} @4.5V</td>
<td>8.2 nC</td>
<td>19.4 nC</td>
</tr>
<tr>
<td>Q_{GD}</td>
<td>1.0 nC</td>
<td>2.5 nC</td>
</tr>
<tr>
<td>Q_{GS}</td>
<td>3.2 nC</td>
<td>5.1 nC</td>
</tr>
</tbody>
</table>

Figure 4.24 Power loss and efficiency comparison with discrete NexFETs
CHAPTER 5  INFLUENCE OF THRESHOLD VOLTAGE OF SYNCHRONOUS POWER MOSFET

5.1 Introduction

In this Chapter, the influence of the threshold voltage of the low side (LS) power MOSFET on the overall performance of buck converters is investigated. The potential benefit of lowering the LS power MOSFET threshold voltage $V_{TH}$ to suppress the switching node voltage overshoot is also studied.

The trend of operating DC-DC converters at even higher switching frequencies mandates further reduction of power MOSFET losses. New switching devices like NexFET, offer very low conduction and switching losses as well as less driving energy requirement, allowing very fast switching. However, it is found that faster switching of power MOSFETs tends to lead to high voltage ringing at the switching node of a buck converter. Usually, additional measures, such as scaled-down gate drive, low package parasitic inductance, external bootstrap resistor and/or snubber circuits are used to reduce the undesirable voltage ringing [46], [47].

There are two major concerns about excessive switching node voltage ringing. One is the initial high voltage overshoot which may induce excessive stress to the power MOSFETs and ultimately device destruction. The other concern is that the voltage ringing causes significant electromagnetic interference (EMI) which is a major system issue. The voltage ringing may also incur significant power loss increase. This chapter is focused on the investigation of the first concern on voltage overshoot and does not
specifically discuss the EMI concern which greatly depends on the overall system design [48].

A power MOSFET with a threshold voltage lower than the typical range of 1.2-1.7 volts used as the LS-switch in a synchronous buck converter is first simulated and optimized with TCAD software. The impact of the low $V_{TH}$ LS MOSFET on the converter performance is highlighted in this chapter.

### 5.2 Basic Concept and Modeling Result of Switch Node Voltage Ringing Reduction and Power Loss Improvement

Figure 5.1 shows a synchronous buck converter with the control FET (high-side switch) and the sync FET (low-side switch) including their integral body diodes. When the low-side (LS) MOSFET initially conducts current but is abruptly turned-off, its gate voltage $V_{GS}$ will decay exponentially as determined by the input capacitance $C_{ISS}$ and the total gate impedance of the low side switch. The switch is considered turned-off as $V_{GS}$ falls below the threshold voltage (typically in a range of 1 to 3 volts). During the dead-time, which is defined as the time period when both high-side (HS) and low-side (LS) switches are turned off, the drain-to-source voltage $V_{DS}$ of the LS MOSFET is negative and its body diode become forward biased [49]. Thus, this body diode is in a conducting state and carries a certain portion of the inductor current. Note that the rest of the inductor current still flows through the LS MOSFET channel depends on the value of its $V_{TH}$, and is larger for low threshold voltage.
During the turn-on of the control FET, the LS body diode reverse recovery extends the time it takes for the switch node voltage to transit from $-V_F$ to $+V_{IN}$ as the voltage across the diode is effectively held constant until reverse recovery current peaks. During this time, HS-switch has to supply the current needed for the reverse recovery of the LS body diode, and then to charge the output capacitance $C_{OSS}$ of the LS-FET. Although the $C_{OSS}$ charging loss contribution is small sometimes [50], the high reverse recovery current adds to the HS current during turn-on and leads to a high $di/dt$ at the switch node generating a higher voltage spike on parasitic inductances on the board. At the same time, the large voltage and current presented across on the HS switch result in an extra power loss during switching.
Figure 5.2 Simulated Switch Node Voltage Waveforms Showing Ringing (a) and LS-FET Body Diode Transient (b)

A series of 30V rating N-channel power MOSFETs, which is the typical device voltage rating for the 12 V conversion application, were simulated with different P-body
region doping levels and diffusion conditions, resulting in different threshold voltages. In Figure 5.2, a low threshold voltage power MOSFET and a normal threshold voltage power MOSFET are compared when they are used as the low-side switch in a typical synchronous buck converter. Figure 5.2(a) shows the switch node voltage during the turn-off of the low-side MOSFET and the turn-on of the high-side MOSFET. Figure 5.2(b) shows the body diode conduction waveforms during the dead-time.

Under the 12V input and 1.3V output operating conditions, the switching node voltage of the sync-buck converter using a normal threshold voltage (1.2V) could reach as high as 30V. Figure 5.2(b) also shows that the body diode of the low-side MOSFET is fully conducting with a 0.7 V forward voltage during the dead-time. However, in the case of the low threshold voltage MOSFET (0.8V), the forward voltage of the body diode drops from 0.7V to 0.6 V, indicating more current going through the MOS channel instead of the body diode. Consequently, the switch node voltage spike is significantly reduced from 30V to 22V due to the suppressed reverse recovery in the synchronous MOSFET.

Another benefit arises from the reduced threshold voltage of the low-side power MOSFET is the lower on-resistance. Since the threshold voltage reduction is made possible through the change in the p-type body dose and thermal drive conditions, lower threshold voltage usually leads to a lower specific on-resistance, as long as punch-through breakdown is prevented. Figure 5.3 shows the relationship between the on-resistance and threshold voltage of the power MOSFET. With the on-resistance
reduction, the employment of a low threshold MOSFET in buck converters can bring even greater improvement on efficiency.

![Graph showing specific on-resistance as a function of threshold voltage of the LS power MOSFET](image)

**Figure 5.3** Specific on-resistance as a function of threshold voltage of the LS power MOSFET

### 5.3 Experimental Results and Discussion

Texas Instrument’s Multi-Chip-Module (MCM) Power Block is used to validate the efficiency improvement and ringing reduction by lowering $V_{TH}$ of the LS-MOSFET. Two otherwise identical buck converters were built using two LS-MOSFETs with $V_{TH}$ of 1.3V and 0.8V respectively. Figure 5.4 shows the switch node voltage waveforms of the two buck converters. As explained in last section, during the high-side switch turn-on process, a reduced reverse recovery current is carried by the HS-MOSFET when the low threshold voltage LS-MOSFET is employed. This leads to a lower $di/dt$ at the switch
node and thus a lower voltage overshoot. In the 12V input and 1.3V output buck converter, a voltage overshoot of 26V is observed at the switch node with the normal threshold voltage LS-MOSFET and only 22.6 V with the low threshold voltage LS-MOSFET.

![Switch node voltage ringing reduction effect of low threshold voltage MOSFET under 12V input application.](image)

Figure 5.4 Switch node voltage ringing reduction effect of low threshold voltage MOSFET under 12V input application.
In addition to minimizing reverse recovery and lowering the switching node voltage ringing, reducing the LS-MOSFET threshold voltage also lowers its on-resistance and reduces the conduction loss. As shown in Fig.5, 0.4% efficiency increase is observed after employing the low threshold voltage MOSFET in 12 V input and 1.3 V output application while switching at 500 kHz and 25 °C.

![Image](image_url)

**Figure 5.5** Efficiency (a) and power loss (b) comparison for 12 V input, 1.3 V output, 500 kHz and 25 °C application

Since the $Q_{RR}$ loss will account for a larger portion of the total power loss of buck converters at high PWM frequencies, the efficiency improvement through implementation of low $V_{TH}$ LS-MOSFET will be an even more attractive solution for the mega-hertz frequency range. As shown in Figure 5.6, over 1.2% efficiency increasing at full load and around 1.8% efficiency increasing at peak value is observed in a 2M Hz application.
Figure 5.6 Efficiency (a) and power loss (b) comparison for 12 V input, 1.2 V output, 2 MHz and 25 °C application
CHAPTER 6  THEORETICAL STUDY ON SYNCHRONOUS MOSFET WITH MONOLITHIC GATE PULL-DOWN CIRCUITRY

6.1 Potential Shoot-Through Risk on Low $V_{TH}$ Synchronous MOSFET

As described in chapter 2.1, replacing the freewheeling diode in the conventional buck converter with a power MOSFET provides a low conduction loss recirculation path for the inductor current. This replacement is advantageously selected for low conduction power loss, and the converter efficiency can be improved a lot. However, addressing one problem introduces another. Specifically, the faster the high-side MOSFET is turned on, the more susceptible the low-side synchronous MOSFET suffer the shoot-through issue, which is also called $C \cdot dV/dt$ induced turn-on. [3,51]

$C \cdot dV/dt$ induced turn-on of the synchronous MOSFET happens after the body diode reverse recovery process. Figure 6.1 shows a low-side MOSFET in a synchronous buck converter at the moment of a positive $dV/dt$ voltage transient appearing across the drain to source. After the high-side MOSFET is turned on, the voltage at the switch node rapidly changes in voltage, $dV$, within a very short time interval, $dt$. This applied high $dV/dt$ charges the Miller capacitance ($C_{GD}$) of the synchronous MOSFET and results in an instantaneous current flow, which in turn injects charge into the gate node of the synchronous MOSFET. As shown in Figure 6.2, this drives the gate has a positive gate bounce voltage value at the very moment when the driver is trying to hold the gate low. The current through $C_{GD}$ would sink down to ground through the low-side gate impedance and output impedance of the gate driver (as shown in Figure 6.1), or would be absorbed by the $C_{GS}$ of the low-side switch.
Figure 6.1 The $dV/dt$ voltage transient across the low-side (synchronous) MOSFET leads to the off-state current conduction.

The worst case of the peak height of the low-side gate voltage bounce can be modeled by an analytical formula as shown in Equation 6.1 [3], [52].

\[
    V_{GS,Bounce} \approx R_G \times C_{RSS} \times \frac{V_{DS}}{T_R} \left( 1 - e^{\frac{-T_R}{R_G C_{ISS}}} \right)
\]  

(6.1)

Where the $R_G$ includes both gate impedance and gate driver output impedance, and $T_R$ is the rising time of the switch node. The $C_{GD}$ and $C_{GS}$ form a capacitive voltage divider which could attenuate the gate step. If the ratio of the $C_{GD}$/$C_{GS}$ is larger than a
critical value and the sink resistance on the gate is large as well, the peak value of the gate bounce will exceed the threshold voltage of synchronous MOSFET, and the low-side switch conducts for a short time. The shoot-through current flows from the input voltage supply through the high-side and low-side transistors to the ground and results in power loss and excessive stress to the power MOSFETs which could eventually failure the device.

Figure 6.2 Key waveforms during the $C \cdot dV/dt$ induced turn-on event
To make the synchronous MOSFET less susceptible to $C \cdot \frac{dv}{dt}$ induced turn-on, the design goal of the low-side switch is to minimize the gate voltage bounce to a maximum value less than threshold voltage. Lowering the Miller capacitance $C_{GD}$ and increasing $C_{GS}$ will result in better $dv/dt$ immunity. The previous study showed that one of the key factors for well-designed synchronous buck converters with typical low-side gate resistance and driver resistance is the gate charge ratio (CR), which is defined as $Q_{GD}/Q_{G(TH)}$ [51], [53]. As shown in Figure 6.3, the $Q_{GD}$ is the gate to drain charge at a specified drain to source voltage, and the $Q_{G(TH)}$ is the gate to source charge for $0<V_{GS}<V_{TH}$. The tradeoff between the charge ratio, the threshold voltage and the gate

Figure 6.3 Typical power MOSFET gate charge waveform

\[
\begin{align*}
V_{GS} (V) & \\
V_{TH} & \\
V_{DS} (V) & \\
Q_{GD} & \\
Q_{G(4.5V)} & \\
Q_{G(TH)} & \\
Q_{GS} & \\
Q_{GD} & \\
\end{align*}
\]
impedance of the synchronous MOSFET is the key issues to improve the $C \cdot dV/dt$ immunity.

It has to be noticed that an increase of the low-side switch gate impedance and output sink resistance of the gate driver which was proposed to reduce the dead time gap and eliminate body diode conduction and $Q_{RR}$ related problems is not allowed if the synchronous MOSFET has a weak shoot-through tolerant.

As described in CHAPTER 5, the current flowing through the low-side switching MOSFET with the forward biased body diode is shared by the integral body diode and the FET channel simultaneously. The lower the threshold voltage of the synchronous MOSFET, the more current flows through the channel and the less reverse recovery charge stored in the body diode. Less $Q_{RR}$ means lower reverse recovery current peak and lower power loss during fast switching. Also, the design of the low-side switching transistor device with a lower threshold voltage reduces its on-resistance value at a given gate drive voltage. This in turn lowers the conduction loss in the synchronous FET and increases the overall system efficiency. However, this exacerbates the shoot-through issue as discussed above.

### 6.2 Concept of Monolithic Integrated Gate Pull-Down Circuitry

One possible solution to suppress the $C \cdot dv/dt$ induced turn-on is attempt to utilizing slower rising time on the high-side MOSFET [52]. As displayed in Equation 6.1, slowing down the rising time results in a smaller gate bounce voltage coupled into the
low-side MOSFET gate. However, of course, this will limit the switching efficiency of the synchronous buck converter.

Another possible solution is to utilize transistors that have a higher threshold voltage [53]. However, since synchronous MOSFET often carries high load current at low duty cycle application, utilizing the lowest on-resistance MOSFET is a primary decision. Since MOSFETs with higher turn-on threshold voltage usually have higher associated on-resistance, this will lead to higher conduction losses and is not a best solution.

Accordingly, there is a demand to implement a power MOSFET switch with a low threshold voltage with better $dv/dt$ immunity during its turn-off event.

As a solution of this problem, an integrated pull-down circuit in low-side MOSFET is proposed, utilizing a capacitive coupling between the gate and drain terminals of a power MOSFET, which is the root cause of $C\cdot dv/dt$ induced turn-on problem in the switch. The integrated pull-down circuit concept can be implemented in any switching power MOSFET, and especially can be implemented at MOSFETs used in push-pull configuration in any switched DC-DC converter topologies. Figure 6.4 shows a switching stage for a switched mode power supply (SMPS) with this pull-down circuit integrated in low-side switch. A pull-down MOSFET has a drain terminal connected to the gate node of the primary low-side power MOSFET and share the same source terminal of the main FET. The gate of the pull-down MOSFET is connected to one terminal of a coupling capacitor and another terminal of the coupling capacitor is connected to the drain node of the primary MOSFET, where the high $dv/dt$ happened
during the turn-off of the primary FET. An optional resistor called bleeding resistor is attached between the gate and source terminal of the pull-down MOSFET.

In operation during the conduction of the low-side primary FET, the pull-down MOSFET is turned off and doesn’t play a role. During the turn-off of the low-side primary FET, the \( dv/dt \) effect across the main switch causes the coupling capacitor to pull up the gate voltage value of the pull-down MOSFET, turning the transistor on, which in turn holds the gate terminal of the primary FET at its source potential. The simulated electron current density distributions of both high-side and low-side MOSFET during the high \( dv/dt \) events are shown in Figure 6.5, in which warmer color
represents higher current density distribution and cooler color means lower current density distribution.

Figure 6.5 Electron current density distribution during high $dV/dt$ event in (a) high-side MOSFET, (b) low-side MOSFET without pull-down circuit and (c) low-side MOSFET with pull-down circuit

When the high-side switch is turned on, which leads to the high $dv/dt$ event, the current density is quite high in the channel under the gate, as shown in Figure 6.5 (a).
Without utilizing the pull-down circuit, there are quite a lot electron current flows from source terminal though the channel under the gate to the drain terminal, as demonstrated in Figure 6.5 (b), which indicates the low-side switch gate voltage is pulled up by the high $dv/dt$ at the switching node charging the $C_{GD}$ of the low-side MOSFET, although at that moment the driver is still sending a voltage signal to hold the gate low in simulation. However, as shown in Figure 6.5 (c), the low-side switch with pull-down circuit protection has much less current density in channel than the LS switch without protection. The self-driven pull-down MOSFET speed up the switching of the low-side primary FET during turn-off, and significantly reduces or eliminates the unintentional voltage bouncing at its gate terminal. Therefore, the Miller effect, which causes the $C \cdot dv/dt$ induced turn-on problem at the gate of the primary FET, is utilized to drive the pull-down MOSFET to remove the gate voltage bouncing and becomes the solution to the problem.

The implementation of such integrated power module in a synchronous buck converter topology could achieve several advantages. The low-side MOSFET can be designed with a low threshold voltage, which lowers the on resistance of the switch for a given gate driving voltage. In turn, the lower threshold voltage reduces the $Q_{RR}$ accumulation of the integral body diode and consequently decreases the related switching losses. Having this integrated pull-down MOSFET leads to a hard turn-off of the low-side switch that keeps the gate node of primary FET firmly at the source potential during the high-side FET turn-on event. Therefore, the switching power loss is reduced as well as the $C \cdot dv/dt$ induced turn-on issue is drastically reduced or
completely eliminated. At the same time, this also increases the reliability of the circuit. The improved specific on-resistance of the low-side switch leads to a smaller conduction loss and a higher efficiency for the converter.

These advantages are illustrated by the TCAD simulations which are shown in Figure 6.6. In this simulation, it is assumed that the power stage module uses thick aluminum wires for the current handling connections so that only a small package inductance of 0.1 to 0.3 nH exists. The threshold voltage of high-side MOSFET is fixed to 1.4V in all the simulations and the low-side switch threshold voltage varies. The input voltage and output voltage were chosen to be 12 volts and 1.3 volts respectively, and the switching frequency is set to 500 kHz.

Figure 6.6 (a) demonstrates the switch node voltage and low-side MOSFET gate to source voltage waveforms of a synchronous buck converter which employs a low-side switch with a high threshold voltage of 1.25V. A 0.8V gate voltage bouncing is observed in the low-side $V_{GS}$ waveform at the moment of high $dv/dt$ event happened at the switch node. Because the gate bouncing is smaller than the low-side switch threshold voltage, there is no shoot-through occurring and the ringing of the switch node is very high.

In Figure 6.6 (b), the synchronous buck converter employs a low-side switch with a low threshold voltage of 0.65V, in which case, the 0.8V gate voltage bouncing is fatal for causing shoot-through. The bended and significantly dampened switch node voltage ringing also indicates shoot-through already occurred in the circuit. Although this dampening of the voltage ringing may look better than Figure 6.6 (a), it’s correlated with a remarkable high power loss during the $C\cdot dv/dt$ induced turn-on, so that the efficiency
of the converter is quite low. This shoot-through reduces the reliability of the buck converter as well.

Figure 6.6 Waveforms of switching node voltage and low-side switch $V_{GS}$
Figure 6.6 (c) shows the simulation results for the case in which the low-side switch has a low threshold voltage of 0.65 V but has the integrated pull-down circuit protection. The low-side MOSFET gate voltage bounce induced by charged $C_{GD}$ is virtually eliminated by the integrated pull-down circuitry. At the same time, comparing to Figure 6.6 (b), at the onset of the turn-on of the high-side switch the voltage ringing on switch node is not a bended waveform any more, which usually indicates strong shoot-through occurred during switching. Therefore, the voltage ringing is safely reduced by the implement of low threshold voltage switch in low-side.

![Low-side Switching Waveforms (with pull-down protection)](image_url)

**Figure 6.7 Gate to source voltage waveform of pull-down FET**

The gate-to-source voltage waveform of the pull-down FET is shown in Figure 6.7. It can be noticed that as soon as the high $dv/dt$ is occurred at the switch node, the gate of pull-down MOSFET is charged by the coupling capacitor and turned on to provide a
low resistive connection between primary FET gate and ground, speeding up the dropping of the gate voltage of primary Sync FET.

6.3 Design Considerations of the Monolithic Integrated Gate Pull-Down Circuitry

For better coupling the pull-down FET gate and holding the pull-down FET at the source potential to eliminate the shoot-through, the coupling capacitor and the pull-down FET have been monolithically integrated with the power MOSFET on the same die. The pull-down FET is an N-channel Power MOSFET which has the same source-down structure as the primary FET described in CHAPTER 4. The placing of the pull-down FET and the primary low-side FET on the same substrate in the common source technology assures a virtually zero parasitic inductance between their source terminals. The coupling capacitance is integrated as insulator and metal layers running on top of the drain region of the main FET.

The size of the pull-down FET determines the resistance of the connection between synchronous FET gate terminal and ground. Larger area of the pull-down FET could provide stronger pull-down effect on higher voltage of low-side primary FET gate. The waveforms of low-side primary FET gate voltage bouncing affected by different area of pull-down FET have been shown in Figure 6.8. When the switch node voltage begins to increase sharply, with the help of the smallest area pull-down FET, the gate voltage bouncing can only be reduced to 0.7V, which may still be a potential risk in high-temperature application where threshold voltage normally decreases. Using a larger area pull-down FET could offer lower resistivity path for the gate of primary FET to
ground and speed up the remaining part of the commutation. Increasing the area by 8 times, the primary FET gate voltage bouncing can be significantly reduced to around 0.4 volts, which is not danger to shoot-through faults anymore. However, unnecessary large pull-down FET will consume the area of the low-side main FET, which in turn will increase the low-side switch specific on-resistance and increase the conduction power loss. As illustrated by Figure 6.8, comparing the pull-down FET with 8 times normalized area, doubling the area to 16 times normalized area cannot further lower the primary FET gate voltage bouncing, but occupies much more active area of the low-side die and lowers the converter overall efficiency.

The coupling capacitor also needs to be carefully selected to provide prompt and strong enough charge of the pull-down FET gate and avoid gate oxide breakdown. The simulation waveforms of pull-down FET gate to source voltage with different value of coupling capacitor are shown in Figure 6.9. The proper coupling capacitor should have a value in the range of 1.5 to 2 times of the $C_{GS}$ of the pull-down MOSFET. In Figure 6.9, it is noted that if the coupling capacitor value is too small, it doesn’t have strong enough pull-down capability, whereas if the coupling capacitor is too large, the pull-down FET gate voltage will be charged by the capacitor to a dangerous level which may lead to gate oxide breakdown.
Figure 6.8 The low-side primary FET gate voltage bouncing is influenced by the pull-down MOSFET area
In order to achieve better pull-down performance, the pull-down FET is distributed across the active area of the primary MOSFET. The distributed layout of the pull-down circuitry is very important in keeping the internal gate resistor between the pull-down FET drain and the gate of the primary FET (as shown in Figure 6.4) as low as possible. In the practical implementation, center gate bus which breaks the gate fingers in the middle is used to lower the parasitic gate resistance. The segments of the pull-down FET are attached to individual segments of the primary FET. This layout assures minimum impact of the internal gate resistance on the switching speed of the combined

Figure 6.9 Pull-down FET gate to source voltage comparison under different coupling capacitor charging
transistors. The simulated switching speed slowing down impact is shown in Figure 6.10. When the gate of the pull-down FET is charged by the coupling capacitor, the pull-down FET is turned on and its drain terminal has a low voltage potential as source terminal. The undesired parasitic internal gate resistance will slow down this low voltage potential to apply on the primary FET gate. Larger resistance will make the gate voltage bouncing waveform close to the waveform without employing a pull-down circuitry.
Figure 6.10 The parasitic resistor from pull-down FET drain to low-side primary FET gate has an influence on low-side primary FET gate-source voltage bounce.
6.4 Integrated Asymmetric Gate Resistance Circuitry on Control MOSFET

Excessive voltage ringing at the switch node is inherent to the use of fast switching FETs in a push-pull configuration. Implementation of low $V_{TH}$ synchronous MOSFETs reduces the impact of $Q_{RR}$ on the first peak of the switch node voltage ringing, but the peak value is still not acceptable sometimes as shown in Figure 5.4. Traditional approach to reduce the voltage spike by adding an external gate resistor slows down both turn-on and turn-off events which leads to excessive loss in efficiency. Slowing turn-on only by adding a boot resistor requires relatively high resistor values which can inhibit proper function of the HS gate driver. In this chapter, an integrated asymmetric gate impedance circuit is introduced to address this high voltage spike problem which is attached to the gate bus of the HS-FET to selectively slow down the turn-on while preserving a fast turn-off $dV/dt$ in order to achieve low voltage ringing with minimum loss in converter efficiency [54].

Figure 6.11 shows the schematic of integrated asymmetric gate impedance circuit [41] [55]. The depletion mode lateral MOSFET integrated in parallel with the shunt resistor fulfills the function of a diode speeding up the discharging of the gate. During the turn-on process, the shunt resistor slows down the charging of the HS-FET gate, while during turn-off the gate resistor value is reduced by the conducting diode. Thus, fast turn-off speed is preserved. The simulated results on the asymmetric gate impedance circuit impact, as shown in Figure 6.12, illustrate that an effective voltage ringing reduction comes along with small efficiency degradation comparing to the conventional single external gate resistor approach.
Figure 6.11 Schematic of integrated asymmetric gate impedance circuit

Figure 6.12 Comparison of efficiency and switch node voltage peak values for single gate resistance and asymmetric gate impedance circuit
6.5 Dead-time Optimization by Low-side Gate Resistance

As described in CHAPTER 2, the power loss due to the dead-time (dead-time loss) is not trivial in the buck converter. In the duration of the dead-time, the freewheeling current conducts through the body diode of the low-side transistor. A large diode conduction loss is generated due to the significant forward voltage drop of the body diode (typically is 0.7V), which is much larger than the voltage drop of the MOSFET (typically is 0.04V). Another loss associated with the conduction of the body diode is the reverse recovery loss. Therefore, reducing the dead-time can substantially decrease the power loss especially at high switching frequency. At the same time, an optimum matching of the gate driver signals to the implemented MOSFET chip set needs to be achieved if possible when the dead-time is reduced.

Usually the dead-time is fixed and determined by the gate driver / controller circuit. The principle of operation of a synchronous buck converter has been explained in CHAPTER 2.1.1. The delay introduced by the gate driver between the turn-off of the low-side switch and turn-on of the high-side switch has to be long enough to avoid shoot-through happened. However, with the inherent fast switching performance of the new NexFET and the aforementioned low-side integrated gate voltage pull-down circuit protection, the shoot-through can be avoided to the greatest extent.

Adding low-side gate impedance is one of the effective approaches to shrink the dead-time. Usually the gate resistor in low-side switch performs two functions: limiting the peak current and damping the switching speed. A proper gate resistor employed in series with the gate terminal of the low-side switch can slow down the turn-off process
of the transistor, which will reduce the transistor body diode conduction time. As shown in Figure 6.13, after adding a suitable external gate resistance in series with low-side switch gate, the body diode reverse recovery accumulation can be effectively reduced. However, excessive large gate resistance will easily results in too short dead-time, which in turn induces the shoot-through and leads to a negative impact on the converter efficiency.

Figure 6.13 Dead-time and body diode conduction loss reduction by adjusting low-side external gate resistance
CHAPTER 7  PERFORMANCE IMPROVEMENT FOR SYNCHRONOUS BUCK CONVERTERS

7.1 Characterization of the NexFET Power MOSFET with Integrated Gate Pull-Down Circuit

The low-side source-down structure transistors and its integrated gate pull-down circuit are fabricated on 8 inches silicon wafers by 0.35µm process, as shown in Figure 7.1. With all the new integrated components, the reliability of the device needs to be carefully optimized.

Figure 7.1 The NexFET power MOSFET is fabricated on 8 inches silicon wafers
Figure 7.2 Avalanche stress curves of the NexFETs after different periods of time

Figure 7.3 \( I_{DS}-V_{DS} \) Curves of the integrated capacitor
Avalanche breakdown is one major concern of the device reliability issue because more components have the potential breakdown risk. Figure 7.2 shows the avalanche stress curves of the integrated power blocks after 4 hours, 8 hours and 12 hours. The avalanche breakdown characteristic is sharp and stable, remains consistently above 30V after long time voltage stress with practically no measurable walk-out for forced avalanche currents in the range of 1 nA to 1 µA. The coupling capacitance is integrated as insulator and metal layers running on top of the drain region of the main FET. Figure 7.3 shows the $I_{DS}$-$V_{DS}$ curves of the integrated capacitor PCM structure in 2 different 25V device wafers. The insulator layer of the capacitor is thick enough to withstand large voltage stress. Same to the main MOSFET, the avalanche breakdown in the capacitor happens in the vertical p-Epi / n-LDD junction. As a result the capacitors have a similar 25V breakdown voltage to the main transistor, which is safe enough for the DC-DC applications.

Gate leakage current is another concern of the reliability. Figure 7.4 shows the gate leakage current of the primary transistor can be kept at a low level till the gate has a positive 12 volts bias. However, when a negative voltage is applied on the gate of the primary FET, the body diode of the integrated pull-down MOSFET is forward bias, which provides a low resistivity path from the ground to the gate. Therefore, after integrated the gate pull-down circuit, while still have good characteristics on positive gate bias, the primary transistor cannot withstand any negative gate bias on gate terminal.
Figure 7.4 Gate leakage current of the NexFETs in different position of the wafer
7.2 Evaluation of the NexFET with Integrated Gate Pull-down Circuit in the Synchronous Buck Converter

As shown in Figure 7.5, high-side and low-side switches are packaged together by the stack-die technology in a SON 5mm×6mm package. In order to illustrate the effective working mechanism of the integrated gate pull-down circuit, the waveforms of the switch node voltage ringing and low-side switch $V_{GS}$ of the power module with and without the gate pull-down circuit are measured and showed in Figure 7.6. The first waveform figure comes from the power module without the pull-down integration. In the room temperature application, without extra external gate resistance as dead-time adjustment, high gate voltage bouncing can be obviously observed in the $V_{GS}$ curve, which will easily induce the turn-on of the low side switch due to the employment of the low threshold transistor. The severe dampened switch node voltage ringing waveform indicates the strong shoot-through happened in the converter. After integrated with the
gate voltage pull-down circuit, the $V_{GS}$ bouncing can be hardly observed in the second figure. $C$-$dv/dt$ induced turn-on can be effectively prevented by the gate pull-down circuit. Especially in the high temperature (125°C) application and with extra $R_G$ to minimize dead-time, when the $V_{TH}$ will be further reduced along with the increasing temperature and $C$-$dv/dt$ induced turn-on becomes more severe with the reduced dead-time, the gate voltage pull-down circuits still can provide effective protection against the shoot-through.

Figure 7.6 Measured waveforms of switch node voltage and $V_{GS}$ in synchronous buck converters with and without gate pull-down circuit protection
Figure 7.7 Comparison of measured switch node voltage ringing in 12 V input application

![Switch Node Voltage Comparison](image)

Figure 7.8 Power loss and efficiency comparison in 12V to 1.3V, 500kHz application

![Power Loss and Efficiency Comparison](image)
Figure 7.7 shows that the switch node ringing is lowered from 26.0 V to 23.4 V by employing a low threshold voltage in low-side and the integrated pull-down circuit in the 12 V input and 1.3 V output applications. The low threshold voltage sync FET helps to reduce the conduction power loss and reverse recovery power loss, meanwhile the integrated pull-down circuit prevents extra power loss comes from shoot-through. The efficiency could have 0.5% improvement in this 500 kHz application, as shown in Figure 7.8.

In high input applications, like 19V input application in laptop power supply system, because the gate voltage bouncing will increase proportional to the input voltage and makes the shoot-through effect easier to happen, the integrated pull-down circuit has deeper impact on the efficiency improvement in higher frequency domain. Figure 7.9 (a) shows the measured waveforms of switch node voltage ringing and $V_{GS}$ in a synchronous buck converter without gate pull-down circuit integration and employing normal threshold voltage transistor in low-side. The voltage ringing exceeds the breakdown voltage and is clamped at 32 V by the vertical junction. After employing a low threshold voltage power MOSFET in low-side, the switch node voltage ringing is dampened to 26V by the shoot-through effect, which induces a lot of extra power loss, as shown in Figure 7.9 (b). Although the low threshold voltage sync FET could provide lower conduction loss and reverse recovery loss, the converter suffer the power loss degradation brought by shoot-through. The total power loss and efficiency is similar to the converter only employs normal $V_{TH}$ MOSFET as indicated in Figure 7.10.
Figure 7.9 Measured waveforms of switch node voltage and $V_{GS}$ in synchronous buck converters with and without gate pull-down circuit integration in 19V input application
Figure 7.10  Power loss and efficiency comparison in 19V to 1.3V, 500 kHz application

As shown in Figure 7.9 (c), after integrated with the gate pull-down circuit, the DC-DC converter is capable to present both less gate bouncing voltage in \( V_{GS} \) waveform and less voltage ringing in switch node waveform. There is no extra power loss degradation brought by shoot-through effect and efficiency improvement is observed in Figure 7.10.
Figure 7.11 Measured waveforms of switch node voltage and $V_{GS}$ in synchronous buck converters with and without gate pull-down circuit integration in 19V input, 125˚C application

$C\cdot dv/dt$ induced turn-on will also be exacerbated in high temperature application as the threshold voltage of the sync FET will be lowered. Figure 7.11 shows the waveforms in a high temperature application, in which the shoot-through is much severer than other cases. The power loss has a huge degradation due to the painful shoot-through in light load. As shown in Figure 7.12, the integrated gate voltage pull-down circuit can improve the light load efficiency by as much as 3% and 2% in the full load in high temperature, high input voltage and megahertz frequency applications.
Conventional way to damp the ringing is to attach a snubber circuit between the drain and source terminals. A snubber circuit can be created by a capacitor and a resistor put in series, which can be integrated in the same die with the switch [56]. This conventional approach always acts as a trade-off between voltage ringing and efficiency. Two similar optimized switch node voltage ringing waveforms are shown in Figure 7.13. The upper one employs normal \( V_{TH} \) MOSFET as the low-side switch while adding a snubber circuit into the system; the bottom one uses low \( V_{TH} \) MOSFET as the low-side switch and utilizes the gate pull-down circuit as protection, which also allows adding extra gate resistor as dead-time optimization.
Figure 7.13 Switch node voltage ringing comparison between two different approaches

(a) Using normal $V_{TH}$ switch in low-side with snubber ($V_{TH} = 1.1V$), $V_{sw} = 25.1V$

(b) Using low $V_{TH}$ switch in low-side with pull-down protection and 1$\Omega$ low side extra $R_g$ ($V_{TH} = 0.75V$), $V_{sw} = 24.3V$
The two approaches could achieve similar effects on the switch node ringing optimization, but the approach utilizing low $V_{TH}$ MOSFET and integrated pull-down circuit could improve the efficiency by 1% at the same time as shown in Figure 7.14.

![Efficiency and Power Loss Comparison](image)

**Figure 7.14** Power loss and efficiency comparison between two different voltage ringing optimization approaches in 12V to 1.3V, 1 MHz and 25°C application

### 7.3 Performance Improvement of the New Power Block

At last, in order to remove the excessive voltage ringing on switch node, the asymmetric gate impedance circuit is integrated into the same power module, as shown in Figure 7.15.
Figure 7.15 Schematic of the power module with integrated asymmetric gate impedance in high-side and integrated gate voltage pull-down circuit in low-side.

Figure 7.16 Switching node voltage ringing and $V_{GS}$ waveform comparison.
Figure 7.17 Switch node voltage ringing optimization comparison in 12V and 19V input applications

The new power module with integrated components in both high-side and low-side delivers fantastic switch node voltage ringing reduction effect and $C \cdot \frac{dv}{dt}$ induced turn-on immunity, as illustrated in Figure 7.16.

As shown in Figure 7.17 and Figure 7.18, even though the voltage ringing reduction by the asymmetric gate impedance will bring a little bit extra power loss, the employment of low threshold voltage MOSFET will compensate the efficiency loss, and as a result, same efficiency is achieved in both 12V and 19V applications while voltage ringing can be significantly reduced at the same time.
Figure 7.18  Power losses don’t suffer any degradation while the voltage ringing is reduced
CHAPTER 8  CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

The future generations of microprocessors are expected to operate at much lower voltages and to draw much higher currents with high \( di/dt \) dynamic characteristics. Accordingly, higher switching frequency is required to reduce the significant size and cost of the bulky and expensive output capacitors. The main bottleneck is the current voltage regulators suffer significant switching losses as operation frequency increases, which in turn impose great challenges to minimize power MOSFET related switching losses. In parallel, the parasitic inductance and resistance introduced by the device package become more important in high frequency applications. In this dissertation an alternative solution, the integrated NexFET power module is introduced to enable next generation converters to work in megahertz frequency range.

Firstly, in order to develop advanced stack-die packaging, new generation NexFET device with the source terminal at the back-side of the die has been designed and developed. With the inherent lateral short gate structure, source-down configuration NexFET presents strongly reduced switching power loss which makes it suitable for high-frequency applications. At the same time, the source-down structure power MOSFET also enables the innovative stack-die packing technology which virtually eliminates the parasitic components of the power module package and provides minimum footprint and excellent thermal performance. While remain the similar on-resistance of the state of the art Trench technology, NexFET combined with innovative
integrated stacked-die package technology reduce the switching losses and deliver a significant efficiency improvement for SPMS systems.

Unfortunately, faster switching FETs usually lead to a higher voltage ringing on the switch node of the buck converter, inducing EMI related problems and/or undesired power stress to the power switches. In this dissertation, low threshold voltage power MOSFET is implemented as the synchronous MOSFET in the buck converter to reduce the switching node voltage ringing. At the same time, the low $V_{TH}$ SyncFET solution also effectively reduces the on-resistance and body diode reverse recovery power loss, leading to an increased efficiency.

As the channel of SyncFET is easier to be inverted, the threshold voltage reduction is limited by the $C \cdot \frac{dv}{dt}$ induced turn-on effect which can reduce converter efficiency at light load and will negatively impact power MOSFET reliability. An integrated gate voltage pull-down circuit has been integrated with the low-side switch to prevent shoot-through during the high $\frac{dv}{dt}$ events. In this dissertation, the circuit mechanism and design considerations of the gate pull-down circuitry have been described in detail. This pull-down circuit, integrated in the same die of the low-side switch, effectively eliminates the shoot-through issue even with dead-time minimization and implementation of low threshold voltage low-side switch in high temperature applications.

All the aforementioned improved technologies are integrated together as a power module, delivering an excellent solution for future high frequency, high current density DC-DC converters. The integrated NexFET power module changes the game not only by
its extraordinary silicon performance, but also by stacked-die packaging technology, low switch node ringing and shoot-through prevention technique. Experimental data are shown to demonstrate its superior high-frequency and high-current capability.

8.2 Future Research Direction

In this dissertation, a high performance low voltage power MOSFET is designed for high-frequency synchronous buck applications. Since the evolution in integrated circuit technology never stops, it always requires the use of high performance power conversion to achieve low cost, low profile, fast transient response and high power density. Optimization of the MOSFETs will continuously play an important role in improving low-voltage DC-DC converter performance. The technology in this dissertation can be continued developing in the following directions.

a) Optimizing lower voltage MOSFETs to substitute higher voltage MOSFETs

Recently the focus of the power MOSFET optimization changes from on-resistance to $Q_G$ and $Q_{GD}$, and now it turns to the $Q_{OSS}$ and voltage ringing on switch node of synchronous buck converter. Because of the high voltage ringing, in the non-isolated DC/DC application, the MOSFET voltage rating normally has to be doubled to the input voltage. For instance, usually 25V MOSFET is selected for 12V input synchronous buck applications. Higher breakdown voltage always has larger $R_{DS\,(ON)}$ resulting in higher conduction power loss. However, following the utilization of the novel technique described in this dissertation, the excessive voltage ringing can be reduced. As a result, this gives a possibility using lower voltage rating switches. For
example, 20V MOSFET instead of 25V MOSFET can be used in 12V input application. Therefore this change in turn raises a new demand for the optimization of lower voltage MOSFET.

b) Applying the super junction technique in the MOSFET

Super-junction is a creative and important concept in power device field since the introduction of the IGBT in 1980s. The drift region of super-junction device is formed of multiple, alternate n and p semiconductor stripes, which is possible to be fully depleted. As a result, the conventional two dimensional electric field in a switch is transformed into a three dimensional field, which can provide the capability to continuously shrink the device cell-pitch and reduce the $R_{DS(ON)}$. Applying this novel technique into the NexFET will further improve the device performance, though it may increase the complexity of fabrication.

c) Developing the integration solution

A major challenge to the further miniaturization of DC-DC converters is the inability to integrate passive components on silicon due to their relatively large size at today’s operating frequencies of 0.5 to 3 MHz. Increasing the switching frequencies into the 3 to 20 MHz region offers the potential for the reduction of passive component values. From the standpoint of device miniaturization, which is a desired objective of many portable electronic devices, it is advantageous to integrate the power supply/management components into a single integrated circuit (IC) chip. As a result, novel techniques, which can facilitate the integration of drivers and power switches on the same silicon substrate as corresponding control circuitry for implementing a power
control device, is preferred in power supply-on-chip (PwrSoC) solutions. To accomplish this, the BiCMOS IC fabrication technology implemented on silicon-on-insulator (SOI) substrates with dielectric lateral isolation is worth to be further exploited.
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