Soft Switching Multi-resonant Forward Converter Dc To Dc Application For Communications Equipment

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SOFT SWITCHING MULTI-RESONANT FORWARD CONVERTER
DC TO DC APPLICATION
FOR COMMUNICATIONS EQUIPMENT

by

DAVID BILLS
B.S.E.E University of Tulsa, 1993

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the School of Electrical Engineering and Computer Science
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ABSTRACT

In the field of power electronics there is always a push to create smaller and more efficient power conversion systems. This push is driven by the industry that uses the power systems, and can be realized by new semiconductor devices or new techniques. This document describes a novel technique for a small, and highly efficient method of converting relatively high DC voltage to a very low voltage for use in the telecommunications industry. A modification to the standard Forward Resonant converter results in improvements in component stress, system efficiency, response time, and control circuitry.

The concept of “soft-switching” is used to increase the efficiency of the topology, while the utilization of newly developed devices allows for significantly increased system efficiency. The topology described benefits from a significant reduction in parts from standard full-bridge DC to DC converters. The added benefit of a simplified control circuit is granted by this topology, along with a reduction in peak device stresses normally found in typical forward resonant circuits.

This document describes background information needed to understand the concepts in DC to DC power systems, “soft-switching” topologies, and control methods for these systems. The document introduces several topologies that are currently being used, and several types that have been previously analyzed, as a starting point for the detailed analysis of the proposed converter topology. A detailed analytical analysis is
given of the proposed topology, including secondary effects, and component stresses. This analysis is compared to the results found from both Pspice simulation, and a working DC to DC converter. Finally, the topology is examined for potential improvements, and possible refinements to the model described.
I would like to dedicate this work to my wife, Angela, without whom, my entire graduate program work would not have been possible. She is the reason that I have felt that the challenge of the work is worth the effort.
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LIST OF ABBREVIATIONS

CMOS – Complementary Metal Oxide Semiconductor

CPLD – Complex Programmable Logic Device

CPU – Central Processing Unit

DC – Direct Current

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

ZCS – Zero Current Switching
CHAPTER ONE: INTRODUCTION

The use of DC to DC converters has been increasing over the last few years, as higher efficiencies in power systems is being demanded. This demand for efficiency is the result of two major factors, which are larger power requirements for the devices themselves, or the reduction in package size of the total device. There are several other important factors to the DC to DC converter, such as response time, regulation precision, noise and immunity, but these factors are all controlled by the system size, and operating efficiencies. Generally the efficiency of a converter describes the desired type of topology, and the package size is defined by the total power requirements. Therefore, once a topology is determined, and the power requirements are known, then the package size can be found. Once these key factors are found, an detailed system analysis of the DC to DC converter can be resolved.

This document describes a novel type of DC to DC converter utilizing advanced “soft-switching” techniques to increase system efficiency. The reader should be familiar with basic electronic concepts, such as the function of a MOSFET device, and the use of Laplace transform math. The specifics of the topology, and the underlying concepts will be described here. For the purposes of this paper, the topology being described is a step-down converter, although in application, it possible to configure this system in any desired method, such as step-up, or step-up/down. The specific application for the DC to DC converter described here, is a power supply for a low voltage CPU (1.0 Volts), in
the telecommunications industry, which has variable input voltages of roughly 30 Volts to 80 Volts.

The typical high-efficient converter has not needed to operate at voltage ranges below 3.3Volts until very recently. This is due to the advances in the CMOS processes in the development of high-speed processors and memory systems, and their low voltage operation. With a 3.3 Volt system, the use of standard topologies with simple components, such as Schottky diodes with their 0.5 “on” Voltage, are relatively sufficient to maintain the needed performance. When the output voltage is below 1.8 Volts, special consideration is needed to maintain high efficiency levels. This can be seen by the loss of a single Schottky diode at 3.3 Volts output results in 86% efficiency, while at 1.0 Volts the result is 65% efficiency. The lower voltage range of the converter being described here requires special handing of the power systems, and care should be made in the selection of the types of devices used for the topology.

One interesting aspect of technology is that as time passes, the size of a particular device tends to be reduced, while maintaining performance. The target size for the converter described here is what is commonly referred to as the “quarter-brick”.

The package size shown here is quite small, when it is considered that the system needs to operate with an output level of 50 Amps. The package size again suggests that the selection of the components, and the type of topology is critical. It will be shown that although device selection is important, the topology has a decisive factor in the size of the package.

The primary goal of this study is to validate the operation of the primary side of the switching supply. This is done through the steps of theoretical analysis, simulations
and measurement of operating circuits. A secondary goal is to create a fully functional power supply with optimal performance characteristics. It will be shown that the primary goal of this effort was fully satisfied while the secondary goals were outside of the scope of the effort. It will also shown that given sufficient resources a resonant switching supply of the proposed new topology with optimal characteristics can be constructed.
CHAPTER TWO: LITERATURE REVIEW

Many papers were evaluated for several basic characteristics. They can be broken down into the following types of evaluations:

Similar Methodology – Used to determine potential pitfalls.

Uniqueness – Used to determine if the proposed topology is indeed unique.

Comparative – Showing the similarities that can be compared.

The following shows a few notes of the documents that were evaluated during the course of study of the new topology:

“A Full Bridge Soft Switched Telecom Power Supply With a Current Doubler Rectifier”\(^{[1]}\) is a good reference source to evaluate the performance of a current doubler secondary stage. This is the basic topology that was used by the proposed topology of this document. It is important to note that the secondary stage diodes are pointed in a direction from ground that allows for simple replacement with a MOSFET device that is ground referenced. The use of MOSFETs dramatically improves the performance of the secondary stage as significant losses are normally seen due to the diodes themselves. The MOSFETs provide reduced voltage drop over a diode, although control, speed and drain to source resistance become critical.

“Unified Theory of Extended Period Quasiresonant Converters”\(^{[2]}\) document was used as a generalized reference in regards to resonant switching topologies. This
document explored similarities in different switching circuits and showed methods of extrapolation that would cover new topologies as shown in this document.

“Some Limits of Integrated L–C–T Modules for Resonant Converters at 1 MHz”[3] explored the limitations of magnetics at high frequencies. It should be noted that limitations such as this did affect the proposed topology as some parameters were scaled back to allow complete evaluation under relatively practical loading.

“Analysis of a Multiresonant Forward Converter Based on Nonideal Coupling of the Transformer”[4] showed a similar topology that utilized non-ideal characteristics of components such as leakage inductance of a transformer can be utilized to realize circuit elements. Although this method was explored by the proposed topology it was not utilized directly.

“Characteristics of Full Resonant ZCS Converter Using a Synchronous Rectifier”[5] showed a similar topology to the one explored in this proposal. The topology described was a second order type and did have a current doubler secondary stage with a similar control scheme. The primary different with this design is the voltage on the transformer does not resonant. The actual system also shows high frequency undesired resonances similar to those found in the topology as described by this document.

Many good documents were found that detailed out the performance of the current doubler scheme. The current doubler scheme used by the proposed topology is the same as described in several of these documents. The literature that covered magnetics topics were excellent, but as the primary goal of this thesis is the analysis and validation of the primary side multi-resonant system a simplified approach was used.
CHAPTER THREE: STEADY STATE ANALYSIS

The nature of a third order switching system is simple to understand yet complex to analyze. As the goal of the proposed topology is to be simple, efficient, small and powerful compromises did need to be weighed. The basic analytical approach was through circuit conceptualization, simulation, followed by numerical and symbolic analysis finally followed by actual circuit construction.

To begin the analysis a study of the operational states of the third order system will be shown. There are four basic states of operation with several intermediate states that will be described in further detail in the appendixes. The following image represents the basic circuit and a description of the operational states will be presented. The system starts in State One.

General equations for the system can be defined by the following:

System voltages:

\[ V_{CR} = V_{LR} \quad \quad V_{in} = V_{Lin} + V_{CR} \quad \quad V_{sec} = n \cdot V_{pri} \]

System currents:

\[ I_{Lin} = I_{CR} + I_{LR} \quad \quad I_{in} = I_{CR} + I_{pri} \]

System power:

\[ P_1 = \frac{V_{in}}{dt_1} \int_0^{dt_1} I_{Lin.1(t)} \, dt + \frac{V_{in}}{dt_2} \int_0^{dt_2} I_{Lin.2(t)} \, dt + \frac{V_{in}}{dt_3} \int_0^{dt_2} I_{Lin.3(t)} \, dt + \frac{V_{in}}{dt_4} \int_0^{dt_4} I_{Lin.4(t)} \, dt \]
\[ P_1 = P_{1.1} + P_{1.2} + P_{1.3} + P_{1.4} \]

The following graph shows the theoretical waveforms for the resonant inductor current and the resonant capacitor voltage:

![Graph showing theoretical waveforms for resonant inductor current and resonant capacitor voltage.]

Figure 3-1  Proposed Topology State 1

The basic flow of the states begins with state four. During state four the system is a second order resonance system with the MOSFET turned off. State one begins the MOSFET turning on. During the sweep through states one to three the equations are all identical although there are variations in initial conditions. The voltage sweep in states one through three describe a fast dip in voltage that crosses into the negative region. The current waveform describes a simple sinusoid.

It is during state three that the current is negative through the MOSFET. This means that if the MOSFET is turned off at any time during state three the body diode of the MOSFET will continue to conduct. This conduction can be optimized by adding an external diode with more desirable characteristics. It should be noted that the closer to the transition of state four that the switch is made the better the efficiency of the system. It should also be noted that this efficiency increase is minimal in that the ration of the voltage swing is on the order of 100 volts, while the diode drop is on the order of 0.65
volts, so the percentage loss to efficiency is less than one percent to ignore improvements in timing and simply switch off the MOSFET the moment when the voltage swings positive, which is the start of state three.

State One represents a resonancy of Lin and Cr around the input voltage. The swing of the resonancy is defined by the ending voltage during State Three. The MOSFET Qp is currently inactive and the diode Dp is not in use.

![Figure 3-2 Proposed Topology State 1](image)

The system equations for state one through three are identical. Only the time in each of the states are different. The following represents the equations for states one through three:

**Fundamental frequency of state one through three:**

\[ \omega_{1.1} = \sqrt{\omega_{1.4}} = \sqrt{\frac{1}{\frac{1}{C_R L_R} + \frac{1}{L_{in} C_R}}} \]

**Resonant capacitor voltage of state one through three:**
\[ V_{CR}(t) = \frac{V_{in}}{L_{in}} + \left(\frac{V_{CR}(0)}{L_{in}} - \frac{V_{in}}{L_{R}} \right) \cos(\omega_{1.1}t) + \frac{l_{Lin}(0) - l_{LR}(0) - \frac{n I_{out}}{2}}{\sqrt{C_{R} L_{in}}} \sin(\omega_{1.1}t) \]

Input current for states one through three require simplification by way of common sets of constants. The constants are given by the “beta” variables shown here:

\[
\begin{align*}
\beta_{1.1} &= l_{Lin}(0) \\
\beta_{1.2} &= V_{in} L_{in} - V_{CR}(0) L_{in} \\
\beta_{1.4} &= V_{in} L_{R} C_{R} L_{in} \\
\beta_{1.3} &= l_{Lin}(0) + l_{LR}(0) + \frac{n I_{out}}{2} \\
\end{align*}
\]

Input current for states one through three:

\[
l_{Lin}(t) = \beta_{1.3} + \frac{\beta_{1.4}}{\omega_{1.1}^2} t + \left(\beta_{1.1} - \frac{\beta_{1.3}}{\omega_{1.1}^2} \right) \cos(\omega_{1.1}t) + \left(\frac{\beta_{1.2}}{\omega_{1.1}^2} - \frac{\beta_{1.4}}{\omega_{1.1}^3} \right) \sin(\omega_{1.1}t) \]

Resonant current through \( L_{r} \) also requires simplification by way of common sets of constants. These constants are given here:

\[
\begin{align*}
\beta_{1.30} &= l_{LR}(0) \\
\beta_{1.31} &= \frac{V_{CR}(0)}{L_{R}} \\
\beta_{1.32} &= \frac{l_{Lin}(0)}{C_{R} L_{R}} - \frac{n I_{out}}{2} \\
\beta_{1.33} &= \frac{l_{LR}(0)}{L_{in} C_{R} L_{R}} \\
\end{align*}
\]

\[
\lambda_{1.31} = \frac{\beta_{1.32}}{\omega_{1.1}^2} + \frac{\beta_{1.33}}{\omega_{1.1}^2} t + \frac{\beta_{1.32}}{\omega_{1.1}^2} - \frac{\beta_{1.33}}{\omega_{1.1}^3} \cos(\omega_{1.1}t) + \lambda_{1.33} \sin(\omega_{1.1}t) \]

The resonant current through \( L_{r} \) for states one through three is given by:

\[
l_{LR}(t) = \lambda_{1.31} + \lambda_{1.32} \cos(\omega_{1.1}t) + \lambda_{1.33} \sin(\omega_{1.1}t) \]

State Two begins when \( Q_p \) turns on. During this state the voltage of \( C_{r} \) is positive which defines which of the Dsec diodes are active. This state ends when the voltage on \( C_{R} \) crosses zero. The state is also noted by a switch in current in \( L_{r} \) that
previously was increasing and now is decreasing and is roughly sinusoid. During this stage Dsec.2 is not used and current in Lsec.1 is increasing.

Figure 3-3 Proposed Topology State 2

State Thee begins when the voltage on Cr is negative and the current in Lr is decreasing. During this stage Dsec.1 is not used and current in Lsec.2 is increasing. This state ends when the voltage at Cr returns to positive and the current in Lr begins to head towards the positive.

Figure 3-4 Proposed Topology State 3
The time spent in state one through three ends when the resonant current reaches zero. The equation set being described cannot be directly simplified and must be numerically determined after input conditions are assigned. The time in states one through three are found with the solution to $dt3$. This is shown described by the following set of equations:

\[
\begin{align*}
\lambda_{1.32} &= \beta_{1.30} - \frac{\beta_{1.32}}{\omega_{1.1}^2} \\
\lambda_{1.33} &= \frac{\beta_{1.31}}{\omega_{1.1}^2} - \frac{\beta_{1.33}}{\omega_{1.1}^3} \\
\lambda_{1.35} &= \frac{\beta_{1.32}}{\omega_{1.1}^2} \\
\lambda_{1.36} &= \frac{\beta_{1.33}}{\omega_{1.1}^2}
\end{align*}
\]

\[0 = \lambda_{1.35} + \lambda_{1.36} dt_3 + \lambda_{1.32} \cos(\omega_{1.1} dt_3) + \lambda_{1.33} \sin(\omega_{1.1} dt_3)\]

State Four is the final state in the sequence. State four is a second order resonancy and therefore contains much simpler analytical solutions. It begins when the voltage on Cr is positive. During this state the MOSFET Qp will be de-activated. Once Qp is de-activated then the diode Dp will take over allowing for a smooth zero current switch-off. This process is what defines the full resonancy soft switch characteristics of this topology. It is important to note that the timing of the MOSFET switch-off is not critical but only needs to be at any time during this state.

![Figure 3-5 Proposed Topology State 4](Image)
General equations for state four:

\[ V_{in} = V_{Lin} + V_{CR} \quad I_{Lin} = I_{CR} \]

System frequency equation for state four:

\[ \omega_{4.1} = \frac{1}{\sqrt{L_{in} C_{R}}} \]

Resonant voltage in Cr during state four:

\[ V_{CR}(t) = V_{in} + \left( V_{CR}(0) - V_{in} \right) \cos(\omega_{4.1} t) + \frac{I_{Lin}(0)}{\omega_{4.1} C_{R}} \sin(\omega_{4.1} t) \]

Resonant current in Lin during state four:

\[ I_{Lin}(t) = \frac{V_{in} - V_{CR}(0)}{\omega_{4.1} L_{in}} \sin(\omega_{4.1} t) + I_{Lin}(0) \cos(\omega_{4.1} t) \]

System input power is used to combine all the operational states and allow for calculation of system gains. The following is a general equation for the summation of the power found at each state. For numerical purposes these are simplified to a single result for each of the states in the subsequent equation:

\[ P_1 = \int_{0}^{t_1} \left( l_{Lin.1}(t) \right) dt + \int_{0}^{t_2} \left( l_{Lin.2}(t) \right) dt + \int_{0}^{t_3} \left( l_{Lin.3}(t) \right) dt + \int_{0}^{t_4} \left( l_{Lin.4}(t) \right) dt \]

\[ P_1 = P_{1.1} + P_{1.2} + P_{1.3} + P_{1.4} \]

The equation for input power for states one through three are identical with the exception of the amount of time spent in each state and the starting and ending parameters. The following represents the equation for power for each of these states:

\[ P_{1.1} = \frac{V_{in}}{\omega_{1.1}} \left( \beta_{1.3} \frac{dt_1}{\omega_{1.1}} + \beta_{1.4} \frac{dt_1^2}{\omega_{1.1}} \right) + \frac{1}{\omega_{1.1}^2} \sin(\omega_{1.1} dt_1) \left( \frac{\beta_{1.3}}{\omega_{1.1}} - \frac{\beta_{1.4}}{\omega_{1.1}^2} \right) + \cos(\omega_{1.1} dt_1) \left( \frac{\beta_{1.2}}{\omega_{1.1}} - \frac{\beta_{1.4}}{\omega_{1.1}^3} \right) \]
The input power for state four is given as:

\[ P_{1,4} = \frac{V_{in}}{T} \left( \sin\left(\omega_{4.1} t\right) \frac{L_{in}(0)}{\omega_{4.1}} - \cos\left(\omega_{4.1} t\right) \frac{V_{in} - V_{CR}(0)}{L_{in}\omega_{4.1}^2} \right) \]

Overall system power should include losses. One important point of loss is due to the voltage drop of the output diode. This loss is a function of the diode drop and the through resistance. An assumption is made here that the current is equal through each of the two secondary diodes. The loss equation for the diode is given as:

\[ P_{\text{diode}} = \left( 0.7 + \frac{R_{\text{diode}}}{2} \right) I_{\text{out}} \]

A complete system equation would need to combine all of the input power values and include them with the output power equation to get a balanced system. A numerical approach is needed for this due to the nature of the equations and a closed form solution cannot be found. The following represents a simplified version of the system gain equation based on the analytical approach given:

\[ M = \frac{V_{out}}{V_{in}} = \frac{R_{out}}{V_{in}} \sqrt{\frac{V_{\text{diode}}^2 + 2 \frac{P_{\text{input}} R_{\text{diode}}}{R_{\text{out}}} + 4 \frac{P_{\text{input}} R_{\text{out}}}{R_{\text{diode}}}}{R_{\text{diode}} + 2 R_{\text{out}}}} \]

During the analysis process a few additional components were added to protect the circuit from having overly high voltages at the lower terminal of Lr during a voltage fly-back. This problem can occur if MOSFET Qp is turned off when positive current is present on Lr and results in abnormally high voltages at the drain of Qp. These voltages can damage Qp. Additional diodes were added to the secondary side that connected back to the primary input voltage. Due to the transformer ratio these diodes are not active during any of the normal operating states. It was deemed necessary to add these
components during analysis due to the requirement of adjusting timing to find an optimal configuration.

Figure 3-6 Proposed Topology With Protection

Full analysis of the topology is given in the appendixes with Appendix A giving a Laplace Transform solution of the third order system. The results of the symbolic approach were then analyzed numerically against the simulation results in Appendix B.

Control of the switches in this circuit require timing that is not only state dependent but also level dependent. This means that the state changes are a function of voltage of the primary resonant capacitor and the system current. There should also be in place a mechanism to handle special conditions. This set of functionality can be easily handled by a typical CPLD and a few comparators. The logic of the CPLD would operate as follows:

State 1: Passive mode – Second order resonancy of Lin and Cr

This CPLD state represents the holding mode for the hysteretic control system.
Exit Criteria: Output voltage drops below threshold

State 2: Wait

During this CPLD state we switch the MOSFET on and wait until we can turn it off. If we have to wait extensively we could end up in a short-circuit mode and we need to test for this condition.

Exit Criteria: Output voltage goes negative, or excessive time

State 3: Switch-Off

Once the MOSFET is switched off we only need to wait a short amount of time then return to state 1.

Exit Criteria: Wait a fixed duration.

As can be seen by the state logic for the CPLD, the control of the proposed circuit is indeed simple to implement. This simplicity does come with a cost as it has poor stability when operating in a continuous fashion. It can be characterized as a hysteretic system using “quanta” of power due to the switching waveform. Without a complex mixed signal simulator that can combine magnetics, analog and VHDL digital components it is not possible to fully simulate the system. It is possible to simulate elements of the design, specifically the primary side waveforms.
CHAPTER FOUR: SIMULATION AND EXPERIMENTAL RESULTS

Full analysis of the topology is given in the appendixes with Appendix A giving a Laplace Transform solution of the third order system. The results of the symbolic approach were then analyzed numerically against the simulation results in Appendix B.

During the analysis of the hardware numerous changes were made to the circuit design to create a working implementation. The schematics shown in the Appendixes represents the final version of this effort. Here are a list of the types of problems encountered and overcome:

1. Fly-back voltage can destroy Qp if timing is incorrect
   1. The fix is to include secondary to primary diodes.
   2. This fix depends on the step-down voltage nature of the transformer.

2. High speed amplifier stability is lacking is a near unity gain and non-regular system.
   1. The fix is to bypass some amplifiers.

3. Low voltage comparators are noisy
   1. Low pass filters near the inputs of the comparators solved this issue.

4. Simple timers cannot be used for MOSFET switching control.
   1. This problem is due to the irregular timing of a hysteretic control scheme.
   2. This was solved by the incorporation of a CPLD.

5. Secondary MOSFETs cannot be easily controlled by their voltage levels.
1. The secondary MOSFETs are used to reduce the losses of the secondary diodes.

2. Once the MOSFET is activated, then the control scheme monitoring voltage would always measure something near zero.

3. The fix is to monitor current of the secondary MOSFETs.

6. Timing and control testing proved challenging.
   1. The use of debug states on the CPLD proved useful throughout the effort.

7. Magnetics were non-optimal.
   1. High frequency resonancies were present in the current waveform.

8. Driver circuit was too fast.
   1. High frequency resonancies were introduced by the MOSFET driver.

9. Secondary side MOSFET and diodes had large capacitance.
   1. Resonancies were introduced by the secondary capacitance.

During the system analysis several interesting characteristics were determined that allow the proposed topology to perform better or equal to other resonant designs.

Normal forward resonant circuits have very high spike voltages relative to ground. In this proposed design when moving from the “non-active” second order state into the “active” third order state the voltage swing starts from a positive value approximately one-half of peak value. It then swings negative to about the same level as the positive value. Finally when returning to the “non-active” second order state the voltage may swing to approximately double the input voltage. The fact that the swing starts positive and heads negative means that the maximum voltage seen at the capacitor
is relatively centered around ground. This helps selection of lower voltage MOSFETs and capacitors.

Switching control is relatively straightforward and involves switching on the MOSFET with then output voltage droops and switching it off when the primary resonant voltage swings from negative to positive. This means that simple comparators are all that are needed besides a CPLD to implement the design.

All the MOSFETs in the proposed design are ground referenced. Many resonant converters utilize “high-side” switching. This requires higher complexity MOSFET drivers.

Due to the simplicity of the drivers, instrumentation and logic the proposed design is very suitable for high speed switching, such as beyond one mega-hertz. Most resonant switchers offer only lower speeds due to the strict timing requirements.

One of the fundamental problems with this design is the efficiency losses when operating at a lower loading level than near maximum performs quite poorly.

The following represents a comparison of the theoretical, simulated and actual performance of the topology. The first characteristic that is being evaluated is the primary voltage waveform.

The graph in figure 4-1 represents the theoretical waveform. This graph begins when the MOSFET is switched on. It is apparent that the rate of change is faster on the earlier period of the waveform than the latter. This demonstrates the variation in the frequency due to the introduction of the higher frequency inductor. A comparison to the simulated waveform in figure 4-2 shows a close approximation. This can be used to validate the theoretical equations that are presented in Appendix A and B.
The presentation of the actual performance of the switching supply is shown in figure 4-3. It is apparent that the voltage waveform is an excellent match on the primary side.

Figure 4-1 Theoretical Voltage Waveform
Figure 4-2  Simulated Voltage Waveform

Figure 4-3  Actual Voltage Waveform
The yellow waveform in figure 4-3 is the primary voltage and the magenta waveform is the MOSFET gate voltage.

When evaluating the performance of the actual voltage waveform it became readily apparent that the hysteretic performance of the controller would be a significant limitation to the performance and efficiency of the switching system. A typical operational waveform of the actual system showing several waveforms is given in figure 4-4. This waveform shows what happens when the output voltage rises above the desired voltage for a short period of time. The resulting waveform shows a compressed set of oscillations followed by a period where the MOSFET is “off” and the primary voltage returns to its lower frequency resonancy with the input inductor only.

Figure 4-4 Hysteretic Performance of Actual Waveform
The next set of comparative results is for the current on the primary side measured at the MOSFET. During simulations and theoretical analysis it is shown there is a tight correlation. It is during the analysis of the actual waveform that it will be shown there is an introduction of a high frequency oscillation that is significantly impacting performance.

The waveform shown in figure 4-5 is the primary current waveform as determined by the theoretical analysis. It should be noted that during theoretical and analysis stages the system loading was quite high and therefore the amplitude of the current waveforms are much greater than that as measured on the actual switching supply.

Figure 4-5 Theoretical Primary Current Waveform
It is again apparent that there is tight coupling between simulation shown in figure 4-6 and theoretical shown in figure 4-5. This does not hold true with actual performance due to the MOSFET driver square wave introducing resonances as shown in figure 4-7. The green waveform in figure 4-7 represents the current through the MOSFET. The parasitics were analyzed in detail with the results shown following. One thing to keep in mind that the desired performance for the ZCS performance of the switching supply is to sweep positive then negative to generate a roughly full cycle sinusoid. It will be shown that using a numerical filter on the oscillating waveform that this sinusoid is present on the data.
Part of the analysis completed on the current waveform was to filter the data by using a block average on the captured waveform. The result of one waveform is shown in figure 4-8. In that graph the captured voltage waveform is in green while the filtered current waveform is shown in black. It should be noted that the units for voltage is one volt per division, so the peak voltage is approximately 60 volts. It should also be noted that the current waveform is in 10 milli-Amps per division, so the peak current is approximately 0.3 amps. The time division is in microseconds. This waveform was generated with a load of 1.00 ohms and an output voltage of 1.00 voltages, hence an output wattage of 1.0.
It can be seen that after filtering the current waveform does correlate with the simulated and theoretical waveforms. The negative portion of the waveform shows the most distortion as it is not a clean sinusoid. The current waveform does show Zero Current Switching characteristics as it starts with zero current and completes the waveform with a smooth transition to zero current.

It was determined that the resonances in the primary side current sensor were due to two components. The primary component was the high speed high current MOSFET driver. This device generates a square wave that is capacitively coupled into the resonant portion of the circuit via the gate to drain capacitance. The square wave would introduce a current pulse with every switch transition. The solution is to limit the rise time of the gate, which was accomplished with a 22 ohm resistor. If this resistor is too high the losses in the MOSFET are too high and the losses and temperature actually go a-stable.
A value of 220 ohms caused the circuit to enter current limiting saturation in under 15 seconds and the surface temperature of the MOSFET was around 100 Celsius.

A lower frequency resonance is present on the secondary side. This is due to the capacitance of the secondary MOSFETs and the secondary diode. This resonancy is undesirable and contributes to the system losses. It was possible to tune this resonance by increasing the capacitance and resulting in a phase shift of the output but reducing the resonant frequency. One the resonant frequency was reduced the losses in the transformer was also reduced.

One analysis technique that can be used to quantify visually the performance of a switching supply is to graph the primary switching parameters of voltage and current on the X and Y axis of a graph. Using this technique since the resonant system described by this topology is a full sinusoid, the resulting shape would be a simple circle. The rotation of the circle is clockwise starting from the 12 o'clock position. The actual shape of the graph is somewhat different. The shape shown in figure 4-9 is the simulated graph while the shape shown in figure 4-10 is the actual waveform as measured. The simulated graph has a generally circular shape while the actual graph has some loss of “roundness” when sweeping up past 6 o'clock.
Figure 4-9 Simulated Voltage/Current Polar Graph

Figure 4-10 Actual Voltage/Current Polar Graph
Once the loading of the system is increased the loss of current on the negative portion of the waveform become less important. A second set of actual measurements were performed at a higher loading level. The previous measurements shown were done with an input wattage of 5.0 Watts. The next series of loading graphs were conducted when the input was loaded at 16.0 Watts. Figure 4-11 shows the filtered time domain waveform of the higher loaded waveform. While figure 4-12 shows the polar graph of that system.

![Figure 4-11 16W Input Primary Voltage and Filtered Current Waveform](image-url)
Continuing analysis of the waveforms shows more detailed characteristics of the secondary side. It can be shown that the secondary side performance is exactly as expected under the assumption of having a performance reducing higher frequency resonancy. The following waveforms show the voltage on the secondary side as simulated (figure 4-14) and measured (figure 4-15).

To generate the simulation additional parasitics were added to the model. This revised schematic is shown in figure 4-13.
The output waveform shown in figure 4-14 includes a red graph that represents the voltage across the terminals on the secondary side. It is expected to be a 4:1 step down voltage that includes the resonant characteristics as seen by the primary side current waveforms. Please note that the scaling in the actual measurement has been changed by a factor of four in relation to the input voltage to shown the performance of the 4:1 transformer. This correlation of actual to theoretical voltage is good for the secondary side of the system.
Figure 4-14 Revised simulation waveforms to include parasitics

Figure 4-15 Secondary Voltage Output
As can be seen in figure 4-15 the secondary voltage across the transform closely matched the input waveform with exception of the voltage ratio and the included parasitic resonancy.

One interesting characteristic of the secondary side control scheme is that the current doubler switching waveform is a simple function based on MOSFET bias and primary side voltage. When the primary side MOSFET is “off” then both diodes passing some current and the secondary MOSFETs can both be turned on. When the primary MOSFET is turned “on” then the secondary MOSFET selection is a function of the primary side voltage. If the primary side voltage is positive then the low side secondary MOSFET is active, and vice versa for the high side MOSFET.

During evaluation of this performance one of the efficiency deficits was evaluated. The actual usage of the MOSFETs when driving the secondary side proved to be non-ideal due to timing dependencies. The specific timing problem is the delay in the response of the voltage on the primary side and the sensing by the CPLD of when it occurred. This could be resolved by better timing algorithms, although the CPLD did not have any available programming space left. It could also be resolved by faster response comparator circuits, although the specific component limit response rate is due to the limiting diode capacitance on the resistor-zener network. The zener parasitic capacitance is high enough to form a simple resistor-capacitor network resulting in a phase shift of the detection circuit.

Figure 4-16 shows a photo image of the evaluation board that was developed for analysis. The layout of the circuit is based on a large ground plane with magnetics and high current parts on one side and digital circuitry on the other. Included in the package
is a header that allows for monitoring of the digital system and internal states of the CPLD. On the edges of the board are BNC connectors that allow oscilloscope measurements. This board is one of two that was created as part of the on-going efforts to analyze the performance of the switching system described herein.
Figure 4-16 Evaluation Circuit Board

Figure 4-17 Evaluation Circuit Board Regions
Evaluation of the thermal performance of the circuit was conducted during operation while loaded during a 1 Watt output condition. The image shown in figure 4-18 image is based on Celsius temperature and shows the input transformer and capacitor to be nominally of the same temperature, while the primary MOSFET and the primary transformer show the highest temperature levels. The thermal image shows that the higher resonancies are limiting performance as the excessive losses due to heat are being generated.

Figure 4-18 Thermal Image of Evaluation Board 1 Watt Output
Final evaluation of performance is measured in efficiency. Actual efficiency of the evaluation board was significantly less than desired. This is due to high frequency resonancy and non-ideal control. Although one of the fundamental premises of this design is simple control, that does not alleviate the need for a more regular timing mechanism. The graph as shown in figure 4-18 shows multiple cycles of the hysteretic control scheme. As can be seen by this graph the regulation of the system is sporadic and resonating as a lower frequency. If the delays between cycles are long enough then the desirable higher voltages in the primary side droop down to that of the input voltage which results in a slow regeneration of primary voltage/current resonancy. This can be seen by the yellow waveform that resonates nicely than when the secondary output voltage is high enough the primary voltage droops down. Although control issues make the system erratic, they do not significantly impact efficiency.
Final efficiency numbers are poor due to magnetics and unwanted parasitics.

Two output power levels were evaluated, 1.0 Watt, 2.6 Watt and 4.6 Watts. The 1.0 Watt system resulted in approximately 28% efficiency, the 2.6 Watt system resulted in 45% efficiency, and the 4.6 Watt system operated at 48% efficiency. The majority of this efficiency is being lost due to the high frequency resonancy. The ferrites used for the primary side took the brunt of the thermal loading are reached temperatures of 57C, while the primary MOSFET was a slightly cooler 50C. The primary capacitor and inductor were much cooler at 40C, and the rest of the circuit was close to room temperature at

Figure 4-19 Hysteretic Control Graph
28C. It is important to note that the ferrite is not thermally attached to any components and has to self radiate for cooling.

Further thermal and efficiency testing was completed using a tuned secondary system. The results show improvement and lead to the statement that further tuning of the resonancies would result in solid system performance. Operating with 4.3 Watts output the system ran at 47% efficiency. The resonancy was found to be a result of the capacitance of the secondary side diode and the secondary side MOSFETs when they were inactive. This tuning caused the secondary side to have a phase shift as shown in figure 4-20 by the yellow trace. In figure 4-20 the red trace is showing reduced resonancy on the primary current waveform, but no change in performance. By adding this capacitor on the secondary side it effectively increases an unwanted resonancy by increasing the magnitude by reducing the frequency. It is the high frequency component that is causing the heat in the inductors. A more proper solution would be to isolate and reduce the secondary resonancy by careful selection of the diode and MOSFETs to reduce their capacitance. Alternatively a more exhaustive analysis of the resonancy would result in a higher performance secondary stage. As the secondary stage itself is not a primary goal of this thesis it was not explored to the extent that would be needed for a commercial product.

The graph shown in figure 4-21 shows the simulation results that include the parasitics and the improved secondary side capacitance.
During the process of creating the working design the following characteristics were deeming important to the selected components.
● CPLD – Large enough to support the timing application for hysteretic control.
● Comparators – Very high speed devices with relatively low current consumption.
● Low capacitance, low forward resistance diodes for the high current regions.
● Low capacitance, low resistance MOSFETs.
● Primary side with all components rated to 150 volts at 4.8 amps minimum.
● Secondary side with all components rated to 60 volts at 40 amps minimum.
● Independent standard communications switcher is included for the low current requirements of the controller portion of the system.
● Switchers and linear regulators to generate 10 volts, 3.3 volts, 1.8 volts, -5.0 volts and -3.3 volts from a 15 to 72 volt primary source.
● Header for interfacing with a logic analyzer.
● BNC connectors to allow easy monitoring of voltages and currents within the system.
● Primary CPLD clock at 50 MHz for low latency of digital logic.
CHAPTER FIVE: FUTURE IMPROVEMENTS

The third order forward resonant converter shown here includes several advantages with the following items being key:

1. Simple primary switching method
2. Full wave rectification secondary with two diodes
3. Standard non-center tapped transformer
4. Full wave resonancy design
5. Zero current switching
6. Natural stability of output voltage over variations in input voltage

Of all the tasks in evaluating various topologies the timing and control task is generally the most troublesome. This problem was alleviated by the use of a CPLD for dynamic control. Future improvements to this design is to utilize larger FPGAs and for more production oriented solutions utilize an ASIC.

Future improvements for the proposed third order resonant switcher is include better timing control by way of more precise measurement circuitry. Monitoring of voltages and currents in the various active components can not only be used to improve efficiency, but also EMI, output ripple and response rate to load fluctuations.
There are several undesirable high frequency resonances in the prototype circuit. These resonances were found to be part of the primary MOSFET driver circuit, the magnetics and the board layout. Future improvements would deal in specific methods of approach in dealing with the undesirable effects. Specifically this would reduce the heat being generated in the magnetics and increase the efficiency significantly. The most effective improvement to the efficiency is most likely found in a custom magnetics design the meets the criteria of the frequency and power requirements. This design requires low parasitics, high performance and low losses from the magnetics section. Tuning of the magnetics will result in significant improvements in the performance of the design.

One of the best possible future improvements for commercialization is the integration of logic, instrumentation and power devices into a single integrated chip set. This would dramatically reduce the size of the circuit. The current design is based upon a collection of generic components and assuming production volumes are high enough, then migrating to a completely custom design makes good business sense.

Through good design practices and significant research and development a unique resonant converter is has been proposed. This new topology offers high speeds, high efficiencies, simple controls and reduced sizes from most resonant topologies. The system analysis and prototype have been validated on this novel forward resonant design.
APPENDIX A: SYMBOLIC SOLUTION OF THIRD ORDER SYSTEM
The FR3 converter is a multi-resonant forward converter utilizing ZCS and ZVS switching modes, and configurations that allow for high speed operation, high efficiency, and low component stresses. It is capable of operating efficiently in a light loading condition, and has very simple primary circuit drivers. The secondary side can be operated either with simple diodes, or a secondary synchronized control system.

The simplified model assumes that there are no non-ideal components, which includes the transformer. This means that there will be no leakage inductance component. The FR3 converter utilizes magnetizing inductance for is primary resonance states, and only during transitions would the leakage inductance play a role. Therefore assuming that leakage is of negligible effect can be a valid assumption. Future work will show the effects of the leakage inductance upon the FR3 model.

There are seven primary operating states of the converter. The first six states are used to define a full-wave "on" state of the system, and the seventh state defines the "off" state. The fundamental configurations for the "on" states are based upon the current doubler scheme, in regards to whether the switching diodes are passing current, or not. In no condition are both diodes off, and due to the assumption of no leakage current, the only case where both diodes are on, is the seventh state.

The equations for the system will be models in separate sections and finally combined. The use of conservation of power will be used to connect all of the various equations. The average input power equals the average output power, which also equals the average power on the primary side of the transformer, and the average power on the secondary side of the transformer.
It will be assumed that the inductors on the secondary side will be of like value, and that the system will be a balanced load, such that when the transformer current is zero, the secondary diode currents will tend to be equal.

States One through Six: Primary Resonance Modes

These states define the modes of operation when the switching device is turning on. Mathematically the states are identical, with only differences in their initial conditions and direction of transformer secondary current. States one and two both end with the Vcr voltage crossing zero, and state three ends with the primary transformer current reaching zero. The critical condition for resonance is that the transformer primary current must be less than zero during the third state, otherwise the system cannot be reset, and acts like a DC hysteretic control system, with little power being transferred to the secondary.

The input inductor is defined as:

\[ L_{in} \]

\[ I_{Lin} = I_{in} \]

\[ V_{Lin} \]

The resonant capacitor is defined as:

\[ C_{R} \]

\[ I_{CR} \]

\[ V_{CR} \]

The resonant magnetizing inductor is defined as:

\[ L_{RM} \]
The input and output voltages are fixed as:
\[ V_{in} \]
\[ V_{out} \]

The output current to the load is balanced, but it varies between the two output inductors. The output current through these inductors will be assumed to be a constant one-half of the total output current. The actual ripple current will be determined later in the analysis.

The output inductor is defined as:
\[ L_{outP} = L_{outN} \]
\[ I_{outP} + I_{outN} = I_{out} \]

The output capacitor is defined as:
\[ C_{out} \]
\[ I_{Cout} \]
\[ V_{Cout} = V_{out} \]

The output load is defined as:
\[ R_{out} \]
\[ I_{out} \]
\[ V_{out} \]

There is one extra element that needs to be considered, but will be discussed in state four, which is the junction capacitor of the switching element. This component is considered
to be lost during this stage, as its charge is simply dumped to the ground level, creating a small current spike. This effect is minimized by selecting a small value for the junction capacitor by proper MOSFET switch selection.

We will now define the initial conditions for the modes. It is assumed that none of the components will be in zero conditions. The resonant inductor will have a small residual current that is due to the secondary resonance in the secondary stage. The input inductor and resonant capacitor will be leaving, at a point defined by switching and not level, a lower frequency resonancy, and will therefore have arbitrary current and voltage levels.

These are the general equations for the primary resonant state:

\[ V_{CR} = V_{LR} \]
\[ V_{in} = V_{Lin} + V_{CR} \]
\[ I_{Lin} = I_{CR} + I_{LR} \]
\[ I_{in} = I_{CR} + I_{pri} \]

Or

\[ V_{sec} = n \cdot k \cdot V_{pri} \]

Where \( n \) is the turns ratio of primary over secondary.

\[ \text{Average } P_{in} = \text{Average } P_{out} = \text{Average } P_{pri} = \text{Average } P_{sec} \]

We now are prepared to solve the state equations for modes one through five.

State One:

This state starts when the switch is turned on, and ends when the secondary voltage equals zero. Since the transformer always is synchronized in voltage for the primary and
secondary sides, and the primary side is connected to the resonance capacitor, then we can also say that the state ends when the capacitor voltage reaches zero.

Initial conditions:

\[ V_{CR}(0) = V_{CR}(T) \]
\[ I_{Lin}(0) = I_{Lin}(T) \]
\[ I_{LR}(0) = I_{LR}(T) \]
\[ dt_1 \]

is the time in state one.

Equations:

\[ V_{CR}(t) = V_{LR}(t) \]
\[ V_{in} = V_{Lin}(t) + V_{CR}(t) \]
\[ I_{Lin}(t) = I_{CR}(t) + I_{LR}(t) \]
\[ n \cdot V_{sec}(t) = V_{pri}(t) \]

Therefore we need to find the voltage in the resonant capacitor as a solution for the time in state one.

\[ V_{CR}(s) = V_{LR}(s) \]

Equivelency

\[ \frac{V_{in}}{s} = V_{Lin}(s) + V_{CR}(s) \]

KVL Equation

\[ I_{Lin}(s) = I_{CR}(s) + I_{LR}(s) + \frac{I_{pri}}{s} \]

KCL Equation

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Some generalized Laplace equations are:

\[ V_{CR}(s) = \frac{1}{sC_R} l_{CR}(s) + \frac{V_{CR}(0)}{s} \]

\[ V_{LR}(s) = sL_R l_{LR}(s) - L_R l_{LR}(0) \]

\[ V_{Lin}(s) = sL_{in} l_{Lin}(s) - L_{in} l_{Lin}(0) \]

\[ l_{CR}(s) = sC_R V_{CR}(s) - C_R V_{CR}(0) \]

\[ l_{Lin}(s) = \frac{V_{Lin}(s)}{sL_{in}} + \frac{l_{Lin}(0)}{s} \]

\[ l_{LR}(s) = \frac{V_{LR}(s)}{sL_R} + \frac{l_{LR}(0)}{s} \]

The constant current draw from the secondary side directly affects the primary side, as can be seen by the previous KCL equation. The primary current is the turns ratio, times the current in the positive diode, due to the current doubler scheme. The diode current, after the settling period during state four, turns into either the output current divided by two, or zero, if the leakage current in the transformer is zero. This means that after state one, the secondary current can always be assumed to be shifted by the output current divided by two.

\[ I_{pri} = n l_{Sec} \]

For state one,

\[ I_{pri} = n \frac{l_{out}}{2} \]

For state three,

\[ I_{pri} = n \frac{l_{out}}{2} \]
For state five.

To solve the complete system, the value for current through the input inductor will be left for the end. This variable will be used with the average power functions to determine the stabilized system power.

Now we can solve for $V_{\text{Lin}}$ using KVL. In general, to solve KVL and KCL system, you should start with the system type that you wish to end with, and use the Laplace current to voltage conversion formulas. This results in the Laplace system type that is desired.

\[
\frac{V_{\text{in}}}{s} = V_{\text{Lin}(s)} + V_{\text{CR}(s)}
\]

\[
s \cdot L_{\text{in}} \cdot I_{\text{Lin}(s)} - L_{\text{in}} \cdot I_{\text{Lin}(0)} = \frac{V_{\text{in}}}{s} - V_{\text{CR}(s)}
\]

\[
s \cdot L_{\text{in}} \cdot I_{\text{Lin}(s)} = \frac{V_{\text{in}}}{s} - V_{\text{CR}(s)} + L_{\text{in}} \cdot I_{\text{Lin}(0)}
\]

\[
I_{\text{Lin}(s)} = \frac{V_{\text{in}}}{s^2 \cdot L_{\text{in}}} - \frac{V_{\text{CR}(s)}}{s \cdot L_{\text{in}}} + \frac{I_{\text{Lin}(0)}}{s}
\]

Using KVL for for equivalency of VCR and VLR.

\[
V_{\text{CR}(s)} = V_{\text{LR}(s)}
\]

\[
V_{\text{CR}(s)} = s \cdot L_{\text{R}} \cdot I_{\text{LR}(s)} - L_{\text{R}} \cdot I_{\text{LR}(0)}
\]

\[
s \cdot L_{\text{R}} \cdot I_{\text{LR}(s)} = V_{\text{CR}(s)} + L_{\text{R}} \cdot I_{\text{LR}(0)}
\]

\[
I_{\text{LR}(s)} = \frac{V_{\text{CR}(s)}}{s \cdot L_{\text{R}}} + \frac{I_{\text{LR}(0)}}{s}
\]

We can now use KCL of the previous two solutions, and the general form of ICR.

\[
I_{\text{Lin}(s)} = I_{\text{CR}(s)} + I_{\text{LR}(s)} + \frac{n \cdot I_{\text{out}}}{2 \cdot s}
\]
\[
\frac{V_{in}}{s^2 L_{in}} - \frac{V_{CR(s)}}{s L_{in}} + \frac{i_{Lin(0)}}{s} = s C_{R} V_{CR(s)} - C_{R} V_{CR(0)} + \frac{V_{CR(s)}}{s L_{R}} + \frac{i_{LR(0)}}{s} + \frac{n i_{out}}{2 s}
\]

Now we can solve for \( V_{CR(s)} \).

\[
\begin{align*}
- \frac{V_{CR(s)}}{L_{in}} - s C_{R} V_{CR(s)} - \frac{V_{CR(s)}}{L_{R}} &= - \frac{V_{in}}{s} - \frac{i_{Lin(0)}}{s} - C_{R} V_{CR(0)} + \frac{i_{LR(0)}}{s} + \frac{n i_{out}}{2 s} \\
\frac{V_{CR(s)}}{L_{in}} + s C_{R} V_{CR(s)} + \frac{V_{CR(s)}}{L_{R}} &= \frac{V_{in}}{s} + \frac{i_{Lin(0)}}{s} + C_{R} V_{CR(0)} - \frac{i_{LR(0)}}{s} - \frac{n i_{out}}{2 s}
\end{align*}
\]

\[
V_{CR(s)} \left( \frac{1}{s L_{in}} + s C_{R} + \frac{1}{s L_{R}} \right) = C_{R} V_{CR(0)} + \frac{i_{Lin(0)} - i_{LR(0)} - \frac{n i_{out}}{2}}{s} + \frac{V_{in}}{s^2 L_{in}}
\]

\[
V_{CR(s)} = \frac{1}{L_{in} + s^2 C_{R} + \frac{1}{L_{R}}}
\]

\[
V_{CR(s)} = \frac{s L_{in} C_{R} + 1}{s^2 L_{in} C_{R} + 1}
\]

To solve the Laplace transform, a simplification may be made by using place holders.

\[
\begin{align*}
\alpha_{1.1} &= V_{CR(0)} \\
\alpha_{1.2} &= \frac{i_{Lin(0)} - i_{LR(0)} - \frac{n i_{out}}{2}}{C_{R}} \\
\alpha_{1.3} &= \frac{V_{in}}{L_{in} C_{R}}
\end{align*}
\]
\[ a_{1.4} = \frac{1}{L_R C_R} + \frac{1}{L_{in} C_R} \]

\[ V_{CR}(s) = \frac{s \cdot a_{1.1} + a_{1.2} + \frac{1}{s} \cdot a_{1.3}}{s^2 + a_{1.4}} \]

The inverse Laplace of this equation results in the following:

\[ V_{CR}(t) = \frac{a_{1.3}}{a_{1.4}} \cdot \cos\left(\sqrt{a_{1.4}} \cdot t\right) - \frac{a_{1.3}}{a_{1.4}} \cdot \cos\left(\sqrt{a_{1.4}} \cdot t\right) + \frac{a_{1.2}}{\sqrt{a_{1.4}}} \cdot \sin\left(\sqrt{a_{1.4}} \cdot t\right) \]

Noting the common frequency modifier allows us to simplify the frequency component.

\[ a_{1.4} = \sqrt{a_{1.4}} = \sqrt{\frac{1}{C_R L_R} + \frac{1}{L_{in} C_R}} \]

We now need to simplify the equations.

\[ a_{1.3} = \frac{V_{in}}{L_{in} C_R} \]

\[ a_{1.4} = \frac{1}{L_R C_R} + \frac{1}{L_{in} C_R} \]

\[ a_{1.4} = \frac{V_{in}}{L_{in} \left(\frac{1}{L_R} + \frac{1}{L_{in}}\right)} \]

\[ a_{1.4} = \frac{V_{in}}{L_{in} + 1} \]
\[
\frac{\alpha_{1.2}}{\sqrt{\alpha_{1.4}}} = \frac{l_{\text{Lin}(0)} - l_{LR}(0)}{C_R} \cdot \frac{n_{\text{out}}}{2} \left( \frac{1}{L_R C_R} + \frac{1}{L_{\text{in}} C_R} \right)
\]

\[
\frac{\alpha_{1.2}}{\sqrt{\alpha_{1.4}}} = \frac{l_{\text{Lin}(0)} - l_{LR}(0)}{C_R} \cdot \frac{n_{\text{out}}}{2} \left( \frac{1}{L_R C_R} + \frac{1}{L_{\text{in}} C_R} \right)
\]

\[
\frac{\alpha_{1.2}}{\sqrt{\alpha_{1.4}}} = \frac{l_{\text{Lin}(0)} - l_{LR}(0)}{C_R} \cdot \frac{n_{\text{out}}}{2} \left( \frac{C_R}{L_R} + \frac{C_R}{L_{\text{in}}} \right)
\]

The final simplified equation, with only frequency as a composite variable, is as follows:

\[
V_{CR}(t) = \frac{V_{\text{in}}}{L_{\text{in}} + 1} \left( V_{CR}(0) - \frac{V_{\text{in}}}{L_{\text{in}} + 1} \right) \cos(\omega_{1.1} t) + \frac{l_{\text{Lin}(0)} - l_{LR}(0)}{2} \cdot \frac{n_{\text{out}}}{2} \left( \frac{C_R}{L_R} + \frac{C_R}{L_{\text{in}}} \right) \sin(\omega_{1.1} t)
\]

To allow the symbolic solution system to function, we need to reduce the variables further.

\[
\lambda_{1.1} = \frac{V_{\text{in}}}{L_{\text{in}} + 1}
\]

\[
\lambda_{1.2} = V_{CR}(0) - \lambda_{1.1}
\]

\[
\lambda_{1.3} = \frac{l_{\text{Lin}(0)} - l_{LR}(0)}{2} \cdot \frac{n_{\text{out}}}{2} \left( \frac{C_R}{L_R} + \frac{C_R}{L_{\text{in}}} \right)
\]
\[ V_{CR,1}(t) = \lambda_{1.1} + \lambda_{1.2} \cos(\omega_{1.1} t) + \lambda_{1.3} \sin(\omega_{1.1} t) \]

Now we need to determine the time it takes to reach state 2. This is done by setting the capacitor voltage to zero, and evaluating the time.

\[ 0 = \lambda_{1} + \lambda_{2} \cos(\omega_{1} dt) + \lambda_{3} \sin(\omega_{1} dt) \]

\[ -\lambda_{1} = \lambda_{2} \cos(\omega_{1} dt) + \lambda_{3} \sin(\omega_{1} dt) \]

Algebra Identities:

\[ \sin(x) = \sqrt{0.5 (1 - \cos(2x))} \]

\[ \cos(x) = \sqrt{0.5 (1 + \cos(2x))} \]

A form of the previous equation with a common sinusoid function.

\[ 0 = \lambda_{2} \sqrt{\frac{1}{2}\left[\frac{1}{2} \cos(2(\omega_{1} dt))\right]} + \lambda_{3} \sqrt{\frac{1}{2}\left[\frac{1}{2} \cos(2(\omega_{1} dt))\right]} + \lambda_{1} \]

This system can be evaluated symbolically and results in a time function for voltage to reach zero of the following:

\[ dt_{1} = \frac{1}{2} \left[ \frac{-1 + \lambda_{2}^{2} + \lambda_{3}^{2} + \frac{\lambda_{3} \lambda_{1}}{\lambda_{2}^{2} + \lambda_{3}^{2}}}{\cos^{-1}\left[-2 \lambda_{1} \lambda_{3} + \frac{2 \lambda_{3} \lambda_{1}}{\lambda_{2}^{2} + \lambda_{3}^{2}} \left(-\lambda_{1}^{2} - 2 \lambda_{2}^{2} + 4 \lambda_{2}^{4} + 2 \lambda_{2}^{2} \lambda_{3}^{2}\right)^{\frac{1}{2}} + 2 \lambda_{1}^{2}\right] + \frac{\lambda_{2}^{2} + \lambda_{3}^{2}}{\omega_{1}}} \right] \]

\[ dt_{1} = \frac{1}{2} \left[ \frac{2 \lambda_{1}^{2} - \lambda_{2}^{2} + \lambda_{3}^{2} + \frac{2 \lambda_{3} \lambda_{1}}{\lambda_{2}^{2} + \lambda_{3}^{2}}}{\cos^{-1}\left[-2 \lambda_{1} \lambda_{3} + \frac{2 \lambda_{3} \lambda_{1}}{\lambda_{2}^{2} + \lambda_{3}^{2}} \left(-\lambda_{1}^{2} - 2 \lambda_{2}^{2} + 4 \lambda_{2}^{4} + 2 \lambda_{2}^{2} \lambda_{3}^{2}\right)^{\frac{1}{2}} + 2 \lambda_{1}^{2}\right] + \frac{\lambda_{2}^{2} + \lambda_{3}^{2}}{\omega_{1}}} \right] \]
This equation is obviously too wieldy to utilize in any manner besides as an algorithm of a computer system.

The voltages for the other active components are as follows:

\[ V_{LR}(t) = V_{CR}(t) \]

\[ V_{Lin}(t) = V_{in} - V_{CR}(t) \]

For a complete model of state one, and of course all of the following states, all of the currents, and voltages must be known for every active component. Presently only the voltages have been derived. We will need to find the currents through the various components. Since the current through the transformer is load dependent, there is no way to exactly define that current level by only viewing state one. The full system will need to be evaluated to determine the output current. Due to the complexity of the system, there will be no way to determine an exact solution for output current, and an iterative method must be employed for a result to be found.

The initial functions that are used for the inductor current is identical to that of the previous voltage equations.

\[ V_{CR}(t) = V_{LR}(t) \]

\[ V_{in} = V_{Lin}(t) + V_{CR}(t) \]

\[ I_{Lin}(t) = I_{CR}(t) + I_{LR}(t) \]

\[ n \ V_{sec}(t) = V_{pri}(t) \]
We need to find the voltage in the resonant capacitor as a solution for the time in state one.

\[ V_{CR}(s) = V_{LR}(s) \]

Equivelency

\[ \frac{V_{in}}{s} = V_{Lin}(s) + V_{CR}(s) \]

KVL Equation

\[ l_{Lin}(s) = l_{CR}(s) + l_{LR}(s) + \frac{l_{pri}}{s} \]

KCL Equation

Some generalized laplace equations are:

\[ V_{CR}(s) = \frac{1}{s \cdot C_R} l_{CR}(s) + \frac{V_{CR}(0)}{s} \]

\[ V_{LR}(s) = s \cdot L_R l_{LR}(s) - L_R l_{LR}(0) \]

\[ V_{Lin}(s) = s \cdot L_{in} l_{Lin}(s) - L_{in} l_{Lin}(0) \]

\[ l_{CR}(s) = s \cdot C_R V_{CR}(s) - C_R V_{CR}(0) \]

\[ l_{Lin}(s) = \frac{V_{Lin}(s)}{s \cdot L_{in}} + \frac{l_{Lin}(0)}{s} \]

\[ l_{LR}(s) = \frac{V_{LR}(s)}{s \cdot L_R} + \frac{l_{LR}(0)}{s} \]

The constant current draw from the secondary side directly affects the primary side, as can be seen by the previous KCL equation. The primary current is the turns ratio, times one half of the output current, due to the current doubler scheme.
\[ l_{pri} = n \frac{l_{out}}{2} \]

Using the KVL equations, we can apply the current/voltage transforms. We will start with the resonant inductor.

\[ \frac{1}{s \cdot C_R} \cdot i_{CR}(s) + \frac{V_{CR}(0)}{s} = s \cdot L_R \cdot i_{LR}(s) - L_R \cdot i_{LR}(0) \]

\[ s \cdot L_R \cdot i_{LR}(s) = \frac{1}{s \cdot C_R} \cdot i_{CR}(s) + \frac{V_{CR}(0)}{s} + i_{LR}(0) \]

\[ i_{LR}(s) = \frac{1}{s^2 \cdot L_R \cdot C_R} \cdot i_{CR}(s) + \frac{V_{CR}(0)}{s^2 \cdot L_R} + \frac{i_{LR}(0)}{s} \]

\[ i_{LR}(s) = \frac{i_{CR}(s) + V_{CR}(0) \cdot C_R}{s^2 \cdot L_R \cdot C_R} + \frac{i_{LR}(0)}{s} \]

We will now use KVL for the capacitor and simplify.

\[ \frac{V_{in}}{s} = s \cdot L_{in} \cdot i_{Lin}(s) - L_{in} \cdot i_{Lin}(0) + \frac{1}{s \cdot C_R} \cdot i_{CR}(s) + \frac{V_{CR}(0)}{s} \]

\[ \frac{1}{s \cdot C_R} \cdot i_{CR}(s) = \frac{V_{in}}{s} - s \cdot L_{in} \cdot i_{Lin}(s) + L_{in} \cdot i_{Lin}(0) - \frac{V_{CR}(0)}{s} \]

\[ i_{CR}(s) = V_{in} \cdot C_R - s^2 \cdot C_R \cdot L_{in} \cdot i_{Lin}(s) + s \cdot C_R \cdot L_{in} \cdot i_{Lin}(0) - V_{CR}(0) \cdot C_R \]

\[ i_{CR}(s) = C_R \left( V_{in} - s^2 \cdot L_{in} \cdot i_{Lin}(s) + s \cdot L_{in} \cdot i_{Lin}(0) - V_{CR}(0) \right) \]

Now we can use the previous resonant inductor KVL equation on the KCL equation to remove ILR.

\[ i_{Lin}(s) = i_{CR}(s) + \frac{i_{CR}(s) + V_{CR}(0)}{s^2 \cdot L_R} + \frac{i_{LR}(0)}{s} + \frac{n \cdot l_{out}}{2 \cdot s} \]
Now we can include the KVL equation for ICR to only leave ILin.

\[ I_{Lin}(s) = I_{CR}(s) \left[ 1 + \frac{1}{s^2 L_R C_R} \right] + \frac{V_{CR}(0)}{s^2 L_R} + \frac{I_{LR}(0)}{s} + \frac{n_{out}}{2s} \]

Now we can include the KVL equation for ICR to only leave ILin.

\[ I_{Lin}(s) = C_R \left( V_{in} - s^2 L_{in} I_{Lin}(s) + s L_{in} I_{Lin}(0) - V_{CR}(0) \right) \left[ 1 + \frac{1}{s^2 L_R C_R} \right] + \frac{V_{CR}(0)}{s^2 L_R} + \frac{I_{LR}(0)}{s} + \frac{n_{out}}{2s} \]

\[ I_{Lin}(s) = \left( V_{in} - s^2 L_{in} I_{Lin}(s) + s L_{in} I_{Lin}(0) - V_{CR}(0) \right) \left( C_R + \frac{1}{s^2 L_R} \right) + \frac{V_{CR}(0)}{s^2 L_R} + \frac{I_{LR}(0)}{s} + \frac{n_{out}}{2s} \]

\[ I_{Lin}(s) + I_{Lin}(s) \left( C_R s^2 L_{in} + \frac{L_{in}}{L_R} \right) = \left( V_{in} + s L_{in} I_{Lin}(0) - V_{CR}(0) \right) \left( C_R + \frac{1}{s^2 L_R} \right) + \frac{V_{CR}(0)}{s^2 L_R} + \frac{I_{LR}(0)}{s} + \frac{n_{out}}{2s} \]

\[ I_{Lin}(s) = \frac{\left( V_{in} + s L_{in} I_{Lin}(0) - V_{CR}(0) \right) \left( C_R + \frac{1}{s^2 L_R} \right) + \frac{V_{CR}(0)}{s^2 L_R} + \frac{I_{LR}(0)}{s} + \frac{n_{out}}{2s} \} {1 + C_R s^2 L_{in} + \frac{L_{in}}{L_R}} \]

\[ I_{Lin}(s) = \frac{\left( V_{in} + s L_{in} I_{Lin}(0) - V_{CR}(0) \right) \left( C_R + \frac{1}{s^2 L_R} \right) + \frac{V_{CR}(0)}{s^2 L_R} + \frac{I_{LR}(0)}{s} + \frac{n_{out}}{2s} \} {1 + \frac{C_R L_{in}}{s^2} + \frac{L_{in}}{L_R C_R}} \]
\[
\begin{align*}
I_{\text{Lin}}(s) &= \frac{V_{\text{in}}}{L_{\text{in}}} + \frac{sL_{\text{in}}I_{\text{Lin}}(0)}{L_{\text{in}}} - \frac{V_{\text{CR}(0)}}{L_{\text{in}}} + \frac{V_{\text{in}}}{s^2 L_{\text{CR}} L_{\text{in}}} - \frac{V_{\text{CR}(0)}}{s^2 L_{\text{CR}} L_{\text{in}}} + \frac{V_{\text{CR}(0)}}{s^2 L_{\text{CR}} L_{\text{in}}} + \frac{l_{\text{LR}(0)}}{2} \frac{n_{\text{out}}}{L_{\text{in}}} \\
I_{\text{Lin}}(s) &= \frac{V_{\text{in}}}{L_{\text{in}}} + \frac{sL_{\text{Lin}}I_{\text{Lin}}(0)}{L_{\text{in}}} - \frac{V_{\text{CR}(0)}}{L_{\text{in}}} + \frac{V_{\text{in}}}{s^2 L_{\text{CR}} L_{\text{in}}} - \frac{V_{\text{CR}(0)}}{s^2 L_{\text{CR}} L_{\text{in}}} + \frac{V_{\text{CR}(0)}}{s^2 L_{\text{CR}} L_{\text{in}}} + \frac{l_{\text{LR}(0)}}{2} \frac{n_{\text{out}}}{L_{\text{in}}} \\
\end{align*}
\]

Now we need to use some composite variables to reduce the size of the inverse Laplace.

\[
\beta_{1.2} = \frac{V_{\text{in}}}{L_{\text{in}}} \frac{V_{\text{CR}(0)}}{L_{\text{in}}}
\]

\[
\beta_{1.1} = I_{\text{Lin}}(0)
\]

\[
\beta_{1.4} = \frac{V_{\text{in}}}{L_{\text{R}} C_{\text{R}} L_{\text{in}}}
\]

\[
\beta_{1.3} = \frac{l_{\text{Lin}}(0)}{L_{\text{R}} C_{\text{R}}} + \frac{l_{\text{LR}(0)}}{2} \frac{n_{\text{out}}}{L_{\text{in}}}
\]

\[
I_{\text{Lin}}(s) = \frac{s^2 \beta_{1.1} + \beta_{1.2} + \frac{\beta_{1.3}}{s} + \frac{\beta_{1.4}}{s^2}}{s^2 + \omega_{1.1}^2}
\]

The inverse Laplace results in:

\[
I_{\text{Lin}}(t) = \frac{\beta_{1.3}}{\omega_{1.1}^2} + \frac{\beta_{1.4}}{\omega_{1.1}^2} t - \frac{\beta_{1.4}}{\omega_{1.1}^2} \sin\omega_{1.1} t - \frac{\beta_{1.3}}{\omega_{1.1}^2} \cos\omega_{1.1} t + \frac{\beta_{1.3}}{\omega_{1.1}^2} + \frac{\beta_{1.2}}{\omega_{1.1}^2} \sin\omega_{1.1} t + \frac{\beta_{1.3}}{\omega_{1.1}^2} - \frac{\beta_{1.4}}{\omega_{1.1}^2} \cos\omega_{1.1} t - \frac{\beta_{1.2}}{\omega_{1.1}^2} \sin\omega_{1.1} t
\]

\[
I_{\text{Lin}}(t) = \frac{\beta_{1.3}}{\omega_{1.1}^2} + \frac{\beta_{1.4}}{\omega_{1.1}^2} t + \left( \frac{\beta_{1.3}}{\omega_{1.1}^2} - \frac{\beta_{1.4}}{\omega_{1.1}^2} \right) \cos\omega_{1.1} t + \left( \frac{\beta_{1.2}}{\omega_{1.1}^2} - \frac{\beta_{1.4}}{\omega_{1.1}^2} \right) \sin\omega_{1.1} t
\]
The frequency of oscillation is the same here, as in the capacitor voltage.

We can also find a maxima/minima for the inductor current by evaluating the first derivative.

\[
\frac{dI_{\text{lin}}}{dt} = \beta \frac{1.4}{\omega_{1.1}^2} - \left( \beta \frac{1.1 - \beta}{\omega_{1.1}^2} \right) \sin(\omega_{1.1} t) - \beta \frac{1.3}{\omega_{1.1}^2} \cos(\omega_{1.1} t)
\]

\[
\frac{dI_{\text{lin}}}{dt} = \beta \frac{1.4}{\omega_{1.1}^2} - \left( \beta \frac{1.1 - \beta}{\omega_{1.1}^2} \right) \sin(\omega_{1.1} t) + \beta \frac{1.2}{\omega_{1.1}^2} \cos(\omega_{1.1} t)
\]

\[
0 = \frac{\beta}{\omega_{1.1}^2} \left( \beta \frac{1.1 - \beta}{\omega_{1.1}^2} \right) \sin(\omega_{1.1} t) + \beta \frac{1.2}{\omega_{1.1}^2} \cos(\omega_{1.1} t)
\]

Using algebraic identity:

\[\sin(x) = \sqrt{0.5 \left( 1 - \cos(2x) \right)}\]

\[\cos(x) = \sqrt{0.5 \left( 1 + \cos(2x) \right)}\]

\[
0 = \frac{\beta}{\omega_{1.1}^2} \left( \beta \frac{1.1 - \beta}{\omega_{1.1}^2} \right) \sqrt{0.5 \left[ 1 - \cos \left( 2 \omega_{1.1} t \right) \right]} + \beta \frac{1.2}{\omega_{1.1}^2} \sqrt{0.5 \left[ 1 + \cos \left( 2 \omega_{1.1} t \right) \right]}
\]

\[
\lambda_{1.20} = \frac{\beta}{\omega_{1.1}^2}
\]

\[
\lambda_{1.21} = \frac{\beta}{\omega_{1.1}^2} - \beta \frac{1.1 - \beta}{\omega_{1.1}^2}
\]

\[
\lambda_{1.22} = \beta \frac{1.2 - \beta}{\omega_{1.1}^2}
\]

\[
0 = \lambda_{1.20} + \lambda_{1.21} \sqrt{\frac{1}{2} \left[ 1 - \cos \left( 2 \omega_{1.1} t \right) \right]} + \lambda_{1.22} \sqrt{\frac{1}{2} \left[ 1 + \cos \left( 2 \omega_{1.1} t \right) \right]}
\]
Solving for \( t_m1.1 \) results in the following equation, which can then be simplified somewhat. In the numerical analysis, it is necessary to break the large equation down into composite variables to allow for simplified calculation, and ease of viewing.

\[
\begin{align*}
\lambda_{1.26} &= \left(\lambda_{1.21}^2 \lambda_{1.25} - \lambda_{1.22} \lambda_{1.20}\right) \\
\lambda_{1.25} &= \sqrt{\lambda_{1.21}^2 - \lambda_{1.20}^2 + \lambda_{1.22}^2} \\
\lambda_{1.27} &= \lambda_{1.21}^2 + \lambda_{1.22}^2 \\
\lambda_{1.28} &= \frac{4 \lambda_{1.20} \lambda_{1.22} \lambda_{1.26}}{\lambda_{1.27}} \\
\lambda_{1.29} &= \lambda_{1.22}^2 + 2 \lambda_{1.20}^2 - \lambda_{1.21}^2 \\
\tau - \text{acos} \left( \frac{\lambda_{1.29} + \lambda_{1.28}}{\lambda_{1.28}} \right) \\
\frac{\pi}{2} \text{acos} \left( \frac{\lambda_{1.29} + \lambda_{1.28}}{\lambda_{1.28}} \right) &= \frac{\lambda_{1.27}}{2}
\end{align*}
\]
The last component that needs to be mapped out for state one is the current in the resonant inductor. This component includes leakage current and magnetizing current. The leakage current component will be the fixed primary transformer current. The magnetizing current will be the actual resonant component. The same procedure for determining input inductor current will be used here, only isolating a different variable. The first KVL equation is used to evaluate for the resonant component voltage equivalency.

\[
\frac{1}{s \cdot C_R} \cdot I_{CR}(s) + \frac{V_{CR}(0)}{s} = s \cdot L_R \cdot I_{LR}(s) - L_R \cdot I_{LR}(0)
\]

\[
\frac{1}{s \cdot C_R} \cdot I_{CR}(s) = s \cdot L_R \cdot I_{LR}(s) - L_R \cdot I_{LR}(0) - \frac{V_{CR}(0)}{s}
\]

\[
I_{CR}(s) = s^2 \cdot C_R \cdot L_R \cdot I_{LR}(s) - s \cdot C_R \cdot L_R \cdot I_{LR}(0) - V_{CR}(0) \cdot C_R
\]

The second equation is used to evaluate the input current.

\[
\frac{V_{in}}{s} = s \cdot L_{in} \cdot I_{Lin}(s) - L_{in} \cdot I_{Lin}(0) + \frac{1}{s \cdot C_R} \cdot I_{CR}(s) + \frac{V_{CR}(0)}{s}
\]

\[
s \cdot L_{in} \cdot I_{Lin}(s) = \frac{V_{in}}{s} + L_{in} \cdot I_{Lin}(0) - \frac{1}{s \cdot C_R} \cdot I_{CR}(s) - \frac{V_{CR}(0)}{s}
\]

\[
I_{Lin}(s) = \frac{V_{in}}{s^2 \cdot L_{in}} + \frac{I_{Lin}(0)}{s} - \frac{1}{s^2 \cdot C_R \cdot L_{in}} \cdot I_{CR}(s) - \frac{V_{CR}(0)}{s^2 \cdot L_{in}}
\]

Now we will use the KCL equation and remove the input inductor current.

\[
\frac{V_{in}}{s^2 \cdot L_{in}} + \frac{I_{Lin}(0)}{s} - \frac{1}{s^2 \cdot C_R \cdot L_{in}} \cdot I_{CR}(s) - \frac{V_{CR}(0)}{s^2 \cdot L_{in}} = I_{CR}(s) + I_{LR}(s) + \frac{I_{pri}}{s}
\]

\[
\frac{V_{in}}{s^2 \cdot L_{in}} + \frac{I_{Lin}(0)}{s} - \frac{1}{s^2 \cdot C_R \cdot L_{in}} \cdot I_{CR}(s) - \frac{V_{CR}(0)}{s^2 \cdot L_{in}} = I_{CR}(s) + I_{LR}(s) + \frac{I_{pri}}{s}
\]
\[ I_{LR}(s) = \frac{V_{in}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \frac{V_{CR(0)}}{s^2 \cdot L_{in}} - I_{CR}(s) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]

Now we can add in the previously found capacitor current to finalize the equation.

\[ I_{LR}(s) = \frac{V_{in} - V_{CR(0)}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \left( s^2 \cdot C_{R} \cdot L_{R} \cdot I_{LR}(s) - s \cdot C_{R} \cdot L_{R} \cdot I_{CR(0)} - V_{CR(0)} \cdot C_{R} \right) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]

\[ I_{LR}(s) = \frac{V_{in} - V_{CR(0)}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \left( s \cdot C_{R} \cdot L_{R} \cdot I_{LR(0)} + V_{CR(0)} \cdot C_{R} \right) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]

\[ I_{LR}(s) = \frac{V_{in} - V_{CR(0)}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \left( s \cdot C_{R} \cdot L_{R} \cdot I_{LR(0)} + V_{CR(0)} \cdot C_{R} \right) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]

\[ I_{LR}(s) = \frac{V_{in} - V_{CR(0)}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \left( s \cdot C_{R} \cdot L_{R} \cdot I_{LR(0)} + V_{CR(0)} \cdot C_{R} \right) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]

\[ I_{LR}(s) = \frac{V_{in} - V_{CR(0)}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \left( s \cdot C_{R} \cdot L_{R} \cdot I_{LR(0)} + V_{CR(0)} \cdot C_{R} \right) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]

\[ I_{LR}(s) = \frac{V_{in} - V_{CR(0)}}{s^2 \cdot L_{in}} + \frac{I_{Lin(0)} - I_{pri}}{s} - \left( s \cdot C_{R} \cdot L_{R} \cdot I_{LR(0)} + V_{CR(0)} \cdot C_{R} \right) \left( 1 + \frac{1}{s^2 \cdot C_{R} \cdot L_{in}} \right) \]
Using composite variables, the resulting equation reduces to the following:

\[ \beta_{1.30} = I_{LR(0)} \]

\[ \beta_{1.31} = \frac{V_{CR(0)}}{L_R} \]

\[ \beta_{1.32} = \frac{I_{Lin(0)} - \frac{I_{out}}{2}}{C_R L_R} + \frac{I_{LR(0)}}{C_R L_{lin}} \]

\[ \beta_{1.33} = \frac{V_{in}}{L_{in} C_R L_R} \]

\[ \omega_{1.1} = \frac{1}{L_{in} C_R} + \frac{1}{C_R L_R} \]

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\[ I_{LR}(s) = \frac{s \beta 1.30 + \beta 1.31 + \frac{\beta 1.32}{s} + \frac{\beta 1.33}{s^2}}{s^2 + \omega 1.1^2} \]

The inverse Laplace transform results in:

\[ I_{LR}(t) = \frac{\beta 1.32}{\omega 1.1^2} + \frac{\beta 1.33}{\omega 1.1^2} t - \frac{\beta 1.33}{\omega 1.1^3} \sin(\omega 1.1 t) + \frac{\beta 1.32}{\omega 1.1^2} \cos(\omega 1.1 t) - \frac{\beta 1.31}{\omega 1.1} \sin(\omega 1.1 t) \]

\[ I_{LR}(t) = \frac{\beta 1.32}{\omega 1.1^2} + \frac{\beta 1.33}{\omega 1.1^2} t + \left( \frac{\beta 1.30}{\omega 1.1^3} \right) \cos(\omega 1.1 t) + \left( \frac{\beta 1.31}{\omega 1.1} - \frac{\beta 1.33}{\omega 1.1^3} \right) \sin(\omega 1.1 t) \]

\[ \lambda 1.31 = \frac{\beta 1.32}{\omega 1.1^2} + \frac{\beta 1.33}{\omega 1.1^2} t \]

\[ \lambda 1.32 = \beta 1.30 - \frac{\beta 1.32}{\omega 1.1^2} \]

\[ \lambda 1.33 = \frac{\beta 1.31}{\omega 1.1} - \frac{\beta 1.33}{\omega 1.1^3} \]

\[ I_{LR}(t) = \lambda 1.31 + \lambda 1.32 \cos(\omega 1.1 t) + \lambda 1.33 \sin(\omega 1.1 t) \]

The only difference between states one and two, is the polarity of primary transformer current. There is no difference between states one and three. The time for state three to end, is when the resonant inductor current plus the primary transformer current reaches zero. This formula will need to be calculated, and then all equations will known for states one through three.

\[ \lambda 1.35 = \frac{\beta 1.32}{\omega 1.1^2} \]
\[ \lambda_{1.36} = \frac{\beta_{1.33}}{\omega_{1.1}^2} \]

\[ 0 = \lambda_{1.35} + \lambda_{1.36} \frac{\text{d}t_3}{\text{d}t} + \lambda_{1.32} \cos\left[\omega_{1.1} \text{d}t_3\right] + \lambda_{1.33} \sin\left[\omega_{1.1} \text{d}t_3\right] \]

For the transition states, the equations are the same, only the values of the resonant inductor is different.

State Four:

This state is the secondary resonance mode. There are only two active elements, with the resonant inductor passing zero current. We will assume here that the junction capacitor, and the resonant inductor are not ringing. In a complete system, this ringing would occur, with some dampening based upon the system losses.

The following represents the system equations:

\[ V_{in} = V_{Lin} + V_{CR} \]

\[ I_{Lin} = I_{CR} \]

The Laplace equations for this state are:

\[ V_{CR}(s) = \frac{1}{s \cdot C_R} \cdot I_{CR}(s) + \frac{V_{CR}(0)}{s} \]

\[ V_{Lin}(s) = s \cdot L_{in} \cdot I_{Lin}(s) - L_{in} \cdot I_{Lin}(0) \]

\[ I_{CR}(s) = s \cdot C_R \cdot V_{CR}(s) - C_R \cdot V_{CR}(0) \]

\[ I_{Lin}(s) = \frac{V_{Lin}(s)}{s \cdot L_{in}} + \frac{I_{Lin}(0)}{s} \]

We now need to solve for these systems of equations to determine capacitor voltage and inductor current at any time.
To determine capacitor voltage, we will start with the KCL equations:

\[ I_{lin} = I_{CR} \]

\[ \frac{V_{lin}(s)}{s \cdot L_{in}} + \frac{l_{lin}(0)}{s} = s \cdot C_{R} \cdot V_{CR}(s) - C_{R} \cdot V_{CR}(0) \]

Now we will combine the KVL equation:

\[ V_{lin}(s) = \frac{V_{in}}{s} - V_{CR}(s) \]

\[ \frac{V_{in}}{s} - \frac{V_{CR}(s)}{s \cdot L_{in}} + \frac{l_{lin}(0)}{s} = s \cdot C_{R} \cdot V_{CR}(s) - C_{R} \cdot V_{CR}(0) \]

\[ \frac{V_{in}}{s^{2} \cdot L_{in}} - \frac{V_{CR}(s)}{s \cdot L_{in}} + \frac{l_{lin}(0)}{s} = s \cdot C_{R} \cdot V_{CR}(s) - C_{R} \cdot V_{CR}(0) \]

\[ \frac{-V_{CR}(s)}{s \cdot L_{in}} - s \cdot C_{R} \cdot V_{CR}(s) = \frac{-V_{in}}{s^{2} \cdot L_{in}} - \frac{l_{lin}(0)}{s} - C_{R} \cdot V_{CR}(0) \]

\[ \frac{V_{CR}(s)}{s \cdot L_{in}} + s \cdot C_{R} \cdot V_{CR}(s) = \frac{V_{in}}{s^{2} \cdot L_{in}} + \frac{l_{lin}(0)}{s} + C_{R} \cdot V_{CR}(0) \]

\[ V_{CR}(s) \left( \frac{1}{s \cdot L_{in}} + s \cdot C_{R} \right) = \frac{V_{in}}{s^{2} \cdot L_{in}} + \frac{l_{lin}(0)}{s} + C_{R} \cdot V_{CR}(0) \]

\[ V_{CR}(s) = \frac{V_{in}}{s^{2} \cdot L_{in}} + \frac{l_{lin}(0)}{s} + C_{R} \cdot V_{CR}(0) \]

\[ V_{CR}(s) = \frac{1}{s \cdot L_{in}} + s \cdot C_{R} \]

\[ V_{CR}(s) = \frac{V_{in}}{s \cdot L_{in} \cdot C_{R}} + \frac{l_{lin}(0)}{C_{R}} + s \cdot V_{CR}(0) \]

\[ V_{CR}(s) = \frac{s^{2} + \frac{1}{L_{in} \cdot C_{R}}}{s^{2} + \frac{1}{C_{R}} + s \cdot V_{CR}(0)} \]
Multiply by \( \frac{s}{s} \) CR

\[ \omega_{4.1} = \sqrt{\frac{1}{L_{in} C_R}} \]

\[ V_{CR}(t) = V_{in} + V_{CR(0)} \cos(\omega_{4.1} t) - V_{in} \cdot \cos(\omega_{4.1} t) + \frac{I_{Lin(0)}}{\omega_{4.1} C_R} \cdot \sin(\omega_{4.1} t) \]

The final form for voltage of the capacitor in state four is:

\[ V_{CR}(t) = V_{in} + V_{CR(0)} \cos(\omega_{4.1} t) - V_{in} \cdot \cos(\omega_{4.1} t) + \frac{I_{Lin(0)}}{\omega_{4.1} C_R} \cdot \sin(\omega_{4.1} t) \]

To calculate the inductor current we will start with the KVL equations.

\[ s L_{in} I_{Lin(s)} - L_{in} I_{Lin(0)} = \frac{V_{in} - \left( \frac{1}{s C_R} \cdot I_{CR(s)} + \frac{V_{CR(0)}}{s} \right)}{s} \]

Now we will substitute in the KCL equation for ICR.

\[ s L_{in} I_{Lin(s)} - L_{in} I_{Lin(0)} = \frac{V_{in} - \left( \frac{1}{s C_R} \cdot I_{Lin(s)} + \frac{V_{CR(0)}}{s} \right)}{s} \]

\[ s L_{in} I_{Lin(s)} + \frac{1}{s C_R} I_{Lin(s)} = \frac{V_{in}}{s} + L_{in} I_{Lin(0)} - \frac{V_{CR(0)}}{s} \]

\[ I_{Lin(s)} \left( s L_{in} + \frac{1}{s C_R} \right) = \frac{V_{in}}{s} + L_{in} I_{Lin(0)} - \frac{V_{CR(0)}}{s} \]

\[ I_{Lin(s)} = \frac{V_{in}}{s} + L_{in} I_{Lin(0)} - \frac{V_{CR(0)}}{s} \]

Multiply by

68
\[
\frac{s}{L_{in}} \quad I_{Lin}(s) = \frac{V_{in} + s \cdot I_{Lin}(0) - \frac{V_{CR(0)}}{L_{in}}}{s^2 + \frac{1}{C_R L_{in}}}\]
\[
\frac{V_{in} - V_{CR(0)}}{L_{in}} + s \cdot I_{Lin}(0) \quad I_{Lin}(s) = \frac{V_{in} - V_{CR(0)}}{L_{in}} + \frac{1}{s^2 + \frac{1}{C_R L_{in}}}
\]

The Laplace transform results in the following:
\[
I_{Lin}(t) = \frac{V_{in} - V_{CR(0)}}{\omega_{4.1} L_{in}} \sin(\omega_{4.1} t) + I_{Lin}(0) \cos(\omega_{4.1} t)
\]

The last piece of information required is the current in the secondary side of the transformer during state four. This network is can be described as a resistor and an inductor. The initial current in the inductor will equal one-half of the output current. The only problem with this concept is that in actuality it starts at zero and decays up to one-half the output current.

This network can be described by the following equation sets:
\[
I_{Sec}(t) = \frac{I_{out}}{2} - I_{Lsec}(t)
\]
\[
V_{Lsec}(t) = V_{Rdide}(t)
\]
\[
V_{Rdide}(t) = I_{Lsec}(t) \cdot R_dide
\]
\[
I_{Lsec}(0) = \frac{I_{out}}{2}
\]

The solution to this simple system is:
The complete system equations are related to the average powers. This means that we will need to calculate the total system wattage on at least one of three points, although a good system check is to calculate the system power at all three points. These three points are the input inductor current times the input voltage, the primary transformer wattage, and the secondary transformer wattage. All three of these points will equal the output wattage. With a known load, we will be able to calculate the output voltage. Due to the complexity of the equations described here, no attempt will be made to determine an exact formula for voltage gain. A numerical approach will be taken, which will result in the same values.

Input power:
\[ P_1 = \frac{V_{in}}{T} \int_0^T I_{Lin}(t) \, dt \]

Primary transformer power:
\[ P_2 = \frac{1}{T} \int_0^T V_{CR}(t) I_{LRM}(t) \, dt \]

Primary transformer power:
\[ P_3 = \frac{n}{T} \int_{0}^{T} V_{CR}(t) I_{sec}(t) \, dt \]

\[ P_4 = I_{out}^2 R_{out} \]

Output power:

The equality of the power on an ideal system result in:

\[ P_1 = P_2 = P_3 = P_4 \]

Including any losses results in:

\[ P_1 = P_{loss} + P_4 \]

Since we have a complete solution for the input current, and it is true that there are no losses prior to the input inductor, we can use \( P_1 \) as our reference for system power. The transformer power can be used to self-check the numerical results, but is not needed here.

\[ P_1 = P_{1.1} + P_{1.2} + P_{1.3} + P_{1.4} \]

\[ P_{1.1} = \frac{V_{in}}{dt_1} \int_{0}^{dt_1} I_{Lin.1}(t) \, dt \]

\[ P_{1.3} = \frac{V_{in}}{dt_3} \int_{0}^{dt_3} I_{Lin.3}(t) \, dt \]

\[ P_{1.2} = \frac{V_{in}}{dt_2} \int_{0}^{dt_2} I_{Lin.2}(t) \, dt \]

\[ P_{1.4} = \frac{V_{in}}{dt_4} \int_{0}^{dt_4} I_{Lin.4}(t) \, dt \]
\[ P_{1.1} = \frac{V_{\text{in}}}{\frac{dt}{dt_1}} \int_0^{dt_1} l_{\text{Lin.1}(t)} \, dt \]

For states one through three:

\[ l_{\text{Lin}(t)} = \frac{\beta_{1.3}}{\omega_{1.1}} \frac{t}{2} + \frac{\beta_{1.4}}{\omega_{1.1}} t + \left( \frac{\beta_{1.1} - \frac{\beta_{1.3}}{2}}{\omega_{1.1}} \right) \cos\left( \frac{\omega_{1.1} \cdot t}{2} \right) + \left( \frac{\beta_{1.2}}{2 \omega_{1.1}} - \frac{\beta_{1.4}}{\omega_{1.1}^3} \right) \sin\left( \frac{\omega_{1.1} \cdot t}{2} \right) \]

\[ P_{1.1} = \frac{V_{\text{in}}}{T} \left[ \frac{\beta_{1.3}}{\omega_{1.1}^2} \frac{dt_1}{2} + \frac{\beta_{1.4}}{\omega_{1.1}^2} \frac{dt_1^2}{2} + \sin\left( \frac{\omega_{1.1} \cdot dt_1}{2} \right) \left( \frac{\beta_{1.1}}{\omega_{1.1}} - \frac{\beta_{1.3}}{2} \right) - \cos\left( \frac{\omega_{1.1} \cdot dt_1}{2} \right) \left( \frac{\beta_{1.2}}{\omega_{1.1}} - \frac{\beta_{1.4}}{\omega_{1.1}^3} \right) \right] \]

\[ P_{1.1} = \frac{V_{\text{in}}}{T \cdot \omega_{1.1}} \left[ \frac{\beta_{1.3}}{\omega_{1.1}} \frac{dt_1}{2} + \frac{\beta_{1.4}}{\omega_{1.1}^2} \frac{dt_1^2}{2} + \sin\left( \frac{\omega_{1.1} \cdot dt_1}{2} \right) \left( \frac{\beta_{1.1}}{\omega_{1.1}} - \frac{\beta_{1.3}}{2} \right) - \cos\left( \frac{\omega_{1.1} \cdot dt_1}{2} \right) \left( \frac{\beta_{1.2}}{\omega_{1.1}} - \frac{\beta_{1.4}}{\omega_{1.1}^3} \right) \right] \]

\[ \beta_{1.1} = l_{\text{Lin}(0)} \]

\[ \beta_{1.2} = \frac{V_{\text{in}}}{L_{\text{in}}} - \frac{V_{CR(0)}}{L_{\text{in}}} \]

\[ \beta_{1.3} = \frac{l_{\text{Lin}(0)}}{L_{CR}} + \frac{n_{\text{but}}}{2} \frac{l_{L(0)}}{C_{LR} L_{\text{in}}} \]

\[ \beta_{1.4} = \frac{V_{\text{in}}}{L_{CR} C_{LR} L_{\text{in}}} \]

For state four:

\[ l_{\text{Lin}(t)} = \frac{V_{\text{in}} - V_{CR(0)}}{\omega_{4.1} L_{\text{in}}} \sin\left( \frac{\omega_{4.1} \cdot t}{2} \right) + l_{\text{Lin}(0)} \cos\left( \frac{\omega_{4.1} \cdot t}{2} \right) \]

\[ P_{1.4} = \frac{V_{\text{in}}}{T} \left( \sin\left( \frac{\omega_{4.1} \cdot dt_1}{2} \right) \frac{l_{\text{Lin}(0)}}{\omega_{4.1}} - \cos\left( \frac{\omega_{4.1} \cdot dt_1}{2} \right) \frac{V_{\text{in}} - V_{CR(0)}}{L_{\text{in}} \omega_{4.1}^2} \right) \]

From these equations, the input power can be calculated, and the resulting output voltage may be calculated.
The losses due to the diodes have the largest impact to the current model. This loss can be approximated by the following expression, which includes the loss of both diodes:

\[ P_{\text{diode}} = \left( 0.7 \cdot R_{\text{diode}} \cdot \frac{l_{\text{out}}}{2} \right) \cdot l_{\text{out}} \]

If this loss is combined with the output power, the total system appears as:

\[ P_1 = P_{\text{loss}} + P_4 \]

\[ P_{\text{input}} = \left( V_{\text{diode}} + R_{\text{diode}} \cdot \frac{l_{\text{out}}}{2} \right) \cdot l_{\text{out}} + l_{\text{out}}^2 \cdot R_{\text{out}} \]

\[ l_{\text{out}} = \frac{\sqrt{V_{\text{diode}}^2 + 2 \cdot P_{\text{input}} \cdot R_{\text{diode}} + 4 \cdot P_{\text{input}} \cdot R_{\text{out}} - V_{\text{diode}}}}{R_{\text{diode}} + 2 \cdot R_{\text{out}}} \]

The output voltage and system gain can be calculated by the following:

\[ M = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_{\text{out}} \cdot \sqrt{V_{\text{diode}}^2 + 2 \cdot P_{\text{input}} \cdot R_{\text{diode}} + 4 \cdot P_{\text{input}} \cdot R_{\text{out}} - V_{\text{diode}}}}{V_{\text{in}} \cdot \sqrt{R_{\text{diode}} + 2 \cdot R_{\text{out}}}} \]
APPENDIX B: NUMERICAL SOLUTION OF THIRD ORDER SYSTEM
This system of equations are built using Mathcad 2001. They are utilized to do iterative analysis for determination of the characteristics of the FR3 type of Forward converter.

The nomenclature of the equations is an initial subscript showing the state of the waveform. All times in a state are referenced to the start of a time, and not the absolute time of the total system. This means that once state two starts, the time variable will start with zero, not dt1.

State Variable Matrix:

These variables are used to store calculated values for the states. They are pre-calculated, and are used to evaluate in the fastest possible manner.

\[
\begin{align*}
total\text{states} := 0 \ldots 4 \\
v_{\text{pre.VCR}}_{\text{totalstates}} := 0 \\
dt_{\text{pre}}_{\text{totalstates}} := 0 \\
i_{\text{pre.Lin}}_{\text{totalstates}} := 0 \\
i_{\text{pre.LR}}_{\text{totalstates}} := 0 \\
i_{\text{pre.Dsec}}_{\text{totalstates}} := 0
\end{align*}
\]

State One Equations:

Frequency of oscillation:

\[
\omega_1 \left( \frac{1}{C_R L_{R}} + \frac{1}{L_{in} C_R} \right) := \sqrt{\frac{1}{C_R L_{R}} + \frac{1}{L_{in} C_R}}
\]

Capacitor voltage:
Several composite functions used in state one for the voltages.

\[ V_{CR,1}|_{CR, L_R, V_{in}, V_{CR0}, L_{in}, L_{R0}, V_{out}, n} = \frac{V_{in}}{L_{in} + 1}. \]

\[ V_{CR0} = \frac{V_{in}}{L_{in} + 1}. \]

\[ V_{CR0} = \frac{V_{in}}{L_{in} + 1}. \]

Alternate shortened form of \( V_{cr} \), utilizing the composite functions.

\[ V_{CR,0,1} = \frac{V_{in}}{L_{in} + 1}. \]

\[ V_{CR0} = \frac{V_{in}}{L_{in} + 1}. \]

\[ V_{CR0} = \frac{V_{in}}{L_{in} + 1}. \]

Time in state one:

\[ t_{1.1} = \frac{V_{in}}{L_{in} + 1}. \]

\[ t_{1.2} = \frac{V_{in}}{L_{in} + 1}. \]

\[ t_{1.3} = \frac{V_{in}}{L_{in} + 1}. \]

\[ t_{1.4} = \frac{V_{in}}{L_{in} + 1}. \]
\[ I_{\text{Lin}}(t) = \beta_{1.3} + \frac{\beta_{1.4}}{\alpha_{1.1}} t + \left( \frac{\beta_{1.1}}{\alpha_{1.1}} - \frac{\beta_{1.3}}{\alpha_{1.1}} \right) \cos(\omega_{1.1} t) + \left( \frac{\beta_{1.2}}{\alpha_{1.1}} - \frac{\beta_{1.4}}{\alpha_{1.1}} \right) \sin(\omega_{1.1} t) \]

\[ \beta_{1.1} = I_{\text{Lin}}(0) \]

\[ \beta_{1.2} = \frac{V_{\text{in}}}{L_{\text{in}}} \cdot \frac{V_{\text{CR}}(0)}{L_{\text{in}}} \]

\[ \beta_{1.4} = \frac{V_{\text{in}}}{L_{R} C_{R} L_{\text{in}}} \]

\[ \beta_{1.3} = \frac{I_{\text{Lin}}(0)}{L_{R} C_{R}} = \frac{I_{L R}(0) + \frac{n_{\text{out}}}{2}}{C_{R} L_{\text{in}}} \]

\[ \beta_{1.10} = \frac{\beta_{1.3}}{\alpha_{1.1}} \]

\[ \beta_{1.11} = \frac{\beta_{1.4}}{\alpha_{1.1}} t \]

\[ \beta_{1.12} = \left( I_{\text{Lin}}(0) - \frac{\beta_{1.3}}{2} \right) \cos(\omega_{1.1} t) \]

\[ \beta_{1.13} = \left( \frac{\beta_{1.2}}{\alpha_{1.1}} - \frac{\beta_{1.4}}{\alpha_{1.1}} \right) \sin(\omega_{1.1} t) \]

\[ \beta_{1.2} \left| \frac{V_{\text{in}}}{L_{\text{in}}} \right| \frac{V_{\text{CR}}}{L_{\text{in}}} = \frac{V_{\text{in}}}{L_{\text{in}}} - \frac{V_{\text{CR}}}{L_{\text{in}}} \]

\[ \beta_{1.3} \left| \frac{I_{\text{Lin}} - L_{R} C_{R} \cdot L_{R} \cdot n_{\text{out}}}{L_{\text{in}}} \right| = \frac{I_{\text{Lin}} - L_{R} \cdot \frac{n_{\text{out}}}{2}}{L_{R} C_{R} L_{\text{in}}} \]

\[ \beta_{1.4} \left| \frac{V_{\text{in}}}{L_{R} C_{R} L_{\text{in}}} \right| = \frac{V_{\text{in}}}{L_{R} C_{R} L_{\text{in}}} \]

\[ \beta_{1.10} \left| \frac{I_{\text{Lin}} - L_{R} C_{R} \cdot L_{R} \cdot n_{\text{out}}}{L_{\text{in}}} \right| = \frac{\beta_{1.3} \left| \frac{I_{\text{Lin}} - L_{R} C_{R} \cdot L_{R} \cdot n_{\text{out}}}{L_{\text{in}}} \right|}{\alpha_{1} \left| C_{R} L_{R} L_{\text{in}} \right|^{2}} \]

\[ \beta_{1.11} \left| \frac{V_{\text{in}}}{L_{R} C_{R} L_{\text{in}} t} \right| = \frac{\beta_{1.4} \left| \frac{V_{\text{in}}}{L_{R} C_{R} L_{\text{in}}} \right|}{\alpha_{1} \left| C_{R} L_{R} L_{\text{in}} \right|^{2}} t \]
\[ \begin{align*}
&\lambda_{1.22}[L_R, C_R, L_{in}, V_{CR0}, V_{in}] = \beta_{1.2} (V_{in} - V_{CR0}) - \frac{\beta_{1.4} (V_{in} - L_R, C_R, L_{in})}{\alpha_{1} L_R, L_{in}}^2 \\
&\lambda_{1.25}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}, V_{CR0}, V_{in}] = \sqrt{\lambda_{1.21}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}]^2 + \lambda_{1.20}[V_{in} - L_R, C_R, L_{in}]^2 + \lambda_{1.22}[L_R, C_R, L_{in}, V_{CR0}, V_{in}]^2} \\
&\lambda_{1.26}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}, V_{CR0}, V_{in}] = \lambda_{1.21}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}]^2 + \lambda_{1.22}[L_R, C_R, L_{in}, V_{CR0}, V_{in}]^2 \\
&\lambda_{1.27}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}, V_{CR0}, V_{in}] = \lambda_{1.21}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}]^2 + \lambda_{1.22}[L_R, C_R, L_{in}, V_{CR0}, V_{in}]^2 \\
&\lambda_{1.28}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}, V_{CR0}, V_{in}] = \lambda_{1.21}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}]^2 + \lambda_{1.22}[L_R, C_R, L_{in}, V_{CR0}, V_{in}]^2 \\
&\lambda_{1.29}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}, V_{CR0}, V_{in}] = \lambda_{1.22}[L_R, C_R, L_{in}, V_{CR0}, V_{in}]^2 + 2 \lambda_{1.20}[V_{in} - L_R, C_R, L_{in}]^2 - \lambda_{1.21}[L_{in0}, L_R, C_R, L_{R0}, R, L_{out}, L_{in}]^2 \\
&\lambda_{1.30} = L_R(0) \\
&\lambda_{1.31} = \frac{V_{CR(0)}}{L_R} \\
&\lambda_{1.32} = \frac{L_{Lin(0)} - \frac{L_{out}}{2}}{C_R L_R} + \frac{L_R(0)}{C_R L_{in}} \\
&\lambda_{1.33} = \frac{V_{in}}{L_{in} C_R L_R}
\end{align*} \]
\[ l_{1.31} = \frac{\beta_{1.32}}{a_{1.1}} + \frac{\beta_{1.33}}{a_{1.1}} \]

\[ l_{1.32} = \frac{\beta_{1.30}}{a_{1.1}} \]

\[ l_{1.33} = \frac{\beta_{1.31}}{a_{1.1}} - \frac{\beta_{1.33}}{a_{1.1}} \]

\[ l_{LR}(t) = l_{1.31} + \lambda_{1.32} \cos(\omega_{1.1} t) + \lambda_{1.33} \sin(\omega_{1.1} t) \]

\[ \frac{\beta_{1.31}}{V_{CR0}, L_R} = \frac{V_{CR0}}{L_R} \]

\[ \frac{\beta_{1.32}}{L_{in0}, n_{out}, C_R, L_R, L_{R0}, L_{lin}} = \frac{l_{Lin0} - n_{out}}{2} + \frac{l_{LR0}}{C_R L_R} \]

\[ \frac{\beta_{1.33}}{V_{in}, L_{in}, C_R, L_R} = \frac{V_{in}}{L_{in} C_R L_R} \]

\[ l_{1.31}[L_{in0}, n_{out}, C_R, L_R, L_{R0}, L_{lin}] = \frac{\beta_{1.32}[L_{in0}, n_{out}, C_R, L_R, L_{R0}, L_{lin}]}{a_{1}[C_R, L_R, L_{lin}]^2} + \frac{\beta_{1.33}[V_{in}, L_{in}, C_R, L_R]}{a_{1}[C_R, L_R, L_{lin}]^3} \]

\[ l_{1.32}[L_{in0}, n_{out}, C_R, L_R, L_{R0}, L_{lin}] = \frac{l_{LR0}}{a_{1}[C_R, L_R, L_{lin}]^2} \]

\[ l_{1.33}[V_{in}, L_{in}, C_R, L_R, V_{CR0}] = \frac{\beta_{1.31}[V_{CR0}, L_R]}{a_{1}[C_R, L_R, L_{lin}]^2} + \frac{\beta_{1.33}[V_{in}, L_{in}, C_R, L_R]}{a_{1}[C_R, L_R, L_{lin}]^3} \]

\[ l_{LRM, 1}[L_{in0}, n_{out}, C_R, L_R, L_{R0}, L_{lin}, V_{CR0}, V_{in}, t] = \frac{n_{out}}{2} + l_{LR, 1}[L_{in0}, n_{out}, C_R, L_R, L_{R0}, L_{lin}, V_{CR0}, V_{in}, t] \]

**State Two Equations:**

\[ V_{CR, 1end}[C_R, L_R, L_{lin}, V_{in}, V_{CR0}, L_{in0}, L_{R0}, L_{Disc0}, n] = V_{CR, 1}\%[C_R, L_R, L_{lin}, V_{in}, V_{CR0}, L_{in0}, L_{R0}, L_{Disc0}, n] + C_R L_R L_{lin} V_{CR0} L_{in0} L_{R0} L_{Disc0}, n] \]

\[ l_{Lin, 1end}[V_{in}, L_{in}, C_R, L_R, L_{Disc0}, V_{CR0}, L_{R0}, L_{Lin0}, n] = l_{Lin, 1}[V_{in}, L_{in}, C_R, L_R, L_{Disc0}, V_{CR0}, L_{R0}, L_{Lin0}, n] \]
State Three Equations:

\[
\begin{align*}
\frac{\text{d}^2L_{\text{RM}2}}{\text{d}t^2} & = 
\frac{-n_0^\text{out}}{2} + \frac{n_1^\text{out}}{2} \frac{1}{L_{\text{RM}2}} \frac{1}{n_0} \frac{1}{L_{\text{in}0}} \frac{1}{C_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} - i_t \frac{1}{L_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} i_t \\
\frac{\text{d}^2L_{\text{LM}2}}{\text{d}t^2} & = 
\frac{-n_0^\text{out}}{2} + \frac{n_1^\text{out}}{2} \frac{1}{L_{\text{LM}2}} \frac{1}{n_0} \frac{1}{L_{\text{in}0}} \frac{1}{C_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} - i_t \frac{1}{L_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} i_t \\
\frac{\text{d}^2L_{\text{RM}3}}{\text{d}t^2} & = 
\frac{-n_0^\text{out}}{2} + \frac{n_1^\text{out}}{2} \frac{1}{L_{\text{RM}3}} \frac{1}{n_0} \frac{1}{L_{\text{in}0}} \frac{1}{C_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} - i_t \frac{1}{L_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} i_t \\
\frac{\text{d}^2L_{\text{LM}3}}{\text{d}t^2} & = 
\frac{-n_0^\text{out}}{2} + \frac{n_1^\text{out}}{2} \frac{1}{L_{\text{LM}3}} \frac{1}{n_0} \frac{1}{L_{\text{in}0}} \frac{1}{C_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} - i_t \frac{1}{L_{\text{in}0}} \frac{1}{V_{\text{CR}0}} \frac{1}{V_{\text{in}0}} \frac{1}{D_{\text{sec}0}} i_t
\end{align*}
\]

State Four equations:

\[
\text{# 4:} \quad |L_{\text{lin}} | \frac{\text{d}}{\text{d}t} \frac{1}{C_{\text{CR}}} = \frac{1}{\sqrt{L_{\text{lin}}} C_{\text{CR}}}
\]
\[ V_{CR.4}(t, V_{in}, V_{CR.0}, C_R, L_{in.0}, L_{in}) = V_{in} + (V_{CR.0} - V_{in}) \cos(\omega_4 L_{in.0} C_R) t + \frac{l_{Lin.0}}{a_4 L_{in.0} C_R} \sin(\omega_4 L_{in.0} C_R) t \]

\[ l_{Lin.4}(t, V_{in}, V_{CR.0}, C_R, L_{in.0}, L_{in}) = \frac{V_{in} - V_{CR.0}}{a_4 L_{in.0} C_R L_{in}} \sin(\omega_4 L_{in.0} C_R) t + l_{Lin.0} \cos(\omega_4 L_{in.0} C_R) t \]

Now we need to calculate the system power, and voltage gain. This is done by calculating the input power, and relating it to the output power.

\[ P_{1,1} = \frac{V_{in}}{dt_1} = a_1 \left[ \beta \frac{1.3 \beta \frac{1.4}{2}}{a_1 1.1} + \beta \frac{1.3}{2} \frac{1.1}{2} + \sin(\omega_1 1.1 t) \left( \beta \frac{1.2}{a_1 1.1} + \beta \frac{1.4}{a_1 3} \right) \right] \]

\[ \beta \frac{1.50}{a_1 L_{in.0} L_{R} C_R L_{R0} n L_{out.0} L_{in}} \cdot \frac{C_R}{dt_1} = \frac{\beta \frac{1.3}{a_1 1.1} \beta \frac{1.4}{a_1 3}}{2 a_1 C_R L_{R} L_{in}} \]

\[ \beta \frac{1.51}{a_1 L_{in.0} L_{R} C_R L_{R0} n L_{out.0} L_{in}} \cdot \frac{C_R}{dt_1} = \sin(\omega_1 1.1 C_R L_{R} L_{in}) \frac{\beta \frac{1.3}{a_1 1.1} \beta \frac{1.4}{a_1 3}}{2 a_1 L_{R} L_{R} L_{in}^2} \]

\[ \beta \frac{1.52}{a_1 L_{in.0} L_{R} C_R L_{R0} V_{CR0}, n L_{out.0} L_{in}} \cdot \frac{V_{in}}{dt_1} = \cos(\omega_1 1.1 C_R L_{R} L_{in}) \frac{\beta \frac{1.3}{a_1 1.1} \beta \frac{1.4}{a_1 3}}{2 a_1 L_{R} L_{R} L_{in}^3} \]

\[ P_{1,0} = \frac{\beta \frac{1.3}{a_1 1.1} \beta \frac{1.4}{a_1 3}}{2 a_1 L_{R} L_{R0} L_{in}} \cdot \frac{V_{in}}{dt_1} = \sin(\omega_1 1.1 C_R L_{R} L_{in}) \frac{\beta \frac{1.3}{a_1 1.1} \beta \frac{1.4}{a_1 3}}{2 a_1 L_{R} L_{R} L_{in}^2} \]

\[ V_{out} = R_{out} L_{out} \]

\[ P_1 = P_{1,1} + P_{1,2} + P_{1,3} + P_{1,4} \]

\[ L_{out} = \frac{\sqrt{V_{diode}^2 + 2 P_{input} R_{diode} + 4 P_{input} R_{out} - V_{diode}}}{R_{diode} + 2 R_{out}} \]
The following represents a test of the numerical analysis, and demonstrates a typical state one voltage waveform. This calculation set will be compared to a Pspice simulated model of the same component values.

\[ l_{LR.0} = 0.0 \]

\[ L_R = 40 \times 10^{-6} \]

\[ C_R = 1.2 \times 10^{-6} \]

\[ V_{in} = 48 \]

\[ L_{sec} = 10 \times 10^{-6} \]

\[ V_{CR.0} = 91.92 \]

\[ L_{in} = 700 \times 10^{-6} \]

\[ l_{Lin.0} = -0.783 \]

\[ n = 0.5 \]

\[ R_{diode} = 0.217 \]

\[ I_{out} = 8.34 \]
First we would like to record the initial state variables into the particular arrays.

\[ I_{pre.Lin_0} := I_{Lin.0} \]
\[ dt_{pre_0} := 0 \]
\[ I_{pre.LR_0} := I_{LR.0} \]
\[ V_{pre.VCR_0} := V_{CR.0} \]
\[ I_{pre.Dsec_0} := I_{Dsec.0} \]

Second we need to calculate the preliminary state variables. This helps to speed up the equations. The functions executed here are very slow, as they are multiple level iterative functions. By storing the result values one time, we are not forced to execute this iterative function multiple times, such as for each point on a graph. This dramatically speeds up the equation process, but means that states two and three will use state one equations, but the initial state variables will reflect what the previous state ended with. This is a correct assumption, as the formulas for states two and three actually are the same, with the exception of the polarity of the Isec current.

\[ dt_{pre_1} := dt \left( C_R \cdot L_R \cdot L_{in} \cdot V_{in} \cdot V_{CR.0} \cdot L_{in.0} \cdot L_{LR.0} \cdot I_{pre.Dsec_0} \cdot n \right) \]
\[ V_{pre.VCR_1} := V_{CR.1end} \left( C_R \cdot L_R \cdot L_{in} \cdot V_{in} \cdot V_{CR.0} \cdot L_{in.0} \cdot L_{LR.0} \cdot I_{pre.Dsec_0} \cdot n \right) \]
\[ I_{pre.Lin_1} := I_{Lin.1end} \left( V_{in} \cdot L_{in} \cdot L_R \cdot C_R \cdot I_{pre.Dsec_0} \cdot V_{CR.0} \cdot L_{LR.0} \cdot L_{in.0} \cdot n \right) \]
\[ I_{pre.LR_1} := I_{LR.1end} \left( V_{in} \cdot L_{in} \cdot L_R \cdot C_R \cdot I_{pre.Dsec_0} \cdot V_{CR.0} \cdot L_{LR.0} \cdot L_{in.0} \cdot n \right) \]
\[ dt_{pre_2} := dt_2 \left( CR, L, L_{in}, V_{in}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{out}, I_{pre.Dsec_0}, n \right) \]

\[ V_{pre.VCR_2} := V_{CR.2end} \left( CR, L, L_{in}, V_{in}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{out}, I_{pre.Dsec_0}, n \right) \]

\[ I_{pre.Lin_2} := I_{Lin.2end} \left( V_{in}, L_{in}, L_R, C_R, I_{out}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{pre.Dsec_0}, n \right) \]

\[ I_{pre.LR_2} := I_{LR.2end} \left( V_{in}, L_{in}, L_R, C_R, I_{out}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{pre.Dsec_0}, n \right) \]

\[ dt_{pre_3} := dt_3 \left( CR, L, L_{in}, V_{in}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{out}, I_{pre.Dsec_0}, n \right) \]

\[ V_{pre.VCR_3} := V_{CR.3end} \left( CR, L, L_{in}, V_{in}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{out}, I_{pre.Dsec_0}, n \right) \]

\[ I_{pre.Lin_3} := I_{Lin.3end} \left( V_{in}, L_{in}, L_R, C_R, I_{out}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{pre.Dsec_0}, n \right) \]

\[ I_{pre.LR_3} := I_{LR.3end} \left( V_{in}, L_{in}, L_R, C_R, I_{out}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{pre.Dsec_0}, n \right) \]

\[ dt_{pre_4} := T - dt_{pre_3} - dt_{pre_2} - dt_{pre_1} \]

\[ V_{pre.VCR_4} := V_{CR.4end} \left( CR, L, L_{in}, V_{in}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{out}, I_{pre.Dsec_0}, n \right) \]

\[ I_{pre.Lin_4} := I_{Lin.4end} \left( V_{in}, L_{in}, L_R, C_R, I_{out}, V_{CR.0}, L_{in.0}, L_{R.0}, I_{pre.Dsec_0}, n \right) \]

\[ I_{pre.LR_4} = 0 \]

\[
\begin{bmatrix}
0 \\
9.81 \times 10^{-6} \\
2.067 \times 10^{-5} \\
9.265 \times 10^{-6} \\
6.026 \times 10^{-5}
\end{bmatrix}
\]

\[ V_{pre.VCR} = \begin{bmatrix}
91.92 \\
3.553 \times 10^{15} \\
-5.832 \times 10^{-4} \\
47.652 \\
48.893
\end{bmatrix} \]
Now that we have the final values for the various states, we can define an equation set for the combined modes, to show a nice combined graph of all states.

This system is dependant upon the above defined variable names, and is not as modular as the other equations. Its sole purpose is to show a nice graph of all states.

\[
\begin{align*}
V_{CR.all} & := V_{CR.1} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR0} \cdot V_{pre.Lin0} \cdot V_{pre.LR0} \cdot V_{pre.Desc0} \cdot n \cdot \text{if } \text{mod}(T) < dt_{pre1} \\
V_{CR.1} & := d_{pre1} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR1} \cdot V_{pre.Lin1} \cdot V_{pre.LR1} \cdot \text{out} \cdot n \cdot \text{if } \text{mod}(T) < dt_{pre1} \cdot dt_{pre2} \cdot \text{mod}(T) < dt_{pre3} \\
V_{CR.2} & := d_{pre2} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR2} \cdot V_{pre.Lin2} \cdot V_{pre.LR2} \cdot \text{out} \cdot n \cdot \text{if } \text{mod}(T) < dt_{pre1} \cdot dt_{pre2} \cdot dt_{pre3} \cdot \text{mod}(T) < dt_{pre1} \cdot dt_{pre2} \\
V_{CR.3} & := d_{pre3} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR3} \cdot C_{R} \cdot \text{pre.Lin3} \cdot \text{lin} \cdot \text{otherwise} \\
\end{align*}
\]

\[
\begin{align*}
I_{Lin.all} & := I_{Lin.1} \cdot V_{in} \cdot \text{lin} \cdot C_{R} \cdot C_{Lin} \cdot V_{pre.Desc0} \cdot V_{pre.VCR0} \cdot V_{pre.Lin0} \cdot V_{pre.LR0} \cdot V_{pre.Desc0} \cdot n \cdot \text{if } \text{mod}(T) = dt_{pre1} \\
I_{Lin.1} & := d_{pre1} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR1} \cdot V_{pre.Lin1} \cdot V_{pre.LR1} \cdot \text{lin} \cdot n \cdot \text{if } \text{mod}(T) = dt_{pre1} \\
I_{Lin.2} & := d_{pre2} \cdot C_{LR} \cdot \text{out} \cdot V_{pre.VCR2} \cdot V_{pre.Lin2} \cdot V_{pre.LR2} \cdot \text{lin} \cdot n \cdot \text{if } \text{mod}(T) = dt_{pre1} \cdot dt_{pre2} \cdot \text{mod}(T) = dt_{pre3} \\
I_{Lin.3} & := d_{pre3} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR3} \cdot C_{R} \cdot \text{pre.Lin3} \cdot \text{lin} \cdot \text{otherwise} \\
\end{align*}
\]

\[
\begin{align*}
I_{LRM.all} & := I_{LRM.1} \cdot V_{pre.Lin0} \cdot n \cdot \text{pre.Desc0} \cdot C_{R} \cdot C_{LR} \cdot V_{pre.VCR1} \cdot V_{pre.Lin1} \cdot V_{pre.VCR0} \cdot V_{in} \cdot \text{if } \text{mod}(T) = dt_{pre1} \\
I_{LRM.1} & := d_{pre1} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR1} \cdot V_{pre.Lin1} \cdot \text{lin} \cdot n \cdot \text{if } \text{mod}(T) = dt_{pre1} \\
I_{LRM.2} & := d_{pre2} \cdot C_{LR} \cdot \text{lin} \cdot V_{in} \cdot V_{pre.VCR2} \cdot V_{pre.Lin2} \cdot \text{lin} \cdot n \cdot \text{if } \text{mod}(T) = dt_{pre1} \cdot dt_{pre2} \cdot \text{mod}(T) = dt_{pre3} \\
0.0 & \text{otherwise} \\
\end{align*}
\]

All of the variables are in place for demonstrating the results of the equations. For states one through three, we will utilize the state one equation, but use the pre.end variables for
the various states. This will allow for fast calculation time, at a minimal amount of
confusion.

**State One Results:**

This is the primary resonance frequency:

\[ \omega_1 = \left( C_R L_R L_{in} \right) = 1.484 \times 10^5 \]

![Graph](image_url)
The following is a screen capture of Pspice simulating the circuit that is modeled above.

The time difference of 9.6u seconds calculated, versus 9.8u seconds simulated is due to various non-ideal components that the simulation does not allow removed. These devices are the diodes, and the switching device.

Now we can graph the current in the input inductor during the first resonance stage.
This is a Pspice simulation of the previously noted circuit. The system matches quite well with these parameters.

We can now evaluate the resonant inductor current. This value will be the addition of both the leakage and the magnetizing current on the primary side of the transformer.
Here is a comparison of state one calculations versus the simulation:

Simulation time for state one = 9.819 micro-seconds
\[
dt_{pre_1} = 9.81 \times 10^{-6}
\]

Sim VCR start = 91.919
\[
V_{CR.1}(0, C_R, L_R, L_{in}, V_{in}, V_{CR.0}, I_{pre.0}, I_{pre.Dsec}, n) = 91.92
\]

Sim VCR end = -0.013
\[
I_{Lin.1}(V_{in}, L_{in}, C_R, I_{pre.Dsec}, V_{pre.VCR}, I_{pre.LR}, I_{pre.Lin}, n, 0) = -0.783
\]

Sim ILin start = -0.7829
\[
I_{Lin.1}(V_{in}, L_{in}, C_R, I_{pre.Dsec}, V_{pre.VCR}, I_{pre.LR}, I_{pre.Lin}, n, dt_{pre}) = -0.891
\]

Sim ILin end = -0.9134
\[
I_{LRM.1}(I_{pre.Lin}, n, I_{pre.Dsec}, C_R, L_R, I_{pre.LR}, L_{in}, V_{pre.VCR}, V_{in}, 0) = 1.52
\]

Sim ILRM start = 1.539
\[
I_{LRM.1}(I_{pre.Lin}, n, I_{pre.Dsec}, C_R, L_R, I_{pre.LR}, L_{in}, V_{pre.VCR}, V_{in}, dt_{pre}) = 15.176
\]

Sim ILRM end = 15.213

State Two Analysis:
\[
\begin{vmatrix}
L_{RM} & L_{P} & C & R & L_{Q} & \gamma_{P} & C_{VCR} & \gamma_{V}\n\end{vmatrix}
\]
A comparison of the Pspice results and the calculation results for state two:

\[ dt_{pre_2} = 2.067 \times 10^{-5} \]

Sim time for state two = 20.623 micro-seconds

\[ V_{CR.1} \left( 0, C_R, L_R, L_{in}, V_{in}, V_{pre.VCR_1}, I_{pre.Lin_1}, I_{pre.LR_1}, I_{out}, n \right) = 3.553 \times 10^{-15} \]

Sim VCR start = 0

\[ V_{CR.1} \left( dt_{pre_2}, C_R, L_R, L_{in}, V_{in}, V_{pre.VCR_1}, I_{pre.Lin_1}, I_{pre.LR_1}, I_{out}, n \right) = -5.832 \times 10^{-4} \]

Sim VCR end = 0

\[ I_{Lin.1} \left( V_{in}, L_{in}, C_R, L_R, I_{out}, V_{pre.VCR_1}, I_{pre.Lin_1}, I_{pre.LR_1}, I_{pre.Lin_1}, n, 0 \right) = -0.891 \]

Sim ILin start = -0.9101

\[ I_{Lin.1} \left( V_{in}, L_{in}, C_R, L_R, -I_{out}, V_{pre.VCR_1}, I_{pre.Lin_1}, I_{pre.LR_1}, I_{pre.Lin_1}, n, dt_{pre_2} \right) = 1.797 \]

Sim ILin end = 1.6932

\[ I_{LRM.1} \left( I_{pre.Lin_1}, n, -I_{out}, C_R, L_R, I_{pre.LR_1}, L_{in}, V_{pre.VCR_1}, V_{in}, 0 \right) = 11.571 \]

Sim ILRM start = 10.984

\[ I_{LRM.1} \left( I_{pre.Lin_1}, n, -I_{out}, C_R, L_R, I_{pre.LR_1}, L_{in}, V_{pre.VCR_1}, V_{in}, -dt_{pre_2} \right) = -10.664 \]

Sim ILRM end = -10.163
State Three Analysis:
A comparison of state three:

\[ dt_{pre_3} = 9.265 \times 10^{-6} \]

Simulation time for state three = 9.036 micro-seconds

\[ V_{CR.1} \left[ 0, C_R, L_R, L_{in}, V_{in}, V_{pre.VCR}, I_{pre.Lin}, I_{pre.LR}, I_{out}, n \right] = -5.832 \times 10^{-4} \]

Sim VCR start = 0

\[ V_{CR.1} \left( dt_{pre_3}, C_R, L_R, L_{in}, V_{in}, V_{pre.VCR}, I_{pre.Lin}, I_{pre.LR}, I_{out}, n \right) = 47.652 \]

Sim VCR end = 43.475

\[ I_{Lin.1} \left( V_{in}, L_{in}, C_R, L_R, L_{in}, V_{in}, V_{pre.VCR}, I_{pre.Lin}, I_{pre.LR}, I_{out}, n, 0 \right) = 1.797 \]

Sim ILin start = 1.6986

\[ I_{Lin.1} \left( V_{in}, L_{in}, C_R, L_R, L_{in}, V_{in}, V_{pre.VCR}, I_{pre.Lin}, I_{pre.LR}, I_{out}, n, dt_{pre_3} \right) = 2.063 \]

Sim ILin end = 2.0070

\[ I_{LRM.1} \left[ I_{pre.Lin}, I_{out}, C_R, L_R, I_{pre.LR}, L_{in}, V_{pre.VCR}, V_{in}, 0 \right] = -6.475 \]

Sim ILRM start = -5.8821

\[ I_{LRM.1} \left[ I_{pre.Lin}, I_{out}, C_R, L_R, I_{pre.LR}, L_{in}, V_{pre.VCR}, V_{in}, dt_{pre_3} \right] = 4.99 \times 10^{-9} \]

Sim ILRM end = 0.006
Now for the equations for state four.
The diagram shows a curve with annotations that appear to be related to time and voltage measurements. The axes are labeled with time and voltage values, and the curve traces a decreasing function over time. Specific points and values are marked, indicating measurements or calculations at certain time intervals.
The following is a comparison of the system in the fourth state.

Simulation time for state four = 60.4 micro-seconds

\[ dt_{pre_4} = 6.026 \times 10^{-5} \]

\[ V_{CR,4} \left( V_{in}, V_{pre..VCR,3}, C_R, I_{pre..Lin,3}, L_{in} \right) = 47.652 \]

Sim VCR start = 43.380

\[ V_{CR,4} \left( dt_{pre_4}, V_{in}, V_{pre..VCR,3}, C_R, I_{pre..Lin,3}, L_{in} \right) = 91.69 \]

Sim VCR end = 92.309

\[ I_{Lin,4} \left( V_{in}, V_{pre..VCR,3}, C_R, I_{pre..Lin,3}, L_{in} \right) = 2.063 \]

Sim ILin start = 2.0074

\[ I_{Lin,4} \left( dt_{pre_4}, V_{in}, V_{pre..VCR,3}, C_R, I_{pre..Lin,3}, L_{in} \right) = -0.991 \]

Sim ILin end = -0.8249
There is a decay in the secondary side current, which is dependant upon the diode resistances, and inductor values. In practice, the diode resistance is a value that is determined by experimental results. It is determined by the voltage difference of two parallel diodes, with the current being defined by the difference of the current in the two devices.

This non-ideal system is required to determine the starting value of the current in the secondary side. In a truly ideal system, the value would remain a constant zero, and result in having no vertical shift in the waveform of ILRM during the start of state one.

\[
I_{\text{Sec}}(t) = I_{\text{out}}(t) + R_{\text{diode}} \cdot L_{\text{sec}} \cdot \frac{\text{d}t}{\text{d}t_{\text{pre}}},
\]

The simulated value is 3.043 Amps.
This is a complete cycle analysis of the three waveforms previously shown. This shows all four states.
Now we need to calculate the system power, and voltage gain. This is done by calculating the input power, and relating it to the output power.

\[ V_d = 0.7 \]

\[ R_{out} = 0.3 \]

\[ P_1(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}) = 36.339 \]

Simulated input power = 48V * 0.585A = 28.08 Watts

\[ I_{out, new}(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}, R_{out}, R_{diode}, V_d) = 8.614 \]

Simulated \( V_{out} = 8.4726 \)

\[ V_{out}(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}, R_{out}, R_{diode}, V_d) = 2.584 \]

Simulated \( I_{out} = 2.5418 \)

\[ P_{1A}(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}) = -4.419 \]

\[ P_{1B}(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}) = 6.68 \]

\[ P_{1C}(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}) = 8.824 \]

\[ P_{1D}(\text{Lin}, 0, \text{L}_R, \text{C}_R, \text{L}_0, \text{V}_{CR}, 0, n, I_{out}, I_{Dsec}, 0, \text{L}_{in}, T, \text{V}_{in}) = 25.254 \]

\[ P_{\text{diode}} = \left( 0.7 + R_{\text{diode}} \frac{I_{out}}{2} \right) I_{out} \]

\[ P_{\text{diode}} = 13.385 \]

Numerical approach:

\[ P_{1A, \text{num}} = \frac{V_{in}}{T} \int_{0}^{dt_{\text{pre}_1}} I_{\text{Lin}, \text{all}(t)} dt \]

\[ P_{1A, \text{num}} = -4.465 \]

\[ P_{1B, \text{num}} = \frac{V_{in}}{T} \int_{dt_{\text{pre}_1} + dt_{\text{pre}_2}}^{dt_{\text{pre}_1}} I_{\text{Lin}, \text{all}(t)} dt \]

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\[ P_{1B.num} = 4.497 \]

\[ P_{1C.num} = 8.824 \]

\[ P_{1D.num} = 25.366 \]

The total numerical solution for input power:

\[ P_{1.num} = 34.231 \]
APPENDIX C: SCHEMATIC OF PROTOTYPE HARDWARE
APPENDIX D: BOARD LAYOUT OF PROTOTYPE HARDWARE
APPENDIX E: VHDL SOURCE CODE OF PROTOTYPE HARDWARE
-- FR3 Project  (Third Order Forward Resonant Converter)

-- David Bills

-- Presented to UCF for Thesis Project Fall 2007

-- The following notes describe configuration options.

-- Assuming a 50 MHz system clock.

-- Switch Controls:  Note that Up is a "0"

-- Switch 1 =>  Master Mode Switch
--  0 => Diagnostics Mode
--  1 => Normal Operation

-- Switch 2 =>  Primary Switch Enable (All Modes)
--  0 => Disable Primary Output
--  1 => Enable Primary Output

-- Switch 3 =>  Current Transition select (Normal Operation)
--  0 => Switch master FET off when current goes from positive to negative
--  This relies heavily on Diode and has worse efficiency.
--  1 => Switch master FET off when current goes from negative to positive
--  This maximizes FET time, but causes some current spikes.
--  During Diagnostics this sets the state of the primary switch driver
-- Switch 4 => Enable Secondary FETs (Normal Operation)
-- 0 => Disabled
-- 1 => Enabled
-- During Diagnostics this sets the state of the both secondary switch drivers

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following lines to use the declarations that are
-- provided for instantiating Xilinx primitive components.
-- library UNISIM;
-- use UNISIM.VComponents.all;

entity main is Port ( 
  system_status : out std_logic_vector( 15 downto 0 );
  system_clk : in std_logic;
  system_reset : in std_logic;
  system_switch : in std_logic_vector( 3 downto 0 );
  COMP_APRIME : in std_logic;
);
COMP_ASEC1 : in std_logic;
COMP_ASEC2 : in std_logic;
COMP_VOUT : in std_logic;
COMP_VPRIME : in std_logic;
COMP_VSEC1 : in std_logic;
COMP_VSEC2 : in std_logic;
DRV_ENBL : out std_logic;
DRV_PRIME : out std_logic;
DRV_SEC1 : out std_logic;
DRV_SEC2 : out std_logic
);
end main;

architecture arc_main of main is

signal system_timer : std_logic_vector( 7 downto 0 );
signal System_State : std_logic_vector( 2 downto 0 );
signal DRV_ENBL_buf : std_logic;
signal DRV_PRIME_buf : std_logic;
signal DRV_SEC1_buf : std_logic;
signal DRV_SEC2_buf : std_logic;
signal ERROR_COND_buf : std_logic;
signal timer_delay : std_logic_vector( 7 downto 0 );

begin

main_system: process( system_reset, system_clk )

begin

if( system_reset = '0' ) then -- Enter reset state.

System_State <= "000";
timer_delay <= "00110010"; -- 50 clocks at 50MHz

elsif( rising_edge( system_clk ) ) then

DRV_ENBL <= DRV_ENBL_buf;
DRV_PRIME <= DRV_PRIME_buf;
DRV_SEC1 <= DRV_SEC1_buf;
DRV_SEC2 <= DRV_SEC2_buf;

system_status( 0 ) <= COMP_APRIME;

system_status( 1 ) <= COMP_ASEC1;

system_status( 2 ) <= COMP_ASEC2;
system_status(3) <= COMP_VOUT;

system_status(4) <= COMP_VPRIME;

system_status(5) <= COMP_VSEC1;

system_status(6) <= COMP_VSEC2;

system_status(7) <= ERROR_COND_buf;

system_status(8) <= DRV_PRIME_buf;

system_status(9) <= System_State(0);

system_status(10) <= System_State(1);

system_status(11) <= System_State(2);

system_status(15 downto 12) <= system_timer(3 downto 0);

DRV_ENBL_buf <= system_switch(1);

if( system_switch(0) = '0' ) then  -- Enter Diagnostics Mode
    DRV_PRIME_buf <= system_switch(2);  -- Primary Driver is a function of Switch 3
    DRV_SEC1_buf <= system_switch(3);  -- Secondary Driver is a function of Switch 4
    DRV_SEC2_buf <= system_switch(3);  -- Secondary Driver is a function of Switch 4

    System_State <= "000";

123
system_timer <= system_timer - '1';

else

if( system_switch( 3 ) = '1' ) then

if( DRV_PRIME_buf = '1' ) then  -- Secondary Switch Enable

DRV_SEC1_buf <= COMP_VPRIME ;  -- Secondary diodes during switching

DRV_SEC2_buf <= NOT COMP_VPRIME ;

else

DRV_SEC1_buf <= '1';  -- Primary switch off. Turn on secondaries

DRV_SEC2_buf <= '1';

end if;

else

DRV_SEC1_buf <= '0';  -- Secondary diodes only during switching

DRV_SEC2_buf <= '0';

end if;

end if;

case System_State is

when "000" => -- This is starting state. Testing the output voltage.

ERROR_COND_buf <= '0';  -- Clear the Error Condition Flag.

if( timer_delay(7 downto 4) < "0011" ) then

    timer_delay <= "00110010";

end if;

124
if( COMP_VOUT = '0' AND COMP_VPRIME = '1' )then

-- The output voltage is low.

    System_State <= "001";
    system_timer <= "01100100"; -- 100 clocks at 50MHz

    DRV_PRIME_buf <= '1';  -- Start the primary switch.

else

    DRV_PRIME_buf <= '0';  -- Reset the primary switch.

end if;

when "001" => -- Wait for transition of current on primary to negative.

    if( COMP_VPRIME = '0' OR system_timer = "00000000" )then

        -- Don't tolerate long delays. This could be a short circuit.

        -- Timer is included here to solve this problem.

    if( system_timer = "00000000" )then

125
ERROR_COND_buf <= '1';

end if;

System_State <= "010";  -- Turn on switch and wait for 2us

system_timer <= "00011001"; -- 25 clocks at 50MHz

else

system_timer <= system_timer - '1';

end if;

when "010" => -- Delay the system for 0.5us.

system_timer <= system_timer - '1';

if( system_timer = "00000000" ) then

System_State <= "011";

system_timer <= "01100100"; -- 100 clocks at 50MHz

end if;
when "$011" => -- Decide when to turn off the primary FET.

if( COMP_VPRIME = '1' OR -- Positive voltage.
    system_timer = "00000000" )then -- Error condition.

    -- Don't tolerate long delays. This could be a short circuit.

    -- Timer is included here to solve this problem.

    if( system_timer = "00000000" )then
        ERROR_COND_buf <= '1';
    end if;

    System_State <= "100";
    DRV_PRIME_buf <= '0'; -- Stop the primary FET
    system_timer <= timer_delay;
else
    system_timer <= system_timer - '1';
end if;
when "100" => -- Delay the system for before testing output voltage.

system_timer <= system_timer - '1';

if( system_timer = "00000000" ) then

    System_State <= "000";

end if;

if( COMP_VOUT = '0' and timer_delay(7 downto 4) > "0011" ) then -- 0.5 us

    timer_delay <= timer_delay - '1';

else

    if( COMP_VOUT = '1' and timer_delay(7 downto 4) < "1111" ) then

        timer_delay <= timer_delay + '1';

    end if;

end if;

end if;
end if;

when others =>

    System_State <= "000";

end case;

end if;

end if;

end if;

end process main_system;

end arc_main;
-- UCF file section

NET "system_clk" TNM_NET = "system_clk";
TIMESPEC "TS_system_clk" = PERIOD "system_clk" 20 ns HIGH 50 %;

#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments

NET "COMP_APRIME" LOC = "P42" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "COMP_ASEC1" LOC = "P37" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "COMP_ASEC2" LOC = "P36" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "COMP_PRIME" LOC = "P43" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "COMP_VOUT" LOC = "P44" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "COMP_VSEC1" LOC = "P34" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "COMP_VSEC2" LOC = "P33" | SCHMITT_TRIGGER | FLOAT |
IOSTANDARD = LVCMOS33 ;
NET "DRV_ENBL" LOC = "P39" | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
NET "DRV_PRIME" LOC = "P41" | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
NET "DRV_SEC1" LOC = "P40" | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
NET "DRV_SEC2" LOC = "P38" | IOSTANDARD = LVCMOS33 | SLEW = FAST ;
NET "system_clk" LOC = "P1" | IOSTANDARD = LVCMOS33 |
SCHMITT_TRIGGER | FLOAT ;
NET "system_reset" LOC = "P8" | IOSTANDARD = LVCMOS33 | FLOAT |
SCHMITT_TRIGGER ;
NET "system_status<0>" LOC = "P12" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<10>" LOC = "P27" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<11>" LOC = "P28" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<12>" LOC = "P29" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<13>" LOC = "P30" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<14>" LOC = "P31" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<15>" LOC = "P32" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<1>" LOC = "P13" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<2>" LOC = "P14" | SLEW = FAST | IOSTANDARD =
LVCMOS33 | FLOAT ;
NET "system_status<3>" LOC = "P16" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_status<4>" LOC = "P18" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_status<5>" LOC = "P19" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_status<6>" LOC = "P20" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_status<7>" LOC = "P21" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_status<8>" LOC = "P22" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_status<9>" LOC = "P23" | SLEW = FAST | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_switch<0>" LOC = "P6" | SCHMITT_TRIGGER | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_switch<1>" LOC = "P5" | SCHMITT_TRIGGER | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_switch<2>" LOC = "P3" | SCHMITT_TRIGGER | IOSTANDARD = LVCMOS33 | FLOAT ;
NET "system_switch<3>" LOC = "P2" | SCHMITT_TRIGGER | IOSTANDARD = LVCMOS33 | FLOAT ;
#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE
LIST OF REFERENCES


