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## Four Terminal Junction Field-effect Transistor Model For Computer-aided Design

Hao Ding  
*University of Central Florida*



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# **FOUR TERMINAL JUNCTION FIELD-EFFECT TRANSISTOR MODEL FOR COMPUTER-AIDED DESIGN**

by

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A dissertation submitted in partial fulfillment of the requirements  
for the degree of Doctor of Philosophy  
in the School of Electrical Engineering and Computer Science  
in the College of Engineering and Computer Science  
at the University of Central Florida  
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## **ABSTRACT**

A compact model for four-terminal (independent top and bottom gates) junction field-effect transistor (JFET) is presented in this dissertation. The model describes the steady-state characteristics with a unified equation for all bias conditions that provides a high degree of accuracy and continuity of conductance, which are important for predictive analog circuit simulations. It also includes capacitance and leakage equations. A special capacitance drop-off phenomenon at the pinch-off region is studied and modeled. The operations of the junction field-effect transistor (JFET) with an oxide top-gate and full oxide isolation are analyzed, and a semi-physical compact model is developed. The effects of the different modes associated with the oxide top-gate on the JFET steady-state characteristics of the transistor are discussed, and a single expression applicable for the description of the JFET dc characteristics for all operation modes is derived. The model has been implemented in Verilog-A and simulated in Cadence framework for comparison to experimental data measured at Texas Instruments.

I dedicate this dissertation

To my Dad, Mom and Sister for instilling the importance of hard work and higher education;

To Dr. Juin J. Liou for encouragement and guidance for me to reach my dreams.

## **ACKNOWLEDGMENTS**

I wish to thank Colin McAndrew at Freescale for his insightful suggestions and discussions.

I wish to thank Keith Green at Texas Instruments for his support and guidance.

I wish to thank the Spice Modeling Group at Texas Instruments for their help in getting measurement data and implementing the model.

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# CHAPTER ONE: JUNCTION FIELD-EFFECT TRANSISTOR MODEL OVERVIEW

## **1.1 Introduction**

The Junction Field-Effect Transistor (JFET) offers several advantages: First, because of its intrinsic radiation tolerance, JFET is suitable for operation in harsh radiation environments. Second, due to its superior noise performance, JFET can be used in low-noise front-end circuits for many different applications. Third, JFET has isolated dual gates and is useful for signal mixing purpose.

In the past 30 years, a handful of models have been developed to describe the function of JFETs [1-6], including the early Berkeley's SPICE model, the Taki's empirical model, and the recent four-terminal model. While these models can adequately predict certain aspects of JFET's behavior, none of them can satisfactorily cover a broad range of physical effects and topologies of such devices. For instance, with the ever-decreasing supply voltage in integrated circuits, JFET tends to operate very closely to the crossover from the linear to saturation region. It is just in this region where the conventional JFET models frequently fail to provide a good fit [7]. Another shortcoming of the existing models is the employment of the Gradual Channel Approximation (GCA), which is only valid for long channel devices. As the technology advance continues to

scale down the device size, short channel effects in JFETs are of paramount importance and required to be included.

## 1.2 Review of the Existing JFET Models

Fig.1-1 illustrates a simplified p-channel JFET structure. In the figure, the gray areas denote the depletion region associated with the top and bottom gate regions, and the conducting channel is the region sandwiched between the two depletion regions, which becomes narrower toward the drain region due to the negative drain voltage applied to the drain terminal.

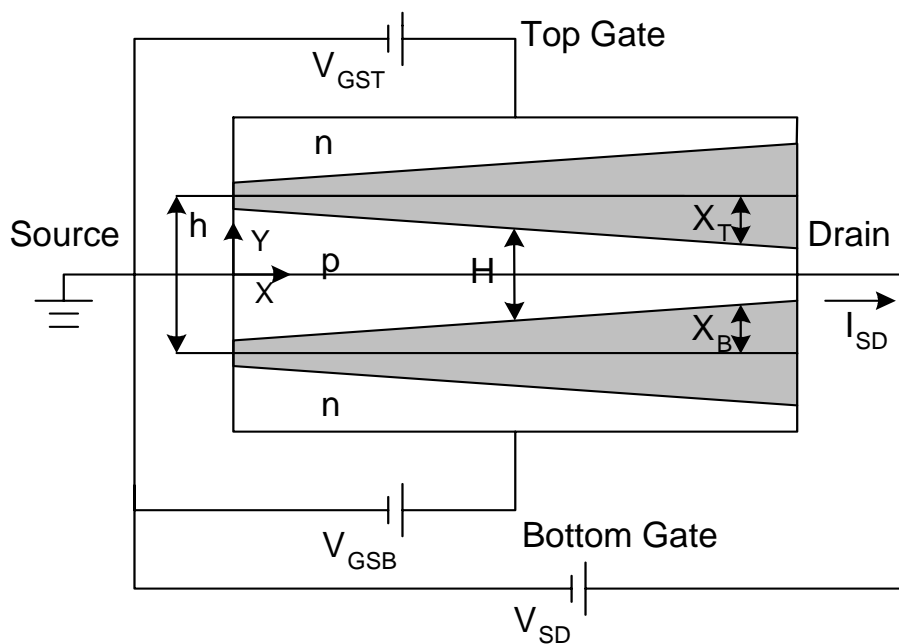


Figure 1-1 Simplified two-dimensional JFET structure

Unlike the MOSFET, which has received broad attentions, effort placed on the modeling of JFET has been scarce and lacked behind

its technology and application. This is particularly true for JFETs operating as four-terminal device.

The early Berkeley model simply utilizes two separate equations to describe the current-voltage characteristics in the linear (before pinch-off) and saturation regions (after pinch-off, but before the channel is entirely cut-off). These equations are:

$$I_{SD} = (W/L)\beta[2(V_P - V_{GS})V_{SD} - V_{SD}^2](1 + \lambda V_{SD}) \quad 1-1$$

$$I_{SD} = I_{SDS}(1 + \lambda V_{SD}) \quad 1-2$$

where  $I_{SD}$  is the source to drain current,  $I_{SDS}$  is the source to drain saturation current,  $V_{SD}$  is the source to drain voltage,  $V_{GS}$  is the gate to source voltage,  $W$  is the channel width,  $L$  is the channel length,  $\beta$  is the quadratic transfer parameter (the slope of  $\sqrt{I_{DS}}$  vs.  $V_{GS}$ ),  $\lambda$  is the channel modulation coefficient, and  $V_P$  is the pinch-off voltage at  $V_{SD}=0$ . This empirical model can be derived from the following more generalized equations [1]:

$$\begin{aligned} I_{DS} &= (W/L)qN_A\mu_F \int_0^{V_{SD}} H(x)dV_i \\ &= G_0V_{SD} - \frac{2}{3}G_0(V_P + \phi)^{-0.5}[(V_P + \phi + V_{GS})^{1.5} - (\phi + V_{GS})^{1.5}] \end{aligned} \quad 1-3$$

$$I_{SDS} = G_0(V_P - V_{GS}) - \frac{2}{3}G_0(V_P + \phi)^{0.5}[(V_P + \phi)^{1.5} - (\phi + V_{GS})^{1.5}] \quad 1-4$$

The above-mentioned models employ the following assumptions and limitations, which are highly questionable for today's JFET technologies:

- 1) JFETs are assumed to have symmetrical top and bottom gates, a case applied only to JFETs having identical doping densities in top and bottom gate regions.
- 2) The electric field in the channel varies gradually in the channel direction (x-direction, see Fig. 1-1), and such a field can be separated from the y-direction electric field in the depletion region. This assumption is appropriate only if the channel length is sufficiently long.
- 3) The top and bottom gate are connected together (3-terminal operation). This is invalid for cases where different voltages are applied to the top and bottom gate terminals.
- 4) The subthreshold behavior near the cutoff region is neglected. This gives rise to a large error when JFETs operate near the pinch-off voltage.
- 5) Separated equations are used to describe the linear and saturation current-voltage characteristics. This can lead to singularity and thus diverge problems during the model calculations and simulations.
- 6) The model is developed based on the traditional JFET topology. It becomes questionable when applied to advanced JFET technologies.

A somewhat better empirical model was suggested by Taki in 1978, which expresses the linear and saturation regions using a single expression:



$$I_{SD} = I_{SDS} \tanh \alpha \left| \frac{V_{SD}}{V_P - V_{GS}} \right| (1 + \lambda V_{SD}) \quad 1-5$$

Where  $\alpha$  is a fitting parameter merging the linear and saturation regions. This model is quite compact, but it still possesses the majority of limitations associated with the Berkeley model mentioned above.

In 1991, Halen [7] developed an improved JFET model based on (1) and (2), by considering asymmetrical top and bottom gates, and including the short channel velocity saturation effect and channel length modulation. The model has the form

$$I_{DS} = \frac{(1 + \lambda V_{DS}^{0.5}) I'_{DS}}{1 + \mu V_{DS} / LV_{SAT}} \quad 1-6$$

$$I'_{DS} = G_0 \left\{ V'_{DS} - \frac{2}{3V_{PT}^{1/2}} [(V'_{DS} + V_{BIT} - V_{TGS})^{3/2} - (V_{BIT} - V_{TGS})^{1.5}] \right. \\ \left. - \frac{2}{3V_{PB}^{1/2}} [(V'_{DS} + V_{BIB} - V_{BGS})^{3/2} - (V_{BIB} - V_{BGS})^{1.5}] \right\} \quad 1-7$$

The model still has the following drawbacks:

- 1) It uses the Gradual Channel Approximation (GCA), and the short-channel effects are only accounted for on a first-order basis.
- 2) It doesn't provide a satisfactory unified model for the linear and saturation regions.
- 3) The subthreshold behavior is neglected.

- 4) The pinch-off voltage is derived based on the three-terminal operation, and the accuracy of the model in four-terminal operations is doubtful.

Extending Taki's work, Wong [4] has proposed an improved JFET model to describe the 4-terminal JFET behavior. This model accounts for the subthreshold region and uses the Hermite interpolation method to merge the quadratic and subthreshold regions without requiring a fitting parameter. The pinch-off voltage takes the dual gates into account. Also, the quadratic transfer parameter  $\beta$  is obtained from device physics, rather than empirical means. What is more, the merging parameter is also modeled without requiring measurements. The equivalent circuit of the JFET model is shown in Fig. 1-2, and the equations for the components in the equivalent circuit proposed by Wong are as follows.

a) Drain to Source Current

$$I_{SD} = I_{SDS} \tanh(\alpha V_{SD} / B_1)(1 + \lambda V_{SD}) \quad 1-8$$

where

$$\begin{aligned} I_{SDS} &= I_{SDS0}(1 - B_2)^2 \\ B_1 &= V_P - V_{GS} \\ B_2 &= V_{GS} / V_P \end{aligned} \quad 1-9$$

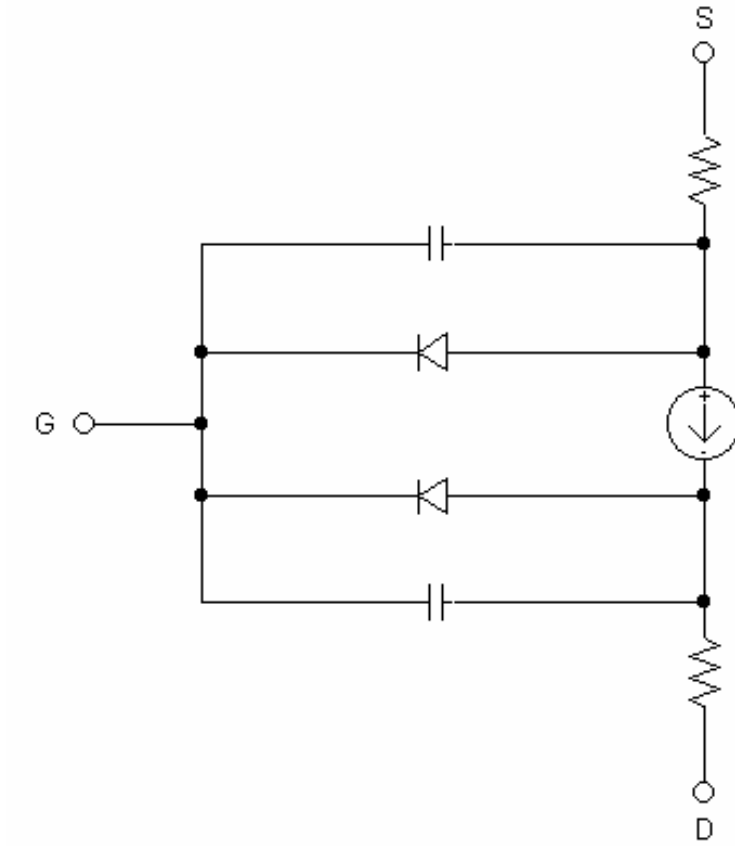


Figure 1-2 Equivalent circuit of JFET model

For a four-terminal JFET, assuming that the effect of  $V_{GSB}$  (the bottom gate to source voltage) on  $X_B$  is much less significant compared to that of  $V_{GST}$  (the top gate to source voltage) on  $X_T$ , (9) can be written as:

$$\begin{aligned}
 B_1 &= V_{PT} - V_{GST} \\
 B_2 &= V_{GST} / V_{PT}
 \end{aligned}
 \tag{1-10}$$

b) Quadratic Transfer Parameter  $\beta$

$$\beta = \frac{1}{2V_p} H \mu_p q N_A
 \tag{1-11}$$

Where  $H$ ,  $\mu_p$ ,  $N_A$  are the height of conducting channel, hole mobility, and acceptor density in the channel, respectively.

c) Subthreshold Region

$$\sqrt{I_{SDS}} = \sqrt{I_{OP}} e^{-V_{GS}V_P/2V_t} \quad 1-12$$

where  $V_t = kT/q$  is the thermal voltage and

$$I_{OP} = \frac{W}{L} \mu_p V_t \sqrt{2\pi q \epsilon_{si} V_t N_A} \quad 1-13$$

$\epsilon_{si}$  is the dielectric permittivity.

d) Transition Region

$$\begin{aligned} \sqrt{I_{SDS}} = & \left\{ \sqrt{I_{SDO}} \left[ 1 - \frac{V_{B1}}{V_P} \right] \left[ 1 - \frac{2V_{GS} - V_{B1}}{V_{B12}} \right] \left[ \frac{V_{GS} - V_{B2}}{V_{B12}} \right]^2 \right. \\ & + \sqrt{I_{OP}} \exp \frac{V_P - V_{B2}}{2V_t} \left[ 1 - \frac{2(V_{GS} - V_{B1})}{V_{B12}} \right] \cdot \left[ \frac{V_{GS} - V_{B1}}{V_{B12}} \right]^2 \\ & \left. - \frac{\sqrt{I_{SDO}}}{V_P} (V_{GS} - V_{B1}) \left[ \frac{V_{GS} - V_{B2}}{V_{B12}} \right]^2 - \frac{\sqrt{I_{OP}}}{2V_t} \cdot \exp \frac{V_P - V_{B2}}{2V_t} (V_{GS} - V_{B1}) \left[ \frac{V_{GS} - V_{B1}}{V_{B12}} \right]^2 \right\} \end{aligned} \quad 1-14$$

Wong's model has made considerable improvements over the Taki's model, but it is far from perfect. The top pinch-off voltage  $V_{PT}$ , which is the top gate-to-source voltage that causes the channel to cutoff, was derived under the condition  $V_{GSB}$  is fixed. On the other hand, the bottom pinch-off voltage  $V_{PB}$  was derived under the condition that  $V_{GST}$  is fixed. Since only a single pinch-off voltage is used in the JFET model, selecting  $V_{PT}$  or  $V_{PB}$  as the pinch-off voltage is crucial because it can give rise to a large discrepancy in the current-voltage characteristics, especially

for JFETs having a relatively small difference in the top and bottom gate doping concentrations [2].

In 1996, Liou and Yue [2] extended Wong's model and presented a more accurate JFET model for four-terminal operations. The main difference between Wong and Liou-Yue models is the equations for  $B_1$  and  $B_2$ :

$$\begin{aligned} B_1 &= [1/(V_{PT} - V_{GST}) + 1/(V_{PB} - V_{GSB})]^{-1} \\ B_2 &= V_{GST}/V_{PT} + V_{GSB}/V_{PB} \end{aligned} \quad 1-15$$

where

$$V_{PT} = [h\sqrt{\frac{q}{2\varepsilon_s K_1}} - \sqrt{\frac{K_2}{K_1}}(\varphi_B + V_{GSB})]^2 - \varphi_T \quad 1-16$$

$$V_{PB} = [h\sqrt{\frac{q}{2\varepsilon_s K_2}} - \sqrt{\frac{K_1}{K_2}}(\varphi_T + V_{GST})]^2 - \varphi_B \quad 1-17$$

This model seems to be the best JFET model to-date because

- 1) It inherited the merits of Taki's work, so the model is very compact yet combines the linear and saturation regions with a single expression.
- 2) It has taken into account the subthreshold current, and provides a smooth transition between the quadratic and subthreshold region using the Hermite interpolation method.
- 3) It has physical expressions for BETA and VTO.
- 4) It enables one to properly describe the 4-terminal JFET behavior.

However, the model still possesses the following limitations:

- 1) It employs the Gradual Channel Approximation (GCA), and short channel effects are not fully accounted for.
- 2) When developing  $V_p$ , the model assumes that the voltage drop along the channel is linear based on the assumption that the hole distribution in the p channel is uniform.
- 3) The four-terminal modeling needs to be further improved to include the effects associated with advance JFET technology.
- 4) The model needs to be extended to other JFET topologies used in modern integrated circuits.
- 5) Temperature and scaling effects are not addressed in the model.

### **1.3 JFET Models Used in Spice**

Here we will review JFET models used in two widely used SPICE platforms: Smart SPICE by Silvaco [8] and Spectre by Cadence [9]. In-house JFET model at Philips Semiconductor [10] will also be briefly discussed.

Smart SPICE provides two DC JFET models:

- 1) The basic SPICE model (Level 1)
- 2) The modified SPICE model with gate modulation of LAMBDA (Level 2)

For linear region:

$$\text{Level 1: } I_{DS} = \beta_{\text{eff}} [2(V_p - V_{GS}) - V_{DS}] (1 + \lambda V_{DS})$$

1-18

$$\text{Level 2: } I_{DS} = \beta_{eff} V_{DS} [2(V_P - V_{GS}) - V_{DS}] \quad 1-19$$

For saturation region:

$$\text{Level 1: } I_{DS} = \beta_{eff} (V_P - V_{GS})^2 (1 + \lambda V_{DS}) \quad 1-20$$

$$\text{Level 2: } I_{DS} = \beta_{eff} (V_P - V_{GS})^2 \{1 + \lambda [V_{DS} - (V_P - V_{GS})]\} (1 + \lambda_1 V_{GS}) \quad 1-21$$

For cut-off region:

$$\text{Level 1: } I_{DS} = 0 \quad 1-22$$

$$\text{Level 2: } I_{DS} = 0 \quad 1-23$$

where

$$\beta_{eff} = \beta \frac{W_{eff}}{L_{eff}}$$

and  $\lambda_1$  is the channel length modulation.

While Smart SPICE Level 1 JFET model looks very much like the traditional SPICE model, it does make a few improvements in the following two areas:

- 1) Temperature compensation;
- 2) Geometry calculation and scaling;

SmartSPICE uses two equations to model the temperature-dependent energy bandgap  $E_g$  as follows:

$$Eg(t) = 1.16 - 7.02e^{-4} \frac{t^2}{t + 1108} \quad 1-24$$

$$Eg(t) = Eg - g_1 \frac{t^2}{t + g_2} \quad 1-25$$

$g_1$  and  $g_2$  are 1.16 and 1108 respectively. Moreover, Smart SPICE provides a simple way to account for the first-order scaling

effect. If the channel length  $L$  is specified in the element statement, then the effective channel length  $L_{eff}$  is given by

$$L_{eff} = L \cdot SCALE + LDEL \cdot SCALM$$

Here  $SCALE$  and  $SCALM$  are empirical parameters that need to be extracted from measured data. The same approach is used for the scaling of channel width  $W$ . Effects of dual gates are not considered in Smart SPICE.

JFET model used in Cadence Spectre is more sophisticated than its Smart SPICE counterpart. The equivalent circuit of JFET model is shown in Fig. 1-3, and four different levels are available in Spectre.

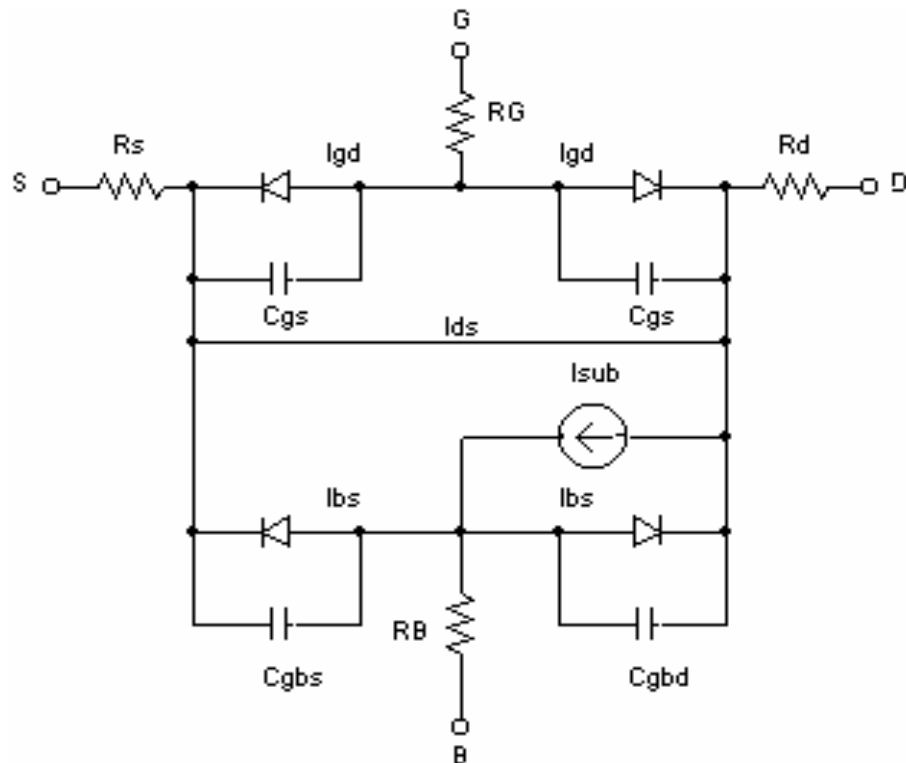


Figure 1-3 Equivalent circuit of JFET model in Cadence Spectre

a) Drain Current for the Subthreshold Region



$$I_{\text{LIMIT}} = \begin{cases} 0 & \text{for Level 1 or 4} \\ \frac{I_{\text{EXP}} I_{\text{LIMIT}}}{I_{\text{EXP}} + I_{\text{LIMIT}}} & \text{Otherwise} \end{cases} \quad 1-26$$

where

$$I_{\text{LIMIT}} = 2\beta V_t^2 \quad 1-27$$

$$I_{\text{EXP}} = (i_0) e^{V_{\text{GST}}/n_s V_t} (1 - e^{-V_{\text{DS}}/V_t}) \quad 1-28$$

b) Drain Current for the Linear Region

$$I_{\text{DS}} = \begin{cases} \beta V_{\text{GST}}^2 (1 + \lambda V_{\text{DS}}) & \text{Level=1} \\ \beta V_{\text{GST}}^{\text{np}} \tanh\left(\frac{\alpha V_{\text{DS}}}{V_{\text{GST}}}\right) (1 + \lambda V_{\text{DS}}) & \text{Level=2} \\ \beta_4 V_{\text{GST}}^{\text{np}} \tanh\left(\frac{\alpha V_{\text{DS}}}{V_{\text{GST}}}\right) (1 + \lambda V_{\text{DS}}) & \text{Level=3} \\ \beta V_{\text{GST}}^2 [1 - \lambda (V_{\text{DS}} - V_{\text{GST}}) C_{\text{lm}}] & \text{Level=4} \end{cases} \quad 1-29$$

where

$$\beta_4 = \beta \left( \frac{V_{\text{to}} + V_{\text{top}}}{V_{\text{to4}} + V_{\text{top}}} \right) \quad 1-30$$

$$\lambda = \lambda (1 + \lambda V_{\text{GST}}) \quad 1-31$$

c) Drain Current for the Saturation Region

$$I_{\text{DS}} = \begin{cases} \beta V_{\text{GST}}^2 (1 + \lambda V_{\text{DS}}) & \text{Level=1} \\ \beta V_{\text{GST}}^{\text{np}} \tanh\left(\frac{\alpha V_{\text{DS}}}{V_{\text{GST}}}\right) (1 + \lambda V_{\text{DS}}) & \text{Level=2} \\ \beta_4 V_{\text{GST}}^{\text{np}} \tanh\left(\frac{\alpha V_{\text{DS}}}{V_{\text{GST}}}\right) (1 + \lambda V_{\text{DS}}) & \text{Level=3} \\ \beta V_{\text{GST}}^2 [1 - \lambda (V_{\text{DS}} - V_{\text{GST}}) C_{\text{lm}}] & \text{Level=4} \end{cases} \quad 1-32$$

where

$$C_{lm} = \begin{cases} \frac{V_{GST}}{V_{to}} & \text{for } V_{GS} \leq 0 \\ 1 + \lambda V_{GS} & \text{for } V_{GS} \geq 0 \end{cases} \quad 1-33$$

d) Substrate Leakage Current

$$I_{sub} = I_{DS}(V_{DS} - V_{DSAT}) \exp\left[\frac{-b}{V_{DS} - V_{DSAT}}\right] \quad 1-34$$

e) Gate Leakage Current

$$I_{gs(gd)} = \begin{cases} i_s \left( e^{\frac{V_{gs(gd)}}{nV_t}} - 1 \right) \\ I_{offset} + G_{Expt} V_{gs(gd)} \end{cases} \quad 1-35$$

here

$$V_t = \frac{kT}{q} \quad 1-36$$

$V_t$  is the thermal voltage

$$V_{Expt} = nV_t \ln\left[1 + \frac{i_{melt}}{i_s}\right] \quad 1-37$$

is the forward explosion voltage,

$$G_{Expt} = \frac{(i_{melt} + i_s)}{nV_t} \quad 1-38$$

is the conductance at  $V_{Expt}$ , and

$$I_{offset} = i_{melt} - V_{Expt} G_{Expt} \quad 1-39$$

is the current linearly extrapolated to  $V = 0$  from  $V_{Expt}$ .

Undoubtedly, a great deal of options and flexibilities has been implemented into JFET models in Cadence Spectre. Unfortunately, most of these additions are somewhat cosmetic and do not address properly the critical physics underlying modern JFETs.

Finally, Philips Semiconductor has also developed a long-channel JFET model to describe the drift region of Power MOS devices [10].

The model is less comprehensive and refined than the Spectre counterpart.

#### **1.4 Conclusions**

The development of several existing JFETs was presented, and JFET models used in SPICE platforms were also reviewed and discussed. While JFETs have continuously been used in various applications, modeling of JFET has not kept pace with the advance of JFET technology. The latest JFET model reported in the literature dated back to 1996, and much work is urgently needed to bring JFET model to a level similar to that of MOS models.

## **REFERENCES**

- [1] Juin J. Liou, Advanced Semiconductor Device Physics and Modeling, Artech House, Inc. 1994 pp: 185~224
- [2] Juin J. Liou and Y. Yue, An Improved Model for Four-Terminal Junction Field-Effect Transistors. IEEE Transactions on Electron Devices, Vol.43.no.8, August 1996
- [3] Waisum W. Wong and Juin J. Liou, JFET Circuit Simulation Using SPICE Implemented with an improved Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.13, No.1 January 1994
- [4] Waisum W. Wong, A Junction Field-Effect Transistor (JFET): Theoretical Analysis and SPICE Modeling. PhD Degree Dissertation, University of Central Florida, 1992
- [5] Jianzhong Xu, JFET Device Simulation and Modeling. Master Degree Dissertation, University of Central Florida, 1996
- [6] Robert F. Pierret, Field Effect Devices, Modular Series on Solid State Devices, Volume IV, Addison-Wesley Publishing Company, 1983
- [7] Paul Van Halen, A Physical SPICE-Compatible Dual-Gate JFET Model, Circuits and Systems, 1990. Proceedings of the 33rd Midwest Symposium, 1991
- [8] SmartSPICE/UTMOST III Modeling Manuals II. Silvaco International, 2000. pp.179-197
- [9] Spectre Manual, Cadence System, 2001.

[10] The MOS model, level 3002 (Used for DMOS) Philips Semiconductor, June 2002.

## **CHAPTER TWO: NEW MODEL FOR FOUR-TERMINAL JUNCTION FIELD-EFFECT TRANSISTORS**

### ***2.1 Introduction***

The junction field-effect transistor (JFET), first analyzed by Shockley in 1952 as a voltage-controlled resistor, has been used in a small but steady portion of the semiconductor market. Nowadays, JFETs are experiencing an increasing interest as an input pair for operational amplifiers, thanks to their lower noise figure and input bias current when compared to CMOS and BJTs, respectively. They are also used in a wide variety of applications, such as low-level audio pre-amplifiers, optical networking, photodiode/detection, and data acquisition, to name a few. Additionally, JFETs offer good radiation tolerance [1], high cutoff frequency [2], and depletion-mode operation among other desirable features [3-4].

Unlike MOS and bipolar transistors that have received significant modeling attention and have well-developed compact models, JFET modeling has largely been overlooked in the past 30 years. Only a handful of JFET models are reported in the literature, which includes the early Berkeley SPICE model [5], which is based on the Schichman-Hodges model, Taki's empirical model [6], which is based on the tanh function, and a few four-terminal JFET models

[7-8]. None of these models are sufficiently comprehensive to include many important physical effects associated with modern JFETs operated under various bias conditions. Furthermore, these models are prone to discontinuities between regions of operation and consequently induce inaccuracy and convergence issues in simulations. Recently, McAndrew [9] developed a fairly comprehensive and accurate JFET model based on the concept of a variable resistor, but the model was intended for three-terminal operations. Thus the availability of a more comprehensive four-terminal JFET model would be both timely and desirable.

In this chapter, we will in Section 2 develop a unified DC equation that models the linear, saturation and cut-off biasing conditions and demonstrate its high order of continuity. In essence, we will extend the model in [9] to include the additional back-gate effect and to enhance the framework to make the model more compact and robust. This is followed by the modeling of the AC and leakage components in Section 3 and 4. The model implementation into designers' framework will be addressed and comparisons of the present model with existing models and data measured at Texas Instruments will be discussed in Section 5. Finally, conclusions are given in Section 6.

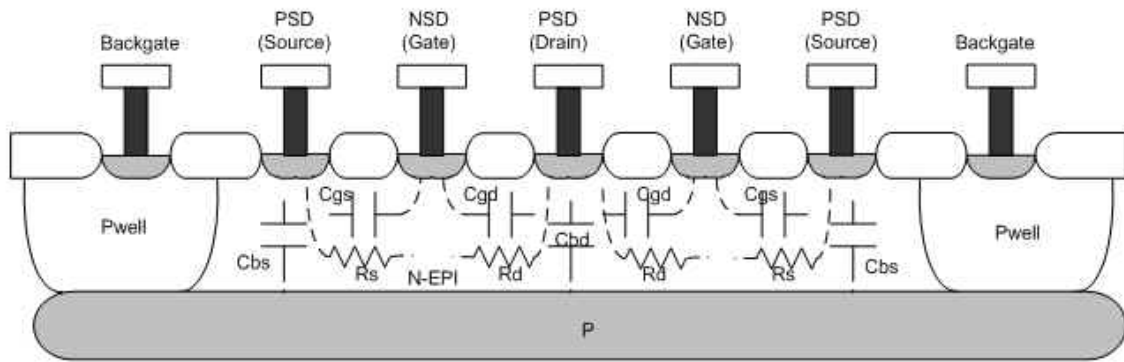


Figure 2-1 Schematic of a typical CMOS process-based n-channel JFET structure



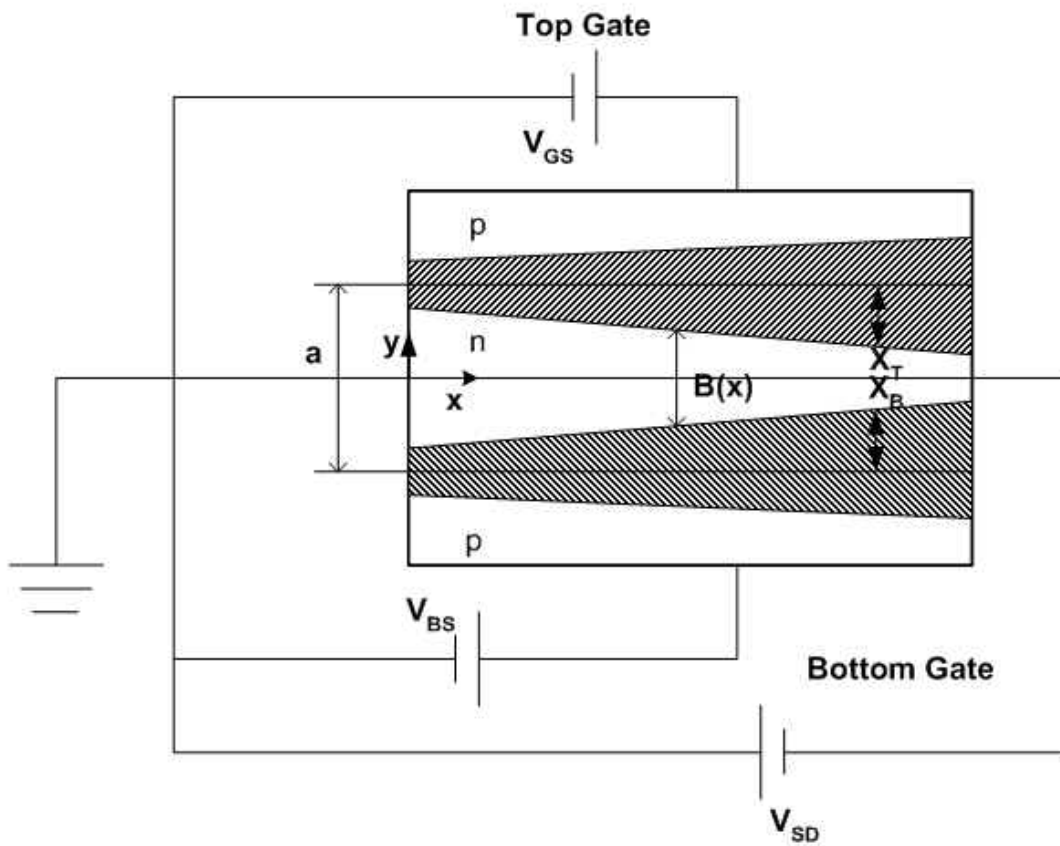


Figure 2-2 Simplified n-channel JFET structure for a single JFET cell, where the shaded regions denote the top- and bottom-gate space-charge regions

## **2.2 DC Modeling**

A four-terminal, n-channel JFET will be considered in the study, but the approach applies to p-channel JFETs as well. Fig. 2-1 shows the cross section of a typical CMOS process-based, n-channel JFET having independent top and bottom gates. The simplified one-dimensional structure considering only a single JFET cell is given in Fig. 2-2, depicting a conducting channel sandwiched between two space-charge regions (shaded regions in Fig. 2-2) associated with the top and bottom gates. Device dimensions which are critical to the JFET behavior are the channel length  $L$ , channel width  $Z$ , channel thickness  $a$ , top space-charge-region thickness  $X_T$ , and bottom space-charge-region thickness  $X_B$ .

The steady-state current-voltage characteristics of a JFET can be categorized into three regions: the linear region, where the drain-to-source voltage  $V_{DS}$  is relatively small and the drain current  $I_D$  is proportional nearly linearly to  $V_{DS}$ ; the saturation region, where  $V_{DS}$  is relatively large and  $I_D$  is a weak function of  $V_{DS}$ ; and the subthreshold region, where the entire channel is cutoff and  $I_D$  is an exponential function of the gate voltage.

### 2.2.1 Linear and Saturation Regions

We now begin to derive analytical equations to describe the current-voltage characteristics of the JFET cell shown in Fig. 2-2. The one-dimensional Poisson equation in the  $y$  direction (vertical direction) in the channel is given by

$$-\frac{\partial^2 V}{\partial y^2} = \frac{dE_y}{dy} = \frac{\rho(y)}{\epsilon_s} = \frac{q \cdot N_D}{\epsilon_s} \quad 2-1$$

Where  $N_D$  is the averaged donor doping density in the channel layer, the extraction of which will be discussed later,  $V$  is the electrostatic potential,  $E_y$  is the electric field in the  $y$  direction,  $\rho$  is the space-charge density, and  $\epsilon_s$  is the dielectric permittivity. Solving (1) yields the top-gate space-charge-region thickness  $X_T$ :

$$X_T = \sqrt{K \cdot (V_{Tbi} - V_{GS} + V(x))} \quad 2-2$$

and the bottom-gate space-charge-region thickness  $X_B$ :

$$X_B = \sqrt{K \cdot (V_{Bbi} - V_{BS} + V(x))} \quad 2-3$$

where  $K = \frac{2 \cdot \epsilon}{q} \cdot \frac{1}{N_D}$ ,  $V_{Tbi}$  is the top-gate junction built-in potential,

$V_{Bbi}$  is the bottom-gate junction built-in potential, and  $V_{GS}$  and  $V_{BS}$  are top-gate and bottom-gate applied voltages, respectively. The junction built-in potentials can be expressed as

$$V_{Tbi} = V_T \cdot \ln\left(\frac{N_D \cdot N_{AT}}{n_i^2}\right) \quad 2-4$$

$$V_{Bbi} = V_T \cdot \ln\left(\frac{N_D \cdot N_{AB}}{n_i^2}\right) \quad 2-5$$

where  $V_T$  is the thermal voltage,  $n_i$  is the intrinsic free-carrier density, and  $N_{AT}$  and  $N_{AB}$  are the averaged acceptor doping densities in the top-gate and bottom-gate layers, respectively. The undepleted channel thickness  $b$  at a particular horizontal position  $x$  is

$$b(x) = a - X_T - X_B \quad 2-6$$

Thus, using the concept of drift tendency for the free-carrier transport in the undepleted channel, the drain current  $I_D$  can be expressed as

$$I_D = q \cdot N_D \cdot \mu_0 \cdot \frac{dV(x)}{dx} \cdot b(x) \cdot Z \quad 2-7$$

where  $\mu_0$  is the low-field electron mobility in the channel, and  $Z$  is the channel width.

Combining the above equations, we get

$$I_D = q \cdot Z \cdot N_D \cdot \mu_0 \cdot \frac{dV(x)}{dx} \cdot [a - \sqrt{K \cdot (V_{Tbi} - V_{GS} + V(x))} - \sqrt{K \cdot (V_{Bbi} - V_{BS} + V(x))}] \quad 2-8$$

Then integrating both sides of (8) with respect to  $x$  yields

$$I_D = M \cdot \int_0^{V_{DS}} [a - \sqrt{K \cdot (V_{Tbi} - V_{GS} + V(x))} - \sqrt{K \cdot (V_{Bbi} - V_{BS} + V(x))}] dV(x) \quad 2-9$$

$$M = \frac{q \cdot Z \cdot N_D \cdot \mu_0}{L}$$

Carrying out the integration, we have

$$I_D = M \cdot \left\{ a \cdot V_{DS} - \frac{2}{3} \cdot \sqrt{K} \cdot [(V_{GTbi} + V_{DS})^{\frac{3}{2}} - V_{GTbi}^{\frac{3}{2}}] - \frac{2}{3} \cdot \sqrt{K} \cdot [(V_{GBbi} + V_{DS})^{\frac{3}{2}} - V_{GBbi}^{\frac{3}{2}}] \right\}$$

2-10

where

$$V_{GTbi} = V_{Tbi} - V_{GS} \quad , \quad V_{GBbi} = V_{Bbi} - V_{BS}$$

This expression describes the JFET current-voltage characteristics in the linear region having independent top and bottom gate biases.

As  $V_{DS}$  is increased, the space-charge-region thicknesses associated with the top and bottom gates increase toward the drain region, and finally the channel near the drain region ( $y = L$ ) is pinched off. At this point, the current can no longer increase nearly linearly with  $V_{DS}$ . It is called current saturation, and  $V_{DS}$  causing the channel pinch-off at  $y = L$  is called the drain saturation voltage  $V_{sat}$ . Note that (10) is only valid for  $V_{DS}$  below  $V_{sat}$ .

The drain saturation voltage can be derived as the drain voltage where  $\partial I_D / \partial V_{DS} = 0$  [6]:

$$V_{sat} = \left\{ -V_{Tbi} \cdot V_{PB} + V_{GS} \cdot V_{PB} + V_{PT} \cdot V_{PB} + V_{PT} \cdot \frac{V_{PB}^{\frac{1}{2}}}{V_{PT} - V_{PB}} \cdot [-2 \cdot V_{PT} \cdot V_{PB}^{\frac{1}{2}} + 2 \cdot (V_{Tbi} \cdot V_{PB} \cdot V_{PT} - V_{GS} \cdot V_{PB} \cdot V_{PT} - V_{PT} \cdot V_{Bbi} \cdot V_{PB} + V_{PT} \cdot V_{BS} \cdot V_{PB} - V_{Tbi} \cdot V_{PB}^2 + V_{GS} \cdot V_{PB}^2 + V_{PT} \cdot V_{PB}^2 + V_{Bbi} \cdot V_{PB}^2 - V_{BS} \cdot V_{PB}^2)^{\frac{1}{2}}] + V_{PT} \cdot V_{Bbi} - V_{PT} \cdot V_{BS} \right\} / (-V_{PT} + V_{PB})$$

2-11

where

$$V_{PB} = \frac{q \cdot a^2}{2 \cdot \epsilon} \cdot \frac{N_D \cdot (N_D + N_{AB})}{N_{AB}}, \quad V_{PT} = \frac{q \cdot a^2}{2 \cdot \epsilon} \cdot \frac{N_D \cdot (N_D + N_{AT})}{N_{AT}}$$

Thus, for the saturation operation ( $V_D > V_{sat}$ ), (10) is still applicable but  $V_D$  in (10) needs to be replaced with  $V_{sat}$ . This will give rise to a constant drain current versus the drain voltage.

As  $V_{DS}$  increases beyond  $V_{sat}$ , however, the pinch-off point moves toward the source region, a larger voltage drop appears across the pinch-off region, and the drain current increases slightly with increasing  $V_{DS}$ . This effect, called the channel-length modulation, can be modeled by including the channel-length modulation coefficient  $\lambda$  in the drain current equation in (10).

Thus, the drain current in the saturation region becomes

$$I_D = M \cdot \left\{ a \cdot V_{sat} - \frac{2}{3} \cdot \sqrt{K} \cdot [(V_{GTbi} + V_{sat})^{\frac{3}{2}} - V_{GTbi}^{\frac{3}{2}}] - \frac{2}{3} \cdot \sqrt{K} \cdot [(V_{GBbi} + V_{sat})^{\frac{3}{2}} - V_{GBbi}^{\frac{3}{2}}] \right\} \cdot (1 - \lambda \cdot V_{DS})$$

2-12

The piecewise model for the linear and saturation regions discussed above (Eqs. (10) and (12)), however, often causes abrupt drain current changes at the crossover point from the linear to saturation region, thereby leading to discontinuities in the first and second order derivatives in the vicinity of the transition region and consequently possible divergence in simulations.

To resolve this problem, we follow an approach in [8] and use a single equation for both the linear and saturation regions. This

is done by using (12) and replacing  $V_{sat}$  and  $V_{DS}$  in (12) with the effective drain voltage  $V_{Def}$ :

$$V_{Def} = V_{sat} \cdot \left\{ 1 - \frac{\log[1 + \exp(B \cdot (1 - \frac{V_{DS}}{V_{sat}}))] }{\log(1 + \exp(B))} \right\} \quad 2-13$$

Here B is the smoothing coefficient. The resulting equation is

$$I_D = M \cdot \left\{ a \cdot V_{Def} - \frac{2}{3} \cdot \sqrt{K} \cdot [(V_{GTbi} + V_{Def})^{\frac{3}{2}} - V_{GTbi}^{\frac{3}{2}}] - \frac{2}{3} \cdot \sqrt{K} \cdot [(V_{GBbi} + V_{Def})^{\frac{3}{2}} - V_{GBbi}^{\frac{3}{2}}] \right\} \cdot (1 - \lambda \cdot V_{DS}) \quad 2-14$$

### 2.2.2 Subthreshold Region

For a given  $V_{DS}$  and sufficiently large top and bottom gate voltages, the entire channel can become the space-charge region, and the JFET operates in the so-called subthreshold region. The drain current in such a region depends exponentially on the gate voltage. The subthreshold operation is very important in analog JFET circuits [9].

To obtain a single expression for the above-threshold and subthreshold drain currents, we propose to replace the top and bottom gate voltages  $V_{GS}$  and  $V_{BS}$  in (14) with the following effective gate voltages  $V_{GSeff}$  and  $V_{BSeff}$ . The expression has the form of

$$I_{DS} = I_D(V_{Def}, V_{GSeff}, V_{BSeff}) \quad 2-15$$

where

$$V_{GS_{eff}} = \frac{n_T \cdot V_T \cdot \ln(1 + \exp(\frac{1}{V_T} \cdot \frac{V_{GS} - V_{pT}}{n_T}))}{1 + M_T \cdot \exp(-\frac{1}{V_T} \cdot \frac{V_{GS} - V_{pT} - V_{offT}}{n_T})} + V_{pT} \quad 2-16$$

$$V_{BS_{eff}} = \frac{n_B \cdot V_T \cdot \ln(1 + \exp(\frac{1}{V_T} \cdot \frac{V_{BS} - V_{pB}}{n_B}))}{1 + M_B \cdot \exp(-\frac{1}{V_T} \cdot \frac{V_{BS} - V_{pB} - V_{offB}}{n_B})} + V_{pB} \quad 2-17$$

where  $I_{DS}$  is the comprehensive and single expression for the 4-terminal JFET's drain current covering both the above-threshold behavior, including the linear and saturation regions, and the subthreshold behavior,  $I_D$  is the drain current in (14),  $V_p$  is the pinch-off voltage,  $n$  and  $M$  are swing factors, and  $V_{off}$  is the offset voltage adjusting  $V_p$ .

To demonstrate the improvement this work provided, a comparison of the present and existing JFET dc models with respect to the compactness, continuity, comprehensiveness, and number of JFET terminals is given in Table 1.



Table 1 Comparison of the present and existing JFET dc models

	<b>McAndrew [7]</b>	<b>Van Halen [6]</b>	<b>SPICE [3]</b>	<b>SPECTRE [12]</b>	<b>Proposed Model</b>
Compactness	Yes	No	Yes	Yes	Yes
One-piece model	Yes	No	No	No	Yes
Continuity	Yes	No	No	No	Yes
Comprehensiveness	Yes	No sub-threshold region	No sub-threshold region	Yes	Yes
Four-terminal	No	Yes	No	Yes	Yes

### 2.3 Parasitic Components Modeling

The JFET's parasitic capacitances and resistances are schematically illustrated in Fig. 2-1, and a complete equivalent circuit of the JFET, including the drain current source, parasitic components, and top- and bottom-gate leakage currents is shown in Fig. 2-3.

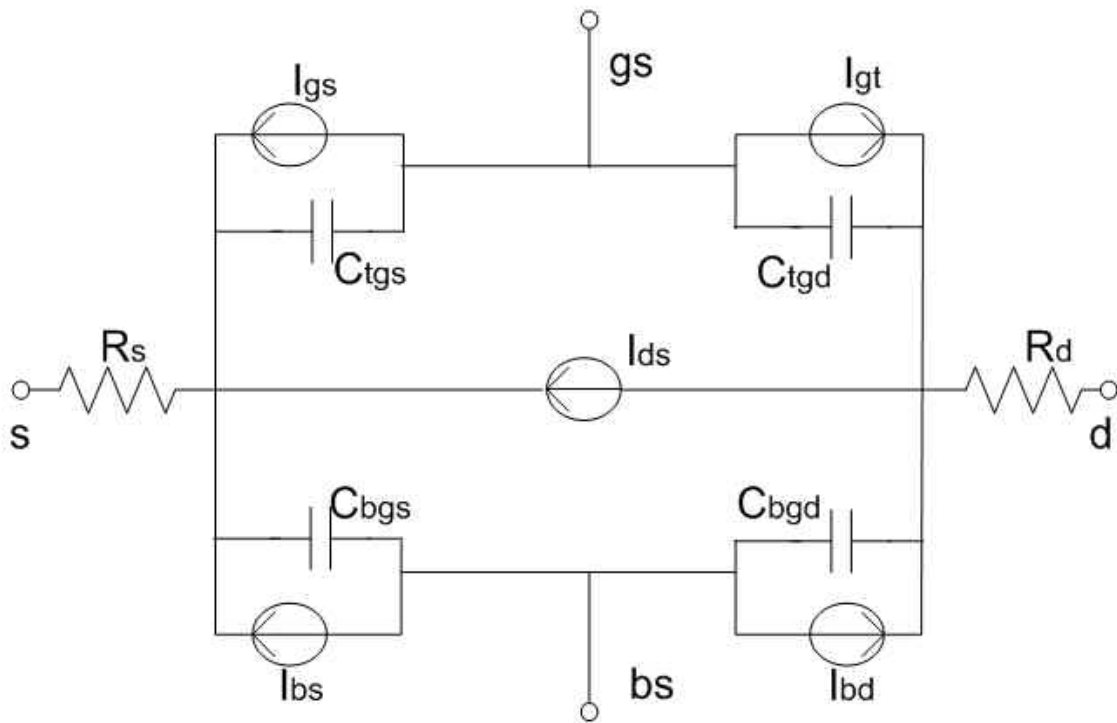


Figure 2-3 Equivalent circuit of the 4-terminal JFET including the drain current source, parasitic capacitances and resistances, and gate leakage current sources.

### 2.3.1 Junction Capacitances

As shown in Fig. 2-3, there are four junction capacitances in a JFET cell: two associated with the top gate and the others associated with the bottom gate. All these capacitances can be described with the same junction capacitance model, only the bias and area for the different capacitances are different.

The junction capacitance  $C$  (in F/cm<sup>2</sup>) of a space-charge region can be obtained from [10-11]

$$C = \epsilon \cdot \frac{d}{dV} E(0) \quad 2-18$$

where  $\epsilon$  is the dielectric permittivity of silicon and  $E(0)$  is the electric field at the metallurgical junction. To derive such a capacitance model, let us first look at the one-dimensional charge density in the space-charge region:

$$\rho(x) = q \cdot (p(x) - n(x) + N(x)) \quad 2-19$$

Where  $\rho(x)$  is the charge density, and  $N(x)$  is  $N_d(x)$  in the n-type space-charge region or  $N_a(x)$  in the p-type space-charge region. Let  $x = -x_n$  denotes the boundary of n-type space-charge region, and  $x = -x_p$  denotes the boundary of the p-type space-charge region.

Assuming nondegeneracy, the electron and hole densities are

$$n(x) = N_C \cdot \exp\left(\frac{E_{FN} - E_C}{k \cdot T}\right) \quad 2-20$$

$$p(x) = N_C \cdot \exp\left(\frac{E_V - E_{FP}}{k \cdot T}\right) \quad 2-21$$

$E_{FN}$  and  $E_{FP}$  are the quasi-Fermi levels for electrons and holes,  $N_c$  and  $N_v$  are effective density of states in the conduction band and valance band, respectively. The Poisson equation is

$$\frac{d^2}{dx^2} \psi(x) = -\frac{\rho(x)}{\epsilon} \quad 2-22$$

$$E(x) = -\frac{d}{dx} \psi(x) \quad 2-23$$

where  $\psi(x)$  is the electrostatic potential. Inserting (22) and (23) into (19), and combining with (20) and (21), we obtain

$$\frac{d^2}{dx^2} \psi(x) = -\frac{q}{\epsilon} \cdot [N_v \cdot \exp\left(\frac{-q \cdot \psi - \frac{E_g}{2} + \frac{q \cdot V}{2}}{k \cdot T}\right) - N_c \cdot \exp\left(\frac{q \cdot \psi - \frac{E_g}{2} + \frac{q \cdot V}{2}}{k \cdot T}\right) - N_{AT}]$$

for  $x < 0$  2-24

$$\frac{d^2}{dx^2} \psi(x) = -\frac{q}{\epsilon} \cdot [N_v \cdot \exp\left(\frac{-q \cdot \psi - \frac{E_g}{2} + \frac{q \cdot V}{2}}{k \cdot T}\right) - N_c \cdot \exp\left(\frac{q \cdot \psi - \frac{E_g}{2} + \frac{q \cdot V}{2}}{k \cdot T}\right) - N_D]$$

for  $x > 0$  2-25

The electric field  $E$  in the space-charge region can be derived using (24) and (25) with the following boundary conditions:

$$\frac{d}{dx} \psi(-x_n) = \frac{d}{dx} \psi(x_p) \quad 2-26$$

$$\frac{d^2}{dx^2} \psi(-x_n) = \frac{d^2}{dx^2} \psi(x_p) \quad 2-27$$

Putting the resulting  $E$  into (18) yields a physics-based but fairly complex expression for the junction capacitance [10]. However, Verilog-A requires that the displacement current passing through a capacitance be described by the charge  $Q$  in the space-

charge region. Based on the capacitance expression and some simplifications, a new charge-based model for the top-gate space-charge region is proposed as

$$Q(V) = 2 \cdot C_{j0} \cdot V_T \cdot \left\{ [X(V) - V_{Tbi}]^{0.5} - [X(V) + \frac{V_{Tbi}}{V_T} \cdot (1 - \frac{V}{V_{Tbi}})]^{0.5} \right\} \quad 2-28$$

where

$$X(V) = \frac{N_A + N_{DT}}{N_A \cdot N_{DT}} \cdot \left( \frac{N_C + N_V}{2} \right) \cdot \exp\left(\frac{V - V_{Tbi}}{2V_T}\right) + 2V_{Tbi} \quad 2-29$$

$$C_{j0} = A \cdot \sqrt{\frac{q \cdot \epsilon}{2 \cdot V_T} \cdot \frac{N_A \cdot N_{DT}}{N_A + N_{DT}}} \quad 2-30$$

The junction capacitance of the top-gate space-charge region can be obtained by taking the derivative of the charge  $Q$  with respect to the voltage:

$$C(V) = C_{j0} \cdot V_T \cdot \left\{ \frac{1}{[X(V) - V_{Tbi}]^{0.5}} \cdot \frac{d}{dv} X(V) - \frac{1}{[X(V) + \frac{V_{Tbi}}{V_T} (1 - \frac{V}{V_{Tbi}})]^{0.5}} \cdot \left[ \frac{d}{dv} X(V) - \frac{1}{V_T} \right] \right\} \quad 2-31$$

The same approach is applicable for deriving the charges and capacitances associated with the bottom gate as well, provided the parameters are changed accordingly. Note that the present capacitance has a single expression, which eliminates possible discontinuities in the first and second order derivations at the transition points. Furthermore, it has no fitting parameter and satisfies charge conservation requirement. Table 2 compares the present model with several existing models [3, 10-13].

Table 2 Comparison of the propose and previous capacitance models

	<b>McAndrew et al. [13]</b>	<b>Van Mieghem et al. [10]</b>	<b>Van Halen [11]</b>	<b>SPICE [3]</b>	<b>SPECTRE [12]</b>	<b>Proposed Model</b>
Compactness	Yes	No	Yes	Yes	Yes	Yes
Charge conservation	Yes	No	No	Yes	Yes	Yes
One-piece model	Yes	Yes	Yes	No	Yes	Yes

### 2.3.2 Gate Leakage Currents and Series Resistances

There are four gate leakage currents; two associated with the top gate and two associated with the bottom gate, as shown in Fig. 2-2. The traditional ideal diode model can be utilized to describe the JFET's gate leakage currents. For the top gate, the leakage currents have a general form of

$$I_{\text{leak}} = i_{\text{ss}} \cdot \left[ \exp\left(-\frac{V}{n \cdot V_T}\right) - 1 \right] \quad 2-32$$

$$i_{\text{ss}} = -q \cdot A \cdot n_i^2 \cdot \left( \frac{D_n}{N_D \cdot L_n} + \frac{D_p}{N_{AT} \cdot L_p} \right) \quad 2-33$$

where  $I_{\text{leak}}$  is the leakage current,  $V$  is the bias between the top gate and drain/source,  $i_{\text{ss}}$  is the reverse saturation current,  $n$  is the ideality factor,  $D_n$  and  $D_p$  are the electron and hole diffusion coefficients, respectively, and  $L_n$  and  $L_p$  are the electron and hole diffusion lengths, respectively. For the leakage currents associated with the back gate,  $N_{AT}$  is replaced with  $N_{AB}$  in (33).

For the modeling of JFET series resistances, because the gate doping is relatively high, the gate series resistance can be neglected, and only the source and drain series resistances are considered. These resistances can be derived from

$$\sigma = n \cdot q \cdot \mu_n + p \cdot q \cdot \mu_p \quad 2-34$$

$$R = \frac{L}{\sigma \cdot W \cdot t} + R_c \quad 2-35$$

## ***2.4 Model Parameter Extraction***

Since the present JFET model is developed from relevant device physics, the number of fitting parameters is minimal, and a great majority of model parameters are related to the device make-ups (dimensions, layer thicknesses, etc.) and can be readily obtained from the topology and cross section of JFET.

A few model parameters need to be extracted from measured data or empirical fitting, and their extraction methods are described below.

### 2.4.1 Channel Length Modulation Coefficient $\lambda$

The channel length modulation coefficient  $\lambda$  affects the I-V curve slope in the saturation region. As shown in Fig. 2-4, this coefficient can be determined by first extrapolating a family of I-V curves to the x-axis, which yields several intersections, and then taking the reciprocal of the averaged intersection values.

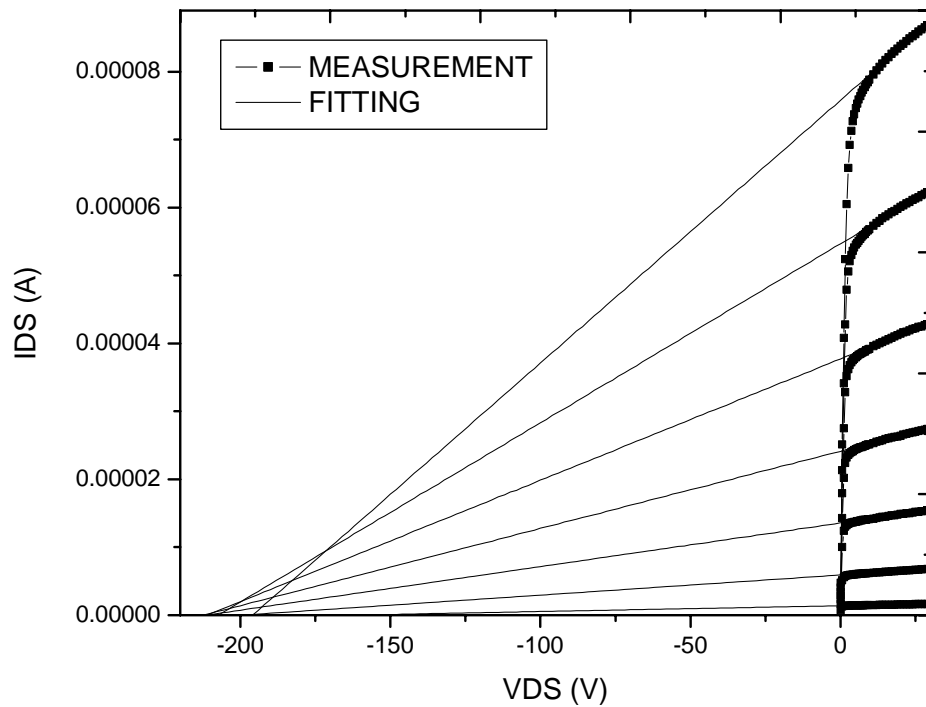


Figure 2-4 Extrapolation of I-V curves for the determination of the channel length modulation coefficient



## 2.4.2 Smoothing Coefficient B

The parameter B is used to ensure a smooth transition from the linear to saturation region. It is empirically determined and typically has a value around 1 to 2. The relationship between the effective drain voltage and drain voltage as a function of B (see Eq. (13)) is shown in Fig. 2-5(a), and the effect of B on the I-V characteristics is shown in Fig. 2-5(b).

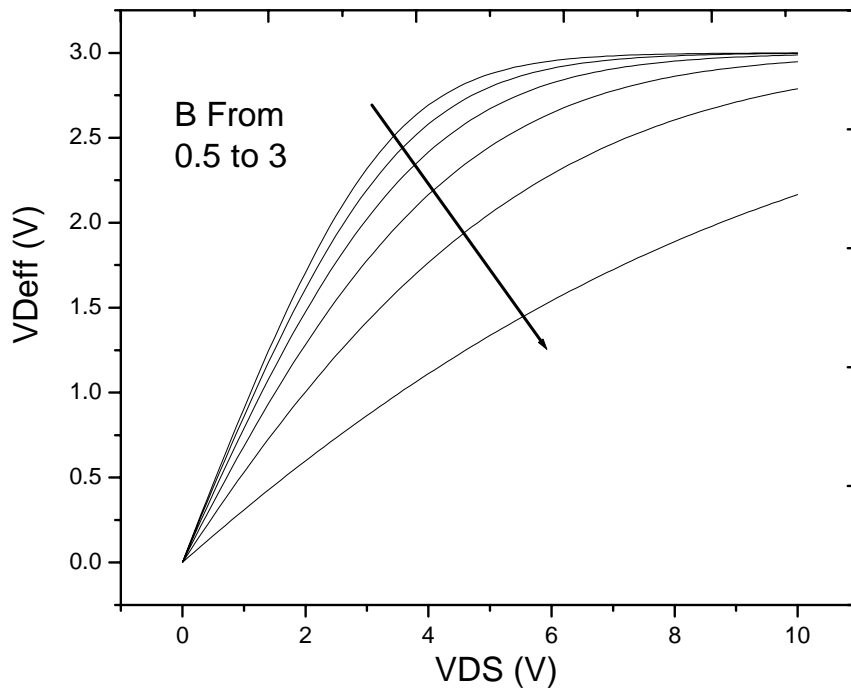


Figure 2-5(a) Effective drain voltage vs. drain voltage characteristics plotted as a function of smoothing function

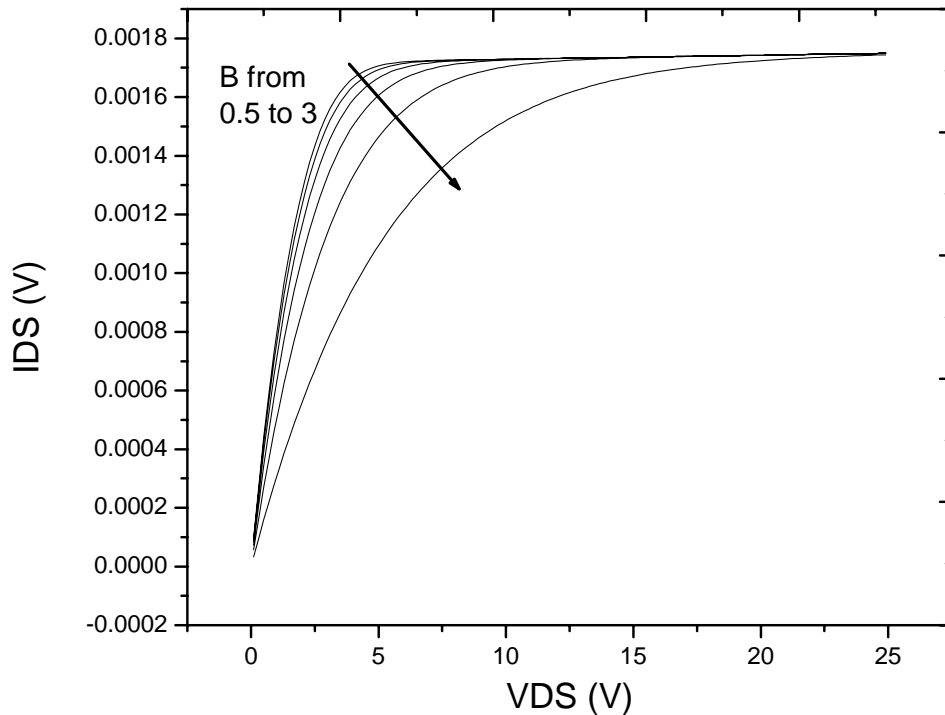


Figure 2-5(b) Effect of smoothing function on the current-voltage characteristics

### 2.4.3 Doping Density

Doping densities in the top-gate, channel and bottom-gate layers, which are not uniform, are key parameters for JFET modeling. Averaged doping densities are used in our model, which can be extracted by first fitting the non-uniform doping profile with polynomials, as shown in Fig. 2-6, carrying out the integration of the polynomials along the length of that region, and then dividing the result with the region length. This approach can be a little bit too time consuming, and our experiences suggest that

the averaged doping density can be estimated as about 80% of the peak value of the doping density.

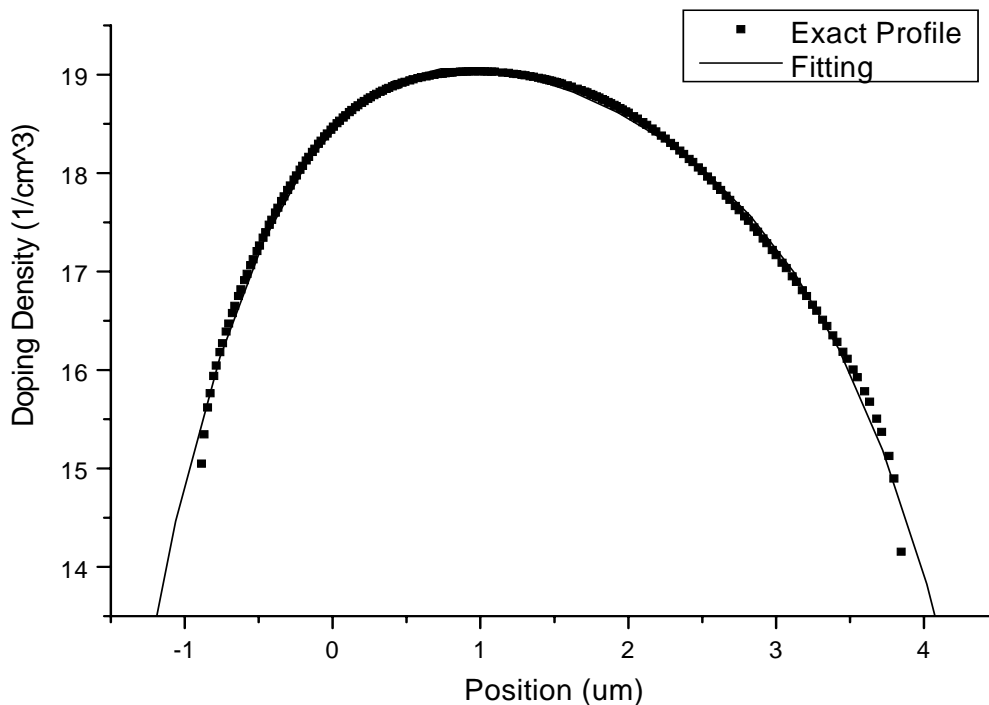


Figure 2-6 Exact and fitted doping profiles for the determination of the averaged doping density

### **2.5 Model Implementation and Results**

The preceding sections have outlined the development of a compact, physics-based, and comprehensive model for independent top- and bottom-gate JFETs. We have implemented the model equations into Cadence Spectre using a description language called Verilog-A.

To verify the model developed, we consider a CMOS process-based, n-channel JFET technology used at Texas Instruments. All the parameter values extracted and used for model calculations are listed in Table 3.

Table 3 Parameters used in the JFET model calculations

$\lambda = 7.898 \times 10^{-4} \text{ 1/V}$	$B = 1.2$	$\epsilon = 11.8 \times 8.85 \times 10^{-14}$	$Q = 1.6 \times 10^{-19} \text{ C}$
$N_{AT} = 6 \times 10^{19} \text{ cm}^{-3}$	$N_D = 3 \times 10^{16} \text{ cm}^{-3}$	$N_{AB} = 3 \times 10^{18} \text{ cm}^{-3}$	$n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$
$a = 0.9 \text{ }\mu\text{m}$	$k = 1.38 \times 10^{-23} \text{ J/K}$	$T = 300 \text{ K}$	$\mu_0 = 650 \text{ cm}^2 \text{ V/s}$
$L = 27 \text{ }\mu\text{m}$	$Z = 90 \text{ }\mu\text{m}$	$n_T = 9.5$	$M_T = 0.005$
$V_{offT} = 2 \text{ V}$	$V_{pT} = -10.516 \text{ V}$	$n_B = 24.5$	$M_B = 0.045$
$V_{offB} = 0 \text{ V}$	$V_{pB} = -4.956 \text{ V}$		

Fig. 2-7(a) compares the JFET current-voltage characteristics calculated from the model and obtained from measurements. Comparison of I-V characteristics simulated from SPICE JFET model and obtained from measurements is illustrated in Fig. 2-7(b). An improved accuracy of the present JFET model is demonstrated. To examine the continuity of the I-V curves, the first and second derivatives of the drain current with respect to the drain voltage are also calculated and presented in Figs. 2-8(a) and (b), respectively. The results of SPICE JFET model are also included in the figures. Clearly, the present model offers much improved smoothness over the conventional model on the I-V characteristics. Fig. 2-9(a) shows the calculated and measured above-threshold and subthreshold behavior of the JFET, and Fig. 2-9(b) compares the

results obtained from SPICE model and measurements. Again, the present model demonstrates a better accuracy than the existing model. To illustrate the model capability in four-terminal operations, we have shown in Fig. 2-10 calculated and measured above-threshold and subthreshold behavior of the JFET biased at a wide range of the top-gate voltages and two different bottom-gate voltages.

The capacitance-voltage characteristics are shown in Fig.2- 11. Here, the top-gate to source junction capacitance is considered, and the present model is compared against several existing models. The results indicate that the present model predicts a physically sound junction capacitance which peaks just before the junction built-in voltage (i.e., 0.95 V) and decreases quickly toward zero as the voltage approaches the built-in voltage (i.e., where the space-charge region vanishes). Device simulation using Silvaco software tool has been performed to examine the accuracy of the model up to a relatively small forward voltage (i.e., before the build-in potential). Furthermore, the present charge-based model satisfies the condition of charge conservation (i.e., total charge in the space-charge region approaches zero as the voltage is approaching the built-in voltage), as evidenced by the results in Fig. 2-12.

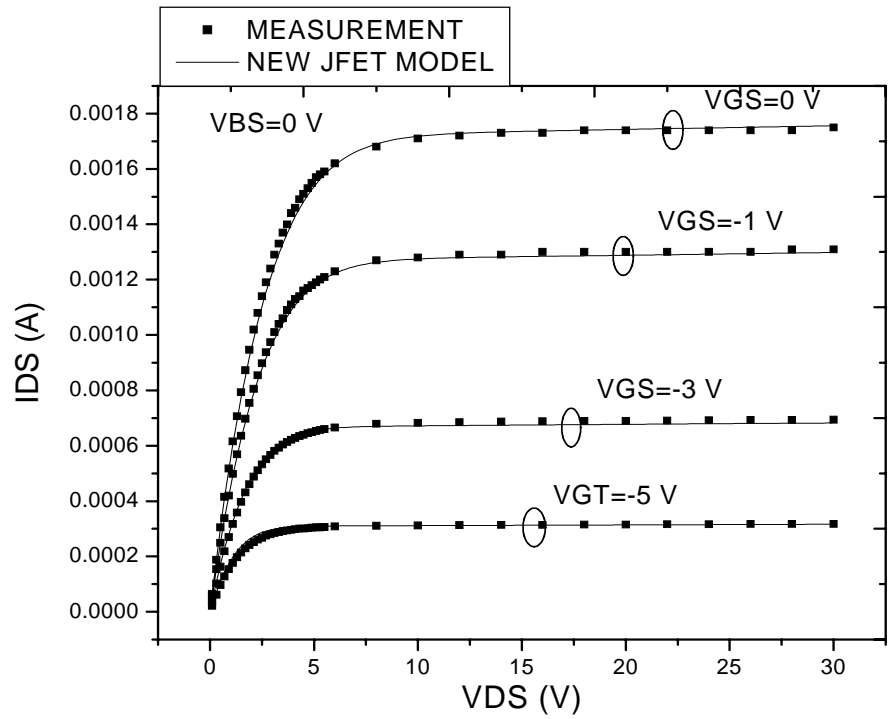


Figure 2-7(a) JFET current-voltage characteristics calculated from the present model and obtained from measurements.

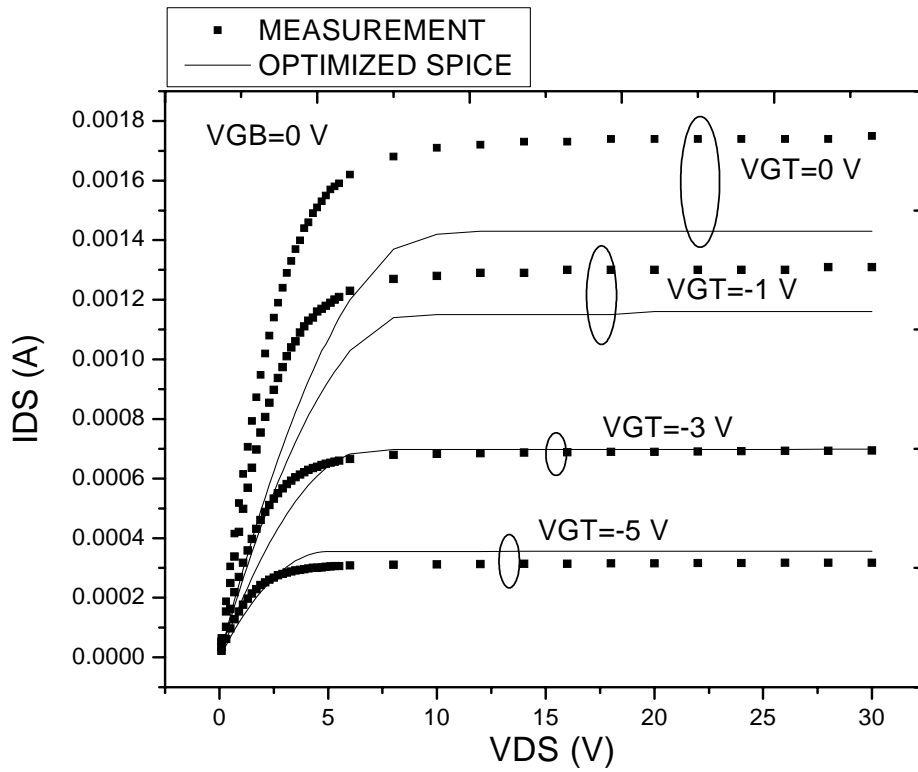


Figure 2-7(b) I-V characteristics obtained from SPICE JFET model and measurements

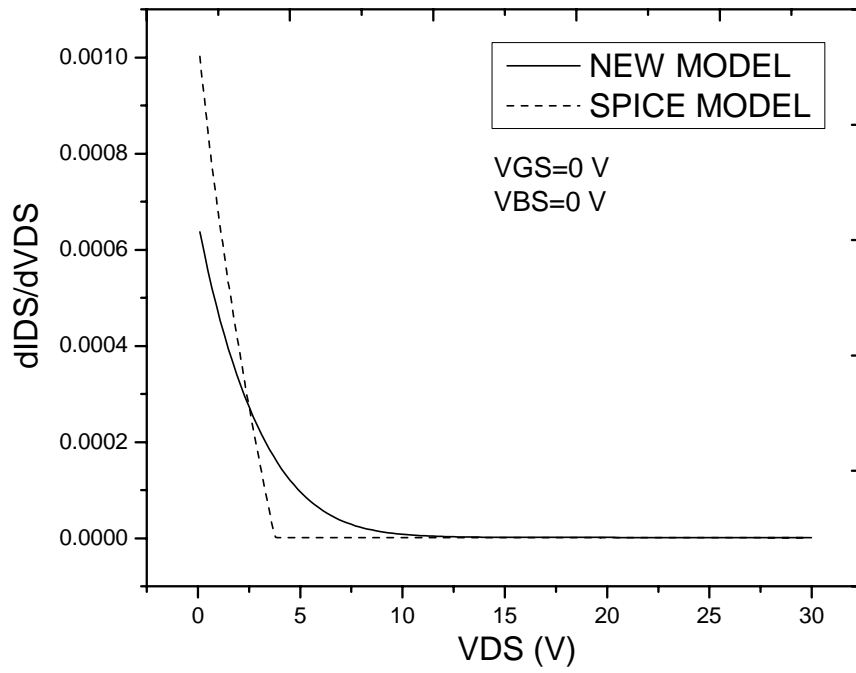


Figure 2-8(a) First derivative of drain current with respect to drain voltage obtained from the present and SPICE models



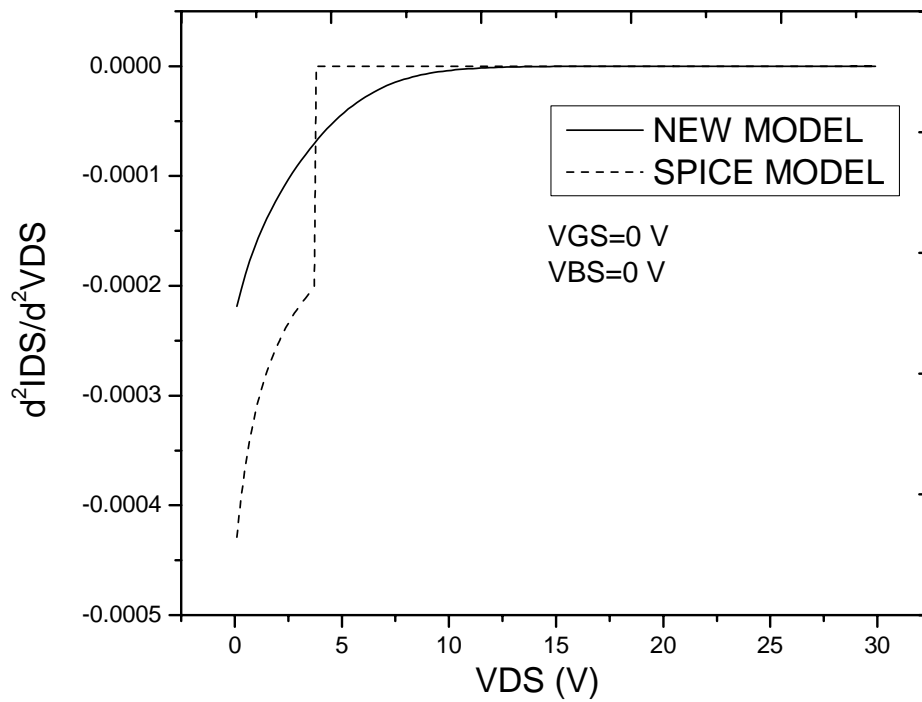


Figure 2-8(b) Second derivative of drain current with respect to drain voltage obtained from the present and SPICE models

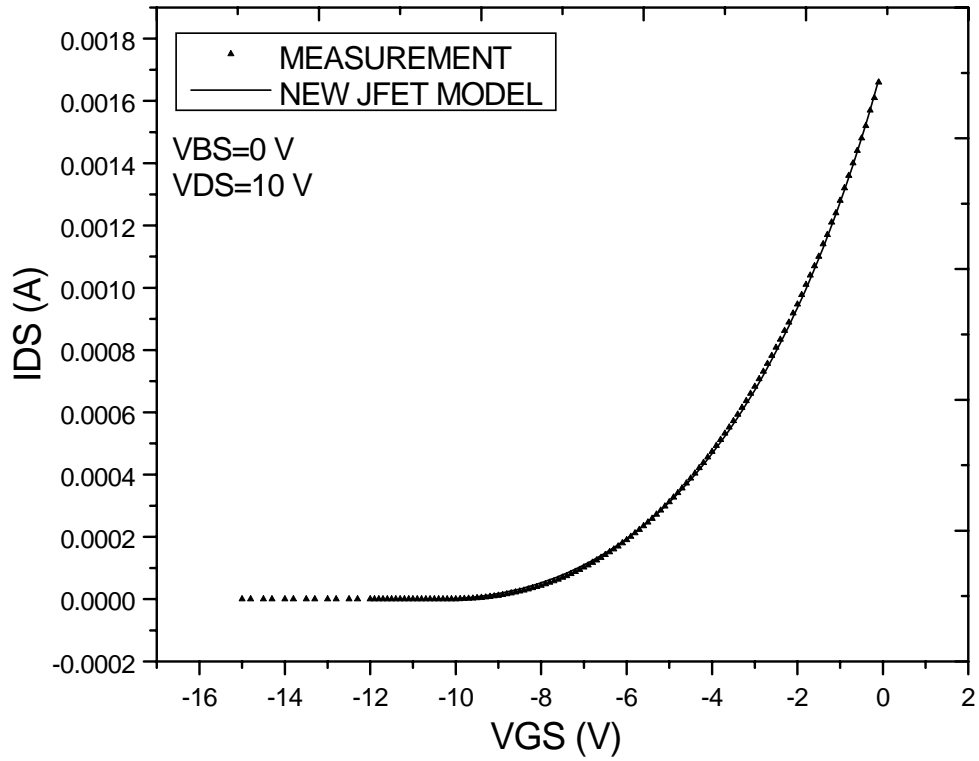


Figure 2-9(a) Above-threshold and subthreshold I-V characteristics calculated from the present model and obtained from measurements.

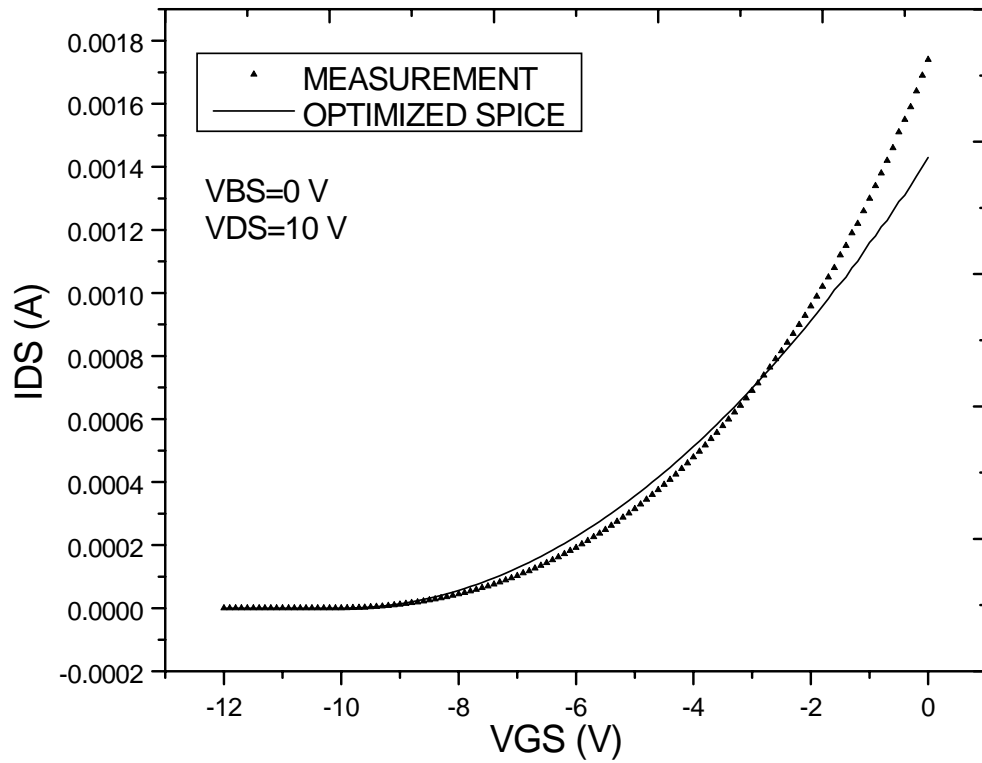


Figure 2-9(b) Above-threshold and subthreshold I-V characteristics calculated from the SPICE model and obtained from measurements.

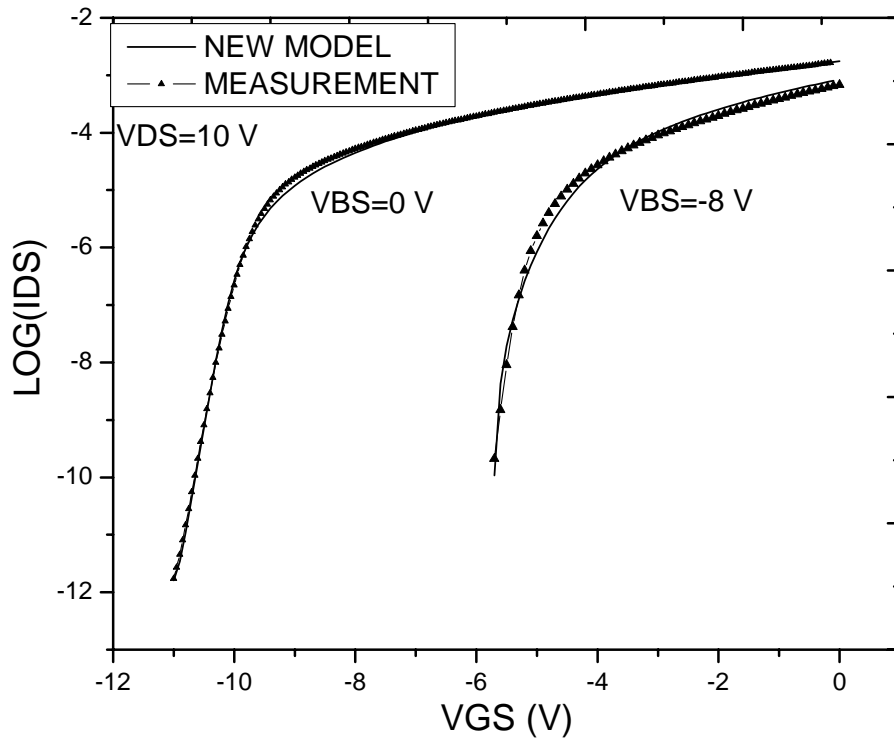


Figure 2-10 Above-threshold and subthreshold I-V characteristics for a wide range of the top-gate voltages and two different bottom-gate voltages calculated from the present model and obtained from measurements.

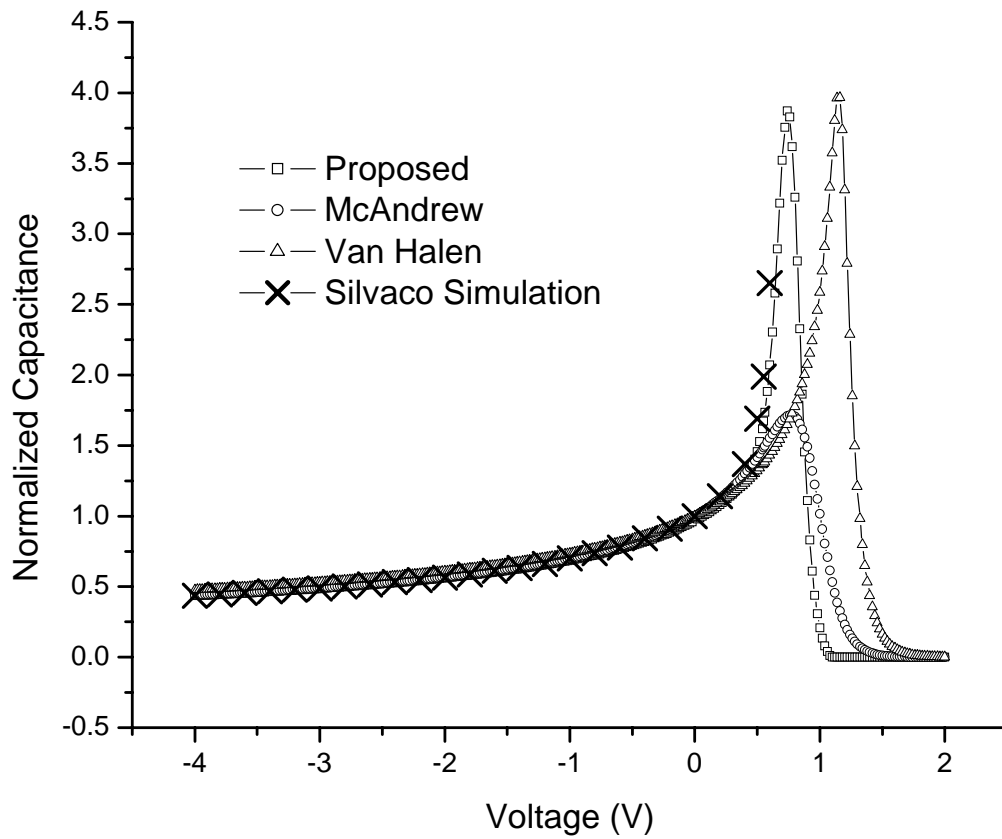


Figure 2-11 Comparison of normalized C-V curves obtained from the present model, previous models, and Silvaco Atlas simulation. The junction built-in potential is 0.95 V.

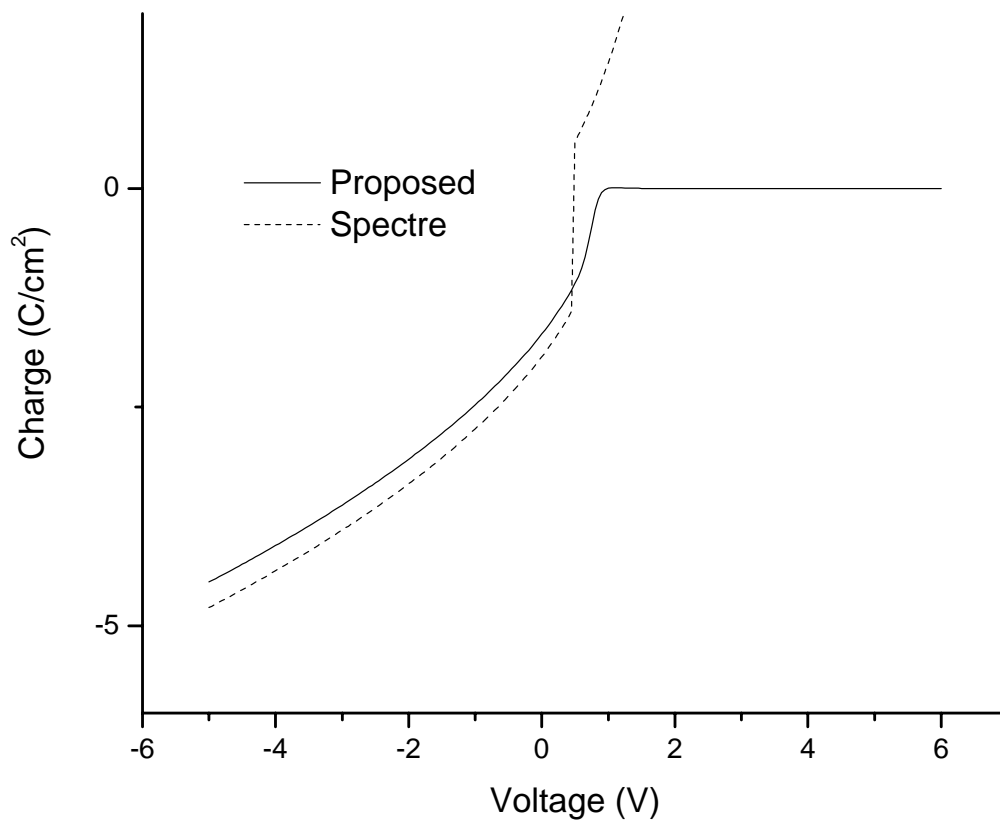


Figure 2-12 Total charge in the space-charge region calculated from the present model and model in Spectre.

## 2.6 Conclusions

Junction field-effect transistor (JFET) is a versatile device for various applications because of its two independent gates and low noise characteristics. However, JFET modeling has not received a great deal of attention in the past. An updated, comprehensive, and compact 4-terminal JFET model has been presented in this work. Issues such as current-voltage continuity, subthreshold behavior, four-terminal operations, and reduction of fitting parameters

have been addressed. Experimental data obtained from CMOS process-based, n-channel JFETs have been used to verify the effectiveness and accuracy of the model developed.

## REFERENCES

- [1] A. B. Grebene and S. K. Ghandhi, "General Theory for Operation of the Junction-Gate FET", *Solid-State Electronics*, vol. 12, pp. 573-589
- [2] Juin J. Liou, ***Advanced Semiconductor Device Physics and Modeling***, Artech House, 1994.
- [3] P. Antognetti and G. Massobrio, ***Semiconductor Device Modeling with SPICE***, New York, McGraw-Hill, 1987
- [4] T. Taki, "Approximation of Junction Field-Effect Transistor Characteristics by a Hyperbolic Function," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 724, 1978.
- [5] Juin J. Liou and Y. Yue, "An Improved Model for Four-Terminal Junction Field-Effect Transistors", *IEEE Transactions on Electron Devices*, vol. 43, 1996.
- [6] Paul Van Halen, "A Physical Spice-Compatible Dual-Gate JFET Model", *Proceedings of the 33rd Midwest Symposium on Circuit and Systems*, vol. 2, pp. 715, Aug. 1990.
- [7] Colin C. McAndrew, "An accurate JFET and 3-Terminal Diffused Resistor Model", *NSTI-nanotech 2004*, vol. 2, 2004.
- [8] Victory, J.; McAndrew, C.C.; Hall, J.; Zunino, M.; "A Four-Terminal Compact Model for High Voltage Diffused Resistors with Field Plates," *IEEE Journal Of Solid-State Circuits*, vol. 33, pp. 1453 - 1458, 1998.
- [9] BSIM4 2.0 MOSFET Model User's Manual, UC Berkeley



- [10] P. Van Mieghem, R. P. Mertens, and R. J. Van Overstraeten, "Theory of the junction capacitance of an abrupt diode" J. Appl. Phys., vol. 67, 1990.
- [11] P. Van Halen, "A new semiconductor junction diode space charge layer capacitance model," Proc. of IEEE BCTM, pp.168-171, 1988.
- [12] Spectre Manual, Cadence System, 2001.
- [13] Colin C. McAndrew, "A Continuous Depletion Capacitance Model", IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 12, 1993.

## **CHAPTER THREE: NEW MODEL WITH VELOCITY SATURATION, IMPROVED AC AND NOISE**

### ***3.1 Introduction***

The source drain current we derived in Chapter Two, Equation 2.12, doesn't consider the velocity saturation effect, which is very important for short channel devices. In this chapter, we derive a new current equation including such an important effect.

### ***3.2 DC Modeling***

An idealized diagram for a portion of the JFET device in the linear regime is shown in Fig. 3-1, depicting the conducting channel sandwiched between two space-charge regions (shaded regions in Fig. 3-1) associated with the top and bottom gate to channel junctions. Device dimensions that are critical to the JFET behavior are the channel length  $L$ , channel width  $W$ , channel thickness  $H(x)$ , top space-charge-region thickness  $X^T$ , and bottom space-charge-region thickness  $X^B$ . The steady-state current-voltage characteristics of a JFET is conceptualized into three different regions: the linear region, where the drain-to-source voltage  $V_{DS}$  is relatively small (i.e., less than the saturation voltage) and the drain current  $I_D$  increases considerably with  $V_{DS}$ ; the saturation region, where  $V_{DS}$  is relatively large (i.e., above

the saturation voltage) and  $I_D$  is a weak function of  $V_{DS}$ ; and the cut-off region, where the entire channel is depleted (the channel from the left to right becomes the depletion region, Fig. 3-1) and  $I_D$  is an exponential function of the gate voltage. In the remainder of the chapter, the drain, gate and bulk terminal voltages, as well as the local channel voltage  $V(x)$  are referenced to the source voltage.



where  $W$  is the channel width and  $W_{\text{offset}}$  is the channel width offset. Similarly,

$$L_{\text{eff}} = L - L_{\text{offset}} \quad 3-3$$

where  $L$  is the channel length and  $L_{\text{offset}}$  is the channel length offset.

$H(x)$  is the undepleted channel thickness given by:

$$H(x) = HC - X^T - X^B \quad 3-4$$

where  $HC$  is the metallurgical channel thickness and  $X$  is gate to channel space-charge region's thickness (superscripts  $T$  and  $B$  denote top and bottom gates, respectively). The space-charge region thickness follows the general expression, written for the top-gate:

$$X^T = \sqrt{K^T (V_{bi}^T - V_{TG} + V(x))} \quad \text{with} \quad K^T = 2\varepsilon_s N_A^T / q(N_D + N_A^T)N_D \quad 3-5$$

where  $V_{bi}^T$  is the gate junction built-in potential,  $N_A^T$  is the top-gate doping density and  $\varepsilon_s$  is the silicon permittivity,  $V_{TG}$  is the top gate voltage.

The carrier drift velocity is given by [10]:

$$v(x) = \frac{\mu \cdot E(x)}{1 + \frac{E(x)}{E_{\text{sat}}}} \quad 3-6$$

where  $\mu$  is the low-field electron mobility in the channel,  $E(x)$  is the electrical field, and  $E_{\text{sat}}$  corresponds to the critical electrical field at which the carrier velocity becomes saturated.

Substituting (2) through (6) in (1), expanding the square root term and take the first two terms, the collecting like terms give:

$$I_D = -A \cdot \frac{\mu \cdot E(x)}{1 + \frac{E(x)}{E_{sat}}} \cdot (M - N \cdot V(x)) \quad 3-7$$

where  $A = q \cdot N_D \cdot W_{eff}$ ,

$$M = HC - \sqrt{K^T} \cdot \sqrt{V_{bi}^T - V_{TG}} - \sqrt{K^B} \cdot \sqrt{V_{bi}^B - V_{BG}}$$

$$N = \sqrt{K^T} \cdot \frac{1}{4} \cdot (V_{bi}^T - V_{TG})^{-\frac{1}{2}} + \sqrt{K^B} \cdot \frac{1}{4} \cdot (V_{bi}^B - V_{BG})^{-\frac{1}{2}} \quad 3-8$$

Equation (7) can be rewritten as follows:

$$E(x) = - \frac{I_D}{A \cdot \mu \cdot (M - N \cdot V(x)) + \frac{I_D}{E_{sat}}} = \frac{dV(x)}{dx} \quad 3-9$$

By integrating equation (7) from  $x=0$  to  $x=L_{eff}$  and  $V(x)=V_s$  to  $V(x)=V_D$ , we arrive at the following:

$$I_D = - \frac{\frac{A \cdot \mu}{L_{eff}}}{1 + \frac{V_{DS}}{E_{sat} \cdot L_{eff}}} \cdot (M \cdot V_{DS} - N \cdot V_{DS}^2) \quad 3-10$$

This equation is only valid for a range of drain biases that do not force the top and bottom depletion regions to contact each other (i.e., no channel pinch-off).

### 3.2.2 Drain Current in Saturation

As  $V_{DS}$  increases, the space charge regions expand until the drain end of the channel is pinched off, and  $I_D$  increases slightly with  $V_{DS}$  beyond this point. The drain bias for which the channel is

pinched off,  $V_{Dsat}$ , is obtained by differentiating equation (10) and letting  $dI_D/dV_{DS} = 0$ , [8]:

$$V_{Dsat} = \frac{1}{2 \cdot N} \cdot (-2 \cdot N \cdot E_{sat} + 2 \cdot \sqrt{(N \cdot E_{sat} \cdot L_{eff})^2 + N \cdot M \cdot E_{sat} \cdot L_{eff}}) \quad 3-11$$

We can extend the validity of equation (10), to  $V_{DS} > V_{Dsat}$ , by replacing  $V_{DS}$  with the effective drain voltage  $V_{Deff}$  [8]. This function provides a smooth second-order differentiable transition of the drain current with respect to applied  $V_{DS}$  around  $V_{Dsat}$ ; it is expressed as follows:

$$V_{Deff} = V_{Dsat} \cdot \left(1 - \frac{\log(1 + \exp(B \cdot (1 - \frac{V_{DS}}{V_{Dsat}})))}{\log(1 + \exp(B))}\right) \quad 3-12$$

where B is a smoothing parameter which controls the curvature in the transition region and usually has a value around 1. Thus replacing  $V_{DS}$  with  $V_{Deff}$  in (10) yields a single equation to describe both the linear and saturation current-voltage characteristics of a four-terminal JFET.

When  $V_{DS}$  increases beyond  $V_{Dsat}$ , the drain current is not strictly independent of drain to source bias. The pinched-off part of the channel extends toward the source, reducing the effective channel length. This channel-length modulation effect is adequately modeled for the JFET technologies used in this work with the simple introduction of a coefficient  $\lambda$ . Thus, the term  $(1 + \lambda V_{DS})$  accounting for the channel length modulation is multiplied to equation (10).

### 3.2.3 Drain Current in Cut-off Condition

For sufficiently large top and bottom applied gate voltages, the entire channel becomes depleted (i.e., channel cut-off) and the drain current exhibits an exponential decay characteristic due to the barrier mode behavior [11]. This behavior is included in the drain current in equation (10) using, written for the top gate, the effective top-gate voltage  $V_{TGeff}$  [10]:

$$V_{TGeff} = m^T V_T \ln \left( 1 + \exp \left( \frac{V_{TG} - V_p^T}{m^T V_T} \right) \right) + V_p^T \quad 3-13$$

where  $V_T$  is the thermal voltage,  $V_p$  is the pinch-off voltage,  $m$  is the swing factor. The superscript  $T$  identifies that the parameters are related to the top gate. The pinch-off voltage is determined from the transition point between the above-cut-off to cut-off regions. Thus  $V_p^T$  can be calculated from equation (4) by letting the channel height at the source end to be zero:

$$V_p^T = V_{bi}^T - \frac{HC^2}{K^T} \cdot \left( 1 - \frac{\sqrt{K^B}}{HC} \cdot \sqrt{V_{bi}^B - V_{BG}} \right)^2 \quad 3-14$$

The graduate transition from the conduction to the cut-off regions is explained by the physics that, while the entire channel becomes the depletion region, the horizontal electric field can still induce a current governing by the space-charge-limited flow [4]. The device under such a condition is similar to a metal-insulator-metal system. The insulator does not conduct a significant current because there are very few free carriers



available, and the current flow is space-charge limited because the injected carriers from the metal can be neutralized by the free carriers of opposite sign.

Replacing the drain voltage with the effective drain voltage and the gate voltages (top and bottom gate voltages) with the effective gate voltages in (10) thus constitutes a single expression that describes all the linear, saturation, and cut-off characteristics of four-terminal JFETs. In addition, the introduction of  $V_{DSeff}$  and  $V_{TGeff}$  ensure smooth transitions among all these regions.

The FJFET model has the capability of four-terminal operations and the description of DC characteristics, including all the linear, saturation, and cut-off regions, using a single expression, thus making the FJFET model compact and robust for analog circuit simulations.

### 3.3 AC Components Modeling

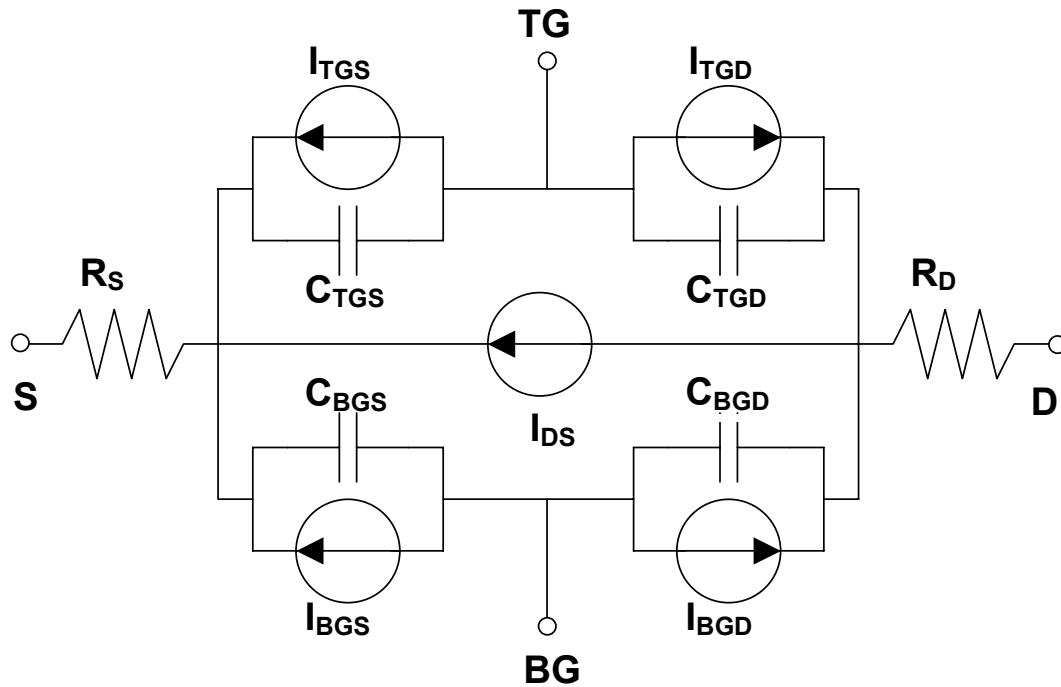


Figure 3-2 Equivalent circuit of the four-terminal JFET describing the drain current source, parasitic capacitances and resistances, and gate leakage current sources.

The four JFET parasitic capacitances, shown in Fig. 3-2, can be described with a physics-based but fairly complex expression [12-14]. For a junction, the charge stored in the neutral regions (NR), formed by minority carriers injected into NR is determined by the formula:

$$Q_s(V) = I_s \cdot \left( \exp\left(\frac{V_{TG}}{n \cdot V_{bi}^T}\right) - 1 \right) \cdot \tau \quad 3-15$$

where  $I_s$  is the gate saturation current,  $n$  is the ideality factor, and  $\tau$  is the diffusion time constant.

To derive such a depletion charge model, let us first look at the one-dimensional charge density in the depletion region:

$$\rho(x) = q \cdot (p(x) - n(x) + N(x)) \quad 3-16$$

where  $\rho(x)$  is the charge density, and  $N(x)$  is  $N_D(x)$  in the n-type depletion region or  $-N_A(x)$  in the p-type depletion region. Let  $x = -x_n$  denotes the boundary of n-type depletion region, and  $x = x_p$  denotes the boundary of the p-type depletion region.

The Poisson equation in the depletion region is:

$$\frac{d^2}{dx^2} \psi(x) = -\frac{\rho(x)}{\epsilon_s} \quad \text{and} \quad E(x) = -\frac{d}{dx} \psi(x) \quad 3-17$$

where  $\psi(x)$  is the electrostatic potential,  $\epsilon_s$  is the permittivity of silicon. Using Fermi-Dirac statistics and assuming nondegenerate conditions, we obtain

$$\frac{d^2}{dx^2} \psi(x) = -\frac{q}{\epsilon} \cdot [N_V \cdot \exp\left(\frac{E_V - E_{fp}}{k \cdot T}\right) - N_C \cdot \exp\left(\frac{E_{fn} - E_C}{k \cdot T}\right) - N_A] \quad \text{for } 0 < x < x_p \quad 3-18$$

$$\frac{d^2}{dx^2} \psi(x) = -\frac{q}{\epsilon} \cdot [N_V \cdot \exp\left(\frac{E_V - E_{fp}}{k \cdot T}\right) - N_C \cdot \exp\left(\frac{E_{fn} - E_C}{k \cdot T}\right) + N_D] \quad \text{for } -x_n < x < 0 \quad 3-19$$

where  $N_C$  and  $N_V$  are the effective electron and hole densities of states.  $E_{fn}$  and  $E_{fp}$  are the quasi-Fermi levels for electrons and holes.

With the following boundary conditions,

$$\frac{d}{dx}\psi(-x_n) = \frac{d}{dx}\psi(x_p) \quad \text{and} \quad \frac{d^2}{dx^2}\psi(-x_n) = \frac{d^2}{dx^2}\psi(x_p) \quad 3-20$$

We arrive at the depletion charge formula for the junction related to the top gate:

$$Q_d(V_{TG}) = 2C_{j0}V_T \left( \left( X(V_{TG}) - V_{bi}^T \right)^{1/2} - \left( X(V_{TG}) - \frac{V_{bi}^T}{V_T} \left( 1 - \frac{V_{TG}}{V_{bi}^T} \right) \right)^{1/2} \right) \quad 3-21$$

where

$$X(V_{TG}) = 2V_{bi}^T + \frac{(N_D + N_A^T)(N_C + N_V)}{2N_D N_A^T} \exp\left(\frac{V_{TG} - V_{bi}^T}{2V_T}\right) \quad 3-22$$

$$C_{j0}^T = A \sqrt{\frac{q\epsilon_s N_D N_A^T}{2V_T (N_D + N_A^T)}} \quad 3-23$$

where A is the portion of the junction area associated with the capacitance considered,  $N_A^T$  and  $N_D$  are the top-gate and channel doping density.

Thus, the total charge can be expressed as:

$$Q(V) = Q_d(V) + Q_s(V) \quad 3-24$$

The first and second terms on the right-hand side of (24) denote the charges associated with the space-charge region and quasi-neutral region, respectively. As such, both the junction and diffusion capacitances are accounted for in the model. The total junction area for each gate is partitioned equally between drain-side and source-side, however, the model allows for different partitioning schemes. For simplicity, only the top gate capacitance model has been illustrated, the back gate uses basically the same equation for the model.

Differentiating equation (24) with respect to voltage yields the expression for the junction and diffusion capacitances. Note that equation (24) is formulated as a single expression that respects charge conservation and features a continuous derivative that reduces potential convergence issues.

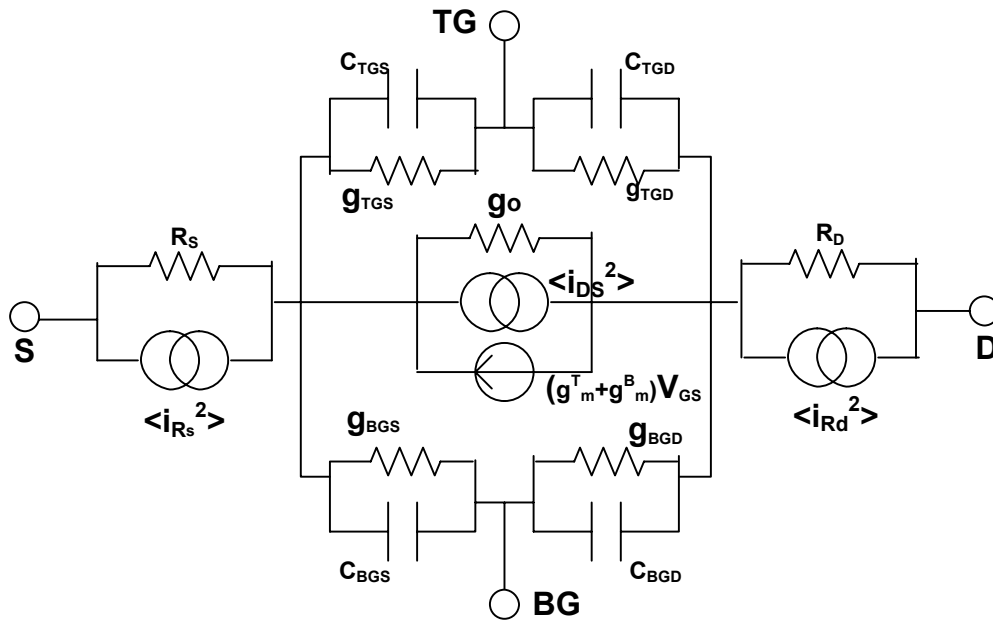


Figure 3-3 Noise equivalent circuit of the four-terminal JFET.

### 3.4 Noise Modeling

Low noise is one big advantage of JFET compared to MOSFET due to the lack of oxide/silicon interface. However, it would be of great help to circuit designers if the model can predict the noise behavior of the JFET. Fig. 3-3 is the noise equivalent circuit we are using in this model.

The source/drain series resistance thermal noise is given by [15]:

$$\overline{i_{R_s}^2} = \frac{4kT}{R_s} \cdot \Delta f \quad \text{and} \quad \overline{i_{R_D}^2} = \frac{4kT}{R_D} \cdot \Delta f \quad 3-25$$

where  $k$  is the Boltzmann constant,  $\Delta f$  is the noise bandwidth.

The channel thermal and flicker noise is determined by:

$$\overline{i_{DS}^2} = \frac{4kT(g_m^T + g_m^B + g_{DS})}{3} \cdot \left( \frac{3}{2} - \frac{V_{D\text{eff}}}{2V_{D\text{sat}}} \right) \Delta f + \frac{KF \cdot (I_D)^{AF}}{L_{\text{eff}}^2 f} \Delta f \quad 3-26$$

where  $g_m^T$  and  $g_m^B$  are the transconductance of top gate and bottom gate respectively,  $g_{DS}$  is the device conductance,  $KF$  is the flicker noise proportional factor,  $AF$  is the current exponent coefficient,  $f$  is the frequency at which the flicker noise is calculated.

### **3.5 Model Implementation and Results**

The FJFET model has been implemented in Verilog-A, which provides a convenient interface to Cadence circuit design framework. The model parameters were optimized to fit an N-channel JFET processed in a CMOS technology used at Texas Instruments.

Figs. 3-4(a) and (b) illustrate that using the FJFET model allows obtaining a good fit to experimental data for JFETs with two different channel lengths of 27 and 4  $\mu\text{m}$ . Fig. 3-5 illustrates the output conductance of the 27- $\mu\text{m}$  JFET calculated from the FJFET model and obtained from measurements for a wide range of gate and drain voltages. The second derivative results of the I-V characteristics for the JFET are shown in Figs. 3-6, indicating the FJFET model yields a very smooth transition between the linear and saturation regions. The drain current versus the gate voltage characteristics from the conduction to cut-off regions is another key JFET performance. Figs. 3-7(a) and (b) show the very

good fit of the new model to experimental data for various top- and bottom-gate biases for the 27- and 4-  $\mu\text{m}$  JFETs.

Fig. 3-8 shows the junction capacitance characteristics of the new model compared to the classic model and the simulation result. The FJFET model predicts a good fit to the simulation result, which peaks and decreases as the voltage approaches the built-in voltage. Note that the conventional capacitance model in SPICE predicts an infinite junction capacitance when the applied voltage approaches the built-in voltage. Fig. 3-9 compares the total capacitance (junction and diffusion capacitances) calculated from the FJFET model and obtained from the measurement data.



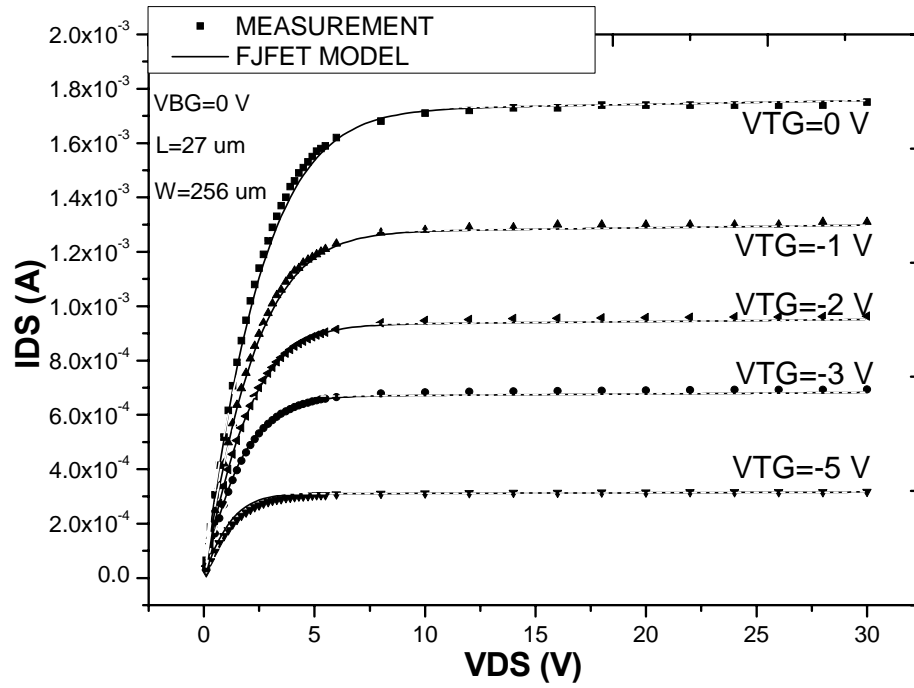


Figure 3-4(a)  $I_{DS}$  vs.  $V_{DS}$  characteristics obtained from FJFET model and measurement data.

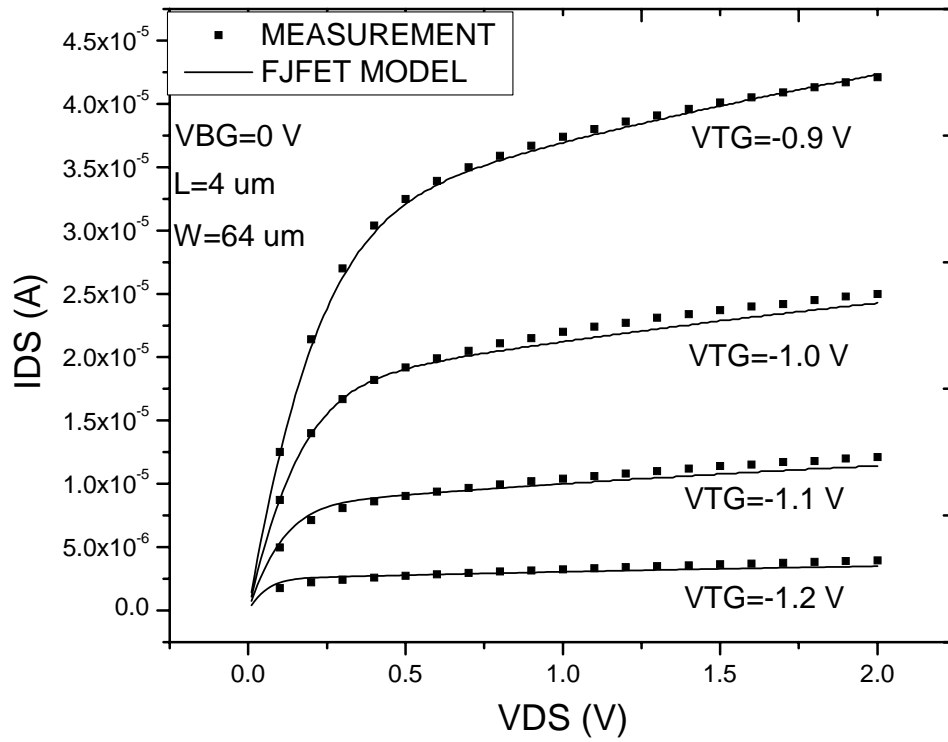


Figure 3-4(b)  $I_{DS}$  vs.  $V_{DS}$  characteristics obtained from FJFET model and measurement data

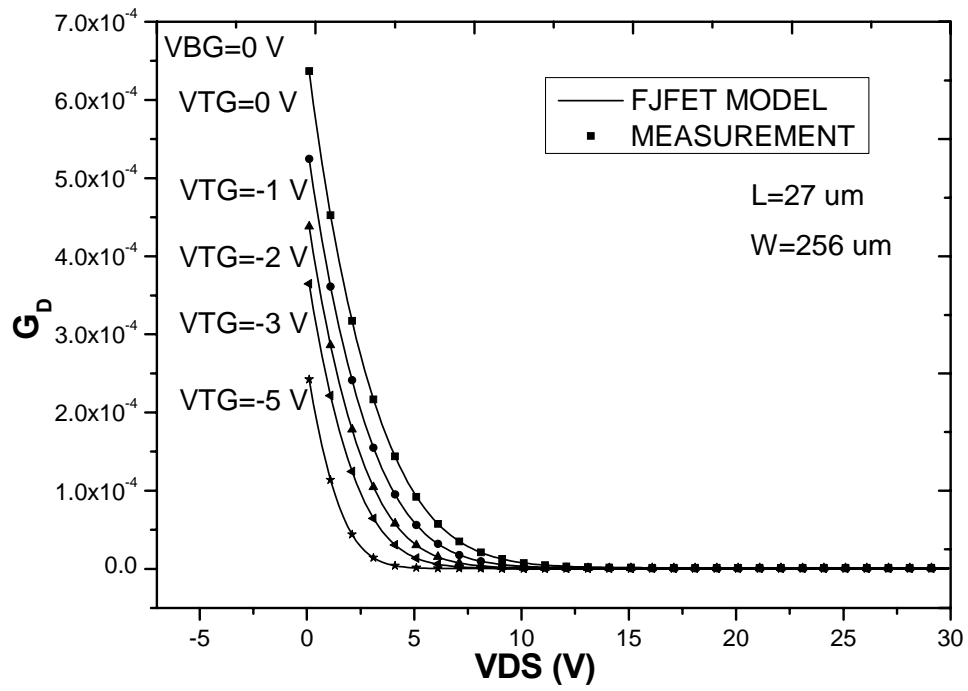


Figure 3-5 Output conductance characteristics obtained from the FJFET model and measurement data

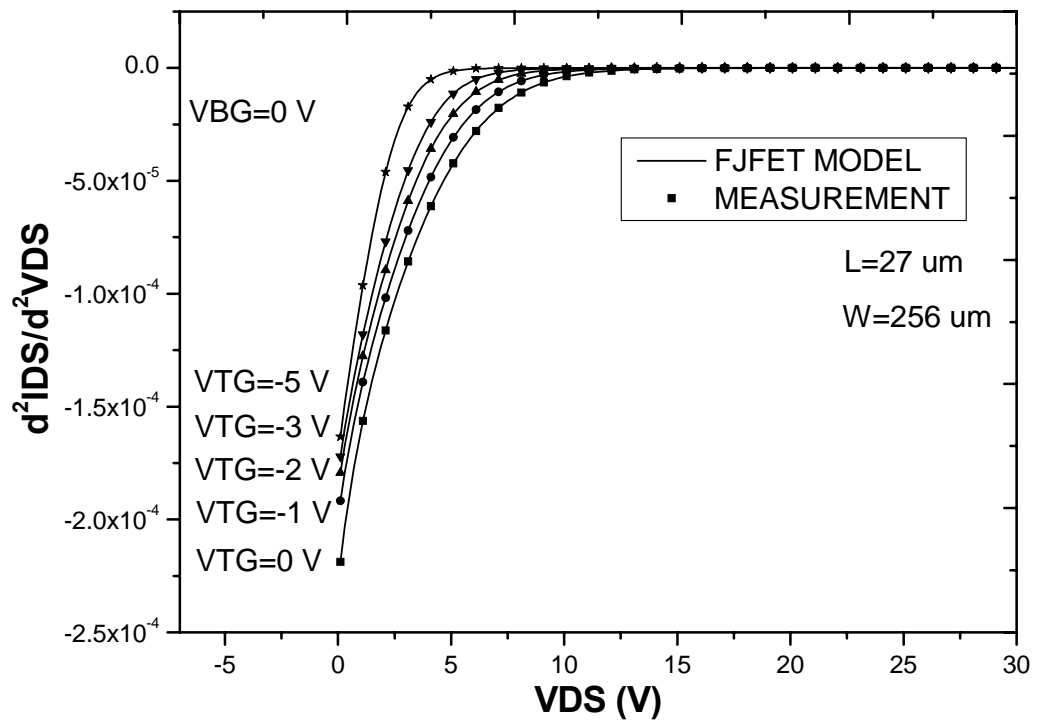


Figure 3-6 Second order derivative of the I-V characteristics obtained from the FJFET model and measurement data.

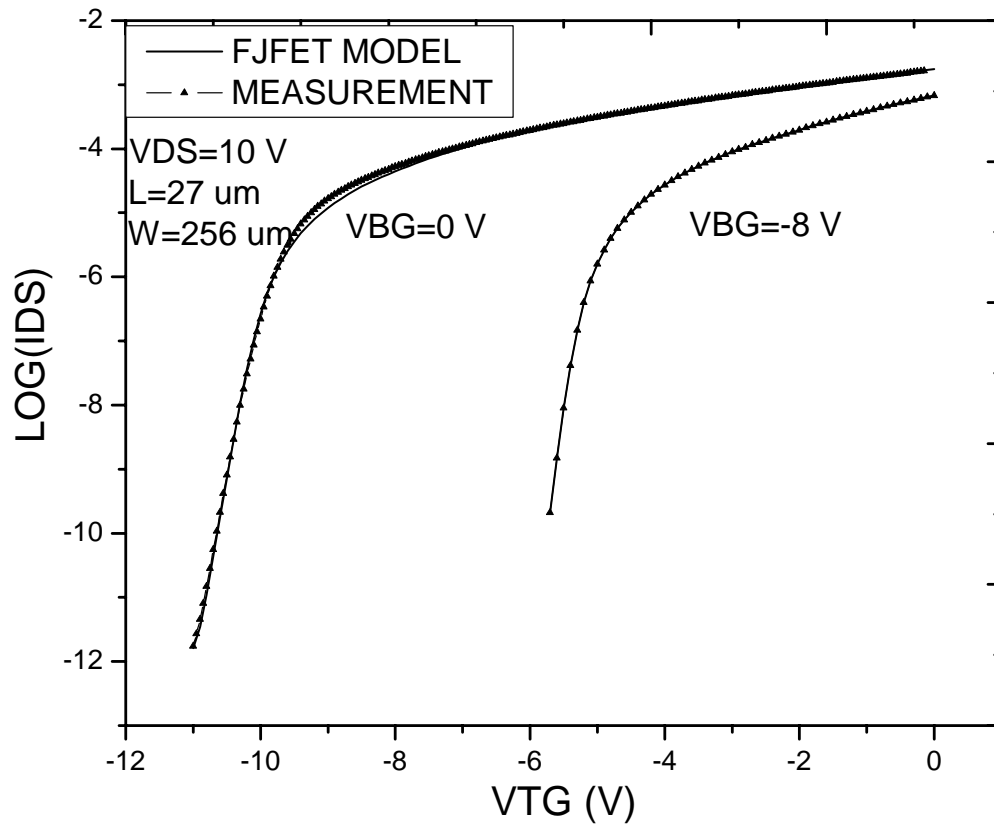


Figure 3-7(a) Drain current vs. gate voltage characteristics obtained from the FJFET model and measurement data.

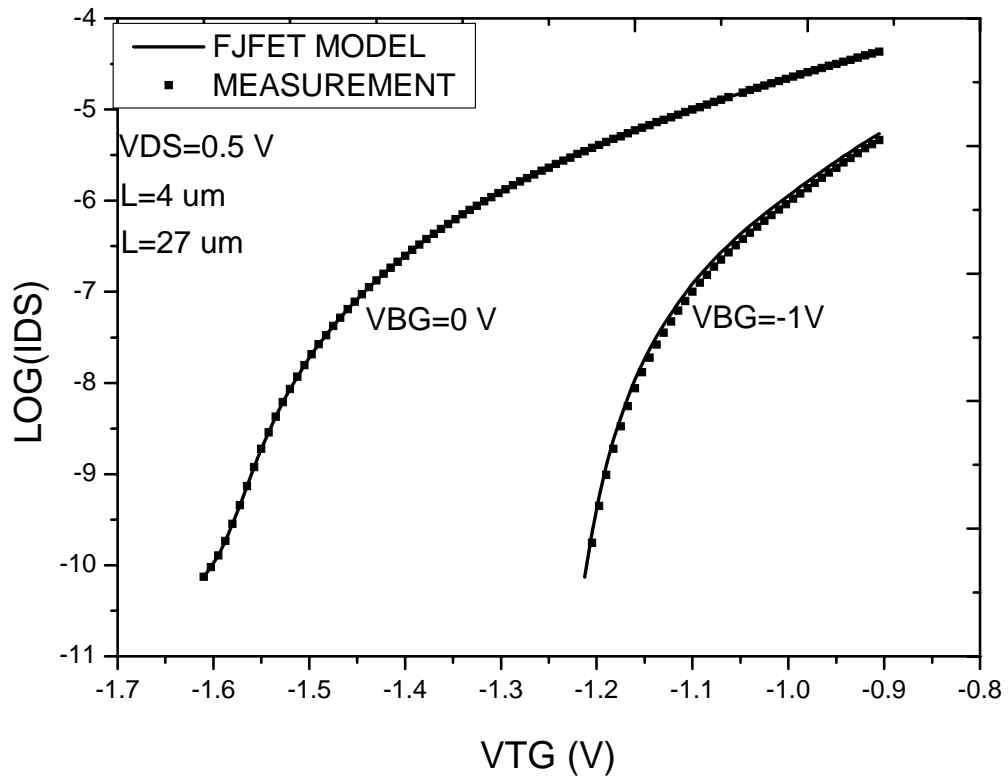


Figure 3-7(b) Drain current vs. gate voltage characteristics obtained from the FJFET model and measurement data.

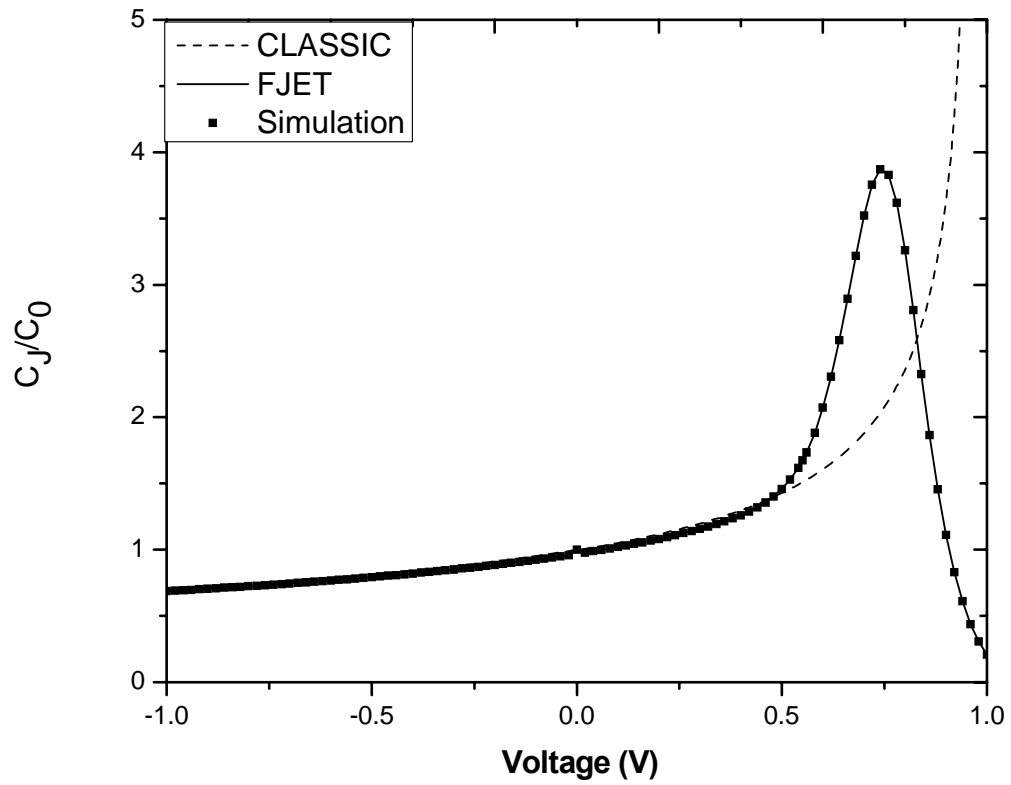


Figure 3-8 Junction capacitance vs. voltage obtained from the FJET model, the classic model and the simulation

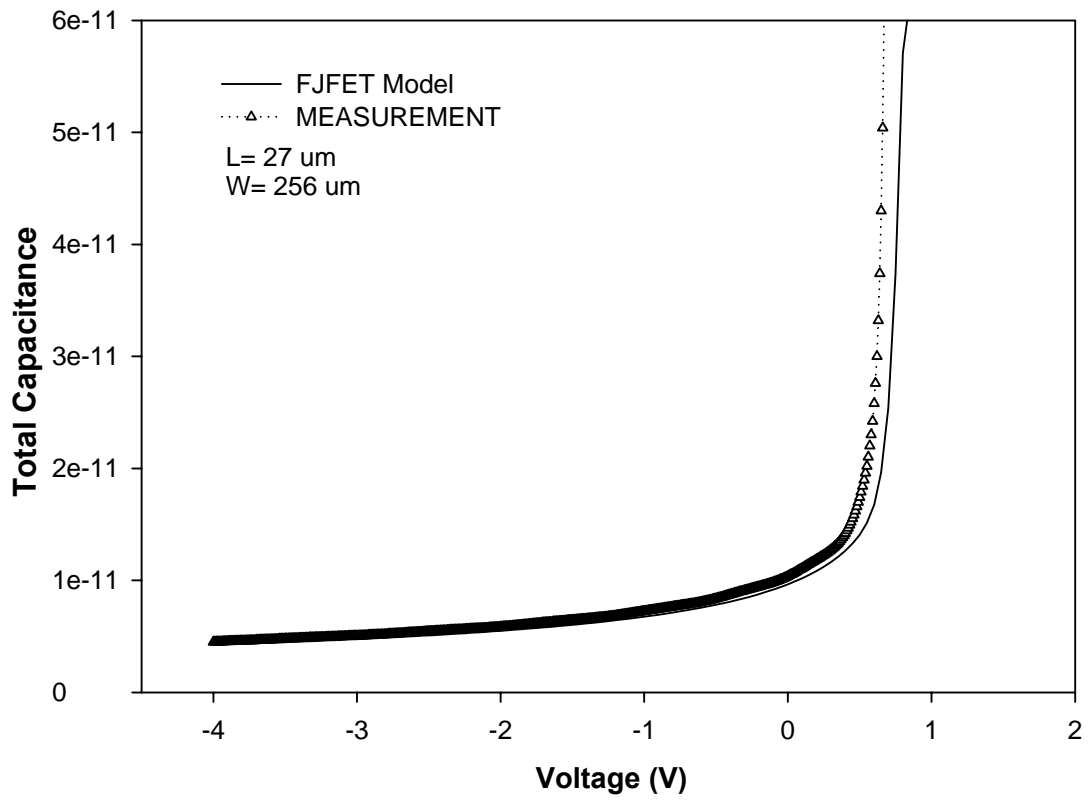


Figure 3-9 Comparison between the total capacitance (junction and diffusion capacitances) calculated of the FJFET model and obtained from measurement data.



### **3.6 Conclusions**

With the increased interest in their low-noise, low input bias current features, JFETs are nowadays incorporated into analog applications for which a higher level of model accuracy and stability is required in order to successfully predict chip performances. Unfortunately, JFET models currently implemented in commercial circuit simulators, while providing a good first-order approximation of overall device performance, lack the added required accuracy for analog applications. We have presented a new and compact four-terminal JFET model. The DC model is described via a unified equation that captures operation under all bias conditions and provides a high accuracy and continuity. The new model accurately reproduced the experimental data taken at Texas Instruments.

## REFERENCES

- [1] M. Manghisoni et al. "JFET front end circuits integrated in a detector grade silicon substrate", IEEE Trans. on Nuclear Science, vol. 50, 2003, p. 942
- [2] Yoshida, N.; Ishizaka, M etc. "A 10 Gb/s optical transmitter module with a built-in modulator driver IC and a receiver module with a built-in preamplifier IC", Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1999. pp 287 - 290
- [3] A. B. Grebene and S. K. Ghandhi, "General Theory for Operation of the Junction-Gate FET", Solid-State Electronics, vol. 12, pp. 573-589
- [4] Juin J. Liou, **Advanced Semiconductor Device Physics and Modeling**, Artech House, 1994.
- [5] P. Antognetti and G. Massobrio, **Semiconductor Device Modeling with SPICE**, New York, McGraw-Hill, 1987
- [6] T. Taki, "Approximation of Junction Field-Effect Transistor Characteristics by a Hyperbolic Function," IEEE J. Solid-State Circuits, vol. SC-13, pp. 724, 1978.
- [7] Juin J. Liou and Y. Yue, "An Improved Model for Four-Terminal Junction Field-Effect Transistors", IEEE Transactions on Electron Devices, vol. 43, 1996.
- [8] Paul Van Halen, "A Physical Spice-Compatible Dual-Gate JFET Model", Proceedings of the 33rd Midwest Symposium on Circuit and Systems, vol. 2, pp. 715, Aug. 1990.

- [9] Colin C. McAndrew, "An accurate JFET and 3-Terminal Diffused Resistor Model", NSTI-nanotech 2004, vol. 2, 2004.
- [10] BSIM4.2.1 Manual, 2001
- [11] Brewer, R. J "The Barrier Mode Behavior of a Junction FET at Low Drain Currents", Solid-State Electron, vol. 18, 1975, pp 1013-1017.
- [12] Colin C. McAndrew, "A  $C_{\text{d}}$ -Continuous Depletion Capacitance Model", IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 12, 1993.
- [13] P. Van Mieghem, R. P. Mertens, and R. J. Van Overstraeten, "Theory of the junction capacitance of an abrupt diode" J. Appl. Phys., vol. 67, 1990.
- [14] P. Van Halen, "A new semiconductor junction diode space charge layer capacitance model," Proc. of IEEE BCTM, pp.168-171, 1988.
- [15] Spectre Circuit Simulator Device Model Equations, Version 5.0, Dec. 2002

## CHAPTER FOUR: IMPROVED CAPACITANCE MODEL FOR JUNCTION FIELD-EFFECT TRANSISTORS

### 4.1 Introduction

The traditional junction capacitance used in SPICE has the form of [1]:

$$C_J(V_J) = \frac{C_{J0}}{\left(1 - \frac{V_J}{\phi}\right)^M} \quad \text{when } V_J \leq F_C \cdot \phi$$

$$\frac{C_{J0}}{(1 - F_C)^{M+1}} \cdot \left(1 - F_C(M+1) + M \cdot \frac{V_J}{\phi}\right) \quad \text{when } V_J > F_C \cdot \phi \quad 4-1$$

where  $C_{J0}$  is the zero-bias junction capacitance,  $V_J$  is the junction voltage,  $\phi$  is the junction built-in potential,  $M$  is the junction gradient coefficient, and  $F_C$  is a fitting parameter to prevent the junction capacitance from going to  $\infty$  at  $V_J = \phi$ .

In this two-piece regional model, the junction capacitance monotonically increases with increasing junction bias, and it unphysically implies that the depletion charge, determined by the integration of Eq. (1), approaches  $\infty$  when in fact the depletion region vanishes at  $V_J = \phi$ . Moreover, the derivative of this junction capacitance is discontinuous at  $V_J = F_C \cdot \phi$ .

A single-piece,  $C_{\infty}$ -continuous junction charge and capacitance model that overcame these problems was derived recently [2]. The model fits capacitance data for a wide range of bias conditions and through the region where the junction capacitance changes from being dominated by junction capacitance to being dominated by diffusion capacitance. The charge model was given as [2]

$$Q_J(V_J) = \frac{C_{J0} \cdot \phi}{1-M} \cdot \left[ (1-R)^{1-M} - \left(1 - \frac{V^L(V_J)}{\phi}\right)^{1-M} \right] \quad 4-2$$

Differentiating Eq. (2) yields the junction capacitance model:

$$C_J(V_J) = \frac{C_{J0}}{\left(1 - \frac{V^L(V_J)}{\phi}\right)^M} \cdot \frac{\partial V^L(V_J)}{\partial V_J} \quad 4-3$$

where

$$V^L(V_J) = R \cdot \phi - \frac{1}{A} \cdot \ln(1 + \exp(-A \cdot (V_J - R \cdot \phi))) \quad 4-4$$

$R$  is a parameter with value close to 1, and  $A$  is a parameter that governs how tightly  $V^L(V_J)$  approaches the corner at  $V_J = R\phi$ .

This model is accurate for typical junction capacitances in diodes, bipolar junction transistors, and MOSFETs. However, in some four-terminal JFETs, the junction capacitance exhibits an abrupt drop-off when the drain/gate bias induces channel pinch-off. Both the capacitance models in SPICE [1] and in [2] are not capable of describing such a behavior.

In this chapter, we present an improved junction capacitance model which maintains all the advantages of the model in [2] but

also includes the capacitance drop-off effect. The new model is also extended to be applicable for different temperatures.

#### 4.2 New Capacitance Model Development

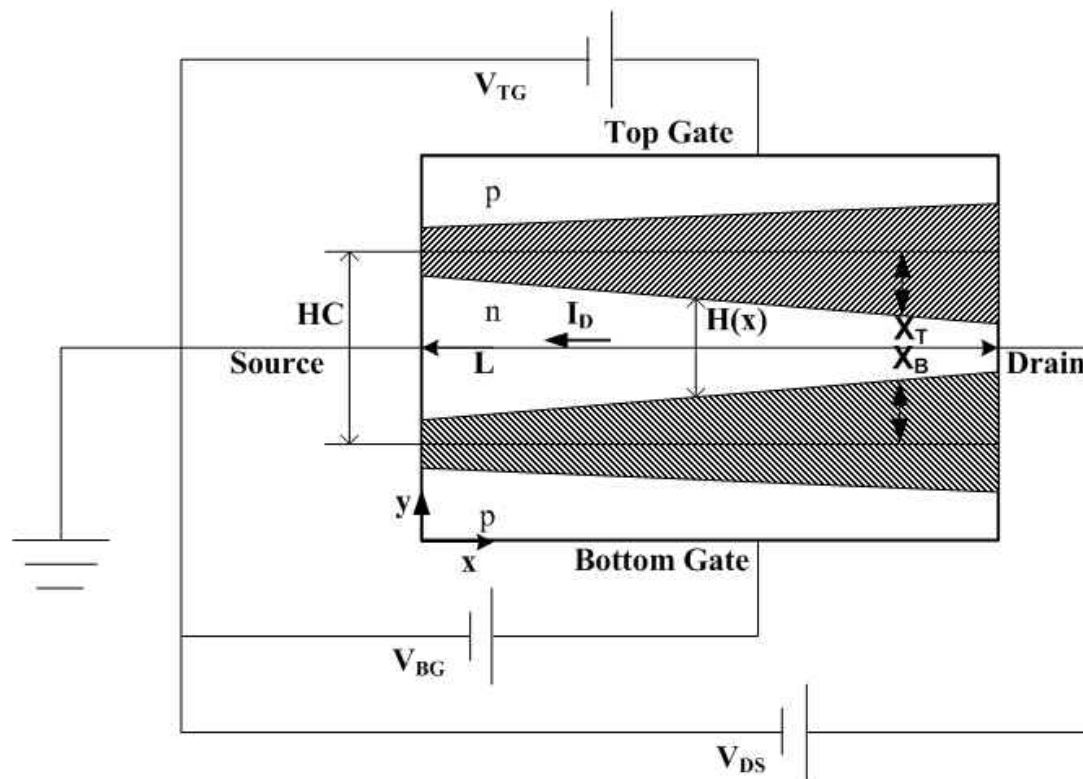


Figure 4-1 N-channel JFET device with applied drain, top-gate and back-gate voltages. Shaded regions denote the top and bottom-gate space-charge regions.

An idealized diagram for a portion of the JFET device is shown in Fig. 4-1, depicting the conducting channel sandwiched between two space-charge regions (shaded regions in Fig.4-1) associated with the top and bottom gate to channel junctions. In the Fig.,  $L$  is

the device channel length, and the conducting channel thickness  $H$  is given by:

$$H(x) = HC - X^T - X^B \quad 4-5$$

where  $HC$  is the metallurgical channel thickness and  $X$  is the gate to channel space-charge region's thickness (superscripts  $T$  and  $B$  denote top and bottom gates, respectively). Let us focus on the top-gate junction. The space-charge region thickness follows the general expression, written for the top-gate:

$$X^T = \sqrt{K^T (\phi^T - V_{TG} + V(x))}, \text{ with } K^T = 2\epsilon_s N_A^T / q(N_D + N_A^T)N_D \quad 4-6$$

where  $\phi^T$  is the top-gate junction built-in potential,  $V(x)$  is the local channel voltage referenced to the source voltage,  $N_A^T$  is the top-gate doping density,  $\epsilon_s$  is the silicon permittivity, and  $V_{TG}$  is the top-gate voltage.

When the channel pinch-off occurs in the JFET near the drain end, the depletion regions associated with the top- and bottom-gate touch each other and all the charges at the drain end are depleted. The top-gate junction capacitance is defined by the displacement of the charge in the junction with respect to the voltage variation. At and beyond channel pinch-off, charge displacement is absent in the junction region near the drain end, and this region no longer contributes to the total junction capacitance. As a result, a sudden drop-off of the junction capacitance is observed experimentally.

Because the JFET is biased with the gate voltage and the drain-to-source voltage  $V_{DS}$ , we use the gate-to-drain voltage  $V_{GD}$  as the bias variable and introduce the concept of the effective gate-to-drain voltage  $V_{GD\text{eff}}$  to model the JFET junction capacitance drop-off effect:

$$V_{GD\text{eff}}(V_{GD}) = f^{-1}(V^L(V_{GD})) \quad 4-7$$

where

$$f(y) = [V_p + \frac{1}{2}[(y - V_p - C) + \sqrt{(y - V_p - C)^2 - 4 \cdot C \cdot V_p}]] \cdot (1 + \alpha \cdot y) \quad 4-8$$

and  $V_p$  is the gate-to-drain voltage at which the channel pinches off at the drain end and at which the capacitance drops off.  $V_p$  can be derived from Eqs. (5) and (6) by letting  $H = 0$  at the drain end. Also,  $V^L(V_{GD})$  has the same form as the expression in Eq. (4), and  $C$  and  $\alpha$  are fitting parameters that govern the capacitance curve in the transition between below and beyond channel pinch-off. Fig. 4-2 shows the relationship between  $V_{GD\text{eff}}$  and  $V_{GD}$  for different  $C$  and  $\alpha$  values.



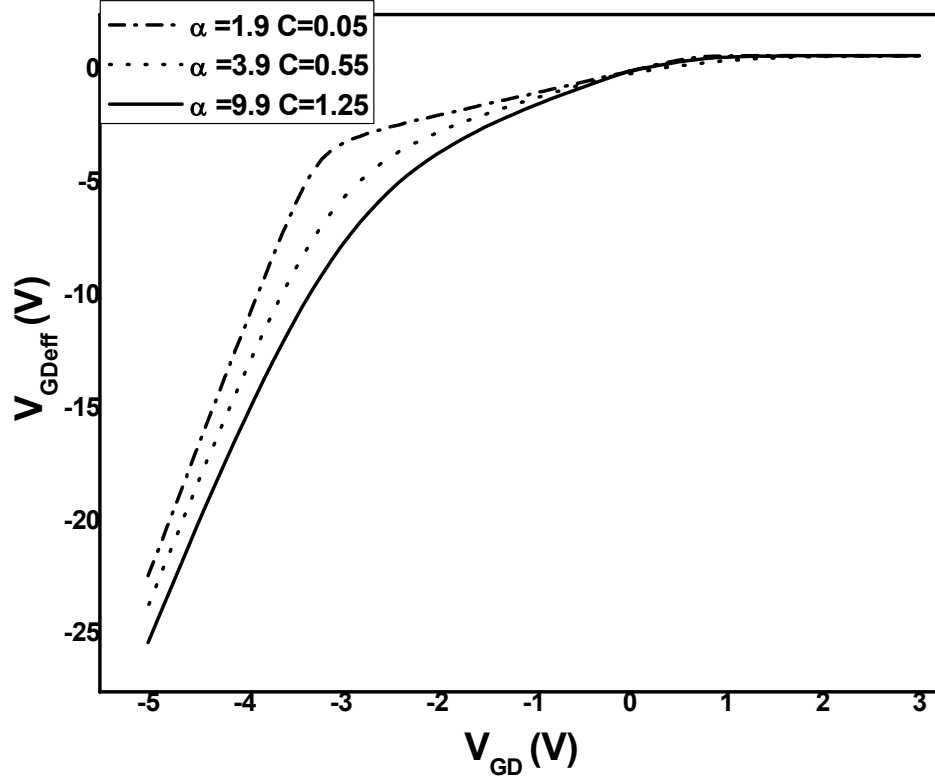


Figure 4-2 Effective gate-to-drain voltage  $V_{GDeff}$  plotted as a function of  $V_{GD}$  for different parameter values

Replacing  $V_J$  and  $V^L(V_J)$  in Eq. (2) with  $V_{GD}$  and  $V_{GDeff}(V_{GD})$ , respectively, the new charge and capacitance expressions are obtained:

$$Q_J(V_{GD}) = \frac{C_{J0} \cdot \phi}{1-M} \cdot \left[ (1-R)^{1-M} - \left(1 - \frac{V_{GDeff}(V_{GD})}{\phi}\right)^{1-M} \right] \quad 4-9$$

$$C_J(V_{GD}) = \frac{C_{J0}}{\left(1 - \frac{V_{GDeff}(V_{GD})}{\phi}\right)^M} \cdot \frac{\partial V_{GDeff}(V_{GD})}{\partial V_{GD}} \quad 4-10$$

At and beyond channel pinch-off,  $V_{GDeff}$  becomes more negative than  $V_{GD}$ , and thus the new model yields a smaller junction capacitance (i.e., capacitance drop-off) than the existing models. Thus, the physics underlying the use of  $V_{GDeff}$  is that the new capacitance model can accurately describe the capacitance drop-off behavior through the use of the effective voltage  $V_{GDeff}$  when the channel pinch-off takes place in the JFET. Furthermore, the single expression for the junction capacitance in Eq. (10) ensures convergence for a wide range of bias conditions.

The capacitance model can be made more comprehensive with the inclusion of the diffusion capacitance. Such a capacitance results from the diffusion charge stored in the neutral regions (NR), formed by minority carriers injected into NR, determined by the formula [3]:

$$Q_s(V_{GD}) = I_s \cdot \left( \exp\left(\frac{V_{GD}}{n \cdot \phi}\right) - 1 \right) \cdot \tau \quad 4-11$$

where  $I_s$  is the junction saturation current,  $n$  is the ideality factor, and  $\tau$  is the diffusion time constant.

The total capacitance model, including both the junction and diffusion capacitances, is given by:

$$C_{total}(V_{GD}) = C_J(V_{GD}) + \frac{\partial Q_s(V_{GD})}{\partial V_{GD}} \quad 4-12$$

This new model thus describes the capacitance in both reverse and forward bias conditions with the drop-off phenomenon included.

Note that the new capacitance model requires two additional parameters,  $C$  and  $\alpha$ , for modeling the capacitance drop-off at relatively large reverse gate voltages. These parameters can be easily extracted from the reverse-bias experimental data. The modeled capacitance-voltage curve outside the drop-off region was first fitted to the measured data by using a fixed  $C$  and optimizing  $\alpha$ . Once a good agreement has been reached, then  $\alpha$  was fixed and  $C$  was optimized until a good fit for the capacitance-voltage characteristics around the drop-off region can be obtained.

Fig. 4-3 shows the comparison of JFET junction capacitances obtained from the new model, existing model [2], and experimental data measured at Texas Instruments under the conditions of a frequency of 100 kHz,  $V_{DS} = 1.5$  V, and room temperature. The capacitance drop-off for  $V_{GD} < -1$  V is accurately predicted by the new model. Fig. 4-4 illustrates how the parameters  $C$  and  $\alpha$  affect the behavior of capacitance drop-off. It can be seen that the drop-off becomes more significant when  $C$  is reduced, and the opposite occurs if  $\alpha$  is reduced. Fig. 4-5 shows the effect of different  $V_{DS}$  on the junction capacitance characteristics. Clearly, the capacitance drop-off is more prominent when  $V_{DS}$  is increased.

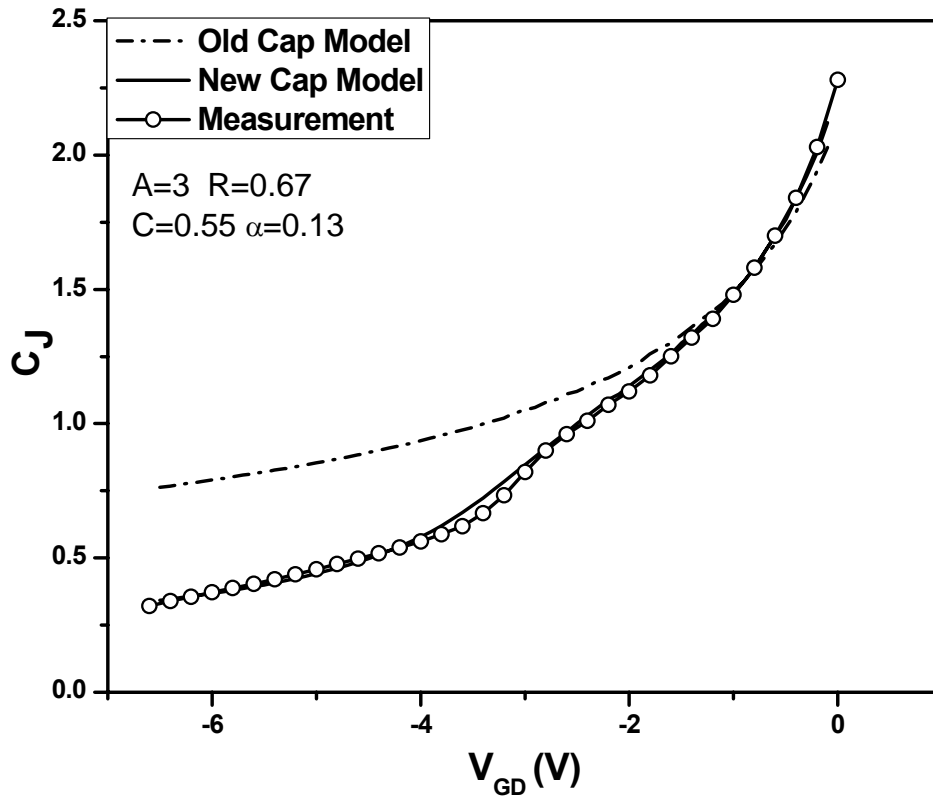


Figure 4-3 Normalized junction capacitances obtained from the new model, existing model [2] and measurements under the conditions of frequency of 100 kHz,  $V_{DS}=1.5$  V, and room temperature. Values of fitting parameters for the new and old models are also listed.

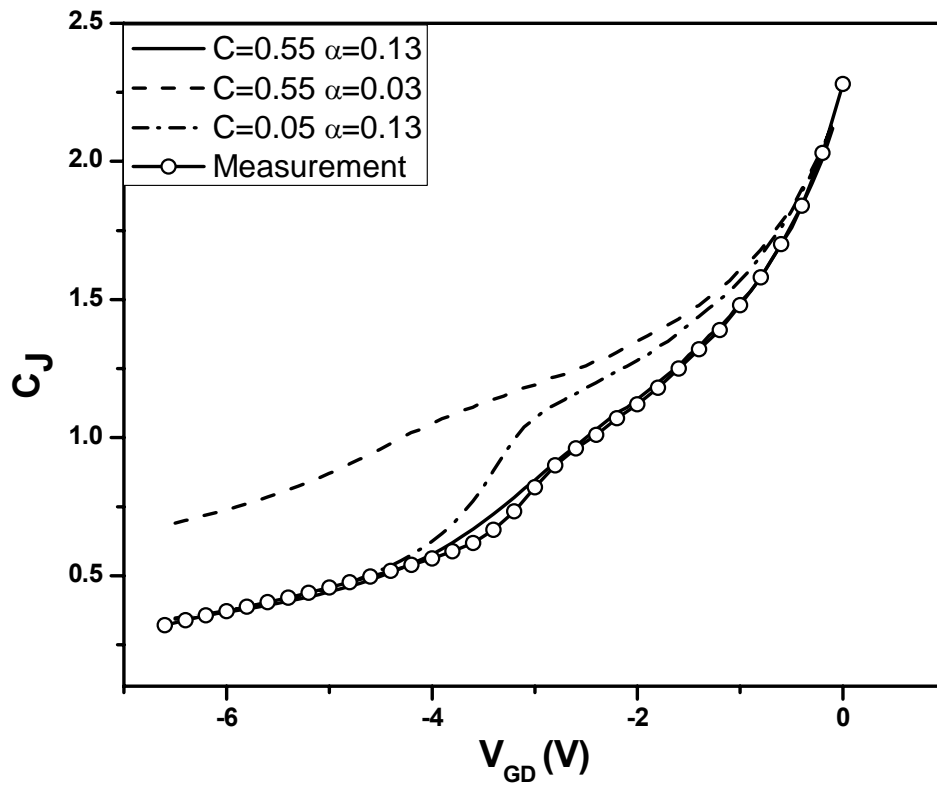


Figure 4-4 Effect of the values of C and  $\alpha$  on the behavior of junction capacitance drop-off

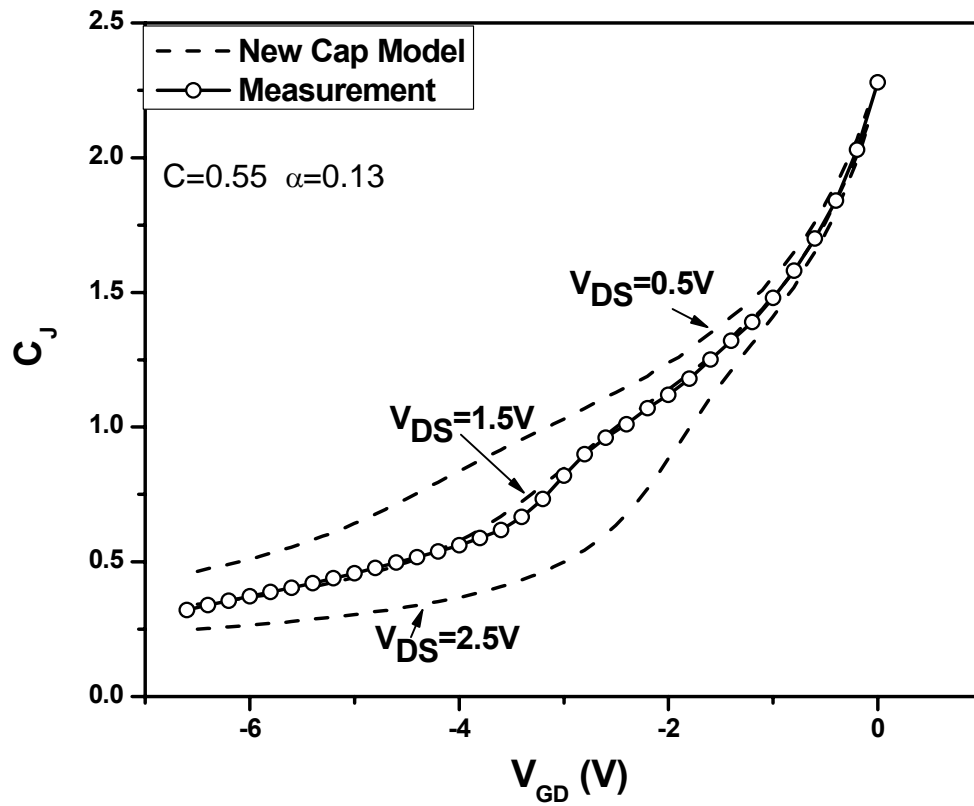


Figure 4-5 Normalized junction capacitance vs. voltage characteristics for three different  $V_{DS}$

To include the temperature effect, the following expressions are used [4]:

$$C_j(T) = C_j(T_{nom}) \cdot (1 + tcj \cdot \Delta T) \quad 4-13$$

$$\phi(T) = \phi(T_{nom}) - tpb \cdot \Delta T \quad 4-14$$

where  $\Delta T = T - T_{nom}$ , tcj and tpb are the temperature coefficients for zero bias junction capacitance and built-in potential, respectively, and  $T_{nom}$  is the nominal temperature (normally the room temperature) at which all other parameters are extracted.

Fig. 4-6 compares the new capacitance model and experimental data at three different temperatures. Again, the model results compare very favorably with the measurements.

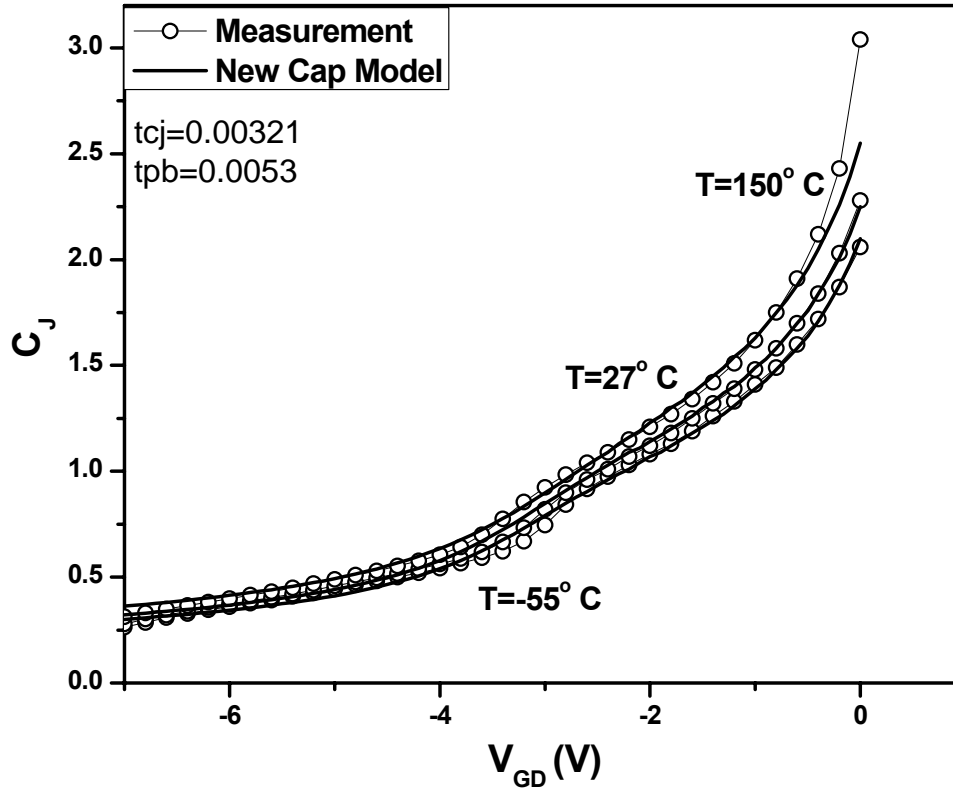


Figure 4-6 Normalized junction capacitances obtained from the new model and measurements at three different temperatures under the conditions of frequency of 100 kHz and  $V_{DS}=1.5$  V. Parameter values used are also listed.



### **4.3 Conclusions**

A new junction capacitance model for junction field-effect transistors has been developed. It improved the previous models by adding the capability to describe accurately the capacitance drop-off phenomenon caused by the channel pinch-off. In addition, the present model is applicable for low and high temperature operations. The use of a single expression for the junction capacitance for a wide range of biases and temperatures eliminated the possibility of divergence in simulations. The model has been verified successfully against measured data taken at Texas Instruments.

## **REFERENCES**

- [1] P. Antognetti and G. Massobrio (Eds.), Semiconductor Device Modeling with SPICE, New York: McGraw-Hill, 1988
- [2] Colin C. McAndrew, "A  $C_{\infty}$ -Continuous Depletion Capacitance Model", IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 12, pp 825, 1993.
- [3] S. M. Sze, Physics of Semiconductor Devices. John Wiley & Sons, 1981
- [4] BSIM4.2.1 Manual, 2001

**CHAPTER FIVE:  
COMPACT MODELING OF FOUR-TERMINAL JUNCTION FIELD  
TRANSISTOR WITH OXIDE TOP-GATE AND FULL ISOLATION**

**5.1 Introduction**

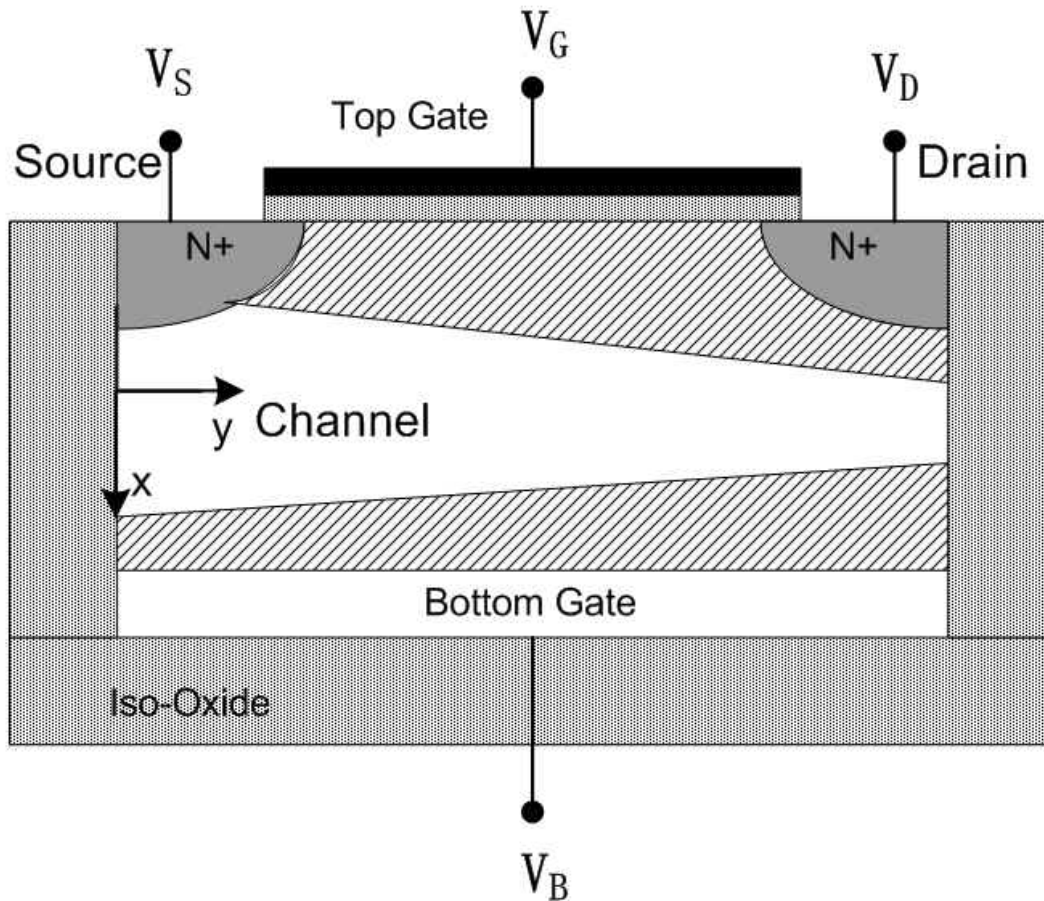


Figure 5-1 Schematic of the N-channel JFET with full isolation and oxide top-gate.

The junction field-effect transistors (JFET) have been widely used in high voltage and/or analog applications. Besides the traditional structure with p/n junction top- and bottom-gates,

JFETs having an oxide top-gate are also being used. Figure 5-1 shows the cross section of such an N-Channel JFET. The JFET is fully isolated by the oxide box on the bottom and oxide trench on the sides, thus making it totally isolated from other devices on the wafer. This gives the following advantages over non-fully-isolated JFET: 1) superb noise performance, 2) higher die densities due to the closer spacing between the devices, and 3) a higher voltage can be applied without the interaction between adjacent devices. In addition, instead of the typical p/n junction top-gate, the device uses the oxide top-gate to allow for a higher degree of flexibility in JFET operations for various analog circuit applications.

The existing models [1-3] for the traditional p/n junction top- and bottom-gate JFET cannot adequately describe the behavior of the structure shown in Fig. 5-1. In this chapter, we will analyze the different operation modes of such a JFET and develop a compact model which takes into account the effect of the oxide top-gate. Experimental data measured at Texas Instruments will be included in support of the model development.

## 5.2 Modes of Operation

In order to derive the model for predicting the dc characteristics of the JFET with an oxide top-gate, we will first need to analyze and understand its top-gate operation modes. The N-channel JFET shown in Fig. 5-1 will be considered, and the modeling approach applies generally to P-channel JFET as well. The device can enter into a number of operating modes including inversion, depletion, pinch-off, and accumulation depending on the doping density distribution, physical dimensions, and bias conditions.

The channel region of the device in Fig. 5-1 is formed by implanting an n-type impurity into a p-type silicon, which gives rise to a doping profile characterized by the Gaussian function [4]:

$$N(x) = \frac{Q_j}{\sqrt{2\pi}\sigma} \exp\left(-\left(\frac{x-R_p}{\sqrt{2}\sigma}\right)^2\right) \quad 5-1$$

where  $Q_j$  is the implant dose,  $\sigma$  is the implant straggle, and  $R_p$  is the implant projected range. An equivalent box profile can be used to represent the Gaussian implant profile, and the channel doping can be approximated by a uniform doping density of [5]

$$N_D = \frac{mQ_j}{2\sqrt{2}q\sigma} \quad 5-2$$

and the depth of this uniformly doped layer is

$$x_j = \frac{2\sqrt{2}\sigma}{m}$$

5-3

where  $m$  is a fitting parameter.

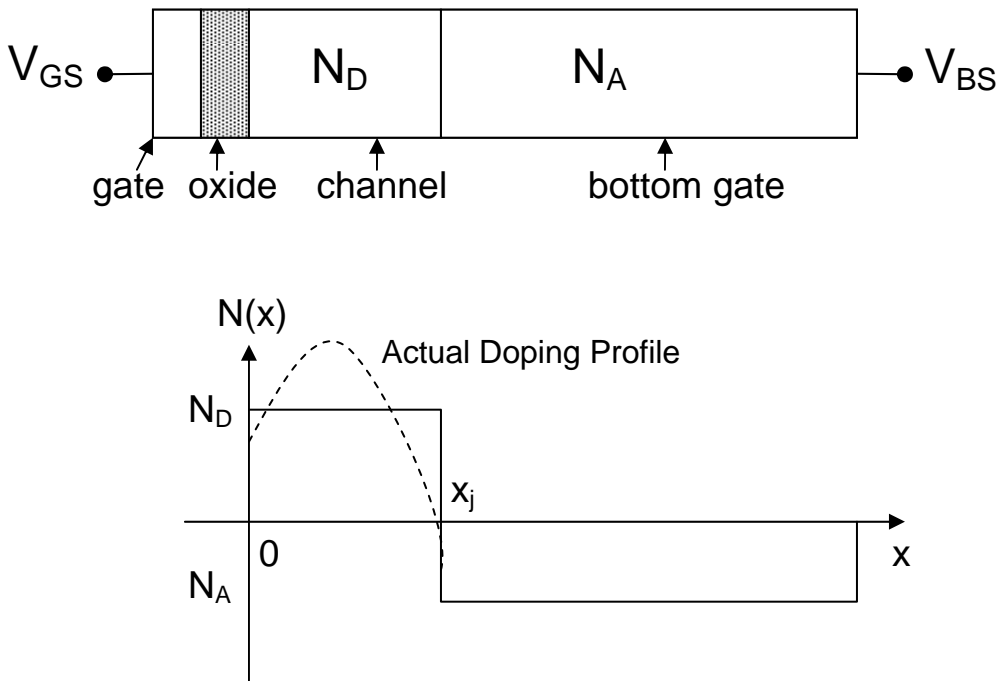


Figure 5-2 JFET doping density profile in the  $x$  direction ( $x=0$  is the oxide-semiconductor interface).

This equivalent box doping profile is shown in Fig. 5-2. The bottom-gate region is uniformly doped with an acceptor density of  $N_A$ . A metallurgical junction exists at the interface between the channel and bottom-gate regions at a distance  $x_j$  from the oxide-semiconductor interface. The built-in voltage  $V_{bi}$  for the channel/bottom-gate junction is

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

5-4

The top-gate oxide thickness is  $t_{ox}$ . The device has a nonzero flat-band voltage  $V_{FB}$  due to the presence of surface states and the work function difference between the top-gate electrode and the semiconductor. The source and bottom gate voltages are denoted  $V_s$  and  $V_{BS}$ , respectively, while the top-gate and drain biases are  $V_{GS}$  and  $V_{DS}$ . The source is grounded and is the reference.

With  $V_{GS} - V_{FB} > V_{DS} + V_{bi}$ , the top-gate region is in the accumulation mode. Under this condition, electrons accumulate near the channel surface (oxide-semiconductor interface). As the top gate voltage  $V_{GS}$  becomes more positive, the channel conductance increases because more electrons are attracted to the surface, and the drain current flowing between the drain and the source will increase with increasing  $V_{DS}$ .

Note that electrons in the channel have a lower mobility when the JFET is operating in the accumulation mode because of the existence of many surface states at the oxide-semiconductor interface.

When  $V_{GS}$  is reduced such that  $V(y) + V_{bi} > V_{GS} - V_{FB}$ , where  $V(y)$  is the channel potential at a  $y$  position along the channel, a partial depletion region appears in the surface region under the top gate. Electron accumulation only takes place between the source contact and the point  $y$ , and the region depleted of

electrons extends from the point  $y$  to the drain end. As a result, the surface region near the drain is no longer conductive.

As  $V_{GS}$  is reduced further, the surface depletion region will extend from the source to drain. This, together with the depletion region associated with the metallurgical junction of the bottom gate, forms a narrow conducting channel. Further reduction in the top-gate voltage and the bottom-gate voltage can cause the two depletion regions to overlap, a condition called the channel pinch-off.

When the top-gate voltage of the JFET is reduced such that the surface potential at the oxide-semiconductor interface becomes sufficiently negative, a significant number of holes will be attracted to the surface. If a large enough negative top-gate voltage is applied, the density of holes at the surface will exceed the doping density of the channel region, and the entire surface region of the JFET is inverted.

The different top-gate operating modes mentioned above will be analyzed in detailed in the following sections.

### **5.2.1 Depletion Mode**

The depletion mode occurs when

$$V_{TH} - V_{FB} < V_{GS} - V_{FB} < V(y) + V_{bi} \quad 5-5$$



where  $V_{TH}$  is the top-gate threshold voltage required to invert the surface,  $V_{GS}$  is the top-gate potential,  $V_{FB}$  is the flat-band voltage,  $V(y)$  is the channel potential, and  $V_{bi}$  is the top-gate built-in potential. The surface depletion region ( $0 < x < x_s$ ) and the bottom space-charge layer ( $x_n < x < x_j$ ) will form a channel through which electrons can flow when a drain bias is applied. Fig. 5-3 illustrates the charge distribution in the  $x$  direction at a point  $y$  in the depletion mode.

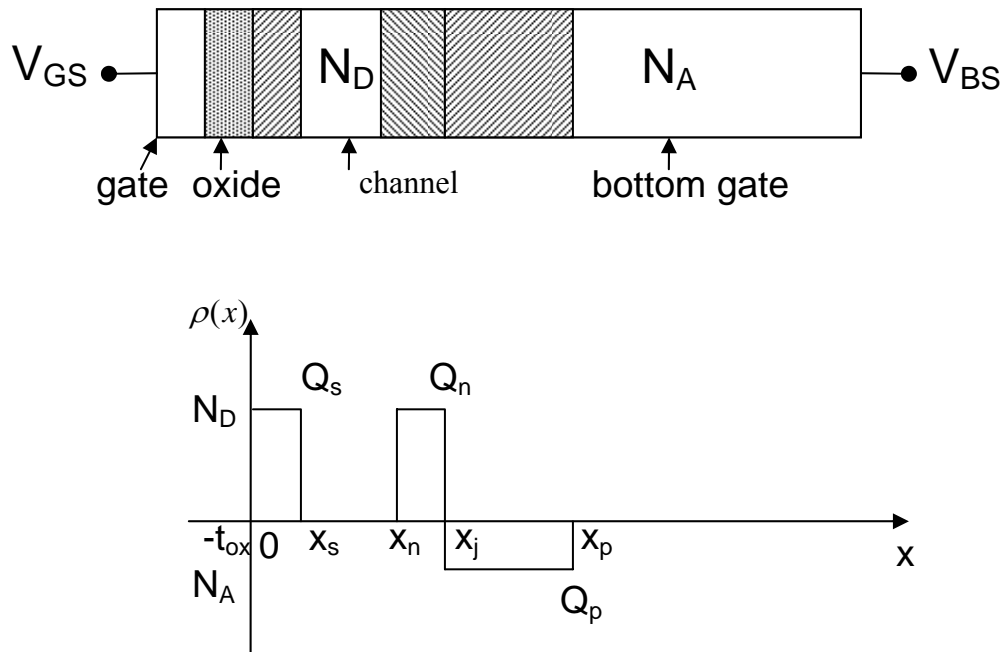


Figure 5-3 JFET one-dimensional structure with doping densities and the charge distribution in the  $x$  direction under the depletion mode ( $Q_s$  is the depletion charge in the surface region, and  $Q_n$  and  $Q_p$  are the depletion charges in the bottom n-region and p-region space charge regions, respectively).

The JFET cross section depicted in Fig.5-3 can be partitioned into the following regions:

- 1) oxide region:  $-t_{ox} < x < 0$ ;
- 2) surface depletion region:  $0 < x < x_s$ ;
- 3) channel region:  $x_s < x < x_n$ ;
- 4) n-side space-charge region:  $x_n < x < x_j$ ;
- 5) p-side space-charge region:  $x_j < x < x_p$ ;
- 6) bulk region:  $x_p < x < \infty$ .

In order to determine the potential distribution, we must solve the Poisson's equation

$$\frac{d^2 \psi}{dx^2} = -\frac{\rho}{\epsilon_s} \quad 5-6$$

The appropriate boundary conditions for the regions are (i.e., the potential must be continuous at the boundaries):

$$\begin{aligned} \psi(x) \Big|_{x=-t_{ox}} &= V_{GS} - V_{FB} \\ \psi(x) \Big|_{x=0^-} &= \psi(x) \Big|_{x=0^+} \\ \psi(x) \Big|_{x=x_s^-} &= \psi(x) \Big|_{x=x_s^+} \\ \psi(x) \Big|_{x=x_n^-} &= \psi(x) \Big|_{x=x_n^+} \\ \psi(x) \Big|_{x=x_j^-} &= \psi(x) \Big|_{x=x_j^+} \\ \psi(x) \Big|_{x=x_p} &= V_{BS} \end{aligned} \quad 5-7$$

Applying the Gauss's law at the interfaces between regions, we obtain additional conditions at the boundaries:

$$\begin{aligned} \epsilon_{ox} E(x) \Big|_{x=0^-} &= \epsilon_s E(x) \Big|_{x=0^+} \\ \epsilon_s E(x) \Big|_{x=x_s^-} &= \epsilon_s E(x) \Big|_{x=x_s^+} \end{aligned}$$

$$\begin{aligned}\varepsilon_s E(x)|_{x=x_n^-} &= \varepsilon_s E(x)|_{x=x_n^+} \\ \varepsilon_s E(x)|_{x=x_j^-} &= \varepsilon_s E(x)|_{x=x_j^+} \\ \varepsilon_s E(x)|_{x=x_p^-} &= \varepsilon_s E(x)|_{x=x_p^+}\end{aligned}$$

5-8

Solving the Poisson's equation in each of these regions, we can determine the potential distribution as

$$\begin{aligned}\psi(x) &= V_{GS} - V_{FB} - E_{ox}(x+t_{ox}), & -t_{ox} < x \leq 0 \\ \psi(x) &= \psi_{ch} - \frac{qN_D}{2\varepsilon_s}(x-t_s)^2 & 0 < x \leq x_s \\ \psi(x) &= \psi_{ch} & x_s < x \leq x_n \\ \psi(x) &= \psi_{ch} - \frac{qN_D}{2\varepsilon_s}(x-x_n)^2 & x_n < x \leq x_j \\ \psi(x) &= \frac{qN_A}{2\varepsilon_s}(x_p-x)^2 + V_{BS} & x_j < x \leq x_p \\ \psi(x) &= V_{BS} & x_p < x \leq \infty\end{aligned}$$

5-9

where

$$\psi_{ch} = V(y) + V_{bi}, \quad 5-10$$

$$x_n = x_j - \left( \frac{2\varepsilon_s}{qN_D} \left( \frac{N_A}{N_A + N_D} \right) (V(y) + V_{bi} - V_{BS}) \right)^{1/2} \quad 5-11$$

$$x_p = \left( \frac{2\varepsilon_s}{qN_A} \left( \frac{N_D}{N_A + N_D} \right) (V(y) + V_{bi} - V_{BS}) \right)^{1/2} + x_j \quad 5-12$$

$$x_s = \left( \frac{2\varepsilon_s}{qN_D} (\psi_{ch} - V_{GS} + V_{FB}) + \left( \frac{\varepsilon_s t_{ox}}{\varepsilon_{ox}} \right)^2 \right)^{1/2} - \left( \frac{\varepsilon_s t_{ox}}{\varepsilon_{ox}} \right) \quad 5-13$$

Note that both the surface depletion region and n-side space-charge layer increase with increasing channel potential. Also, the mobile electrons in the channel region are pushed away from the oxide-silicon interface when the channel potential is increased.

## 5.2.2 Inversion Mode

When the top-gate voltage of the JFET is reduced in such a way that the surface potential at the oxide-semiconductor interface becomes sufficiently negative, a significant number of holes will be induced near the surface. If a sufficiently negative top-gate voltage is applied, the density of holes at the surface will equal the channel doping density. The surface potential  $\psi_{inv}$  for this case is given by

$$\psi(x)|_{x=0} = \psi_s = \psi_{inv} \quad 5-14$$

We can determine an expression for  $\psi_{inv}$  by relating the hole concentration at the surface to the equilibrium hole concentration in the channel. The hole concentration at the surface is given by

$$p_s = N_A e^{-\frac{1}{V_T}(\psi_s - V_{BS})} \quad 5-15$$

where  $V_T$  is the thermal voltage. At the onset of inversion, the surface hole concentration will become equal to the channel doping density:

$$p_s \approx N_D \quad 5-16$$

Therefore, the surface potential at onset of inversion is

$$\psi_{inv} = V_T \ln\left(\frac{N_A}{N_D}\right) + V_{BS} \quad 5-17$$

In order to determine the top-gate voltage at which inversion occurs, we need to determine a relationship between  $V_{GS}$  and the

surface potential  $\psi_s$ . The surface potential can in general be expressed as

$$\psi(x)|_{x=0} = \psi_s = \psi_{ch} - \frac{qN_D}{2\epsilon_s} x_s^2 \quad 5-18$$

where  $x_s$  is given as

$$x_s = \left( \frac{2\epsilon_s}{qN_D} (\psi_{ch} - V_{GS} + V_{FB}) + \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right)^2 \right)^{1/2} - \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right) \quad 5-19$$

For onset of inversion,  $\psi_s = \psi_{inv}$  and (20) becomes

$$\left( \frac{2\epsilon_s}{qN_D} (\psi_{ch} - \psi_{inv}) \right)^{1/2} = \left( \frac{2\epsilon_s}{qN_D} (\psi_{ch} - V_{GS} + V_{FB}) + \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right)^2 \right)^{1/2} \quad 5-20$$

Solving for  $V_{GS}$ , the top-gate threshold voltage  $V_{TH}$  for inversion is

$$V_{TH} = V_{FB} + \psi_{inv} - \frac{1}{C_{ox}} (2q\epsilon_s N_D (\psi_{ch} - \psi_{inv}))^{1/2} \quad 5-21$$

where

$$C_{ox} = \frac{\epsilon_s}{t_{ox}} \quad 5-22$$

$$\psi_{ch} = V(y) + V_{bi} \quad 5-23$$

Thus, when  $V_{GS} < V_{TH}$ , the surface at a point  $y$  along the channel will become inverted, and the hole inversion charge  $Q_{inv}$  will be induced near the surface.

When the surface inversion becomes strong, the surface potential will not change much with a further decrease in the top-gate voltage, and the surface potential is said to be pinned. In other words, when the JFET is operating in the inversion mode, the

potential at the oxide-semiconductor interface remains pinned at  $\psi_{inv}$  and the potential variation throughout the semiconductor is independent of the top-gate voltage. A consequence of this surface potential pinning is that the surface depletion region, with the inversion layer of holes at the surface, also remains relatively constant and its thickness is given by

$$x_{Smax} = \left( \frac{2\epsilon_s}{qN_D} (\psi_{ch} - \psi_{inv}) \right)^{1/2} \quad \text{for } V_{GS} < V_{TH} \quad 5-24$$

The potential distribution in the channel depth direction under the inversion mode is essentially a special case of the depletion mode and can be determined by the following:

$$\begin{aligned} \psi(x) &= V_{GS} - V_{FB} - E_{ox}(x+t_{ox}) & -t_{ox} < x \leq 0 \\ \psi(x) &= \psi_{ch} - \frac{qN_D}{2\epsilon_s} (x - x_{smax})^2 & 0 < x \leq x_{smax} \\ \psi(x) &= \psi_{ch} & x_{smax} < x \leq x_n \\ \psi(x) &= \psi_{ch} - \frac{qN_D}{2\epsilon_s} (x - x_n)^2 & x_n < x \leq x_j \\ \psi(x) &= \frac{qN_A}{2\epsilon_s} (x_p - x)^2 + V_{BS} & x_j < x \leq x_p \\ \psi(x) &= V_{BS} & x_p < x \leq \infty \end{aligned} \quad 5-25$$

where

$$x_{smax} = \left( \frac{2\epsilon_s}{qN_D} (\psi_{ch} - \psi_{inv}) \right)^{1/2} \quad 5-26$$

$$E_{ox} = \frac{V_{GS} - V_{FB} - \psi_{inv}}{t_{ox}} \quad 5-27$$

If a channel exists between the surface depletion region and the n-side space-charge region at the onset of inversion, then it is impossible to pinch off the device with only the top-gate bias.

Pinch-off can only be achieved by decreasing the bottom gate voltage and increasing the drain voltage until the n-side space-charge region widens and touches the surface depletion region.

The charge distribution in the x direction at a point y along the channel under the inversion condition is illustrated in Fig. 5-4.

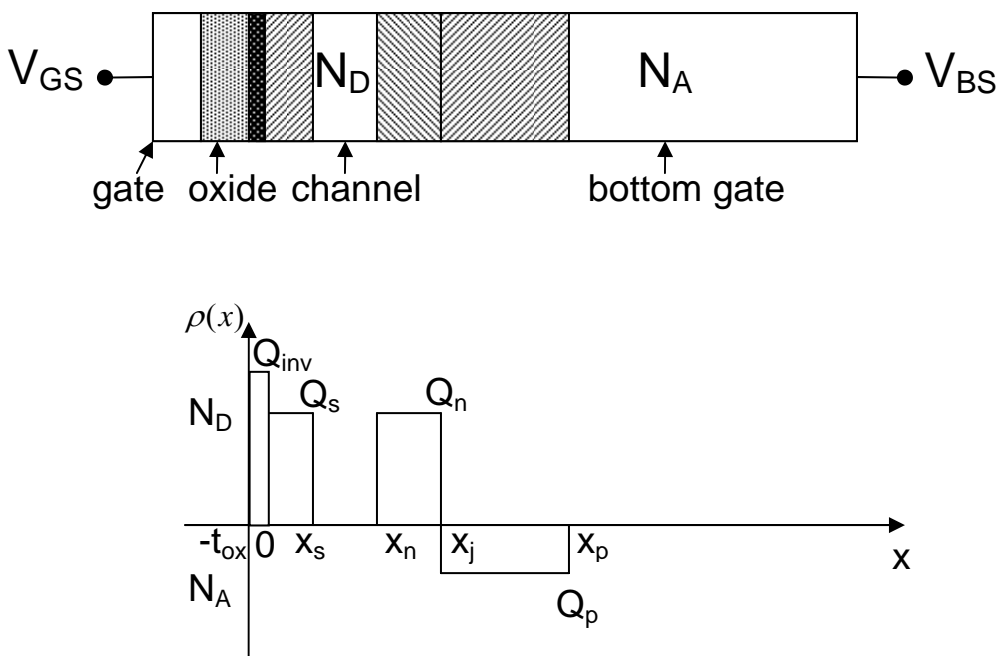


Figure 5-4 One-dimensional structure with doping densities and the charge distribution in the x direction under the inversion mode.

### 5.2.3 Pinch-off Mode

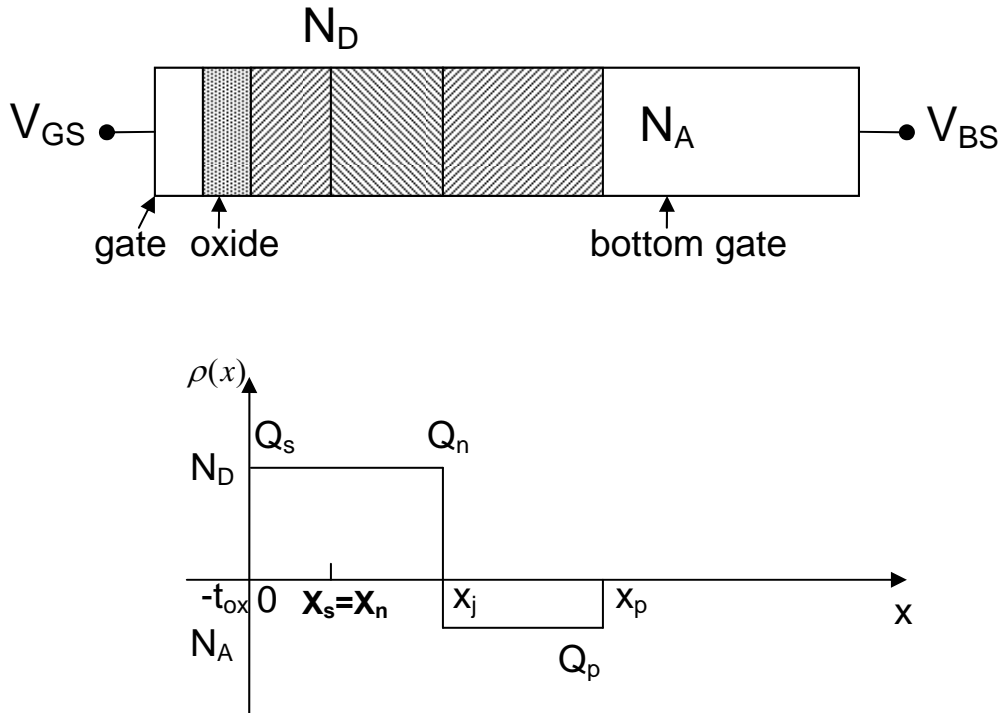


Figure 5-5 JFET doping density profile and the charge distribution in the x direction under the pinch-off mode

When the surface depletion region and n-side space-charge region touch each other, the channel is pinched off. The charge distribution in the x direction under the pinch-off condition is shown in Fig. 5-5. At and beyond the point y where the channel is pinched off, there are no mobile charges, and the JFET can be partitioned into the following regions:

- 1) oxide region:  $-t_{ox} < x < 0$ ;



- 2) depleted channel region:  $0 < x < x_j$ ;
- 3) p-side space-charge region:  $x_j < x < x_p$ ;
- 4) bulk region:  $x_p < x < \infty$ .

The potential must be continuous at the boundaries, giving

$$\begin{aligned}
 \psi(x)|_{x=-t_{ox}} &= V_{GS} - V_{FB} \\
 \psi(x)|_{x=0^-} &= \psi(x)|_{x=0^+} \\
 \psi(x)|_{x=x_j^-} &= \psi(x)|_{x=x_j^+} \\
 \psi(x)|_{x=x_p} &= V_{BS}
 \end{aligned} \tag{5-28}$$

From the Gauss's law, we can formulate the additional conditions:

$$\begin{aligned}
 \epsilon_{ox} E(x)|_{x=-t_{ox}} &= 0 \\
 \epsilon_s E(x)|_{x=x_p} &= 0 \\
 \epsilon_s E(x)|_{x=x_j^-} &= \epsilon_s E(x)|_{x=x_j^+} \\
 \epsilon_s E(x)|_{x=0^-} &= \epsilon_s E(x)|_{x=0^+}
 \end{aligned} \tag{5-29}$$

Using the one-dimensional Poisson's equation and the depletion approximation, together with the above boundary conditions, we can determine the potential distribution in the  $x$  direction at the point  $y$  where pinch-off occurs:

$$\begin{aligned}
 \psi(x) &= V_{GS} - V_{FB} - E_{ox}(x + t_{ox}), & -t_{ox} < x \leq 0 \\
 \psi(x) &= \psi_{ch} - \frac{qN_D}{2\epsilon_s}(x - x_s)^2 & 0 < x \leq x_j \\
 \psi(x) &= \frac{qN_A}{2\epsilon_s}(x_p - x)^2 + V_{BS} & x_j < x \leq x_p \\
 \psi(x) &= V_{BS} & x_p < x \leq \infty
 \end{aligned} \tag{5-30}$$

where

$$\psi_{ch} = \left( \frac{N_A + N_D}{N_D} \right) \left( (V_{GS} - V_{FB} + V_i - V_{BS} + \left( \frac{\sqrt{V_{ox}}}{2} \right)^2)^{1/2} + V_{BS} \right) \tag{5-31}$$

$$V_i = \frac{qN_D x_j^2}{2\epsilon_s} \left(1 + 2 \frac{\epsilon_s t_{ox}}{\epsilon_{ox} x_j}\right) \quad 5-32$$

$$V_{ox} = \frac{2qN_A x_j^2}{\epsilon_s} \left(1 + \frac{\epsilon_s t_{ox}}{\epsilon_{ox} x_j}\right)^2 \quad 5-33$$

$$x_s = x_j - \left(\frac{2\epsilon_s}{qN_D} \left(\frac{N_A}{N_A + N_D}\right) (\psi_{ch} - V_{BS})\right)^{1/2} \quad 5-34$$

$$x_p = x_j + \frac{N_D}{N_A} (x_j - x_s) \quad 5-35$$

### 5.2.4 Accumulation Mode

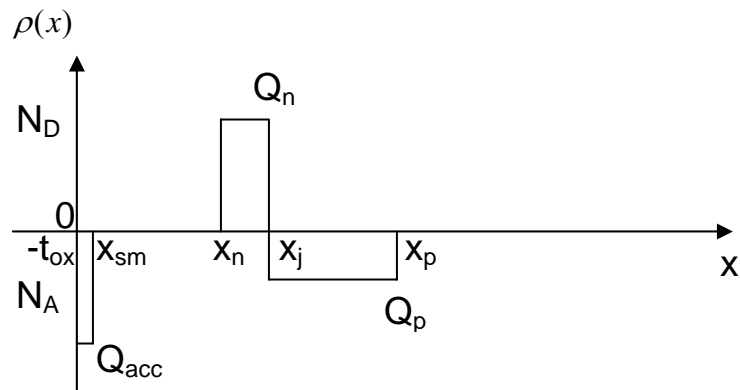
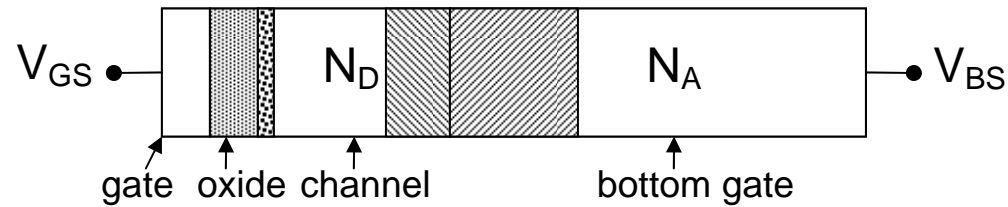


Figure 5-6 JFET doping density profile and the charge distribution in the x direction under the accumulation mode.

The accumulation of electrons in the surface region occurs when

$$V_{GS} - V_{FB} > V(y) + V_{bi} \quad 5-36$$

The charge distribution in the  $x$  direction under the accumulation condition is shown in Fig. 5-6. Under such a condition, the JFET is partitioned into the following regions:

- 1) oxide region:  $-t_{ox} < x < 0$ ;
- 2) surface accumulation region:  $0 < x < x_s$ ;
- 3) neutral channel region:  $x_s < x < x_n$ ;
- 4) n-side space-charge region:  $x_n < x < x_j$ ;
- 5) p-side space-charge region:  $x_j < x < x_p$ ;
- 6) bulk region:  $x_p < x < \infty$ .

Again, we can solve the Poisson's equation to determine the potential distribution within the oxide, channel, n-side space charge, p-side space charge, and bulk regions under the accumulation mode. In the accumulated surface region, the depletion approximation no longer applies, and we must use the Boltzmann relationship to describe the electrons in the region:

$$n(x) = n_{no} e^{\frac{1}{V_T}(\psi(x) - \psi_{ch})} \quad 5-37$$

where  $n_{no}$  is the equilibrium electron concentration,  $\psi(x)$  is the potential along the  $x$  direction, and  $\psi_{ch}$  is the potential in the channel region (i.e.,  $\psi_{ch} = V(y) + V_{bi}$ ). Combining the Poisson's equation and the Boltzmann relation yields,

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon_s} = -\frac{qN_D}{\epsilon_s} \left(1 - e^{\frac{1}{V_T}(\psi(x) - \psi_{ch})}\right) \quad 0 < x \leq x_s \quad 5-38$$

Using the above expression, the potential distribution within the accumulation region can be determined.

In addition, we can obtain the following set of equation to describe the potential distribution in other regions:

$$\begin{aligned}
\psi(x) &= V_{GS} - V_{FB} - E_{ox}(x + t_{ox}) & -t_{ox} < x \leq 0 \\
\psi(x) &= V_T \ln(\tan^2((\frac{qN_D}{2\epsilon_s V_T})^{1/2}(K - x)) + 1) + \psi_{ch} & 0 < x \leq x_s \\
\psi(x) &= \psi_{ch} & x_s < x \leq x_n \\
\psi(x) &= \psi_{ch} - \frac{qN_D}{2\epsilon_s}(x - x_n)^2 & x_n < x \leq x_j \\
\psi(x) &= \frac{qN_A}{2\epsilon_s}(x_p - x)^2 + V_{BS} & x_j < x \leq x_p \\
\psi(x) &= V_{BS} & x_p < x \leq \infty
\end{aligned} \tag{5-39}$$

where  $E_{ox}$  and  $\psi_s$  are determined by the simultaneous solution of

$$E_{ox} = \frac{\epsilon_s}{\epsilon_{ox}} \left( \frac{2qV_T N_D}{\epsilon_s} \right)^{1/2} (e^{\beta(\psi_s - \psi_{ch})} - 1)^{1/2} \tag{5-40}$$

$$\psi_s = V_{GS} - V_{FB} - E_{ox} t_{ox} \tag{5-41}$$

where

$$\psi_{ch} = V(y) + V_{bi} \tag{5-42}$$

$$K = \left( \frac{2V_T \epsilon_s}{qN_D} \right)^{1/2} \tan^{-1} \left( e^{\frac{1}{V_T}(\psi(x) - \psi_{ch})} - 1 \right)^{1/2} \tag{5-43}$$

$$x_n = x_j - \left( \frac{2\epsilon_s}{qN_D} \left( \frac{N_A}{N_A + N_D} \right) (V(y) + V_{bi} - V_{BS}) \right)^{1/2} \tag{5-44}$$

$$x_p = \left( \frac{2\epsilon_s}{qN_A} \left( \frac{N_D}{N_A + N_D} \right) (V(y) + V_{bi} - V_{BS}) \right)^{1/2} + x_j$$

### 5.3 JFET Model Development

In the section, a compact model to describe the JFET's current-voltage characteristics under the various operations will be developed.

#### 5.3.1 Linear Operation

Consider only the drift tendency, the drain current in the JFET under the linear operation is given by

$$I_{DS} = -W_{eff} \mu(V) Q(V) \frac{dV}{dy} \quad 5-45$$

where  $W_{eff}$  is the effective channel width,  $\mu(V)$  is the voltage dependent mobility and  $Q(V)$  is the net mobile charge in the conducting channel.

Under conditions of surface accumulation, the charge  $Q(V)$  is

$$Q(V) = Q_{total}^{acc} = Q^{acc} + Q_n + Q_i \quad 5-46$$

where

$$Q^{acc} = -\frac{\epsilon_s}{t_{ox}} (V_{GS} - V_{FB} - V_{bi}) \quad 5-47$$

is the accumulated electron charge in the surface region,

$$Q_n = qN_D \left( \frac{2}{qN_D} \left( \frac{N_A}{N_A + N_D} \right) (V(y) + V_{bi} - V_{BS}) \right)^{1/2} \quad 5-48$$

is the depletion charge in the n-side space-charge region, and

$$Q_i = -qN_D x_j \quad 5-49$$

is the electron charge in the channel.

Under conditions of the depletion mode, the charge is given as

$$Q(V) = Q_{total}^{dep} = Q^{dep} + Q_n + Q_i \quad 5-50$$

where

$$Q^{dep} = qN_D \left( \left( \frac{2\epsilon_s}{qN_D} (V_{bi} - V_{GS} + V_{FB}) + \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right)^2 \right)^{1/2} - \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right) \right) \quad 5-51$$

The above are piece-wise equations for the accumulation and depletion modes, which is likely to give rise to convergence problem when calculating the transition region between the two different modes. The effective charge  $Q_{eff0}$  can be used as a smoothing function for the accumulation and depletion modes [6]:

$$Q_{eff0}(V_{GS}) = f^{-1}(V_{GS}', Q_{dep}') \quad 5-52$$

where

$$f(y) = [Q^{acc} + \frac{1}{2} [(y - Q^{acc} - C) + \sqrt{(y - Q^{acc} - C)^2 - 4 \cdot C \cdot Q^{acc}}]] \quad 5-53$$

$$V_{GS}' = V_{GS} \cos \alpha + Q_{dep}' \sin \alpha \quad 5-54$$

$$Q_{dep}' = -V_{GS} \sin \alpha + Q_{dep}' \cos \alpha \quad 5-55$$

$$\alpha = \tan^{-1}(C_{ox}) \quad 5-56$$

C is a fitting parameter which controls the transition region shape.

When including the effect of the drain voltage, the effective charge  $Q_{eff0}$  becomes  $Q_{eff}$ , and it can be expressed as [7]

$$Q_{eff}(y) = Q_{eff0}(1 - N \cdot V(y)) \quad 5-57$$

$$N = C_{ox} \cdot q \epsilon_s \left( \frac{2\epsilon_s}{N_D} (-V_{GS} + V_{FB} + V_{bi}) + \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right)^{-1/2} \quad 5-58$$

So, replacing  $Q(V)$  with  $Q_{eff}$  in (46) yields an expression for the drain current valid for the accumulation and depletion modes under the linear operation.

Another important physics is that, under the accumulation mode, a large portion of the drain current is flowing near the surface, and the free-carrier mobility will be affected by the surface scattering due to the vertical electric field. On the other hand, under the depletion mode, the current is flowing in the channel away from the surface region where the mobility is not affected by the interface condition. The following can be used to describe the free-carrier mobility in both modes of operation:

$$\mu_{eff} = \frac{\mu_0}{1 + \ln(1 + \exp(\theta(V_{GS} - V_{FB} - V_{bi})))} \quad 5-59$$

where  $\mu_{eff}$  is effective mobility,  $\theta$  is the mobility modulation factor and  $\mu_0$  is the low-field mobility. The free-carrier velocity is given by [3]

$$v(y) = \frac{\mu_{eff} E(y)}{1 - \frac{E(y)}{E_{sat}}} \quad 5-60$$

$E(x)$  is the electric field and  $E_{sat}$  corresponds to the critical electric field at which the free-carrier velocity becomes saturated.

Using the concept of  $Q_{eff}$ , we obtain

$$I_{DS} = -W_{eff} (Q^{eff} + Q_n + Q_i) v(y) \quad 5-61$$

Combining the above equations we have

$$I_{DS} = \frac{E(y)}{E_{sat}} I_{DS} - W_{eff} (Q_{eff} (1 - N \cdot V(y)) + Q_n + Q_i) \mu_0 E(y) \quad 5-62$$

Substituting  $E(y) = dV(y)/dy$  into (63) and integrating it from  $y=0$  to  $y=L$  and  $V(y) = V_s$  to  $V(y) = V_d$ , we arrive at the following expression for the drain current for the top-gate accumulation and depletion modes under the linear operation:

$$I_{DS} = -\frac{\frac{W_{eff}}{L_{eff}} \mu_{eff}}{1 - \frac{V_{DS}}{E_{sat} \cdot L_{eff}}} \left( Q_{eff} \left( V_{DS} - \frac{N}{2} V_{DS}^2 \right) + \frac{2}{3} M \left( (V_{DS} + V_{bi} - V_{BS})^{\frac{3}{2}} - (V_{bi} - V_{BS})^{\frac{3}{2}} \right) + Q_i \cdot V_{DS} \right) \quad 5-63$$

where

$$M = \left( 2q \cdot \frac{N_A N_D}{N_A + N_D} \right)^{\frac{1}{2}} \quad 5-64$$

As  $V_{GS}$  is decreased more and more, eventually the surface inversion occurs and the surface depletion layer is limited to its maximum thickness  $x_{smax}$ . Under this condition, the surface potential won't change with a further decrease in the top-gate voltage, a phenomena called the pinning effect. Thus, the drain current remains unchanged with further reduced top-gate voltage. Due to the pinning effect, the top-gate voltage  $V_{GS}$  for the inversion mode operation is essentially limited to  $V_{TH}$ , and the following effective top-gate voltage  $V_{GS_{eff}}$  is valid for the non-inversion and inversion modes [3]:



$$V_{GS_{eff}} = V_{TH} \cdot \left(1 - \frac{\log(1 + \exp(B \cdot (1 - \frac{V_{GS}}{V_{TH}})))}{\log(1 + \exp(B))}\right) \quad 5-65$$

where B is a fitting parameter with a typical value around 1,  $V_{TH}$  is the threshold voltage of the inversion mode from (22):

$$V_{TH} = V_{FB} + V_T \ln\left(\frac{N_A}{N_D}\right) + V_{BS} - \frac{1}{C_{ox}} (2q\epsilon_s N_D (V_{DS} + V_{bi} - V_T \ln\left(\frac{N_A}{N_D}\right) + V_{BS}))^{1/2} \quad 5-66$$

Thus, replacing  $V_{GS}$  with  $V_{GS_{eff}}$  in (64), we obtain a single expression to model the drain current for all the accumulation, depletion, and inversion modes under the linear operation with a high degree of continuity and convergence.

### 5.3.2 Saturation Operation

When the drain voltage increases, the depletion regions will expand, the channel is pinched off when the two depletion regions touch each other at the drain end, and  $I_{DS}$  increases only slightly with increasing  $V_{DS}$  beyond this point. The drain voltage causes the onset of pinch-off is the saturation drain voltage,  $V_{DSat}$ , defined by

$$g_{DS} = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{DS}=V_{DSat}} = 0 \quad 5-67$$

It would be ideal to solve for the saturation drain voltage directly, however, due to the complexity of the drain current equation this is not possible. The other way is to use the Newton-Raphson iteration to determine such a voltage. It's determined by evaluating the drain current at the saturated drain voltage using

$$I_{DSat} = I_{DS}(V_{DSat}) \quad 5-68$$

Thus, for the case  $V_{DS} > V_{DSat}$  (i.e., saturation operation), we can extend the validity of (64) by replacing  $V_{DS}$  with the effective drain voltage  $V_{Deff}$ . In other words, when replacing  $V_{GS}$  with  $V_{GSeff}$  and  $V_{DS}$  with  $V_{Deff}$  in (64), the resulting single equation is capable of describing the drain current for all the accumulation, depletion, and inversion modes under both the linear and saturation operations.

When  $V_{DS}$  increases beyond  $V_{Dsat}$ , the drain current is not entirely independent of the drain bias, as the pinch-off point moves toward the source and the effective channel length is reduced. To account for this effect, the term  $(1+\lambda V_{DS})$ , where  $\lambda$  is the channel length modulation [3] is multiplied to the right-hand side of (64).

### 5.3.3 Cut-Off Operation

For a sufficiently large applied bottom-gate voltage, the entire channel becomes depleted (i.e., channel cut-off), and the drain current exhibits an exponential decay vs. increasing gate voltage. This behavior can be included in the drain current in (64) by introducing the following effective bottom-gate voltage [3]:

$$V_{BSeff} = mV_T \ln(1 + \exp(\frac{V_{BS} - V_p}{mV_T})) + V_p \quad 5-69$$

where  $V_p$  is the pinch-off voltage, and  $m$  is the swing factor. The pinch-off voltage is determined from the transition point between the above and below cut-off regions, and  $V_p$  can be calculated from (12) and (14) by letting the channel height at the source end to be zero:

$$V_p = V_{bi} - \left( \frac{x_j + \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} - \left( \frac{2\epsilon_s}{qN_D} (V_{bi} - V_{GS} + V_{FB}) + \left( \frac{\epsilon_s t_{ox}}{\epsilon_{ox}} \right)^2 \right)^{\frac{1}{2}}}{\frac{2\epsilon_s}{qN_D} \frac{N_A}{N_A + N_D}} \right)^2 \quad 5-70$$

Thus, replacing  $V_{BS}$  with  $V_{BSeff}$  in (64), together with the use of  $V_{GSeff}$  and  $V_{Deff}$ , allows one to calculate the current-voltage

characteristics of the 4-terminal JFET with an oxide top-gate for all the accumulation, depletion, and inversion modes under all the linear, saturation, and cut-off operations. The single expression makes the JFET model compact and robust for analog circuit simulations.

The modeling of the parasitic junction diodes, capacitances, and temperature effect of the JFET has been reported previously and will not be reiterated here [3, 6].

#### **5.4 Model Results**

Two n-channel JFETs having 3- and 14- $\mu\text{m}$  channel lengths fabricated using the SOI CMOS technology at Texas Instruments were considered, and their I-V characteristics calculated from the JFET model and obtained from measurements were compared.

Figs. 5-7(a) and (b) show the drain current vs. drain voltage characteristics of the 3- and 14- $\mu\text{m}$  JFETs, respectively, calculated from the present model and obtained from measurements for a zero bottom-gate voltage and different top-gate voltages. It is demonstrated that the present model is capable of producing very accurate and smooth I-V curves. Similar results for the case a -2.5 V bottom-gate voltage are given in Figs. 5-8(a) and (b). Again, the model shows a good agreement with measured data. Note that for the case of 3- $\mu\text{m}$  JFET operated at  $V_{\text{BS}} = -2.5$  V and  $V_{\text{GS}} = -$

5 V, the drain current is very low because the channel is cut-off at this bias condition. Figs. 5-9(a) and (b) show the very good fit of the new model to experimental data for the drain current vs. top-gate voltage characteristics of the 3- and 14- $\mu\text{m}$  JFETs, respectively, with a smooth transition from the above cut-off to cut-off region. For the 3- $\mu\text{m}$  JFET, we can see clearly that with the bottom-gate voltage equals to zero, the channel can't be fully cut off even if the top-gate voltage is sufficiently low. But with the bottom gate voltage equals to -2.5 V, the channel can be fully cut off when the top-gate voltage reaches around -5 V. Similar observations can be found in the 14- $\mu\text{m}$  JFET.

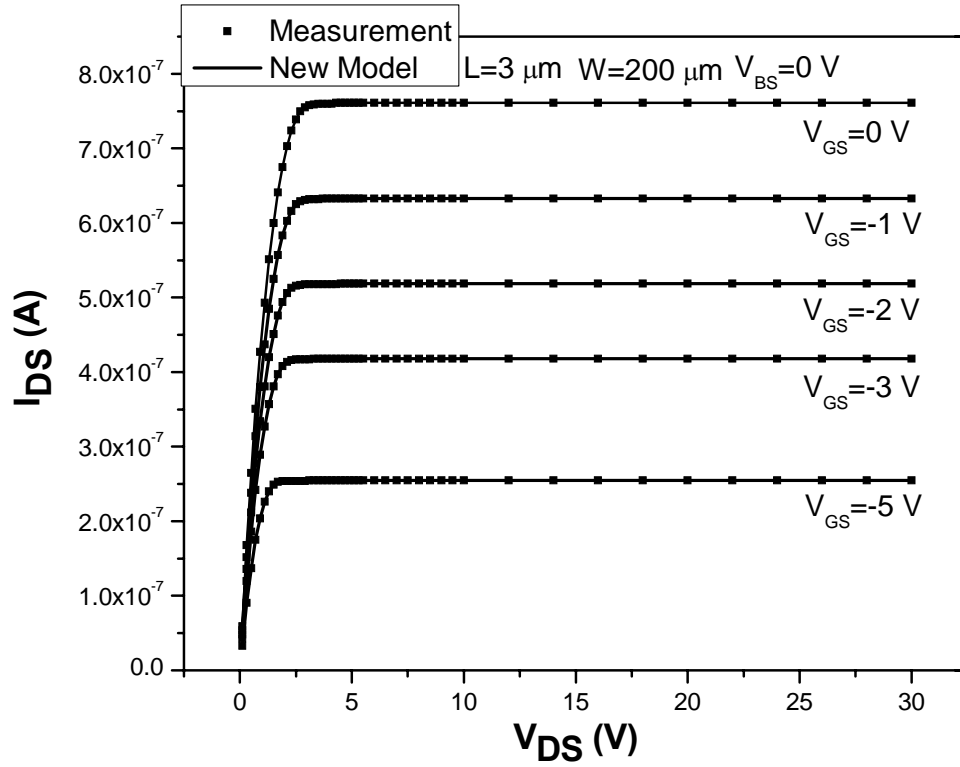


Figure 5-7(a)  $I_{DS}$  versus  $V_{DS}$  characteristics of  $L = 3 \mu\text{m}$ ,  $W = 200 \mu\text{m}$  JFET obtained from model calculations and measurements for  $V_{BS} = 0$  and different  $V_{GS}$ .

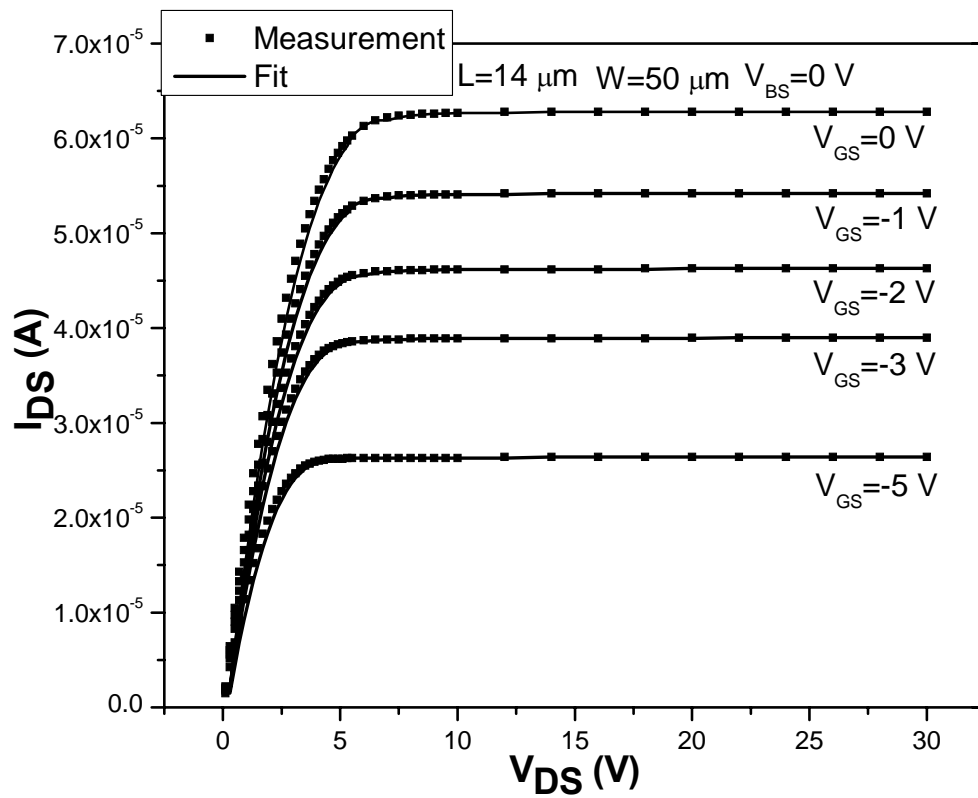


Figure 5-7(b)  $I_{DS}$  versus  $V_{DS}$  characteristics of  $L = 14 \mu\text{m}$ ,  $W = 50 \mu\text{m}$  JFET obtained from model calculations and measurements for  $V_{BS} = 0$  and different  $V_{GS}$ .

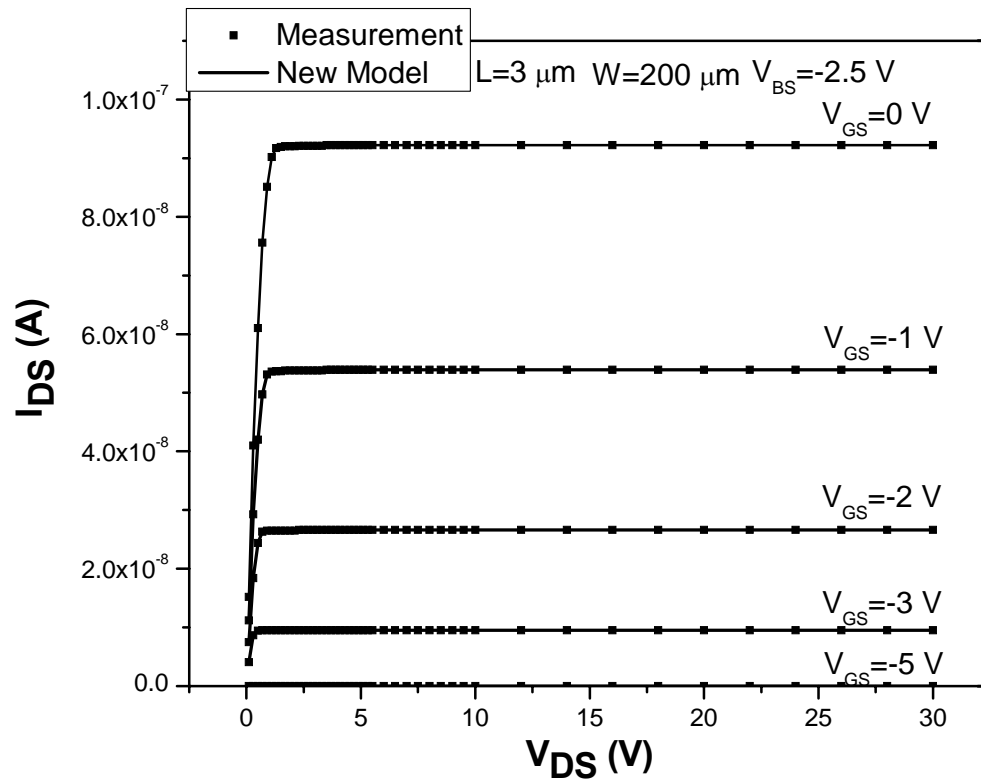


Figure 5-8(a)  $I_{DS}$  versus  $V_{DS}$  characteristics of  $L = 3 \mu\text{m}$ ,  $W = 200 \mu\text{m}$  JFET obtained from model calculations and measurements for  $V_{BS} = -2.5 \text{ V}$  and different  $V_{GS}$ .



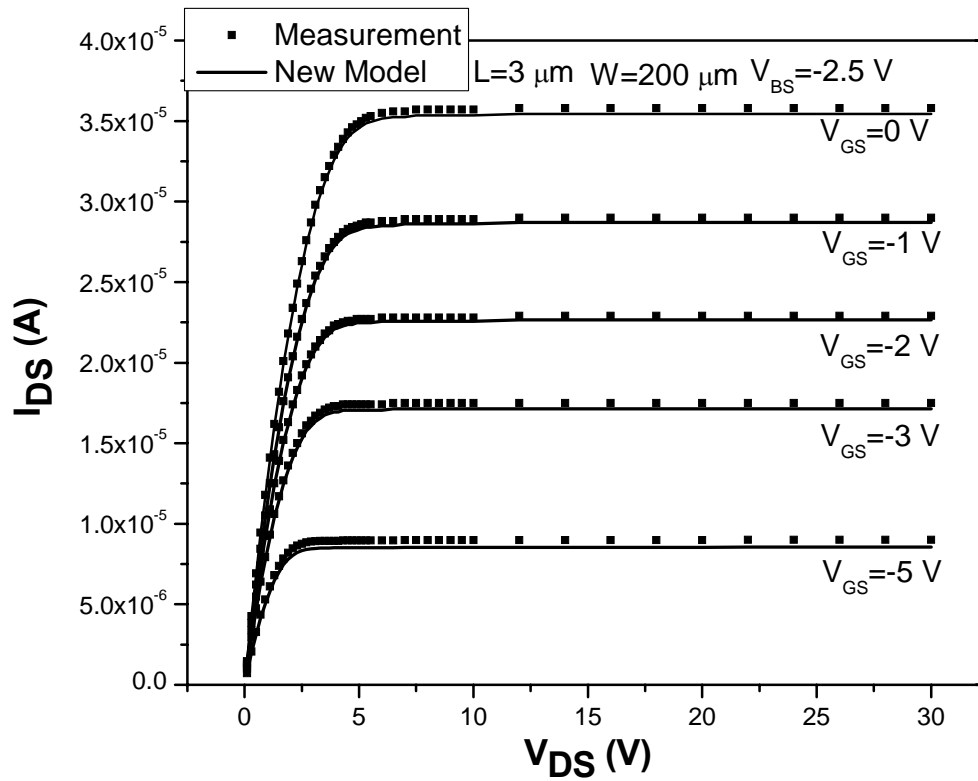


Figure 5-8(b)  $I_{DS}$  versus  $V_{DS}$  characteristics of  $L = 14 \mu\text{m}$ ,  $W = 50 \mu\text{m}$  JFET obtained from model calculations and measurements for  $V_{BS} = -2.5 \text{ V}$  and different  $V_{GS}$ .

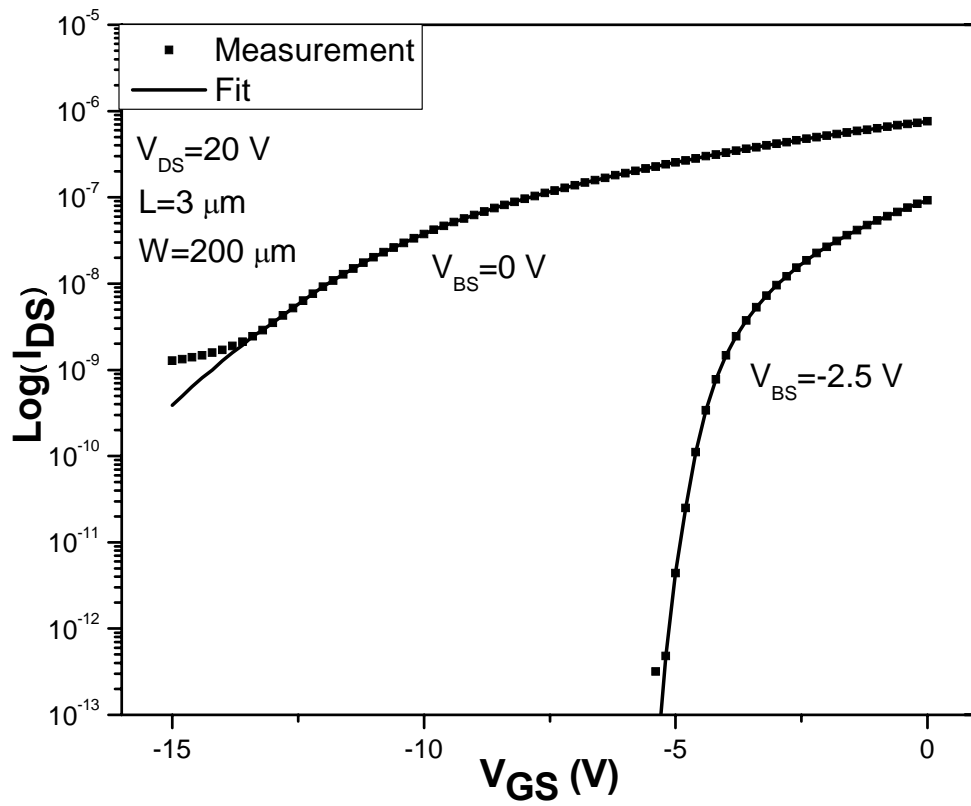


Figure 5-9(a)  $I_{DS}$  versus  $V_{GS}$  characteristics of  $L = 3 \mu\text{m}$ ,  $W = 200 \mu\text{m}$  JFET obtained from model calculations and measurements for two different  $V_{BS}$ .

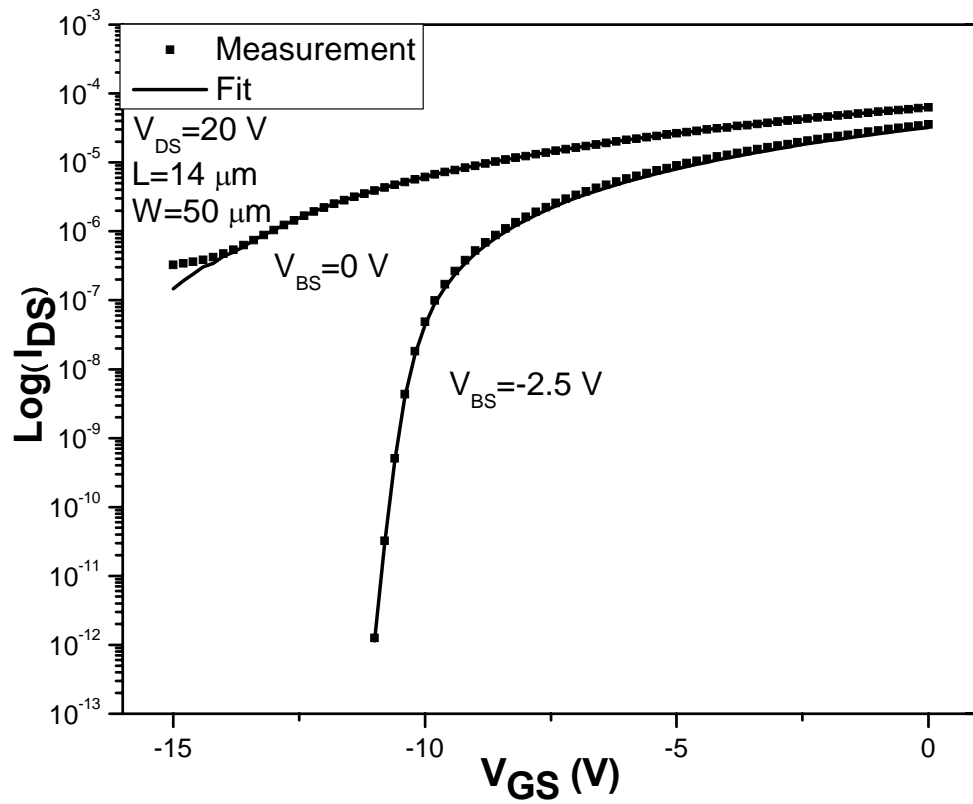


Figure 5-9(b)  $I_{DS}$  versus  $V_{GS}$  characteristics of  $L = 14 \text{ } \mu\text{m}$ ,  $W = 50 \text{ } \mu\text{m}$  JFET obtained from model calculations and measurements for two different  $V_{BS}$ .

## **5.5 Conclusions**

Junction field-effect transistor (JFET) with an oxide top-gate has been used some analog circuit applications, but a full analysis of such a device is absent in the literature. In this chapter, a compact model for this device under the different operation modes has been developed. A single expression has been used as the backbone of the JFET model to describe comprehensively and accurately the current-voltage characteristics of the JFET. The model has been verified against experimental data measured from JFETs fabricated Texas Instruments.

## **REFERENCES**

- [1] Colin C. McAndrew. "An accurate JFET and 3 terminal diffused resistor model", Nanotech Compact Modeling Workshop, vol. 2, 2004.
- [2] Juin J. Liou and Y. Yue. "An improved model for four-terminal junction field-effect transistors". IEEE Trans. Electron Devices, 1996.
- [3] H. Ding, Juin J. Liou, etc. "A new model for four-terminal junction field-effect transistors". Solid-State Electronics, Jan. 2006.
- [4] G. R. Rao, "An accurate model for a depletion mode IGFET used as a load device," Solid-State Electronics., vol. 21, pp. 711-714, May 1978.
- [5] S. M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons Inc, Mar. 1982.
- [6] H. Ding, Juin J. Liou, etc. "An improved junction capacitance model for junction field-effect transistors", Solid-State Electronics, July, 2006.
- [7] BSIM4.2.1 Manual, 2001.