Hot Carrier Effect On Ldmos Transistors

Liangjun Jiang
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HOT CARRIER EFFECT ON LDMOS TRANSISTORS

By

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M.S. Zhejiang University, 2001
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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

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2007

Major Professor: Jiann S. Yuan
ABSTRACT

One of the main problems encountered when scaling down is the hot carrier induced degradation of MOSFETs. This problem has been studied intensively during the past decade, under both static and dynamic stress conditions. In this period it has evolved from a more or less academic research topic to one of the most stringent constraints guaranteeing the lifetime of sub-micron devices. New drain engineering technique leads to the extensive usage of lateral doped drain structures. In these devices the peak of the lateral field is lowered by reducing the doping concentration near the drain and by providing a smooth junction transition instead of an abrupt one. Therefore, the amount of hot carrier generation for a given supply voltage and the influence of a certain physical damage on the electrical characteristics is decreased dramatically.

A complete understanding of the hot carrier degradation problem in sub-micron 0.25um LD MOSFETs is presented in this work. First we discuss the degradation mechanisms observed under, for circuit operation, somewhat artificial but well-controlled uniform-substrate hot electron and substrate hot-hole injection conditions. Then the more realistic case of static channel hot carrier degradation is treated, and some important process-related effects are illustrated, followed by the behavior under the most relevant case for real operation, namely dynamic degradation. An Accurate and practical parameter extraction is used to obtain the LD MOSFETs model parameters, with the experiment verification. Good agreement between the model simulation and experiment is achieved. The gate charge transfer performance is examined to demonstrate the hot carrier effect. Furthermore, In order to understand the dynamic stress on the LD MOSFET and its effect on RF circuit, the hot-carrier injection experiment in which dynamic
stress with different duty cycle applied to a LD MOS transistor is presented. A Class-C power amplifier is used to as an example to demonstrate the effect of dynamic stress on RF circuit performance. Finally, the strategy for improving hot carrier reliability and a forecast of the hot carrier reliability problem for nano-technologies are discussed.

The main contribution of this work is, it systemically research the hot carrier reliability issue on the sub-micron lateral doped drain MOSFETs, which is induced by static and dynamic voltage stress; The stress condition mimics the typical application scenarios of LD MOSFET. Model parameters extraction technique is introduced with the aid of the current device modeling tools, the performance degradation model can be easily implement into the existing computer-aided tools. Therefore, circuit performance degradation can be accurately estimated in the design stage.

CMOS technologies are constantly scaled down. The production on 65 nm is on the market. With the reduction in geometries, the devices become more vulnerable to hot carrier injection (HCI). HCI reliability is a must for designs implemented with new processes. Reliability simulation needs to be implemented in PDK libraries located on the modeling stage. The use of professional tools is a prerequisite to develop accurate device models, from DC to GHz, including noise modeling and nonlinear HF effects, within a reasonable time. Designers need to learn to design for reliability and they should be educated on additional reliability analyses. The value is the reduction of failure and redesign costs.
ACKNOWLEDGMENTS

I would like to express my sincere gratitude and appreciation to my advisor, Professor J. S. Yuan, for providing me with the unique opportunity to work in the research area of semiconductor device modeling and reliability, for his expert guidance and mentorship, and for his encouragement and support at all levels. I would also like to thank my committee members for reading this dissertation and offering constructive comments.

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Also, the research in this dissertation has been supported in part by the Enpirion Company and Semtech Incorporation. I have appreciated the financial support of the Department of Electrical Engineering, University of Central Florida during the years of my Ph.D. study.

Finally, I would like to thank my family for their life-long love and support. I especially owe much to my parents for offering their invaluable practical experience to help me debug the life difficulties during the period.
# TABLE OF CONTENTS

LIST OF FIGURES ..................................................................................................................... viii

LIST OF TABLES ......................................................................................................................... xi

LIST OF ACRONYMS AND ABBREVIATIONS ........................................................................ xii

1 CHAPTER ONE: INTRODUCTION ............................................................................................. 1

   1.1 Motivation ....................................................................................................................... 1
   1.2 Research Goals ................................................................................................................ 2
   1.3 Outlines ........................................................................................................................... 2

2 CHAPTER TWO: DEVICE MODELING PROCESS ..................................................................... 3

   2.1 Introduction ..................................................................................................................... 3
   2.2 General Process ............................................................................................................... 3
   2.3 BSIM3 Model and Equivalent Circuit Model ................................................................. 9
   2.4 Device ........................................................................................................................... 11
       2.4.1 Technology and LDMOS Description .................................................................. 12
       2.4.2 The Performance of the LDMOS .......................................................................... 13
       2.4.3 Model Parameter Extraction ................................................................................. 17

3 CHAPTER THREE: DEVICE RELIABILITY ........................................................................... 22

   3.1 Introduction ................................................................................................................... 22
   3.2 Hot Carrier Injection of LD MOSFETs ........................................................................ 36

4 CHAPTER FOUR: CIRCUIT DESIGN AND PERFORMANCE ANALYSIS ............................. 49

   4.1 Introduction ................................................................................................................... 49
LIST OF FIGURES

Fig. 2.1: The device modeling process ................................................................. 4
Fig. 2.2: From DC to CV to S-parameters ............................................................ 6
Fig. 2.3: Depicts this extension of modeling towards nonlinear HF ................. 7
Fig. 2.4: How harmonic balance simulators work ............................................. 8
Fig. 2.5: A RF equivalent subcircuit model for nMOS transistor ....................... 11
Fig. 2.6: The cross section of an LDMOS transistor .......................................... 12
Fig. 2.7: Drain current versus drain-source voltage (nMOS transistor) ............. 14
Fig. 2.8: Drain current versus gate-source voltage (nMOS transistor) ............... 14
Fig. 2.9: Drain current versus grain source voltage (pMOS Transistor) ............ 15
Fig. 2.10: Drain current versus gate-source voltage (pMOS) .............................. 15
Fig. 2.11: Reverse Bias Characteristic (a) nMOSFET (b)pMOSFET .................. 16
Fig. 2.12: Drain-source current versus drain-source voltage ............................. 19
Fig. 2.13: (a) $S_{11}$, (b) $S_{12}$, (c) $S_{21}$, and (d) $S_{22}$ measured from 100 MHz to 20 GHz biased at $V_{GS} = 2.4$ V and $V_{DS} = 5$ V. Line: simulated, Symbol: measured ........................................... 21
Fig. 3.1: A pMOS transistor used in the TDDB experiment ............................... 24
Fig. 3.2: Mechanisms of Hot Carrier Effects. (a) DAHC injection involves impact ionization of carriers near the drain area; (b) CHE injection involves propelling of carriers in the channel toward the oxide even before they reach the drain area; (c) SHE injection involves trapping of carriers from the substrate; (d) SGHE injection involves hot carriers generated by secondary carriers ................................................................. 35
Fig. 3.3: Band diagram and experiment setup for substrate hot electron injection in an nMOSFET................................................................. 37

Fig. 3.4: (a) $\Delta V_{th}$ versus frequency for n-LD MOSFET with 0.24um channel length stressed at $V_d = 9.5V$, stress time = 10800s. (b) $\Delta g_m$................................. 41

Fig. 3.5: Lifetime ($\Delta V_{th} = 10\%$) as a function of $1/Vd$, Close circles are DC lifetime measurement, Open circle is for the dynamic degradation experiments. ............... 43

Fig. 4.1: An equivalent MOSFET gate circuit showing just $C_{gs}$, $C_{gd}$ and $R_g$.......................... 52

Fig. 4.2: Turn-on transient of the MOSFET .................................................................................. 53

Fig. 4.3: Turn-off transient of the MOSFET .................................................................................. 54

Fig. 4.4: Combination of gate charge and capacitance to obtain switching times .................... 57

Fig. 4.5: Sketch showing definition of turn-on and turn-off times .............................................. 59

Fig. 4.6: A simplified schematic of the full bridge DC-DC converter ........................................ 60

Fig. 4.7: A schematic of a class-C power amplifier................................................................. 62

Fig. 5.1: Transconductance and threshold voltage as a function of stress time.................... 65

Fig. 5.2: Normalized on-resistance change as a function of stress time .................................... 66

Fig. 5.3: Normalized on-resistance degradation versus normalized threshold voltage degradation ................................................................................................................. 67

Fig. 5.4: (a) Normalized threshold voltage change versus duty cycle, (b) normalized transconductance change versus duty cycle, and (c) normalized drain current degradation versus drain-source voltage at $V_{GS} = 2.4$ V................................................................. 71
Fig. 5.5: (a) gate-drain capacitance versus gate-drain voltage, (b) gate-source capacitance vs. gate-source voltage, and (c) gate-body capacitance vs. gate-body voltage for different stress times.

Fig. 5.6: Gate resistance versus gate-drain voltage.

Fig. 5.7: (a) $S_{11}$, (b) $S_{12}$, (c) $S_{21}$, and (d) $S_{22}$ measured from 100 MHz to 20 GHz biased at $V_{GS} = 2.4$ V and $V_{DS} = 5$ V. In those plots line with open circles: fresh, line with inverse open triangles: 50% duty cycle dynamic stress, line with x marks: DC stress. The stress time is 10800 s.

Fig. 5.8: Cutoff frequency versus gate-source voltage. The drain-source voltage is 5 V.

Fig. 5.9: The comparison between simulation and measurement, Drain-source current versus drain-source voltage, after stressed.

Fig. 5.10: A gate charge test circuit.

Fig. 5.11: Gate-source and drain-source voltages versus time.

Fig. 5.12: Enlarged gate-source voltage versus time before and after stress.

Fig. 5.13: Simulated voltage waveforms of the primary side of the transformer. (a) Simulation from 0 us to 10 us; (b) Details in the circle shown in (a).

Fig. 5.14: Simulated voltage waveforms of the primary side of the transformer. (a) Simulation from 0 us to 10 us; (b) Details in the circle shown in (a).

Fig. 5.15: Efficiency curves stress time is 300 s.

Fig. 5.16: (a) Output power versus input power and (b) power-added efficiency versus input power. The stress time is 10800 s.

Fig. 6.1: A proposed complete flow to compute reliability circuit simulation.
# LIST OF TABLES

Table 1: NMOS DC performance ..................................................................................... 13  
Table 2: PMOS DC performance ...................................................................................... 13  
Table 3: Proposed levels of power MOSFET model validation ................................. 18  
Table 4: Key transistor parameter changes subject to two different stress conditions  80  
Table 5: Parameter shifts due to HC stress ................................................................. 84
<table>
<thead>
<tr>
<th>ACRONYM</th>
<th>ABBREVIATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>BD</td>
<td>Breakdown BPF Band Pass Filter</td>
</tr>
<tr>
<td>BSIM</td>
<td>Berkeley Short-Channel IGFET Model</td>
</tr>
<tr>
<td>CHE</td>
<td>Channel Hot Electron</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>C-V</td>
<td>Capacitance versus Voltage</td>
</tr>
<tr>
<td>CVS</td>
<td>Constant Voltage Stress</td>
</tr>
<tr>
<td>DAHC</td>
<td>Drain Avalanche Hot Carrier</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DSB</td>
<td>Double-Side Band</td>
</tr>
<tr>
<td>DUT</td>
<td>Device-Under-Test</td>
</tr>
<tr>
<td>EOS</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrical Over-stress</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
</tr>
<tr>
<td>HBD</td>
<td>Hard Breakdown</td>
</tr>
<tr>
<td>HC</td>
<td>Hot Carrier</td>
</tr>
<tr>
<td>HCI</td>
<td>Hot Carrier Injection</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input Third-Order Intercept Point</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
</tr>
<tr>
<td>--------------</td>
<td>------------------------------------------------</td>
</tr>
<tr>
<td>IM3</td>
<td>Third-Order Intermodulation Distortion</td>
</tr>
<tr>
<td>IV</td>
<td>Current versus Voltage</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s Current Law</td>
</tr>
<tr>
<td>KVL</td>
<td>Kirchhoff’s Voltage Law</td>
</tr>
<tr>
<td>LCR</td>
<td>Inductance Capacitance Resistance</td>
</tr>
<tr>
<td>LD</td>
<td>Lateral Doping Drain</td>
</tr>
<tr>
<td>LF</td>
<td>Low Frequency</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NB</td>
<td>Combined NBTI and Breakdown Stress</td>
</tr>
<tr>
<td>NBH</td>
<td>Combined NBTI, Breakdown, and HC Stress</td>
</tr>
<tr>
<td>NBTI</td>
<td>Negative Bias Temperature Instability</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>NMOSFET</td>
<td>N-type MOS Field Effect Transistor</td>
</tr>
<tr>
<td>NQS</td>
<td>Non-Quasi-Static</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PMOSFET</td>
<td>P-type MOS Field Effect Transistor</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SBD</td>
<td>Soft Breakdown</td>
</tr>
<tr>
<td>SGHE</td>
<td>Secondary Generated Hot Electron</td>
</tr>
<tr>
<td>SHE</td>
<td>Substrate Hot Electron</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>SOA</td>
<td>Safe Operation Area</td>
</tr>
<tr>
<td>SOC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon-on- Insulator</td>
</tr>
<tr>
<td>SS</td>
<td>Small Signal</td>
</tr>
<tr>
<td>TDDB</td>
<td>Time Dependent Dielectric Breakdown</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very-Large-Scale Integration</td>
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</table>
1 CHAPTER ONE: INTRODUCTION

1.1 Motivation

One of the main problems encountered when scaling down been the hot carrier induced degradation of MOSFETs. This problem has been studied intensively during the past decade, under both static and dynamic stress conditions. In this period it has evolved from a more or less academic research topic to one of the most stringent constraints guaranteeing the lifetime of sub-micron devices [1].

New process and technology advances the development of semiconductors industry. Well defined device is extensively improved to meet the stringent requirements of modern electronics market. Reliability model has been introduced into the circuit design stage in order to reduce the final product cost. Therefore, reliability research can’t stay at the artificial experiment setup. The real circuit operation environment has to be considered. On the other hand, not only is the device level degradation is necessary to meet the lifetime, but also circuit level reliability model has to be produced to circuit designers so that they can consider these reliability effects in the early stages of design to make sure there are enough margins for circuits to function correctly over their entire lifetime.

With the help of previous colleagues’ work at the Chip Design and Reliability Laboratory (CDRL) at UCF [2] - [5], this research focuses on the submicron lateral doped drain (LD) MOSFETs, continues the work of reliability modeling and circuit simulations in its flows, offers new suggestions to enhance HCI circuit robustness.
1.2 Research Goals

The research presented here focuses on the following issues:

1. Understanding of hot carrier reliability mechanism in the sub-micron 0.25um lateral doped drain (LD) MOSFETs under static and dynamic stress
2. Device modeling of degraded LD MOSFETs
3. Performance degradation in LD MOSFETs typical application circumstance gate-charge transfer circuit and RF Power Amplifier

1.3 Outlines

In chapter 2, a complete device modeling process is introduced. An understanding of the voltage stress- induced reliability issue – Hot carrier, Breakdown and NBTI in MOSFETs is presented in Chapter 3, with focusing on the hot carrier effect mechanism. In chapter 4, an accurate and practical parameter extraction is used to obtain the model parameters of LD MOSFETs, with the experiment verification. In chapter 5, the gate charge transfer performance is examined to demonstrate the hot carrier effect, which is the most important performance characteristic for DC-DC converter design; The hot-carrier injection experiment in which dynamic stress with different duty cycle is presented to understand the dynamic stress on the LD MOSFET and its effect on RF circuit. Finally, the conclusion is made, and the complete reliability solution, including model extraction, calibration to silicon and full-chip reliability simulation and analysis, is proposed.
2 CHAPTER TWO: DEVICE MODELING PROCESS

2.1 Introduction

The use of professional tools is a prerequisite to develop accurate device models, from DC to GHz, including noise modeling and nonlinear HF effects, within a reasonable time. With technology going faster and faster towards ultra-high frequencies, circuit designs can only be accurate and right-the-first-time if the underlying device models are accurately modeled with physically meaningful model parameters.

In order to successfully design chips with higher integration and higher transmission speed, the work of modeling engineers to develop accurate device models up to tens of Gigahertz becomes more and more challenging. An absolute prerequisite for achieving this goal are accurate measurements, checked for data consistency, accurate instrument calibration, and correct de-embedding. Furthermore, today's high-frequency components require a lot of flexibility for the parameter extraction and device modeling process [6].

2.2 General Process

An idea of the general device modeling process is depicted in Fig. 2.1.
Fig. 2.1: The device modeling process

For a given device, an adequate model is selected first. This can be a single model (like for transistors), or a composed sub-circuit consisting of standard devices. Next, the model equations, which are solved for the model parameters during model parameter extraction, give a clear indication about what kind of measurements and what type of stimulus sweeps are required for characterization. After all these measurements have been performed, the parameters of the selected model are reset. This means, the model becomes a very simple one: no bias dependency, and no frequency dependency. Then, during the parameter extraction process, more and more model parameters are extracted, and the selected model will fit more and more precisely the measured device. This extraction process is usually a combination of direct parameter determination out of the measured data, followed interactively by parameter fine-tuning with an optimizer.
For a general transistor modeling as an example, the measurement of the DC performance with respect to its input and output characteristics as well as its transfer function is done first, followed by the so-called CV modeling, i.e. the characterization of the depletion capacitances at 1MHz. Finally, the S-parameters of the transistor as well as of the dummy devices (contact pad capacitances and inductances) are measured. The dummy devices consist of an OPEN dummy (representing the contact pads and the open connection lines to the device-under-test (DUT), a SHORT (the device is replaced by a metal plane, thus shorting both ports to ground at the location of the device), and a THRU (the device is replaced by a strip-line between port1 and port2 of the network analyzer).

After the de-embedding process has been verified (by modeling the THRU dummy device for example), the S-parameters of the inner device-under-test are de-embedded (OPEN and SHORT dummy de-embedding) and the device modeling can be applied. Referring back again to Fig.2.2, the model parameters are extracted and fine-tuned for each sketched step bottom-up. For the DC case, it is the non-linear model parameters, for the CV the junction capacitance parameters and for the S-parameters the transit time, and also the parasitic which are only visible at HF (e.g. the Gate resistance of a MOS transistor).
However, we should keep in mind that the HF application of a device is not necessarily linear. While a S-parameter measurements by a network analyzer is usually performed at HF-signal levels below -30dBm (<1uW), and while therefore modeling is based on these data, it must be checked if the model can also predict correctly the device performance above these low HF power levels. In most cases, spectrum analyzers will be involved, but also nonlinear network analyzers are available [7] - [9].
It should be noted that such kind of performance cannot be simulated using conventional SPICE-like simulators. This kind of simulators does not need to perform any linearization in order to predict the HF performance. Applying a Fourier analysis, harmonic balance simulators 'balance the harmonics' at each node of the circuit in order to fulfill Kirchhoff's law that the sum of currents into a node is zero for all frequencies and for all HF power levels.
Fig. 2.4: How harmonic balance simulators work

Harmonic Balance Iterations

Start in the Frequency Domain

Calculate currents

Convert time -> frequency

Test Kirchhoff’s law.

Sum of currents for all elements into node 2 is not zero!!!

Iterate again.

Last estimate for spectral voltage with least error for sum of currents at node 2

within tolerance -> ok.
2.3 BSIM3 Model and Equivalent Circuit Model

BSIM is a physics-based, accurate, scalable, robust and predictive MOSFET SPICE model for circuit simulation and CMOS technology development. It is developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. The third iteration of BSIM3 was established by SEMATECH as the first industry-wide standard of its kind in December of 1996. BSIM3v3 has since been widely used by most semiconductor and IC design companies world-wide for device modeling and CMOS IC design. It is a consortium of semiconductor companies and simulator vendor world-wide promoting BSIM3v3 development as the industry standard compact model [10]. The BSIM model will be adopted as the basic model for our devices.

BSIM3 model is extracted from DC and CV measurement. It is difficult to represent a MOS transistor operating under the high frequency. Usually, an equivalent subcircuit model is more accurate. Fig.2.5 shows the equivalent circuit representing the MOS device [11]. The equivalent circuit includes the terminal inductances (\(L_d\), \(L_g\), \(L_s\), and \(L_b\)), internal region (gate resistance \(R_g\), intrinsic MOSFET, gate-drain capacitance \(C_{gd}\), and gate-source capacitance \(C_{gs}\)), and substrate network (diodes \(D_{db}\) and \(D_{sb}\) and resistances \(R_{bd}\), \(R_{sb}\), \(R_{bpd}\), and \(R_{bps}\)).

DC and s-parameters measurement are performed to extract the model parameters. Among the intrinsic device, the gate resistance is extracted using the following equation:

\[
R_g = \frac{\text{Im}(Y_{21}) + \omega C_{gd}}{\omega g_m C_{gs}}
\]
where $\omega$ is the angular frequency, $Y_{21}$ is the $Y$-parameter, $C_{gg}$ and is the gate capacitance. The gate capacitance and gate-drain capacitance can be obtained from

$$C_{gg} = \frac{\text{Im}(Y_{11})}{\omega}$$  \hspace{1cm} (2)

$$C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega}$$  \hspace{1cm} (3)

where $Y_{11}$ and $Y_{12}$ are converted from measured $s$-parameters.

Also, the gate-source capacitance $C_{gs}$ is given as

$$C_{gs} = C_{gg} - C_{gd}$$  \hspace{1cm} (4)

$L_d, L_g, L_s, L_b, D_{db}, D_{sb}, R_{bd}, R_{sb}, R_{bd}$, and $R_{bps}$ are obtained by optimizing the model in Fig. 2.5 to fit $Y$-parameters.
Motivated by emerging portable applications that demand ultra-low-power and low voltage device to maximize battery run-time, efficiency, many efforts is being put to develop the silicon LDMOS to meet the requirements from all design aspects of an integrated portable device. Sub-micro LDMOS transistors present versatile flexibility in the market of smart power and RF power application, and its compatibility with the current VLSI technology provides unique benefit for a single chip solution [12] – [18]. We present a high performance LDMOS transistor integrating in a pure 0.25um silicon VLSI technology, which could be used as a power MOSFET and RF power amplifier with suitable adjustment.

Fig. 2.5: A RF equivalent subcircuit model for nMOS transistor

2.4 Device
2.4.1 Technology and LDMOS Description

In this technology, the LDMOS performance working as power MOSFET is maximized, and efforts are paid to fully compatibility with the 0.25um, 2.5V 4-metal CMOS process.

The cross section of the LDMOS is shown in Fig. 2.6. It was built on a highly doped p-type substrate to provide isolation to the n-channel device. A lightly doped p-type epi-layer was added to accommodate high voltage capability. The self-aligned channel below the metallized poly-silicon gate was used to improve the device transconductance and gain. The lightly doped drain extension region was introduced to sustain the high drain-source voltage in combination with the epi-layer.

Fig. 2.6: The cross section of an LDMOS transistor
2.4.2 The Performance of the LDMOS

The main DC performance of the LD MOS is summarized in Table 1 and Table 2.

Table 1: NMOS DC performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Value</th>
<th>Measurement conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage ($V_{th}$)</td>
<td>V</td>
<td>0.511</td>
<td>$V_{DS} = 0.1$ V</td>
</tr>
<tr>
<td>Saturation Current ($I_{sat}/W$)</td>
<td>μ A/ μ m</td>
<td>0.5</td>
<td>$V_{DS} = V_{GS} = 6$ V</td>
</tr>
<tr>
<td>Off-current ($I_{off}$)</td>
<td>pA/ μ m</td>
<td>3.2</td>
<td>$V_{DS}=6$ V, $V_{GS}=0$ V</td>
</tr>
<tr>
<td>Breakdown voltage ($BV_{DSS}$)</td>
<td>V</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>$R_{on} \times W \times L$</td>
<td>Ω*mm²</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td>Sub-threshold current ($I_{sub}$)</td>
<td>μ A/ μ m</td>
<td>2.1</td>
<td>$V_{DS}=6$ V, $V_{GS}=2.5$ V</td>
</tr>
</tbody>
</table>

Table 2: PMOS DC performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Value</th>
<th>Measurement conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage ($V_{th}$)</td>
<td>V</td>
<td>0.626</td>
<td>$V_{DS} = - 0.1$ V</td>
</tr>
<tr>
<td>Saturation Current ($I_{sat}/W$)</td>
<td>μ A/ μ m</td>
<td>0.26</td>
<td>$V_{DS} = V_{GS} = - 6$ V</td>
</tr>
<tr>
<td>Off-current ($I_{off}$)</td>
<td>pA/ μ m</td>
<td>1.14</td>
<td>$V_{DS} = - 6$ V, $V_{GS}=0$ V</td>
</tr>
<tr>
<td>Sub-threshold current ($I_{sub}$)</td>
<td>μ A/ μ m</td>
<td>0.03</td>
<td>$V_{DS} = - 6$ V, $V_{GS} = - 2.5$ V</td>
</tr>
<tr>
<td>Breakdown voltage ($BV_{DSS}$)</td>
<td>V</td>
<td>12.5</td>
<td></td>
</tr>
<tr>
<td>$R_{on} \times W \times L$</td>
<td>Ω*mm²</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>
Fig. 2.7 and Fig. 2.8 show the I-V characteristic for the LD nMOS transistor. Fig. 2.9 and Fig. 2.10 are the I-V characteristic of the LD pMOS transistor. Fig. 2.11 (a) and (b) show the reverse bias characteristic of the nMOS transistor.

Fig. 2.7: Drain current versus drain-source voltage (nMOS transistor)

Fig. 2.8: Drain current versus gate-source voltage (nMOS transistor)
Fig. 2.9: Drain current versus grain source voltage (pMOS Transistor)

Fig. 2.10: Drain current versus gate-source voltage (pMOS)
Fig. 2.11: Reverse Bias Characteristic (a) nMOSFET (b)pMOSFET
2.4.3 Model Parameter Extraction

To evaluate a proprietary or unknown power MOSFET model one needs: 1) The gate charge plot, 2) C-V plots and 3) The body-drain diode reverse recovery waveform. Model validation represents the process of establishing standards for model performance. Proposed new performance standards for power MOSFET models are listed in Table 5. For any given application, the simplest model which satisfies the required performance should always be chosen for each simulation. The level 1 model is used for simulation of general power electronic circuits where an occasional phase error is acceptable. Users of the level 1 model should be aware of its limited range of operation to assure a reasonable accuracy. The level 2 model is used where highly accurate waveform simulations are required. The level 3 model is intended for dynamic thermalelectric simulations within the specified SOA, and finally the level 4 model is for applications beyond the device SOA. [74]
<table>
<thead>
<tr>
<th>Level</th>
<th>Required performance for power MOSFET models</th>
<th>Appropriate applications</th>
</tr>
</thead>
</table>
| 1     | 1. Relatively accurate for gate-drain capacitance CGD  
       2. Constant value for CGS  
       3. Omits body-diode recovery.  
       4. Used by a wide range of device and simulator | Used for general power electronic circuit simulation:  
1. Where VGs(t) is always above zero Volts, and  
2. Where the body diode is not used.  
3. Not accurate for resonant gate drive circuits. |
| 2     | 1. Accurate gate-drain, gate-source, and  
       2. Includes body-diode reverse recovery.  
       3. Non-destructive avalanche breakdown.  
       4. drain-source capacitances CGD, CGS, CDS | Used for highly accurate waveform simulation:  
1. Accurate for all operating states within the rated current and voltage (within SOA).  
2. Accurately predicts static and dynamic switching losses. |
| 3     | 1. In addition to features in level 2 model:  
       2. Calculates heat due to internal power dissipation.  
       3. Contains external thermal nodes as well as thermal properties of device die and package. | Used for analyzing temperature and dynamic thermal effects.  
1. Dynamic thermal-electric simulations within the SOA  
2. Heat-sink design of a Power MOSFET.  
3. Analysis of thermal stress. |
| 4     | 1. In addition to features in level 3 model,  
       2. Parasitic JFET effects at over voltage and over current operation.  
       3. Over temperature operation.  
       4. Device failure modes. | Used for simulating fault and high stress condition beyond SOA:  
1. Operation under short circuits.  
2. High stress condition that may lead to thermal run away or possible failure of a power MOSFET. |
Test devices located at the center of wafers are measured. The on-wafer device is measured in a Cascade 12000 Probe Station. Agilent 4156B Precision Semiconductor Parameter Analyzer is used to measure DC characteristics and for hot-electron stress. The device under test (DUT) has the oxide thickness of 5.86 nm, channel width of 10 μm, and channel length of 0.24 μm. IC-CAP 2004 is used for parameter extraction.

The DC simulation results are compared with the experimental data as shown in Fig. 2.12. The S-parameters comparison between measurement and simulation is showed in Fig. 2.13. Good agreement between the model predictions and measurement for the device is obtained.

Fig. 2.12: Drain-source current versus drain-source voltage
Fig. 2.13: (a) $S_{11}$, (b) $S_{12}$, (c) $S_{21}$, and (d) $S_{22}$ measured from 100 MHz to 20 GHz biased at $V_{GS} = 2.4$ V and $V_{DS} = 5$ V. Line: simulated, Symbol: measured
3 CHAPTER THREE: DEVICE RELIABILITY

3.1 Introduction

With the smaller dimensions for each successive generation of transistors for improving speed and functionality, the power dissipation, which results in heat flux to be removed to the ambient, required development of thermal management for reliability? High performance silicon-on- insulator (SOC) can have hot spots in a circuit design leading to large temperature gradients across a chip. Using MEDICI simulation, the temperature at the gate-drain opening for the bulk devices was estimated to be 315 K [19]. While for the SOC devices, the simulated temperature was up to 550 K. The net result is pattern dependent dispersion in the activation of negative bias temperature instability (NBTI) processes and NBTI drift. If care is not taken to understand these issues, timing degradation dependent paths can lead to accelerated circuit failures during burn-in or field operations. Detection of these failures may become difficult due to circuit complexity and hence lead to erroneous data or output conditions. NBTI is one of the major temperature-induced reliability issues for p-channel MOSFET, which is caused by the interface traps under high temperature and negative gate voltage bias. Beside the NBTI effects, the pMOS transistors in real circuits also suffer from the gate oxide breakdown (TDDB) due to high vertical electrical field in the oxide and the hot carriers injection (HCI) because of high lateral electrical field in short-channel MOSFETs [20]-[22]. Increased temperature accelerates the combined NBTI, TDDB and HCI degradation significantly in our test transistors. Consequently the performance degradation in circuits follows.
The semiconductor process evolution that produces small transistors increases the potential for interface traps in PMOS transistors during prolonged times of negative bias stress. An interface trap is created when a negative voltage is applied to the gate of a PMOS device for a prolonged time, as shown in Fig. 3.1. An interface trap is located near the Si-oxide/Si-crystal lattice boundary where holes (positive charge) can get stuck, and in doing so, they shift the threshold voltage. This hole trapping creates interface states as well as fixed charges. Both are positive charges and result in a negative shift of threshold voltage. This phenomenon is called PMOS Negative Bias Temperature Instability (NBTI). NMOS transistors are far less affected because interface states and fixed charges are of opposite polarity and eventually cancel each other.

NBTI can determine the useful lifetime of complementary metal-oxide semiconductor (CMOS) devices. The designer must consider the bias conditions of each PMOS transistor, not only at the beginning of life but throughout the expected lifetime of the product [23]. Typically, these conditions must allow for at least ten years of operation at the highest voltage and the highest temperature. Removal of power allows for some release (annealing) of the trapped charges [24]. Static stress shifts the voltage threshold roughly ten times more than does dynamic stress [25]. For example, a shift of 10 mV can occur in a dynamic (switching) situation, and a shift of 100 mV can occur in the static case.
Fig. 3.1: A pMOS transistor used in the TDDB experiment.

TDDB is wear-out of the insulating properties of silicon dioxide in the CMOS gate leading to the formation of a conducting path through the oxide to the substrate. With a conducting path between the gate and the substrate, it is no longer possible to control current flow between the drain and source by means of the gate electric field. TDDB lifetime is strongly affected by the number of defects in the gate oxide produced during wafer fabrication. Therefore, foundries strive to produce an ultra-clean oxide in their process to maximize the TDDB lifetime. Even if a foundry could produce a perfectly defect free oxide, TDDB would remain a concern for ASIC designers.

TDDB occurs at all gate voltage bias conditions. The goal of the foundry is to trade off gate oxide thickness with operating voltage specifications to achieve both speed and lifetime targets for the technology. The lifetime of a particular gate oxide thickness is determined by the total amount of charge that flows through the gate oxide by tunneling current. The electron tunneling current is modeled by the Fowler-Nordheim equation for oxide current density, \( J \):

\[
J = AE^2e^{\frac{B}{E}}
\]  

(5)
where, A and B are constants related to effective mass and barrier height and E is the electric field.

It is clear from this relationship that operating a CMOS device at voltages greater than foundry specification results in an exponential increase in the amount of oxide current. Once electrons have breached the oxide potential barrier they are accelerated through the oxide by the electric field which is determined by the applied voltage and the oxide thickness. Charge accelerated in the gate oxide achieves greatest energy at the oxide-silicon interface presuming there have been no collisions in transit. At the end of its travel through the oxide, it deposits its energy at the oxidesilicon interface.

Under high negative gate voltage bias in pMOSFETs at elevated temperature-NBTI stress, the electrochemical reaction at Si-SiO2 interface is:

$$Si - H + O_3 - Si - O - Si + h^+ \leftrightarrow O_3 - Si - OH^+ - Si$$ (6)

The interface state (Si·) is generated from the dissociation of hydrogen terminated trivalent Si bonds (Si-H) by holes (h+) in the Si inversion layer. The released hydrogenated species (H+) diffuse and are trapped near the oxide interface resulting in the positive oxide charges (Si-OH+-Si). Experiments show that the positively charged hydrogen (H+) reacts with the SiO2 lattice to form an OH group bonded to an oxide atom, leaving a trivalent Si atom (Si$_{0+}$) in the oxide and one trivalent Sis at the Si surface. The $Si_{0+}$ forms the fixed positive charge ($N_f$) and the Sis forms the interface trap ($N_{it}$). NBTI stress causes $N_{it}$ and $N_f$ shifts, contributing mainly to the shift in device characteristics. The $N_{it}$ and $N_f$ shifts are given by:

$$\Delta N_{it}(E_{ox}, T, t, t_{ox}) = 9 \times 10^{-4} E_{ox}^{1.5} t_{ox}^{0.25} \exp(-0.2 / kT)/t_{ox}$$ (7)
\[ \Delta N_f (E_{ox}, T, t) = 490 E_{ox}^{1.5} t^{0.14} \exp(-0.15 / kT) \]  \hspace{1cm} (8)

where \( E_{ox} \) is the electric field in the oxide, \( T \) is the temperature, \( t \) is the stress time, \( t_{ox} \) is the oxide thickness, and \( k \) is Boltzmann’s constant. The shift of threshold voltage is:

\[ \Delta V_{th} (\Delta N_{it}, \Delta N_f) = B_1 [1 - \exp(-t / \tau_1)] + B_2 [1 - \exp(-t / \tau_2)] \]  \hspace{1cm} (9)

where \( B_1 \) and \( B_2 \) relate to \( \Delta N_{it} \) and \( \Delta N_f \), \( \tau_1 \) and \( \tau_2 \) are the reaction limiting time constants.

The channel mobility degradation (\( \Delta \mu \)) also depends on the interface traps.

The NBTI induced \( N_{it} \) and \( N_f \) shifts causes the change in device characteristics, as well as the performance degradation. The degradation is thermally activated (See (17) and (18)) and, therefore, is sensitive to temperature. It degrades severely under higher temperature.

Companying with NBTI under high gate voltage bias and temperature, hydrogen release, hole injection and thermo -chemical electric field create defects in the oxide and likely trigger breakdown. On the other hand, constant high voltage at the drain terminal in real pMOS devices can also result in another reliability issue - hot carrier effects. The carriers accumulate sufficient energy to surmount the Si-SiO\(_2\) surface and enter the oxide. The injected carriers enhance the interface state generation and increase the NBTI sensitivity.

The oxide-silicon interface has some special properties produced by the fact that there is a large thermal coefficient of expansion (TCE) difference between silicon dioxide and silicon (silicon: 2ppm/°C vs. Silicon Dioxide: 0.3ppm/°C). This large difference in TCE leads to strained chemical bonds that can be broken by the accelerated charge. Once the chemical bonds have been broken, the sites become locations where charge can become trapped. This trapped charge will have an influence upon the channel carrier mobility in transistors and reduce their...
gain. This trapped charge also has the effect of increasing the electric field locally and therefore increasing the local tunneling current. The process has positive feedback that leads to rapid charge build-up until the tunneling current is large enough to literally burn a hole through the gate oxide.

Modeling TDDB lifetime has been a challenging task. The specific physical process details leading to failure are somewhat complex, and as a result, simple models tend to be inaccurate if the gate oxide is substantially different from the thickness used for collecting the data used to develop the model. A great deal of material has been published about TDDB modeling with various relationships of electric field to lifetime. Debate has raged for some time over whether the lifetime is related to \( E \) (electric field), or \( 1/E \), or just applied gate Voltage. Currently it appears that simple models will only be valid over certain ranges of gate oxide thickness. Moderately thick oxides seem to have a lifetime related to \( 1/E \) (at high electric field) or \( E \) (at low electric field) while for very thin oxides (thinner than 5nm) the lifetime appears to be related to applied Voltage.

All of the following models are based upon data fitting from experimental data under different amounts of electric field stress with different oxide thickness. Tests are performed at very high electric field (greater than under normal use conditions) and at elevated temperature to reduce testing time to a few weeks instead of tens of years. These models include the temperature dependence.

For thick oxides at relatively low electric field (moderately greater than at-use conditions) TDDB lifetime has been shown to obey [26]:

\[
t_{BD1} = t_i \exp(-\gamma E_{ox})
\]

(10)
where \( t_1 = 6.3 \times 10^{14} \text{ sec.} \) and \( E_{\text{ox}} = 2.66 \text{cm/MV} \)

Temperature effects:

\[
t_1 = t_{10} \exp(\Delta H_0 / k_B T) \tag{11}
\]

\[
\gamma = b + \frac{c}{T} \tag{12}
\]

Similarly, for thick oxides under high field stress (much greater than at-use conditions):

\[
t_{BD2} = t_2 \exp\left(\frac{G}{E_{\text{ox}}}\right) \tag{13}
\]

where \( t_2 = 1.0 \times 10^{-11} \text{ sec.} \) and \( G = 350 \text{ MV/cm} \)

Temperature effects:

\[
t_2 = t_{20} \exp\left[-\frac{E_h}{k_B} \left(\frac{1}{T} - \frac{1}{300}\right)\right] \tag{14}
\]

and

\[
G = G_0 \left[1 + \frac{\delta}{k_B} \left(\frac{1}{T} - \frac{1}{300}\right)\right] \tag{15}
\]

Both of the above equations contain constants that are extracted from data and will vary depending upon specific oxide properties and defect content. Foundries will characterize their
process using experimental accelerated TDDB lifetime data to extract model parameters. From these parameters they are able to tune the fabrication process to produce gate oxide that has at least 20 to 40 year lifetime at the specified operating voltage. When oxides are thinner than about 5nm the lifetime modeling begins to show voltage dependence as discussed in a paper by P. E. Nicollian, et. al. [27]. Even with the insights from this paper the prediction of TDDB lifetime is not an exact science. As a result of the imprecise modeling of TDDB lifetime over all, it is not possible to accurately engineer a device lifetime using the existing TDDB models. Also, it is not possible to use model parameters from one fabrication line to extrapolate TDDB lifetime on another fabrication line. It is much safer for ASIC designers to stay within the foundry operating voltage specifications.

Time-Dependent Dielectric Breakdown (TDDB) is an important failure mechanism in ULSI devices. The dielectric fails when a conductive path forms in the dielectric, shorting the anode and cathode. The two models widely used in describing TDDB are field-driven (E-model) and current-driven (1/E - model). There are some constrains:

- These models are intended for application to SiO₂ with thickness greater than approximately 40A (4 nm).
- Accuracy of these models for thinner (silicon) oxide is unknown.
- Models and parametric values to effectively model “hi K” oxides (based on materials or composites other than silica) are unknown.

Recently, several low-field/long-term TDDB studies showed that TDDB data were described more effectively by the E-Model than the 1/E model [45] – [49]. The E-model is now based on fundamental, physical parameters (not empirically fitted parameters) and fits TDDB
data more effectively than the 1/E model [50] – [52]. The good fit of the physics-based E-model to the low-field/long-term TDDB data strongly suggests electric field is the dominant degradation driver at low stresses characteristic of customer applications, and that constant current stress is not relevant to customer application.

**E-Model**

In the E-Model [45] – [62], the cause of low-field (< 10MV/cm) TDDB is due to field-enhanced thermal bond-breakage at the silicon-silica interface. The E-field serves to reduce the activation energy required for thermal bond breakage and therefore exponentially increases the reaction rate for failure. Time-to-failure, inverse to reaction rate, decreases exponentially:

\[
TF = A_0 \exp(-\gamma E_{ox}) \exp(E_a / kT) \tag{16}
\]

where:

- \(A_0\) = arbitrary scale factor, dependent upon materials and process
- \(\gamma\) = field acceleration parameter, is temperature dependent, \(\gamma(T) = a/kT\) where \(a\) is the effective dipole moment for the molecule.

\(E_{ox}\) = electric field across the dielectric in MV/cm. It must be voltage. compensated for band bending if an accumulation layer is formed, but no compensation is needed if an inversion layer is formed. \(E_{ox}\) is the quotient of the compensated voltage & the oxide thickness, \(t_{ox}\). Note that tox should be electrically or physically measured.

Previous work [58] provides values for \((\Delta H)_0\) and "a" and shows that \(\gamma\) has a 1/T dependence. This means that the activation energy reduces linearly with the electric field,

\[
E_a = (\Delta H)_0 - aE_{ox} \tag{17}
\]

where:
\( E_a = \) effective activation energy (eV). \( E_a \) may be nearly temperature-independent if several types of disturbed bonding states are present in the dielectric and the reaction rates are mixed during high-field and/or high temperature TDDB testing.

\( (\Delta H)_o = \) the enthalpy of activation for bond breakage in the absence of external electric field (~2.0 eV)

\( a = \) effective molecular dipole-moment for the breaking bonds which value is ~7.2 Å.

For intrinsic failures in SiO\(_2\) dielectrics of thickness < 100Å, \( \gamma \sim 2.5-3.5 \) Naperians per MV/cm (~1.1-1.5 decades per MV/cm) and \( E_a = 0.6-0.9 \) eV. For extrinsic defects, effective oxide thickness can be quite thin and therefore the effective field can be very high. This leads to the apparently lower activation energy of about 0.3 eV observed during burn-in.

**1/E – Model [59] – [62]**

The cause of TDDB, even at low fields, is postulated to be due to current through the dielectric by Fowler-Nordheim (FN) conduction. F-N injected electrons (from the cathode) cause impact ionization damage of the dielectric as they accelerate through the dielectric. Additionally, when these accelerated electrons reach the anode, hot holes may be produced which can tunnel back into the dielectric causing damage (hot-hole anode injection mechanism). The time-to-failure is expected to show an exponential dependence on the inverse electric field, 1/E:

\[
TF = \tau_0(T) \exp\left[ G(T) / E_{\text{ox}} \right]
\]

where:

\( \tau_0(T) = \) a temperature dependent prefactor, \(~ 1 \times 10^{-11} \) sec

\( G = \) field acceleration parameter, \(~ 350 \) MV/cm with a weak temperature dependence
\( E_{\text{ox}} = \) electric field across the dielectric in MV/cm. It must be voltage compensated for band bending if an accumulation layer is formed, but no compensation is needed if an inversion layer is formed. \( E_{\text{ox}} \) is the quotient of the compensated voltage and the oxide thickness, \( t_{\text{ox}} \). Note \( t_{\text{ox}} \) that should be electrically or physically measured.

Under the influence of the high lateral fields in short channel MOSFETs, electrons and holes in the channel and pinch-off regions can gain sufficient energy to surmount the energy barriers or tunnel into the oxide. This leads to the generation of traps, both at the interface and in the oxide, and to electron and hole trapping in the oxide, which will cause changes in transconductance, threshold voltage and drive current of the MOSFET [1].

There are four commonly encountered hot carrier injection mechanisms [27]. These are 1) the drain avalanche hot carrier injection; 2) the channel hot electron injection; 3) the substrate hot electron injection; and 4) the secondary generated hot electron injection. The drain avalanche hot carrier (DAHC) injection, as shown in Fig. 2.1, is said to produce the worst device degradation under normal operating temperature range. This occurs when a high voltage applied at the drain under non-saturated conditions \( (V_D > V_G) \) results in very high electric fields near the drain, which accelerate channel carriers into the drain's depletion region. Studies have shown that the worst effects occur when \( V_D = 2V_G \). The acceleration of the channel carriers causes them to collide with Si lattice atoms, creating dislodged electron-hole pairs in the process. This phenomenon is known as impact ionization, with some of the displaced electron-hole (e-h) pairs also gaining enough energy to overcome the electric potential barrier between the silicon substrate and the gate oxide. Under the influence of drain-to-gate field, hot carriers that surmount the substrate-gate oxide barrier get injected into the gate oxide layer where they are
sometimes trapped. This hot carrier injection process occurs mainly in a narrow injection zone at the drain end of the device where the lateral field is at its maximum. Hot carriers can be trapped at the Si-SiO$_2$ interface (hence referred to as 'interface states') or within the oxide itself, forming a space charge (volume charge) that increases over time as more charges are trapped. These trapped charges shift some of the characteristics of the device, such as its threshold voltage ($V_{th}$) and its conveyed conductance ($g_m$). Injected carriers do not get trapped in the gate oxide become gate current. On the other hand, majority of the holes from the e-h pairs generated by impact ionization flow back to the substrate, comprising a large $\approx V$. Channel carriers that travel from the source to the drain are sometimes driven towards the gate oxide even before they reach the drain because of the high gate voltage. Substrate hot electron (SHE) injection occurs when the substrate back bias is very positive or very negative, i.e., $V_B$ portion of the substrate's drift current. Excessive substrate current may therefore be an indication of hot carrier degradation. In gross cases, abnormally high substrate current can upset the balance of carrier flow and facilitate latch-up. Channel hot electron (CHE) injection occurs when both the gate voltage and the drain voltage are significantly higher than the source voltage, with $|V_B| >> 0$. Under this condition, carriers of one type in the substrate are driven by the substrate field toward the Si-SiO$_2$ interface. As they move toward the substrate-oxide interface, they further gain kinetic energy from the high field in surface depletion region. They eventually overcome the surface energy barrier and get injected into the gate oxide, where some of them are trapped. Substrate hot electron (SHE) injection occurs when the substrate back bias is very positive or very negative, Under this condition, carriers of one type in the substrate are driven by the substrate field toward the Si-
SiO\textsubscript{2} interface. As they move toward the substrate-oxide interface, they further gain kinetic energy from the high field in surface depletion region. They eventually overcome the surface energy barrier and get injected into the gate oxide, where some of them are trapped. Secondary generated hot electron (SGHE) injection involves the generation of hot carriers from impact ionization involving a secondary carrier that was likewise created by an earlier incident of impact ionization. This occurs under conditions similar to DAHC, i.e., the applied voltage at the drain is high or $V_D > V_G$, which is the driving condition for impact ionization. The main difference, however, is the influence of the substrate's back bias in the hot carrier generation. These back bias results in a field that tends to drive the hot carriers generated by the secondary carriers toward the surface region, where they further gain kinetic energy to overcome the surface energy barrier. Hot carrier effects are brought about or aggravated by reductions in device dimensions without corresponding reductions in operating voltages, resulting in higher electric fields internal to the device. Problems due to hot carrier injection therefore constitute a major obstacle towards higher circuit densities. Recent studies have even shown that voltage reduction alone will not eliminate hot carrier effects, which were observed to manifest even at reduced drain voltages, e.g., 1.8 V. Thus, optimum design of devices to minimize, if not prevent, hot carrier effects is the best solution for hot carrier problems. Common design techniques for preventing hot carrier effects include: 1) increase in channel lengths; 2) n+ / n- double diffusion of sources and drains; 3) use of graded drain junctions; 4) introduction of self-aligned n- regions between the channel and the n+ junctions to create an offset gate; and 5) use of buried p+ channels. Hot carrier phenomena are accelerated by low temperature, mainly because this condition reduces charge detrapping.
Fig. 3.2: Mechanisms of Hot Carrier Effects. (a) DAHC injection involves impact ionization of carriers near the drain area; (b) CHE injection involves propelling of carriers in the channel toward the oxide even before they reach the drain area; (c) SHE injection involves trapping of carriers from the substrate; (d) SGHE injection involves hot carriers generated by secondary carriers.
3.2 Hot Carrier Injection of LD MOSFETs

Here we give our present understanding of the hot carrier degradation problem. The mechanism that is the basis of the hot carrier degradation is hot electron injection. The ideal tool to study the phenomena is the uniform hot electron injection technique. In the technique the LD MOSFETs are stressed under artificial conditions, but the field and effluence conditions can study the degradation of devices at room temperature in order to gain a better insight in the interface degradation mechanisms under both hot hole and hot electron injection. This is the subject of the first part of the paper. In the second part of the paper, the degradation of LD MOSFETs under the more realistic conditions of channel hot carrier injection is reviewed. The different degradation mechanisms under static stress conditions are introduced, lifetime determination methods are briefly described and some important process-related factors and effects will be highlighted. Going to even more realistic conditions, the degradation under dynamic stress conditions is described, emphasizing the influence of the measurement set-up, the comparison with static stress. The strategy for improving hot carrier reliability and a forecast of the hot carrier reliability problem is summarized in the final part.

The experimental set-up and a schematic band diagram, illustrating the substrate hot electron injection technique, are shown in Fig. 3.3. [1]. The gate of the MOSFET is biased at a certain voltage; source and drain are grounded, while the well is held at a high reverse voltage. Minority carriers (electrons) are injected into the well from the underlying substrate by forward-biasing the well-substrate junction diode. Most of the injected electrons will be heated in and gain a high energy. If their energy is higher than the Si-SiO$_2$ energy barrier, they have a high
probability of being injected into the oxide. The oxide field of injection is determined by the
gate-to-source drain voltage; the silicon field, and thus the energy of the injected carriers, is
determined by the well-to-source/drain voltage and the substrate doping, and the injected current
can be controlled by the forward current from the well-substrate diode. Therefore, all important
parameters that can influence the degradation can be controlled separately.

Fig. 3.3 : Band diagram and experiment setup for substrate hot electron injection in
an nMOSFET

First of all it is important to understand the different degradation mechanisms that play a
role under various stress conditions and for different transistor types. Next, a method for the
lifetime determination and extrapolation towards normal operating conditions has to be
established. Finally, a number of processing related factors that can influence the degradation
and the hot carrier lifetime will be discussed.
1) Degradation mechanisms. The hot carrier degradation mechanisms under static conditions have been extensively studied during the last decade, and there exists more or less a consensus on a consistent picture of the degradation mechanisms for both n-type and p-type MOSFETs. A full description falls beyond the scope of this paper, but can be found in [29]–[31]. The main difference with LD n-MOS devices is that for this type of MOSFET the maximum current degradation is dominated by a series resistance increase of the n-region, due to electron trapping in the spacer above this region [1].

2) Lifetime determination. As for all reliability failure mechanisms, it is important to be able to predict the lifetime of a component or device under operating conditions. Such lifetime methods are always based on experiments in which the failure mechanism is accelerated, either by temperature or by high voltages or high currents. During the experiment a degradation parameter relevant for the damage is monitored, and the lifetime is defined as the time taken to reach a certain shift in this degradation monitor.

For the hot carrier degradation mechanism, several accelerated lifetime determination methods have been proposed in the past. They are, however, all based on acceleration of the degradation by increased (drain) voltages, since hot carrier degradation is one of the few mechanisms that is not accelerated by an increase of the temperature [32]. Most accelerated lifetime determination methods are based on the lucky electron model [33].

\[
\Delta N_n(t) = c_i \left[ \frac{I_d}{W} t \exp\left( - \frac{\phi_{a,c}}{q\lambda_c E_m} \right) \right]^n
\]  

(19)
where $w$ is the width of the device, $\Phi_{it,e}$ is the energy an electron must possess in order to create an interface trap and $\lambda_e$ is the hot electron mean free path. A measure for the electrical field $E_m$ is the multiplication factor $M = \frac{I_{sub}}{I_d}$, given by:

$$M = \frac{I_{sub}}{I_d} = c_2 \exp\left(\frac{\Phi_{it,e}}{q\lambda_e}\right)$$  \hspace{1cm} (20)

If one plots the lifetime as a function of the multiplication factor on a double logarithmic scale, according to (13) one obtains a straight line with slope $m$, where $m$ is an indication of the energy of the electrons that are causing the damage.

$$\frac{\tau I_d}{W} = c_3 \left(\frac{I_{sub}}{I_d}\right)^{\frac{\Phi_{it,e}}{\Phi_{t}}} = c_3 M^{-m}$$  \hspace{1cm} (21)

In a simplified form of (2.1) the lifetime is related to the drain voltage, and thus the power supply voltage, as

$$\tau = c_4 \exp\left(\frac{B}{V_d}\right)$$  \hspace{1cm} (22)

Plot the logarithm of the lifetime $\tau$ as a function of $I/V_d$ yields again a straight line. The latter method has the advantage that the lifetime can be directly related to the power supply voltage, but it is only valid in a narrow range of gate voltages, near the maximum of the substrate current.

For monitoring the degradation, several parameters have been used electrical parameters, like $\Delta V_t/V_t$, $\Delta g_m/g_m$ and $\Delta I_d/I_d$, which measure the change of the electrical characteristics, as well as more physical parameters, like the charge pumping current, which is more a measure of the real damage of the interface [30, 34]. The shift of the electrical parameters is determined both by
the Hot-carrier degradation in sub-film MOSFETs amount of damage itself and by the influence of the damage on the electrical characteristics.

3) Influence of processing

When understanding the degradation mechanisms for the type of MOSFETs and having at one’s disposal the methods and models for the determination of the hot carrier lifetime, it is important to understand the processing factors and the parameters that affect the hot carrier resistance of the devices. In this respect, three parameters are of major importance [1]:

(i) The amount of hot carrier generation and injection in the channel

(ii) The amount of physical damage, generated by the injected hot carriers

(iii) The influence this damage has on the electrical characteristics of the MOSFET

All processing factors that can influence the hot carrier resistance have an impact on one of these three parameters.

In digital circuits, the devices are seldom stressed under static conditions. Although the static degradation conditions, treated in the previous section are already more realistic, they are still not relevant for the waveforms the devices see in real operation. Therefore, it is mandatory to study the degradation of the devices under the most realistic, i.e. dynamic, conditions and to know which effects have to be taken into account in order to extrapolate the results deduced under static stress conditions in a reliable way.
Fig. 3.4: (a) $\Delta V_{th}$ versus frequency for n-LD MOSFET with 0.24um channel length stressed at $V_d = 9.5V$, stress time = 10800s. (b) $\Delta g_m$
Taking into account the influence of these imperfections of the measurement setup, a renewed study of hot carrier induced dynamic degradation effects has been carried out, showing that for all studied cases the degradation behaves quasi-statically. A typical measurement that is used to verify the quasi-static nature of the degradation behavior, and that is very sensitive to non-quasi-static effects occurring during the edges of the gate voltage pulse, is the constant pulse shape experiment in which the rise and fall times are a constant portion of the period of gate voltage pulse. This means that when the frequency is increased, rise and fall times are decreased.

This is illustrated in Fig. 3.4 where the lifetime curve (full line) is extrapolated based on static stress experiments and compared with results of dynamic stress conditions.
Fig. 3.5: Lifetime ($\Delta V_{th} = 10\%$) as a function of $l/Vd$, Close circles are DC lifetime measurement, Open circle is for the dynamic degradation experiments.

One of the key factors for improving the hot carrier reliability is the drain engineering, which determines the amount of hot carrier generation for a given supply voltage and the influence of a certain physical damage on the electrical characteristics, the other is the oxide quality, which determines the amount of physical damage for a given hot carrier injection effluence.

In order to reduce these lateral electric fields for a given supply voltage and dimension, lightly doped drain (LD) structures have been used successfully for the 1.2 um down to 0.7 um generations for a 5 V supply voltage [35]. In these devices the peak of the lateral field is lowered by reducing the doping concentration near the drain and by providing a smooth junction
transition instead of an abrupt one. By self-aligned processing, the n-region is located underneath a spacer oxide and connects the channel to the highly doped junction. Because the gate has only limited control over the underlying LD region, the channel current is indeed extremely sensitive to the build-up of negative charge in the spacer oxide. The degradation behavior of these LD devices is therefore quite different from that in the conventional transistors and is characterized by a serious increase with time of the series resistance and a corresponding decrease of the channel current.

Several advanced drain-engineered structures have therefore been proposed which attempt to overcome the major drawbacks of the LD approach, being the reduced current drive due to the n+-gate offset and the spacer-induced degradation [36] – [39].

Besides the suppression of hot carrier generation by alternative drain engineering techniques, it is equally important to minimize the damage in the oxide for a given hot carrier injection effluence. In the past years, a lot of attention has been paid to the use of nitrided oxides and/or oxynitrides for improved dielectric reliability [40] – [44]. Such silicon oxynitride dielectrics are composed primarily of silicon dioxide, but with a small fraction of nitrogen build-up at the interface. There are different approaches for obtaining such nitrided oxides. In the so-called ROXNOX process (re-oxidized nitrided oxide), the nitridation consists first of an oxidation in \( \text{O}_2 \), followed by a nitridation step in \( \text{NH}_3 \), and finally a reoxidation again in \( \text{O}_2 \) [41]. In another approach, \( \text{N}_2\text{O} \) is used as the nitridation gas. In this approach, the nitridation can be done by growing the oxide in pure \( \text{O}_2 \), followed by a nitridation step in \( \text{N}_2\text{O} \), or the dielectric can be directly grown in \( \text{N}_2\text{O} \) ambient [42].
Concerning the influence of the nitridation on the charge trapping and interface trap generation, the picture is rather complicated. First of all, interface trap generation is found to be suppressed by the nitridation. This is attributed to the presence of nitrogen at the silicon-oxide interface, which reduces the number of strained Si-4 bonds at the interface, which normally act as interface trap precursors. Dielectrics with higher nitrogen content are therefore more effective in the suppression of the interface trap generation.

In all, hot carrier injection describes the phenomena by which carriers gain sufficient energy to be injected into the gate oxide. This occurs as carriers move along the channel of MOSFET and experience impact ionization near the drain end of the device. The damage can occur at the interface, within the oxide and/or within the sidewall spacer. Interface-state generation and charge trapping induced by this mechanism result in transistor parameter degradation, typically as switching frequency degradation rather than a “hard” functional failure.

It has been demonstrated that the hot carrier reliability problem has evolved from a more or less academic topic towards a real bottleneck to the further scaling down of MOSFET technologies. The main degradation mechanisms have been reviewed, under uniform and non-uniform static and dynamic conditions; some important processing-related effects have been illustrated, and the strategies for the improvement of the hot carrier lifetime have been briefly discussed.

Here are some constraints and limitations about HCI effect discussed [63] – [70]:

- HCI-induced transistor degradation is well modeled by peak substrate-current for the n-channels and peak gate current for the p-channels, at least for transistors at > 0.25μm.
• For sub-0.25μm P-channel, the drive current tends to decrease like NMOS after hot carrier stress.

• For sub-0.25μm P-channel, worst case lifetime occurs at maximum substrate current stress. The TF model is the same as N-channel.

• The drive-currents for the n-channel transistors tend to decrease after HCI stressing, the p-channel drive current tends to decrease.

• The off-state leakage can increase dramatically [70], especially for initially high current-drive p-channels.

• HCI-induced transistor degradation modeling seems to be accurate, but the extrapolation from transistor degradation to circuit-level degradation is uncertain and should be the focus of future research efforts.

• There is growing evidence that HCI physics may be starting to change at 0.25μm and smaller, leading changing worst-case stress conditions [67].

• Precise voltage models (rather than substrate current or gate current) would be very useful.

• HCI evaluations are almost always performed on test structures rather than products and done under dc conditions, thus the calculated lifetime should be considered a Figure of Merit for process comparison.

• A short “lifetime” observed with dc test structures does NOT imply unacceptable product performance under ac conditions.

• Typically, HCI degradation causes reduced circuit speed rather than catastrophic failure; although clearly a large enough speed reduction can cause device failure.
• For products where the substrate or gate current is unknown, large voltage acceleration is possible because gate and substrate current are exponential to the reciprocal gate oxide electric field.

• There have been reports that the temperature dependent of substrate current has positive activation energy when $V_{dd}$ is lower than 2.5V. The temperature dependent model for lower $V_{dd}$ is still under investigation.

Also, the models which describe the degradation induced by HCI are summarized as:

$$\Delta p = At^n$$  \hspace{1cm} (23)

where, $p$ is the parameter of interest ($V_t$, $g_m$, $I_{dsat}$, etc.), $A$ = material dependent parameter, $t$ = time, $n$ = empirically determined exponent which is a function of stressing voltage, temperature and effective transistor channel length.

**N-channel Model**

N-channel devices use an Eyring model (which makes the practical assumption of mathematically separable and independent variables):

$$TF = B(I_{sub})^{-N} \exp(E_a / kT)$$  \hspace{1cm} (24)

where:

$B$ = arbitrary scale factor (function of proprietary factors like doping profile, sidewall spacing, dimensions, etc.)

$I_{sub}$ = peak substrate current during stressing

$N = 2$ to $4$, typically $3$
$E_a = -0.1 \text{ eV to } -0.2 \text{ eV}$

**P-channel Model**

$$TF = B(I_{gate})^{-M} \exp(E_a / kT)$$

(25)

where:

$B = \text{arbitrary scale factor (function of proprietary factors, such as doping profiles,}$

$\text{sidewall spacing dimensions, etc.)}$

$I_{gate} = \text{peak gate current during stressing.}$

$M = 2 \text{ to } 4$

$E_a = -0.1\text{eV to } -0.2\text{eV}$

A “rough rule-of-thumb”, for the substrate current versus voltage dependence of P-channel devices is peak substrate current doubles for each 0.5V increase in source-drain voltage ($V_{ds}$).
CHAPTER FOUR: CIRCUIT DESIGN AND PERFORMANCE ANALYSIS

4.1 Introduction

DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, which are supplied with power from batteries. Such electronic devices often contain several sub-circuits with each sub-circuit requiring a unique voltage level different than that supplied by the battery (sometimes higher or lower than the battery voltage, and possibly even negative voltage). Additionally, the battery voltage declines as its stored power is drained. DC to DC converters offer a method of generating multiple controlled voltages from a single variable battery voltage, thereby saving space instead of using multiple batteries to supply different parts of the device.

Power amplifiers, also known as PAs, are used in the transmit side of RF circuits, typically to drive antennas. Power amplifiers typically trade off efficiency and linearity, and this tradeoff is very important in a fully monolithic implementation. Higher efficiency leads to extended battery life, and this is especially important in the realization of small, portable products. There are some additional challenges specifically related to being fully integrated. Integrated circuits typically have a limited power supply voltage to avoid breakdown, as well as a metal migration limit for current. Thus, simply achieving the desired output power can be a challenge. Power amplifiers dissipate power and generate heat, which has to be removed. Due to the small size of integrated circuits, this is a challenging exercise in design and packaging.
Several recent overview presentations have highlighted the special problems with achieving high efficiency and linearity in fully integrated power amplifiers.

4.2 Circuit Design

4.2.1 DC-DC Converter

Switching behavior of power MOSFETs in practical application circuits and shows the reader/designer how to choose the right device for the application using the specifications typically provided on manufacturer datasheets. The article goes through several methods of assessing the switching performance of power MOSFETs and compares these against practical results. The comparison shows that datasheet values can be used to obtain a reasonable indication of the switching performance of a MOSFET as well as its switching losses, but calculated switching transients will always be shorter than those actually achieved. Therefore, maximum parameters from the datasheet should always be used to give realistic results [71].

To get a fundamental understanding of the switching behavior of a MOSFET, it is best first to consider the device in isolation and without any external influences. Under these conditions, an equivalent circuit of the MOSFET gate is illustrated in Fig. 4.1, where the gate consists of an internal gate resistance \( R_g \), and two input capacitors, \( C_{gs} \) and \( C_{gd} \). With this simple equivalent circuit it is possible to obtain the output voltage response for a step gate voltage.

The voltage \( V_{gs} \) is the actual voltage at the gate of the device, and it is this point that should be considered when analyzing the switching behavior of the device.

If a step input is applied at \( V_{gs, app} \), then the following holds true:
\[ i_g = \frac{V_{gs_{\text{app}}} - V_{gs}}{R_g} \]  
(26)

\[ i_g = i_{gs} + i_{gd} \]  
(27)

\[ i_{gs} = C_{gs} \frac{dV_{gs}}{dt} \]  
(28)

and since \( V_{DS} \) is fixed

\[ i_{gd} = C_{gd} \frac{dV_{gs}}{dt} \]  
(29)

therefore:

\[ \frac{V_{gs_{\text{app}}} - V_{gs}}{R_g} = C_{gs} \frac{dV_{gs}}{dt} + C_{gd} \frac{V_{gs}}{dt} \]  
(30)

and

\[ \frac{dV_{gs}}{V_{gs_{\text{app}}} - V_{gs}} = \frac{dt}{(C_{gs} + C_{gd})R_g} \]  
(31)

giving

\[ -\ln(V_{gs_{\text{app}}} - V_{gs}) = \frac{t}{(C_{gs} + C_{gd})R_g} + k \]  
(32)

\[ V_{gs} = V_{gs_{\text{app}}} - k' e^{\left(\frac{-t}{(C_{gs} + C_{gd})R_g}\right)} \]  
(33)
when $t = 0$, $V_{gs} = 0$, therefore

$$V_{gs} = V_{gs_{\text{app}}} (1 - e^{(C_{gd} + C_{gs}) R_g})$$

(34)

This gives an indication of how long the actual gate voltage ($V_{gs}$) takes to get to the threshold voltage.

![Fig. 4.1: An equivalent MOSFET gate circuit showing just $C_{gs}, C_{gd}$ and $R_g$](image)

When the MOSFET is considered with additional parasites, it becomes increasingly difficult to manipulate these equations manually for such a practical circuit. If these second-order, or parasitic, components are ignored, then it is possible to come up with formulas for the turn-on and turn-off time periods of the MOSFET. These are given in Equations 10 through to 15 and the resulting waveforms are shown in Fig. 4.2 and Fig. 4.3. These equations are based on those developed by [72], where $R_g$ is the internal gate resistance, $R_{g_{\text{app}}}$ is the external gate resistance, $V_t$ is the MOSFET threshold voltage, and $V_{Gp}$ is the gate plateau voltage.
\[ t_1 = (R_g + R_{\text{g-app}})(C_{gs} + C_{gd}) \ln\left(\frac{1}{V_{th}} - \frac{V_{th}}{V_{gs_{\text{app}}}}\right) \]  

(35)

\[ t_2 = (R_g + R_{\text{g-app}})(C_{gs} + C_{gd}) \ln\left(\frac{1}{V_{gp}} - \frac{V_{gp}}{V_{gs_{\text{app}}}}\right) \]  

(36)

\[ t_3 = \frac{(V_{gs} - V_I)(R_g + R_{\text{g-app}})C_{gd}}{V_{gs_{\text{app}}} - V_{gp}} \]  

(37)

$V_F$ is the voltage across the MOSFET when conducting full load current and $V_{DS}$ is the voltage across the MOSFET when it is off.

This gives an accurate $t_1$ and $t_2$ when using datasheet values, but the time period $t_3$ is difficult to calculate since $C_{gd}$ changes with $V_{DS}$.

Fig. 4.2: Turn-on transient of the MOSFET
Using the same principles for turn-off, the formulas for the switching transients are given below:

\[ t_4 = (R_g + R_{g_{app}})(C_{gd} + C_{gs})\ln\left(\frac{V_{gs_{app}}}{V_{gs}}\right) \] (38)

\[ t_5 = (R_g + R_{g_{app}})C_{gd}\left(\frac{V_{ds} - V_F}{V_{gs}}\right) \] (39)

\[ t_6 = (R_g + R_{g_{app}})(C_{gd} + C_{gs})\left(\frac{V_{gs}}{V_t}\right) \] (40)

In this instance, \( t_4 \) and \( t_6 \) can be calculated accurately, but it is the formula for \( t_5 \) which is more difficult to solve, since during this time period \( V_{DS} \) will change, causing \( C_{gs} \) to also change. Therefore some method is required to calculate \( t_3 \) and \( t_5 \) without using the dynamic \( C_{gd} \).

Fig. 4.3: Turn-off transient of the MOSFET

Looking at the gate charge waveform [2] in Fig. 4.4, \( Q_{gs} \) is defined as the charge from the origin to the start of the Miller Plateau \( (V_{GP}) \); \( Q_{gd} \) is defined as the charge from \( V_{GP} \) to the end of
the plateau; and $Q_g$ is defined as the charge from the origin to the point on the curve at which the

driving voltage $V_{GS}$ equals the actual gate voltage of the device.
The rise in $V_{GS}$ during $t_2$ (Fig. 4.4) is brought about by charging $C_{gs}$ and $C_{gd}$. During this time $V_{DS}$ does not change and as such $C_{gd}$ and $C_{ds}$ stay relatively constant, since they vary as a function of $V_{DS}$. At this time $C_{gs}$ is generally larger than $C_{gd}$ and therefore the majority of drive current flows into $C_{gs}$ rather than into $C_{gd}$. This current, through $C_{gd}$ and $C_{ds}$, depends on the time derivative of the product of the capacitance and its voltage. The gate charge can therefore be assumed to be $Q_{gs}$.

The next part of the waveform is the Miller Plateau. It is generally accepted that the point at which the gate charge figure goes into the plateau region coincides with the peak value of the peak current. However, the knee in the gate charge actually depends on the product ($C_{gd}V_{GD}$) with respect to time. This means if there is a small value of drain current and large value of output impedance, then $I_{DS}$ can actually reach its maximum value after the left knee occurs. However, it can be assumed that the maximum value of the current will be close to this knee.
point and throughout this application note it is assumed that the gate voltage at the knee point corresponds to the load current, $I_{DS}$.

The slope of the Miller Plateau is generally shown to have a zero, or a near-zero slope, but this gradient depends on the division of drive current between $C_{gd}$ and $C_{gs}$. If the slope is non-zero then some of the drive current is flowing into $C_{gs}$. If the slope is zero then all the drive current is flowing into $C_{gd}$. This happens if the $C_{gd} V_{GD}$ product increases very quickly and all the drive current is being used to accommodate the change in voltage across $C_{gd}$. As such, $Q_{gd}$ is the charge injected into the gate during the time the device is in the Miller Plateau.

It should be noted that once the plateau is finished (when $V_{DS}$ reaches its on-state value), $C_{gd}$ becomes constant again and the bulk of the current flows into $C_{gs}$ again. The gradient is not as steep as it was in the first period ($t_2$), because $C_{gs}$ is much larger and closer in magnitude to that of $C_{gd}$.

![Fig. 4.4: Combination of gate charge and capacitance to obtain switching times](image)

The objective of this note is to use datasheet values to predict the switching times of the MOSFET and hence allow the estimation of switching losses. Since it is the time from the end of $t_1$ to the end of $t_3$ that causes the turn-on loss, it is necessary to obtain this time (Fig.4.2).
Combining (35) and (36) it is possible to obtain the rise time of the current \( t_{ir} = t_2 - t_1 \) and because \( V_{DS} \) stays constant during this time then it is possible to use the specified datasheet value of \( C_{iss} \) at the appropriate \( V_{DS} \) value. Assuming the transfer characteristic is constant, then \( V_{GP} \) can be substituted for \( V_{th} + I_DS/g_{fs} \), hence:

\[
t_{ir} = (R_g + R_{g\_app})C_{iss}V_{ds} \ln\left(\frac{g_{fs}(V_{gs\_app} - V_{th})}{g_{fs}(V_{GS\_app} - V_t) - I_DS}\right) \tag{41}
\]

\[
t_{of} = \frac{Q_{gd\_d}}{(V_{DS\_d} - V_{F\_d})} \frac{(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_{gs\_app} - (V_{th} + I_{ds}/g_{fs}))} \tag{42}
\]

It is difficult to use a value of \( C_{gd} \) for the fall time period of \( V_{DS} (t_{of} = t_3) \). Therefore if the data sheet value of gate charge is used \( (Q_{gd\_d}) \) and divided by the voltage swing seen on the drain connection \( (V_{DS\_d} \text{ minus } V_{F\_d}) \) then this effectively gives a value for \( C_{gd} \) based on the datasheet transient.

Similarly for the turn-off transition, the voltage rise time \( (t_{vr} = t_5) \) is:

\[
t_{vr} = \frac{Q_{gd\_d}}{(V_{DS\_d} - V_{F\_d})} \frac{(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_t + I_{ds}/g_{fs})} \tag{43}
\]

and the current fall time \( (t_{if} = t_6) \) is:

\[
t_{if} = (R_g + R_{g\_app})(C_{iss}V_{ds}) \ln\left(\frac{V_t + I_{ds}}{g_{fs}}\right) \tag{44}
\]

The definition of the turn-on and turn-off times given in the datasheet can be seen in Fig. 4.5. These definitions can be equated to the equations described above and are shown here:

\[
t_{d(on)} \approx t_1 + t_{ir} \tag{45}
\]
\[ t_r \approx t_{vf} \] \hspace{2cm} (46)

\[ t_{d(off)} \approx t_4 \] \hspace{2cm} (47)

\[ t_f \approx t_{vr} \] \hspace{2cm} (48)

**Fig. 4.5: Sketch showing definition of turn-on and turn-off times**

The minimum switching transients were calculated using the appropriate value of the parameters, which resulted in producing the shortest switching transient value. In some circumstances this meant that the maximum value of a parameter was used to calculate the minimum switching transient and vice versa for the maximum switching transients.

The rise and fall times for power MOSFETs can be approximated with relative ease when evaluated in isolation. By plugging in datasheet values into the formulas derived above, we can get a reasonable indication of the switching performance of the MOSFET as well as the switching losses. However, since second order parasitic is not included the analytical equations
will always be shorter than those actually achieved. Hence the maximum parameters from the datasheet should always be used to give realistic results.

A full bridge DC-DC converter given in [74, 75] was established in Cadence with the extracted models from the test device, as shown in Fig. 4.4.

![Fig. 4.6: A simplified schematic of the full bridge DC-DC converter](image)
4.2.2 Power Amplifier

RF LDMOS becomes increasingly important in wireless communication applications. LDMOS used in RF power amplifiers has high voltage in gate and drain simultaneously. The simplified schematic of power amplifier under study [76] is shown in Fig. 4.7. The supply voltage is 3.3 V and the gate bias is 1.5 V. It is operated in class-C mode. The power supply is given by

$$ P_{cc} = \frac{V_{cc} I_{cc}}{\pi} (\sin \theta - \theta \cos \theta) \quad (49) $$

Efficiency for this maximum possible voltage swing is given by

$$ \eta_{\text{max}} = \frac{2\theta - \sin 2\theta}{4(\sin \theta - \theta \cos \theta)} \quad (50) $$

The actual output power for an output peak voltage of $V_{op}$ can be found as a function of $\theta$. 
Fig. 4.7: A schematic of a class-C power amplifier
5 CHAPTER 5: DEGRADATION SUBJECT TO STRESS

Smart power management applications often require high current power devices. These technologies combine bipolar, CMOS, and power DMOS on a single chip. The n-channel lateral double-diffused MOS (or LDMOS) is a common choice for the transistor driver. In addition, RF LDMOS becomes increasingly important in wireless communication applications. With continuous scaling of device dimensions, MOS transistors are more vulnerable to high field phenomenon such as hot-electron effect. It is known that hot-electron induces MOS LDMOS device/circuit degradations [77] – [83]. LDMOS used in RF power amplifiers has high voltage in gate and drain simultaneously. The power device is forced to operate at high electric field and while carrying high current, suffering from a critical hot-carrier attack.

Recently, Moens et al [84] – [85] explained two different and competing mechanisms in LDMOS hot carrier behavior. The channel mobility degradation leads to an increase in on-resistance upon stressing and the hot hole injection and trapping in the accumulation region decrease the on-resistance. Brisbin et al [86] discussed layout optimization of LDMOS array to improve the hot carrier reliability. Manzini [87] evaluated hot carrier degradation of n-channel LDMOS for various gate lengths and oxide thicknesses. Gajadharsing [88] presented an LDMOS transistor with improved distortion characteristics utilizing a distributed threshold voltage concept. Smart power management applications combine bipolar, CMOS, and power DMOS on a single chip. The n-channel lateral double-diffused MOS (LDMOS) is a common choice for the transistor driver. In addition, RF LDMOS becomes increasingly important in wireless communication applications. LDMOS used in RF power amplifiers has high voltage in gate and
drain simultaneously. The power device is forced to operate at high electric field while carrying high current, suffering from a critical hot-carrier (HC) attack.

Hot-carrier degradations subject to dynamic (or AC) stress waveforms were compared with the static stress condition. Previous publications focused on modeling [89] – [91], physical mechanism [92] – [95], and device damage [96] – [98]. With the competing degradation mechanisms involved in deep-sub micrometer MOS transistors, the DC evaluation becomes inaccurate to estimate the HC circuit degradation. Dynamic stress condition correlating to the real circuit operation is required to insure the hot-carrier circuit reliability in a meaningful way [99] – [102].

In this work, we examine the threshold voltage, transconductance, on-resistance, gate capacitances, and gate charge of the n-channel LDMOS transistor subject to hot electron stress. Transistor model parameters before and after stress are extracted. The stress effect on the gate charge energy is evaluated via simulation.

We study the LDMOS transistor hot carrier effect subject to dynamic stress for different duty cycles. The high frequency equivalent circuit model is introduced. The modeling results are verified by experimental data. RF characteristics such as $s$-parameters are examined via measurement and simulation.

### 5.1 Device Degradation

#### 5.1.1 DC

The transconductance $g_m$ represents the sensitivity of drain current with respect to gate-source bias. The threshold voltage is defined as the minimum gate bias required turning on the
conduction channel between the source and drain. Fig. 5.1 shows that the transconductance and threshold voltage as a function of stress time. The transconductance decreases and the threshold voltage increases after stress. The on-resistance is an important parameter for determining the switching power loss. The on-resistance includes the source diffusion resistance, channel resistance, and drift region resistance. From Fig. 5.2, $R_{on}$ increases about 5% after 5.5 hours of stress. Fig. 5.3 displays the normalized degradation of $R_{on}$ versus normalized $V_{th}$ degradation. $\Delta R_{on}/R_{on}$ exhibits a linear relationship with respect to $\Delta V_{th}/V_{th}$ at low threshold voltage degradation and then saturates when $\Delta V_{th}/V_{th}$ is greater than 6%.

![Fig. 5.1: Transconductance and threshold voltage as a function of stress time](image)
Fig. 5.2: Normalized on-resistance change as a function of stress time
Fig. 5.3: Normalized on-resistance degradation versus normalized threshold voltage degradation
In the meantime, the dynamic stress is applied into our experiment. The on-wafer LDMOS transistors are tested in a Cascade 12000 Probe station. Agilent 4156 is used to set the hot-electron stress also. A pulse generator generates square waveforms with adjustable frequency, amplitude, and duty cycle. An oscilloscope observes the waveforms produced by the function generator.

There are two stress conditions, namely, 1) constant gate-source voltage $V_{GS}$ and constant gate-drain voltage $V_{GD}$ (DC stress) and 2) constant gate-source voltage and pulsed gate-drain voltage (dynamic stress). In this work the DC stress is at $V_{GS} = 3$ V and $V_{GD} = 11.5$ V and the dynamic stress is pulsed at 100 MHz. The pulsed stress condition intends to mimic the circuit operating condition.

Fig. 5.4 (a) and (b) show the normalized transconductance $g_m$ and threshold voltage $V_{th}$ degradations versus duty cycle for different stress conditions. The stress experiment was stopped at 3600 seconds and 10800 seconds in order to measure $g_m$, $V_{th}$, and $I_d$ data. Both $\Delta g_m/g_m$ and $\Delta V_{th}/V_{th}$ increase with duty cycle because of more stress time for a given period at high duty cycle. For example, $V_{th}$ changes 1.5% after 10800 s of dynamic stress at 25% duty cycle, and 7.45% after 10800 s of DC stress (duty cycle is 100%). The threshold voltage before stress was 0.52 V. The normalized $I_d$ shift as a function of drain-source voltage is plotted in Fig. 5.4 (c). $\Delta I_d/I_d$ decrease with drain-source voltage because the drain current degradation is enhanced in the linear region than the saturation region after hot electron stress. It is clear in Fig. 5.4 (c) that the DC stress results in more degradation than that of dynamic stress.
$\Delta V_{\text{th}} / V_{\text{th}}$ (%)

Duty Cycle (%)

- stressed for 3600 s
- stressed for 10800 s

(a)
(b)
Fig. 5.4: (a) Normalized threshold voltage change versus duty cycle, (b) normalized transconductance change versus duty cycle, and (c) normalized drain current degradation versus drain-source voltage at $V_{GS} = 2.4$ V.

5.1.2 CV

Using Agilent 4284A LCR precision meter, capacitances are measured at different biases. Fig. 5.5 (a) shows the gate-drain capacitance $C_{GD}$ versus gate-drain voltage before and after stress. $C_{GD}$ is a nonlinear function of bias and provides a feedback path between the input and the output of the device. Fig. 5.5 (b) shows the gate-source capacitance versus gate-source voltage and Fig. 5.5(c) shows the gate-body capacitance and gate-body voltage before and after stress.
The experimental results demonstrate significant change of $C_{GD}$ and $C_{GB}$ after hot electron stress, while $C_{GS}$ is relatively unchanged. Hot electron induces interface charges which alter the surface potential and change $C_{GD}$ and $C_{GB}$. The trapped charge at the drain end of the channel doesn’t change $C_{GS}$ much.
(b)
5.1.3 RF

S-parameters are measured up to 20 GHz. The ‘open’, ‘short’, and ‘through’ structures surrounding the device-under-test is used to de-embed parasites. Fig. 5.6 shows the extracted gate resistance versus gate-drain voltage after 10800 seconds of dynamic stress (50% duty cycle) and DC stress. The gate resistance increases with gate voltage and increased under the DC stress. The shift of S-parameters as a function of duty cycle is shown in Fig. 5.7. The decrease in $S_{21}$
indicates the reduction of power gain after stress. The gate-source and drain-source voltage are set to 2.4 V and 5 V, respectively, in this experiment. The device is operating in the saturation region. The inductance and resistance values used in the transistor simulation are $L_g = 12 \text{ nH}$, $L_d = 96.9 \text{ nH}$, $L_s = 10 \text{ nH}$, $L_b = 0.01 \text{ nH}$, $R_g = 251 \text{ } \Omega$, $R_{bd} = 0.1 \text{ } \Omega$, $R_{sb} = 0.1 \text{ } \Omega$, $R_{bpd} = 55.5 \text{ } \Omega$, and $R_{bps} = 55.5 \text{ } \Omega$. All S-parameters changed after the dynamic stress of 10800 seconds. Fig. 5.8 displays the cutoff frequency $f_T$ degradation from measured S-parameter data and IC-CAP extraction as a function of gate-source voltage after 10800 seconds of dynamic stress (50% duty cycle) and DC stress. The cutoff frequency decreases after stress due to the reduction in transconductance and an increase in gate capacitance. The DC stress decreases $f_T$ more than that of dynamic stress. Key device parametric shifts are summarized in Table 3.
Fig. 5.6: Gate resistance versus gate-drain voltage
Fig. 5.7: (a) $S_{11}$, (b) $S_{12}$, (c) $S_{21}$, and (d) $S_{22}$ measured from 100 MHz to 20 GHz biased at $V_{GS} = 2.4$ V and $V_{DS} = 5$ V. In those plots line with open circles: fresh, line with inverse open triangles: 50% duty cycle dynamic stress, line with x marks: DC stress. The stress time is 10800 s.
Table 4: Key transistor parameter changes subject to two different stress conditions

<table>
<thead>
<tr>
<th>Parameters</th>
<th>50% duty cycle stress</th>
<th>DC stress</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>after 1 hour</td>
<td>after 2 ½ hrs</td>
</tr>
<tr>
<td>BSIM3 Core</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{th0}$</td>
<td>1.75%</td>
<td>3.45%</td>
</tr>
<tr>
<td>$\Delta k_1$</td>
<td>0.92%</td>
<td>2.15%</td>
</tr>
<tr>
<td>$\Delta \mu_0$</td>
<td>-2.39%</td>
<td>-4.77%</td>
</tr>
<tr>
<td>$U_a$</td>
<td>-3.16%</td>
<td>-4.72%</td>
</tr>
<tr>
<td>$\Delta C_{gd0}$</td>
<td>1.23%</td>
<td>3.24%</td>
</tr>
<tr>
<td>$\Delta C_{gs0}$</td>
<td>1.11%</td>
<td>2.23%</td>
</tr>
<tr>
<td>$\Delta C_j$</td>
<td>1.18%</td>
<td>3.45%</td>
</tr>
</tbody>
</table>
Fig. 5.8: Cutoff frequency versus gate-source voltage. The drain-source voltage is 5 V.
5.2 Circuit Degradation

5.2.1 DC-DC Converter

The BSIM3 model parameters for fresh and stressed devices are extracted using IC-CAP. The simulation results are compared with the experimental data as shown in Fig. 5.9. Good agreement between the model predictions and measurement for fresh and stressed transistors is obtained. The fresh and stressed device models will be used in DC-DC converter circuit simulation.

The threshold voltage ($V_{th}$), peak transconductance ($g_{m,max}$), on-resistance ($R_{on}$), gate-source capacitance ($C_{GS}$), and gate-drain capacitance ($C_{GD}$) are reported and summarized in Table 4.
Fig. 5.9: The comparison between simulation and measurement, Drain-source current versus drain-source voltage, after stressed.
Table 5: Parameter shifts due to HC stress

<table>
<thead>
<tr>
<th>Stress Time (s)</th>
<th>$V_{th}$ (V)</th>
<th>$g_{m,\text{max}}$ (S)</th>
<th>$R_{on}$ (Ω)</th>
<th>$C_{GS}$ (pF)</th>
<th>$C_{GD}$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.514</td>
<td>0.044</td>
<td>7.88</td>
<td>0.378</td>
<td>0.014</td>
</tr>
<tr>
<td>120</td>
<td>0.519</td>
<td>0.0446</td>
<td>8.85</td>
<td>0.381</td>
<td>0.015</td>
</tr>
<tr>
<td>300</td>
<td>0.52</td>
<td>0.0447</td>
<td>9.0</td>
<td>0.382</td>
<td>0.016</td>
</tr>
</tbody>
</table>

From the design point of view, the gate charge is more important than gate capacitance since it is easier to calculate the amount of charge or current required to turn on the device in a desired time frame. A test circuit to determine the gate charge is displayed in Fig. 5.10. In this circuit, a small current source (1 pA) is connected to the gate of the device making the switching time visible. A constant current is in the drain so that the gate charge is related to a given current and voltage in the source-to-drain path [103] Fig. 5.11 shows the typical switching waveforms $V_{GS}$ and $V_{DS}$ before and after stress. In Fig. 5.12 the solid lines represent the voltage waveforms before stress and the dashed lines represent the voltage waveforms after stress. When the switch turns on, the gate-source voltage begins to increase until it reaches $V_{th}$ at which the drain current charges the gate-source capacitance, $C_{GS}$ continues to charge up, while the gate voltage rises and the drain current increases proportionally. At 4.05 s the gate-source capacitance is charged completely and the drain current reaches the predetermined current and stays constant while the drain voltage falls. When the gate-source capacitance is fully charged at 4.05 s ($V_{GS}$ remains the same), the drive current now charges the Miller capacitance $C_{GD}$ until 4.45 s as shown in Fig. 5.13. In Fig. 5.14 the area covered by solid line represents to the gate charge for the fresh device, and the area under the dash line is corresponding to the stressed device. The initial slope of $V_{GS}$
for fresh and stressed devices is about the same. The stressed device, however, has a smaller transconductance and requires higher voltage for a given amount of drain current. Therefore, $Q_{GS}$ for the stressed device is larger than that of the fresh device. The total charge required to turn on the fresh device is less than that required for the stressed device. Since the energy is the product of the gate charge and the gate voltage, the fresh device requires less energy than that of the stressed device to turn on a driver device.

Fig. 5.10: A gate charge test circuit
Fig. 5.11: Gate-source and drain-source voltages versus time
A full bridge DC-DC converter using extracted model parameters is simulated in Cadence, as shown in Fig. 4.6; In Fig. 4.6 the input voltage is 12 V, the output voltage is 3.3 V, and the output inductance is 2.3 μH. The isolation transformer turn ratio is 4 to 2. The switching frequency is 200 kHz.

To investigate the stress effects on the switching performance. The oscillograms of the gate-to-source voltage neatly delineate between the charge required for the gate-to-source capacitance, and the charge required for the gate-to-drain, or “Miller” capacitance [104]. The switching performances of transistors are determined by the parasitic capacitances, which shifted after stress. The shifts in switching performance were carried out by applying the compact model
extracted from the test device before and after stress using IC-CAP. Initially, the switch is closed. The gate voltage and drain current are zero. The switch is opened at about 5 us; the gate-to-source capacitance starts to charge, and the gate-to-source voltage increases. Because the shifts in gate-to-source capacitance due to stress, the $V_{GS}$ curve changed after stress in this period. No current flows in the drain until the gate reaches the threshold voltage. At next period, the gate-to-source capacitance continues to charge, the gate voltage continues to rise and the drain current rises proportionally. The threshold voltage changed after stress. Therefore, the start rising point for the drain current shifts. So long as the actual drain current is still building up towards the available drain current, $I_D$, the freewheeling rectifier stays in conduction, the voltage across it remains low, and the voltage across the switch continues to be virtually the full circuit voltage, $V_{DD}$. The top end of the drain-to-gate capacitance therefore remains at a fixed potential. When the drain current reaches $I_D$, and the freewheeling rectifier shuts off; the potential of the drain now is no longer tied to the supply voltage. The drain current now stays constant at the value $I_D$ enforced by the current source starts to fall. Since the gate voltage is inextricably related to the drain current by the intrinsic transfer characteristic of the device, the gate voltage now stays constant because the “enforced” drain current is constant. For the time being therefore, no further charge is consumed by the gate-to-source capacitance, because the gate voltage remains constant. Thus the drive current now diverts, in its entirety, into the capacitance $C_{GD}$, and the drive circuit charge now contributes exclusively to discharging the $C_{GD}$ capacitance. Due to the shifts in $C_{GD}$ after stress, the $V_{GS}$, $V_{DS}$, and drain current curves shift due to the stress this. The drain voltage excursion during the next period is relatively large, and hence the total drive charge is typically higher for the $C_{GD}$ than for the $C_{GS}$. When the drain voltage falls to a value equal to $I_D \times R_{ON}$, and
the switch device now comes out of the “active” region of operation. The gate voltage is now no longer constrained by the transfer characteristic of the device to relate to the drain current, and is free to increase. From Sec. 2, one gets that $R_{ON}$ degraded after stress. Therefore, the second start rising point of $V_{GS}$ changed after stress. The switching performances degraded significantly after stress for 300 seconds.

For the DC-DC converter application, $C_{GS}$ is the most important capacitance [75]. It dominates the output switching waveforms through the ‘Miller’ effects. The effects of gate-source capacitance on gate voltage - $C_{GS}$ and current waveforms are determined by gate drive internal impedance. From Sec. 2, one gets that $C_{GD}$ changed 12.5% and $C_{GS}$ changed 1% after 300 second stress. Therefore, the performance degradation in the DC-DC converter is anticipated. The primary voltage and transformer primary current waveforms are given in Fig. 5.13 and Fig. 5.14. One gets that the switching performance shifts in the power LDMOSFET can bring slight changes in the primary voltage and current.
Fig. 5.13: Simulated voltage waveforms of the primary side of the transformer. (a) Simulation from 0 us to 10 us; (b) Details in the circle shown in (a).

The efficiency relates to the transient (dynamic) performance of the switching devices. As discussed above, the transient performance of the power device changed after stress. Although the changes is not severe, the efficiency curves for the fresh and stressed devices tell us that it degraded significantly after HC stress, as shown in Fig. 5.14.
Fig. 5.14: Simulated voltage waveforms of the primary side of the transformer. (a) Simulation from 0 us to 10 us; (b) Details in the circle shown in (a).

The power efficiency versus output power is simulated and shown in Fig. 5.15. The power efficiency is related to the transient performance of the switching devices [75]. In Fig. 5.15 the power efficiency increases with output power, and decreases after hot electron stress at a given output power.
Fig. 5.15: Efficiency curves stress time is 300 s.
5.2.2 Power Amplifier

In the previous chapter, both measured and simulated results show that the FOMs degrade in device after dynamic stress. It is predictive that the RF circuit performance degradation will follow. Good agreement between simulation and measurement verify that the developed model is suitable to evaluate the RF performance degradation in RFICs.

A RF power amplifier (PA) is given in Fig. 4.12. The PA is designed to operate in the class-C mode [76]. The LDMOS has the channel length of 0.25 μm, the channel width of 36 μm, and 80 multi-fingers. For single-tone harmonic distortion analysis, a large-signal sinusoid with 960 MHz frequency is applied at the input to the power device and the steady-state large-signal response is evaluated. The simulated power gain versus input power is shown in Fig. 5.17(a). The power-added efficiency (PAE) is plotted in Fig. 5.17(b). Two-tone simulations are performed for the PA at 960 MHz, with 1 MHz separation. The HSPICE circuit simulation results show that the PAE and output power degrade after hot carrier stress and the degradation is enhanced under the DC stress.
Output power (dBm)

Input power (dBm)

(a)

- DC stress
- 50% duty cycle
- fresh
5.3 Summary

The LDMOS transistor subject to hot electron stress is evaluated experimentally. The threshold voltage increases and the transconductance decreases after hot electron stress. Transistor model parameters are extracted and used in the model simulation. The model predictions agree with the experimental data for the both fresh and stressed devices. The gate charge transfer characteristic using the LDMOS model before and after stress is then simulated. The gate charge required to turn on the driver device increases after hot electron stress. A full
bridge DC-DC converter is simulated using Cadence SPICE. The simulation result shows that the power efficiency decreases after hot carrier stress.

Although the parameters shift slightly in our 0.25μm high voltage LDMOS, the switching performances degraded significantly. A full bridge DC-DC converter was evaluated by simulation. The primary voltage and current change slightly due to HC stress. However, the key performance – efficiency, suffers from the HC stress significantly.

RF LDMOS performances subject to dynamic stress are compared with those under DC stress. The LDMOS is more vulnerable to DC stress than dynamic stress. The n-channel LDMOS transconductance decreases and threshold voltage increases with stress time. The transistor model predictions (drain current and S-parameters) are verified with experiments. Good agreement between the model predictions and measurement data before and after stress is obtained. Power amplifier RF performances such as the output power and power-added efficiency degrade after dynamic hot electron stress.
6 CHAPTER SIX: CONCLUSIONS

6.1 Summary

First of all, the hot carrier reliability on submicron LD MOSFETs has been demonstrated. The main degradation mechanisms have been reviewed, under uniform and non-uniform static and dynamic conditions; some important processing-related effects have been illustrated, and the strategies for the improvement of the hot carrier lifetime have been briefly discussed.

Moreover, this study presents that the gate charge transfer characteristic shows great vulnerability due to the hot carrier effect on the LD MOSFETs. The parameter extraction is used to simulate the gate charge transfer performance. Measured results are provided to verify accuracy of models. In the end, the discussion about the gate charge transfer characteristic provides an insight into the hot carrier effect on the drive circuit design of power switching application.

In the end, the RF performance degradation under the dynamic stress has been studied. Different duty cycle waveforms are used to stress the 0.25um LD MOSFETs. The result shows the device is more vulnerable to DC stress (100% duty cycle), compared to other duty cycle stress. The ac large-signal model for the LD MOSFETs is cited with improved parameter extraction procedures. Measurement result has been used to verify the accuracy of models. With the calibrated model, RF performance curves for large-signal gain, efficiency and linearity of a power amplifier is examined.

This research presents a system thought about the hot carrier effect on LD MOSFETs.
6.2 Further Work

The use of professional tools is a prerequisite to develop accurate device models and simulation circuits, from DC to GHz, including noise modeling and nonlinear HF effects, within a reasonable time. With technology going faster and faster towards ultra-high frequencies, circuit designs can only be accurate and right-the-first-time if the underlying device models are accurately modeled with physically meaningful model parameters.

Designers need to learn to design for reliability and they should be educated on additional reliability analyses. The value is the reduction of failure and redesign costs.

A complete flow allowing digital and analog designers to compute reliability circuit simulation is necessary. Reliability circuit simulation tools are expected to build with those blocks: (1) Stress measurement (2) Reliability analysis (3) Extraction and modeling (4) Circuit simulation with reliability parameters and specification. The system-level reliability computer-aided tool will be my next research focus.
Fig. 6.1: A proposed complete flow to compute reliability circuit simulation
REFERENCES


[10] [http://www-device.eecs.berkeley.edu/~bsim3/intro.html](http://www-device.eecs.berkeley.edu/~bsim3/intro.html)


