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COMPARISON OF SINGLE STAGE AND
TWO STAGE GRID-TIE
INVERTERS

by

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B.S. University of Central Florida, 2005

A thesis submitted in partial fulfillment of the requirements
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ABSTRACT

This thesis compares two methods of designing grid-tie inverters. The first design topology is a traditional two stage approach consisting of an isolated DC-DC converter on the input followed by a high switching frequency SPWM (Sinusoidal Pulse Width Modulation) stage to produce the required low frequency sine wave output. The novel second design approach employs a similar DC-DC input stage capable of being modulated to provide a rectified sine wave output voltage/current waveform. This stage is followed by a simple low frequency switched Unfolding Stage to recreate the required sine wave output.

Both of the above designs have advantages and disadvantages depending on operating parameters. The following work will compare the Unfolding Output Stage and the SPWM Output Stage at various power levels and power densities.

Input stage topologies are similarly examined in order to determine the best design approach for each output stage under consideration.
ACKNOWLEDGMENTS

I would like to thank my advisor Dr. Batarseh for his support and guidance. Along with Dr. Siri for his helpful insight which saved me months of time working in the lab without seeing daylight. I would not be here at this point if it was not for them. Also, I would like to thank everyone at SURGE lab, ApECOR, and Florida PEC for all their unyielding help, support, and guidance as well. I would have not been able to finish if it was not for you all, thank you very much.
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CHAPTER 1: INTRODUCTION

The law of supply and demand states that as the demand for a product increases, the supply of that product will decrease. Since the supplier can not keep up with the demand for the product the price of that product will increase to lower the demand and allow the supplier to keep up with the demands of the consumers. This leads to the rise in the price of the product, in this case energy. Since most energy comes from non-renewable sources such as fossil fuel or nuclear energy, the more we use the less supply there will be further increasing the price.

To make matters worse, during the process of creating this energy, pollution is created as a by-product. This means the more energy the world requires the more pollution the world creates. There are alternative sources of energy that do not pollute and are renewable which means that they can’t be used up such as the fossil fuels or nuclear types of energy. These renewable energies can help lower the cost of energy and also slow down pollution. The way that the renewable energy can help lower cost is by offsetting the demand for energy.

Renewable energy sources could on there own replace the non-renewable types of energy if properly sized. However, the renewable energies have a down side to them that is most don’t produce energy continuously such as with the non-renewable types. This is due to the way that the renewals produce the energy such as: solar only creating energy during the daytime and power level lowering dependant on ambient conditions, wind only creating energy when the wind is between certain speeds (i.e. if the wind is too low the generator can’t produce energy and too high the generator will break), and tidal gets its power related to the distance the moon is from the earth. Due to this non-continuous energy production the renewals need energy storage devices (such as batteries and super capacitors) that can store the excess energy during peak
power production and distribute the stored up energy during times of low power production. Because of this non-continuous energy production the renewable energy generator must be oversized so that it can meet the average power needs.

To find the simplified average power that the renewable generator can produce an assumption is made. This assumption is that the maximum power that can be generated from the renewable source is constant at that maximum power over the time that the renewable can generate the power as can be seen in Figure 1. However, using this simplification excess average power will be introduced and the generator may not be oversized enough.

![Figure 1 Renewable Power Production Curve](image)

The amount of power that the renewable power generator needs to be oversized by to meet the average power needs can be calculated by EQ. 1.

\[
P_{avg} = \frac{1}{T_s} \int_0^{T_f} P_p(t) \cdot dt \Rightarrow \frac{1}{T_s} \left( \int_0^{T_{on}} P_{pk} \cdot dt + \int_{T_{on}}^{T_f} 0 \cdot dt \right) \Rightarrow P_{pk} \cdot \frac{T_{on}}{T_s} \Rightarrow
\]

\[
P_{pk} = \frac{P_{avg} \cdot T_s}{T_{on}}
\]
However, if the renewals were not used to replace the non-renewable sources but merely offset the peak power production as such as with distributed generation. Then renewable sources do not need to be oversized as if they were the only generation source. Along with more appropriately sizing the renewable sources distributed generation has the potential to lower cost to the consumer, increase power quality (which in turn lowers cost to the utility company), increase reliability of the grid, enable peak power shaving, and reduce the need to build or upgrade new transmission/distribution lines.

The renewable source that is particularly useful in distributed generation is solar arrays. This is because the time that the utility company sees peak power consumption is during the day which is when the solar array would be providing power, enabling the ability to peak power shave. This ability of peak power shaving is having another power generation source paralleled to the grid and only starts to produces power when the power being consumed rises above a specified level. Another reason that solar arrays are preferable to other renewable sources for lower power levels is location and safety. A solar array panel can easily be installed on the top of a house where space is not being used so wanted space will not be used up like with other generators. Also unlike wind generators there are no moving parts so there is less likeliness of anyone getting hurt. The major draw backs to solar are that the panels have low efficiency conversions (but this can increase with time) and the power is produced at low voltage (but could be stacked to higher voltages).

The main reasons that the renewable sources are slow to be accepted is because of the high initial cost to the consumer, it is unknown what adding many small distributed sources in parallel to the power grid will do, and cost for restructuring the grid for improved
communication of loads and sources. However, the potential benefits for distributed sources if properly and carefully considered can outweigh the costs. As stated before due to the high initial cost and locations of the sources the preferred renewable source is a low power (around 1 kW) solar array which is what the inverter for this thesis is based on. The main purpose of this work is to compare Single Stage versus the Two Stage inverter approach. CHAPTER 2 and CHAPTER 3 will discuss the Two Stage approach while CHAPTER 4 will focus on the Single Stage and CHAPTER 5 will be a summery and conclusions of the finding.
CHAPTER 2: INVERTER STAGE

Introduction

A DC to AC inverter system usually has two high switching frequency stages. The first stage of the inverter system is a DC to DC converter regulating the input voltage to the second stage (the bus voltage).

![Figure 2: Inverter System](image)

The second stage, the Inverter Stage, shown in Figure 2, is where the conversion from DC to AC happens. This conversion happens due to the duty ratio varying in a sinusoidal pattern for a wanted sine wave output. Also, almost any other waveform can be created here where the main limiting factor is the frequency of the outputted waveform.

One of the main reasons the inverter is placed on the secondary side is so that the isolation transformer can operated at high frequencies, shrinking the size and weight of the transformer significantly. In addition, having the inverter stage on the secondary side allows for easier control, and it also enables the system to be more adaptive over a wider range of requirements. The inverter stage yields more adaptability due to its nature to be bi-directional,
which means the load doesn’t have to be purely resistive. Since the inverter stage is Bi-
directional by nature an inductive load can be applied with minimum component increase.

Component Selection

Inductance

The first step in creating the inverter stage is choosing the correct components. \( L_o \) is used
to filter the output current to decrease the total harmonic distortion (THD) and as a result to
increase the power factor. The phase displacement due to the increased inductance value can be
offset through a properly designed controller. So with a correctly chosen \( C_o \) (output capacitor
chosen to do the same thing as \( L_o \) but for the voltage) and \( L_o \) a power factor near unity can be
achieved.

From EQ. 4, EQ. 5 (that will be stated later) the duty ratio is different for the HPWM
(hybrid pulse width modulation) and Bi-Polar driving schemes therefore the current ripple will
be different for those two driving schemes. In addition, the voltage that is being applied to the
output is different using those two schemes. With the Bi-Polar method, a positive, negative bus
voltage, and zero is being applied while the HPWM only has either positive and zero or negative
and zero being applied to the output. Since the Bi-Polar has twice the voltage swing of the
HPWM, the Bi-Polar will require larger capacitance and inductance values to have the same
ripple as the HPWM method.
Figure 3 Current Ripple for a Constant $L_o$

From Figure 3 the current ripple with a constant $L_o$ can be observed, based upon EQ. 2, EQ. 4, and EQ. 5. Figure 3 shows that the HPWM has a much lower current ripple than that of the Bi-Polar and simply adding more inductance value is impractical due to the fact that the ESR (equivalent series resistance), the cost, the size, and/or the weight will increase.

$$L_o = \frac{D \cdot (V_{\text{bus}} - V_o)}{f_s \cdot \Delta I}$$

(2)

Capacitance

There are two main capacitors that need to be selected/sized appropriately for proper operation of any Switch Mode Power Supply (SMPS). These two capacitors are $C_o$ or the output capacitor, which will filter the output voltage, and $C_{\text{bulk}}$ or the input filter that is used to help regulate a constant DC bus voltage.
While $L_o$ is used to filter the current, $C_o$ is used to filter the output voltage or to help attenuate the switching ripple and any other harmonics that are superimposed upon the output of the inverter. The superimposed ripple is due to the fact that the inverter uses a frequency much higher than the fundamental frequency of the output. To properly determine the size of the output capacitor the output inductance ($L_o$), the switching frequency ($f_s$) that is being attenuated, the duty cycle ($D$), and the allowable normalized voltage ripple ($V_{rip}$) all must be known and taken into account.

$$C_o = \frac{(1 - D)}{8 \cdot L_o \cdot f_s^2 \cdot V_{rip}} \quad (3)$$

From EQ. 3 the minimum capacitance needed for a specific $V_{rip}$ can be found for varying switching frequencies to minimize component size as well as losses associated with the ESR of the components as well as the MOSFETs. When the switching frequency is varied, $L_o$ and $C_o$ need to be varied to keep a constant output current ripple and voltage ripple.

![Figure 4 $C_o$ vs. $f_s$ for HPWM](image-url)
Figure 5 $C_o$ vs. $f_s$ for Bi-Polar

Figure 4 and Figure 5 shows the capacitance increase for both driving methods going from 20 kHz to 120 kHz which is approximately three times more capacitance needed to keep that constant voltage ripple at the lower switching frequency than the higher switching frequency.

Figure 6 Voltage Ripple for HPWM and Bi-Polar (Constant $C_o$)

The power loss savings, current ripple, and voltage ripple savings for the HPWM does not come at any obvious cost. As can be seen from Figure 6 the voltage ripple for the HPWM
driving scheme is lower than that of the Bi-Polar. This is due to how the voltage is being applied which can be seen through the duty ratios given by EQ. 4 and EQ. 5.

\[ D_{bi} = 0.5 \cdot (1 + \frac{V_o}{V_{bus}}) \]  

(4)

\[ D_{HPWM} = \frac{V_o}{V_{bus}} \]  

(5)

Since the Bi-Polar method has both positive and negative voltage being applied to the output, this causes a higher voltage swing. This higher voltage swing causes the higher voltage ripple that needs to be attenuated.

\[ C_{bulk} \text{ or } C_{in} \]

Since the inverter being design will be tested under a close to purely inductive load, this means that the inverter will receive power as well as generating power or be bi-directional with an average output power of one kilowatt.

![Figure 7 Output Power](image)

**Figure 7 Output Power**

The output power is going to be sine squared which given by a sine property shown in EQ. 6 shows that the 60 Hz output sine wave is turned into a 120 Hz ripple upon the input bus voltage
due to a purely resistive load, if there was an inductive load the ripple would increase and even go negative.

\[(\sin(x))^2 = .5 \cdot (1 - \cos(2 \cdot x)) \quad (6)\]

Since the 120 Hz ripple propagates back to the DC bus voltage there needs to be a bulk capacitor to store the input voltage so that the bus voltage does not drop below the maximum output voltage. To determine the capacitance needed EQ. 7 is used to keep the minimum bus voltage above the maximum output voltage due to the energy stored in the capacitor.

\[C_{\text{bulk}} = \frac{P_o \cdot 2}{120 \cdot \pi \cdot [(V_{\text{max}})^2 - (V_{\text{min}})^2]} \quad (7)\]

In EQ. 7 \(P_o\) is the average output power; \(V_{\text{min}}\) is the minimum acceptable DC bus voltage. To obtain \(V_{\text{max}}\) EQ. 8 is used, where \(V_{\text{want}}\) is the DC bus voltage that is being applied from the isolated DC-to-DC converter.

\[V_{\text{max}} = 2 \cdot V_{\text{want}} - V_{\text{min}} \quad (8)\]

It is a preferable feature of the Two Stage inverter system that the bulk storage capacitance is placed in the middle of the two stages. Compared to the bulk capacitor needed for the Single Stage approach, the capacitor of a Two Stage system allows a higher percentage voltage swing, referenced to its dc value, and thus is able to accommodate a larger amount of power ripple for the same storage density. Another advantage is that the alternating component of the output power is captured within that stage, and is not transmitted through the DC-DC converter stage. In other words, the DC-DC converter stage is responsible for supplying the averaged power, while the peak power stress is confined to the efficient, bi-directional and non-isolated, SPWM inverter stage.
Frequency

From the power loss calculations done earlier it can be seen that for both methods the power loss is dependant on the switching frequency as well as some of the components. So to minimize the losses and component size, components as well as the power loss calculations need to be recalculated with varying switching frequencies.

![Power Loss vs. f_s (HPWM)](image)

**Figure 8 Power Loss vs. f_s (HPWM)**

From Figure 8 with HPWM driving it can be seen that the power loss decreases and the efficiency increases as the frequency decreases. This leads us to believe that the lower the switching frequency the higher the efficiency, however, this is true but this is not all the information. In addition, as seen from Figure 4 the system will need more capacitors to keep the same voltage ripple but has the draw back of increased parts size, cost, and board space.
If the counter argument of lower power loss in the ESR of the capacitor is taken than that is offset by the fact that very little current will travel through the capacitor as compared to that of the inductor. From Figure 9 \(L_0\) must be increase by a large factor to keep the same current ripple. This means that the size and weight of the inductor will be extremely large for smaller switching frequencies but also there will be an increase in the power lost in the inductor due to the increase of the ESR from the increased inductance needed.

For the Bi-Polar driving there is also power loss decrease with the decrease of switching frequency as shown in Figure 10.

---

**Figure 9 Current Ripple vs. \(f_s\) (HPWM)**

**Figure 10 Power Loss vs. \(f_s\) (Bi-Polar)**
From Figure 8 and Figure 10 it can be seen that there is less lost in the HPWM rather than the Bi-Polar. However the component selection must be taken into account and seen if the trade of efficiency for components/size/space is worth the price. So the next thing is to take a look at the components specifically $L_o$.

Like the HPWM the Bi-Polar’s $L_o$ must be increased to keep the same output current ripple at lower frequencies as compared to the high frequencies. So with the lower frequencies both HPWM and Bi-Polar have a small decrease in power loss but this fact is offset by the increase in $L_o$ and $C_o$. To optimize efficiency as well as size, cost, and components selection a switching frequency of 50 kHz has been chosen.

**SPWM Driving Schemes**

There are several methods to create the outputted sine wave from the DC voltage bus. The methods that will be discussed are based on the H-Bridge Inverter topology with sinusoidal pulse width modulation (SPWM) technique. Two particular driving schemes are considered; one method, dubbed bi-polar, as stated earlier, is based on switching all four of the MOSFET’s thus
applying positive and negative bus voltage to the output over the entire sine wave. With the Bi-Polar method, the sine wave is created by varying the duration the positive bus voltage is being applied. Anytime that the positive bus voltage is not being applied the negative bus voltage will be applied to the output, hence the name Bi-Polar.

![Figure 12 MOSFET and Leg Locations](image)

For the second method, the HPWM, which is where only a positive bus voltage and zero volts will be applied to the output for the positive half of the sine wave, and a negative bus voltage and zero volts for the negative half of the sine wave. The way this is achieved is by turning on and off of the MOSFET’s of one leg at the switching frequency. While for the other leg, the low side switch is kept on and the high side switch off (for the positive half of the sine wave). To create the positive half of a sine wave, leg 1 will be the switching leg, while leg 2 will have switch D constantly on, and switch C will be constantly off. Then to create the negative half of the sine wave, leg 1 will still be the switching leg while switch C will turn on and D will turn off.
Both Figure 13 and Figure 14 show the method for switching is only for the positive half of the sine wave. To create the negative half of the sine wave switch D and C exchange switching schemes while switches A and B will do the same for both SPWM driving schemes. The HPWM is very similar to that of the Uni-Polar method with the exception that half of the switches will be switching at twice line frequency as apposed to the switching frequency. With the reduction in switching frequency half the switching loss will be saved. This was observed in [1]; where the HPWM, Uni-Polar, and Bi-Polar switching losses were compared.
While in [2] the HPWM, Bi-Polar, and SPWM EMI (electro-magnetic interference) was examined and compared to each other to determine if there are any adverse effects in the EMI from the HPWM driving method. However, the opposite is true; the EMI was actually reduced with the use of HPWM. The reason that [2] gave for the reduction of the conducted EMI for the HPWM is due the fact that not all the switches are switching at a high frequency, which also is the same reason why the switching loss is reduced.

A modification shown in [3] allows ZVS to be achieved for all the switches by adding an additional switch, capacitor, and inductor. While the added inductance and capacitance are small they do increase the space needed as well as the driving and control circuitry needed for the extra switch. From [3] there will be no switching loss associated with any of the switches due to the ZVS, however; the conduction loss will be increased. The increase in conduction loss will be due to having the extra switch directly in the main power flow path also the resonance to create the ZVS on all the switches will increase the circulating current which in turn will also increase the conduction loss. While switching loss at full load seen from Figure 17 is about 10 W and the conduction loss is 50 W removing the 10 W of switching loss would be beneficial but the conduction loss of the entire system would approximately double due to the insertion of the extra switch, that is why it is not feasible to add the extra circuitry for ZVS operation at this switching frequency. However, if the switching frequency were increased the ZVS operation may become a more feasible option.

Now one other concern came about from HPWM method and that is the difference in the number of times switching as well as the heat sink used in dissipating the heat in each particular switch. [4] and [5] purpose and evaluate modified switching schemes for the HPWM where the
slow and fast switching frequency will be more evenly distributed among the MOSFET. In this way the switching loss and number of times switched will be evenly distributed among the MOSFETs thus increasing the lifetime of the MOSFET as well as sharing the heat evenly among the MOSFETs. Also, with the losses/heat evenly distributed among the MOSFETs there can be one MOSFET and/or heat sink chosen/designated for all the switches. Table 1 shows the advantages and disadvantages of each driving schemes.

Table 1 Switching Scheme Comparison

<table>
<thead>
<tr>
<th>Switching Scheme</th>
<th>EMI</th>
<th>Reliability</th>
<th>Efficiency</th>
<th>Thermal Distribution</th>
<th>Switch Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uni-Polar</td>
<td>Poor</td>
<td>Average</td>
<td>Poor</td>
<td>Average</td>
<td>Average</td>
</tr>
<tr>
<td>Bi-Polar</td>
<td>Poor</td>
<td>Average</td>
<td>Poor</td>
<td>Average</td>
<td>Average</td>
</tr>
<tr>
<td>HPWM</td>
<td>Average/Better</td>
<td>Average</td>
<td>Better</td>
<td>Poor</td>
<td>Hard</td>
</tr>
<tr>
<td>TEHPWM</td>
<td>Average</td>
<td>Best</td>
<td>Average</td>
<td>Average</td>
<td>Average</td>
</tr>
<tr>
<td>Modified HPWM</td>
<td>Average</td>
<td>Average</td>
<td>Best</td>
<td>Poor</td>
<td>Hard</td>
</tr>
</tbody>
</table>

TEHPWM

With the TEHPWM (a.k.a. “Temperature equalization HPWM”) the number of times switching occurs is evenly distributed among all four switches may lead to a reduction of efficiency but evenly distribute the heat. This reduction is due to the fact that if a fast switching MOSFET was chosen for the high switching frequency leg and a low R_{DS(on)} MOSFET was chosen for the slow switching leg a minimum loss could be achieved. That is why the MOSFET
selection for the HPWM in Table 1 is listed as hard and the efficiency is the best. However, if this is done the thermal distribution would be poor as seen in Table 1 because only one side would see the switching losses and since that one side is switching at a high frequency the reliability of the system would be the same if not insignificantly increased.

Also, the TEHPWM EMI should be the same as the HPWM. However, the layout of the TEHPWM is more critical than the layout of HPWM. The reason for this is due to the EMI source, the switching MOSFET, is changing to two different locations with the TEHPWM while the HPWM EMI noise source is in a constant location. The generated EMI for both TEHPWM and HPWM should be the same however the location of the sources varies in the TEHPWM while it is constant in the HPWM. This varying noise source location is why the TEHPWM needs a more sophisticated layout than the HPWM. This is why HPWM was the chosen driving scheme to be compared to that of the Bi-Polar method instead of the TEHPWM being compared to the Bi-Polar.

**Modified HPWM**

The modified HPWM technique can slightly improve efficiency over the HPWM technique by having two changes. The first modification is that there will not be a slow switching leg. Instead the slow switches will be on the high side while the fast switches will be on the low side of both legs. Shown in Figure 12 where switches A and C are slow switched while B and D are fast switched. The second modification is instead of a MOSFET being used for the slow switches an IGBT is used with a fast reverse recovery anti-parallel diode. The reason for this is so that the switching loss due to the shot through caused by the reverse recovery of the MOSFETs body diode will be reduced.
This is because the MOSFETs body diode is intrinsic and can’t be improved without adversely affecting the MOSFET itself. However, if an IGBT replaces the MOSFET an anti-parallel diode can be added. Because the added diode is not an intrinsic diode it can be improved to reduce the reverse recovery without any adverse effects. This also could be done for the slow switching MOSFET but a diode must be added to block the intrinsic body diode of the MOSFET. However, when adding this blocking diode the conduction loss will increase and may be even higher than the power that is saved from adding the diode. Also, the component count and cost will increase as well as the chance of failure.

The modified HPWM technique can save power lost to shot through but at the price of conduction loss for lower power levels. This is because the HPWMs conduction loss is due to MOSFETs over the entire switching period except for the dead time (which is when the body diode will conduct). While the modified HPWMs loss is due to IGBT and a diode for the off time (1-D time) and an IGBT and MOSFET for the on time (D time). Also, with the modified HPWM the high side driving becomes slightly more difficult due to the length of time that the switch must be on. The method that is more suited for this nominal power level is the HPWM technique.

**Power Loss Calculations**

**Switching Loss**

Dead-time intervals are inserted into the switching waveforms to avoid short-circuit conditions during switching. The duration of this dead-time is designed to allow ZVS operation of the switches, whenever enabled by topology operation. For the HPWM, switch A and B can
achieve ZVS during the positive and negative halves of the sine waves, respectively. For Bi-Polar, both B and C can achieve ZVS for the positive half of the sine wave and the other two switches can achieve ZVS for the negative half of the sine wave.

Operating switches at ZVS minimizes their switching losses as well as increases reliability. The reason that ZVS only allows the minimization of switching loss and not completely rids the system of switching losses is the fact that the output current will discharge the body capacitance, and then that same current will start to flow through the body diode. Once the current starts to flow through the body diode, this will cause a voltage drop of approximately 0.7 V. With a 0.7 V drop across the MOSFET, the MOSFET is now technically not at zero volts anymore but rather 0.7 V. Therefore you can only achieve a minimized switching loss or minimized voltage across the MOSFET rather than zero volts across the MOSFET or zero switching loss.

![Figure 15 Switching Voltage](image)

**Figure 15 Switching Voltage**

Figure 15 shows the switching voltage; the switching current looks approximately the same however with a time shift and the maximum current is constantly changing from switching period to another. Power loss due to switching is given by EQ. 9.
\[
P_{\text{switch}} = \frac{V_{\text{in}} \cdot f_s \cdot (T_{\text{on}} + T_{\text{off}}) \cdot I_o}{6}
\]  

(Since EQ. 9 gives the instantaneous power and the current changes from switching period to switching period. EQ. 9 needs to be modified to find the average power loss due to switching over the entire cycle (or half of the sine wave period), which is given by EQ. 10. The reason that switching loss is only found over the positive half of the sine wave and not the entire sine wave is due to the fact that the switching loss repeats every half sine wave period (i.e. the power loss in the positive half is the same as the negative half.).

\[
P_{\text{switch}} = \frac{V_{\text{in}} \cdot f_s \cdot (T_{\text{on}} + T_{\text{off}})}{6 \cdot \pi} \cdot \int_0^\pi I_o(\omega) \cdot d\omega
\]  

\[
P_{\text{avg}} = \frac{V_{\text{in}} \cdot f_s \cdot (T_{\text{on}} + T_{\text{off}}) \cdot V_o \cdot \sqrt{2}}{3 \cdot \pi \cdot R_{\text{load}}}
\]  

EQ. 10 can be further simplified to EQ. 11 where \( V_o \) is the rms output voltage, \( R_{\text{load}} \) is the load resistance, \( V_{\text{in}} \) is the bus voltage (input voltage to the inverter not system), \( f_s \) is the switching frequency, and \( T_{\text{on}} \) and \( T_{\text{off}} \) are the rise and fall time before the MOSFETs are completely on or off. This is the switching power loss for each individual switch that is not switching at ZVS.

So to calculate the switching loss for the entire system the singular switching power loss needs to be multiplied by the number of switches that are not switching at ZVS over the half sine wave period.
Figure 16 Current Flow Positive Half of Sine Wave

For the Bi-Polar method, all the switches are used to create the sine wave. As can be seen from Figure 16 switches B and C will have current flowing through the body diode of the MOSFETs during the dead time of the positive half of the sine wave enabling those two MOSFETs to achieve ZVS. So switches A and D will be hard switched, during the positive half of the sine wave and for the negative half switches B and C will be hard switched. Therefore, Bi-Polar will always have two switches that are being hard switched so the switching power loss is two times \( P_{avg} \) from EQ. 11.

For the HPWM method, one of the low side switches will be constantly on so no switching loss will be associated with it. While one of the high side switches will be constantly off, as a result no switching loss will be associated with that one either. The HPWM compared to the Bi-Polar so far has the same amount of switches that do not have switching lost associated with them. Once the dead time current flow is taken into consideration it can be seen that the low side switch that is switching at the switching frequency not twice the line frequency does indeed switch at ZVS. Which means 1 out of the 4 switches for the HPWM will not have ZVS and 2 out of the 4 switches for the Bi-Polar will not have ZVS. This means that HPWM not only has half the switching loss compared to the Bi-Polar but also the MOSFETs of the HPWM will have the
same if not insignificantly higher reliability because half of the switches will be switched less often than in the Bi-Polar method.

**Conduction Loss**

To calculate the conduction loss for both methods, the current path first must be analyzed. Since, the positive half of the sine wave switching scheme is the same as the negative half the current only needs to be analyzed for that portion. The current path for the Bi-Polar has switches A and D on so $I_o$ will flow through them; this is also the power delivering time. Then an optimal dead time will occur so that ZVS occurs across switches B and C so that $I_o$ will flow through the body diode for the dead time period. The reason an optimal dead time is chosen is so that enough time for safety can be taken into consideration while not too much time is spent with the current flowing through the less efficient body diode, before the MOSFET is turned on. Once that has happened switches B and C will turn on and $I_o$ will flow through them or the equalization period. So, EQ. 12 gives the equation for the conduction loss in the Bi-Polar method.

$$
\begin{align*}
P_{\text{con}}(\omega) &= \left( (R_H + R_L) \cdot I_o(\omega)^2 \cdot D(\omega) + (R_L + R_H) \cdot I_o(\omega)^2 \cdot (1 - D(\omega) - 2 \cdot D_{dt}) \\
&+ 4 \cdot V_d \cdot I_o(\omega) \cdot D_{dt} \right) \\
&= (R_H + R_L) \cdot I_o(\omega)^2 \cdot D(\omega) + (R_L + R_H) \cdot I_o(\omega)^2 \cdot (1 - D(\omega) - 2 \cdot D_{dt}) \\
&+ 4 \cdot V_d \cdot I_o(\omega) \cdot D_{dt}
\end{align*}
$$

The current will flow in the HPWM method almost in the same manner as in the Bi-Polar method except for the dead time period. Instead of $I_o$ flowing through two MOSFET body diodes, $I_o$ will flow through one low side’s MOSFET body diode and the other low side on resistance. This enables the designer to not be as strict in designing the optimal dead time and still achieve the same if not better conduction loss depending on EQ. 15. Also, the Equalization
period of the Bi-Polar method is the same as the free wheeling period of the HPWM method except that instead of a high and low side MOSFET being on, the two low side MOSFETs will be on. So, EQ. 13 gives the equation for the conduction loss of the HPWM method.

\[
P_{\text{con}}(\omega) = \left( R_H + R_L \right) I_o(\omega)^2 \cdot D(\omega) + 2 \cdot R_L \cdot I_o(\omega)^2 \cdot (1 - D(\omega) - 2 \cdot D_{dt}) + (V_d \cdot I_o(\omega) + R_L \cdot (I_o(\omega))^2) \cdot 2 \cdot D_{dt}
\]

In EQ. 12 and EQ. 13 \( R_H \) and \( R_L \) are the high and low side \( R_{ds(\text{on})} \) resistance, \( D \) is the varying duty cycle, \( D_{dt} \) is the fixed dead time for ZVS and safety issues, \( V_d \) is the voltage drop across the MOSFET body diode, and \( I_o \) is the varying output current. To find the average conduction loss the instantaneous conduction loss must be integrated over half a sine wave period or from zero to \( \pi \), and then the integration over that period must be divided by \( \pi \) as shown in EQ. 14. The reason for the integration is the same as for finding the average switching loss from EQ. 10 but the switching loss could be easily simplified whereas the conduction loss has many parameters that are dependant on omega.

\[
P_{\text{avg}} = \frac{1}{\pi} \int_0^\pi P_{\text{con}}(\omega) \cdot d\omega
\]

As can be seen from EQ. 12 and EQ. 13 there is a slight difference in the conduction losses, which occurs during the dead time. The difference is that Bi-Polar has \( I_o \) flowing through two body diodes while HPWM has \( I_o \) flowing through only one body diode and one MOSFETs on-state resistance. This difference allows HPWM to have a lower conduction loss for this specific application; however the amount of power that is reduced by the HPWM method is negligible.

\[
X = V_d - R_{ds} \cdot I_o
\]
Each application will have differences on how much conduction loss is saved or lost from using the Bi-Polar or HPWM method. For ease refer to EQ. 15 and if X is positive then Bi-Polar will have less conduction loss and if X is negative then HPWM will have less loss associated with it. However, as stated previously, the amount of power saved or lost is negligible for most applications based purely on conduction loss. In addition, the amount of saving in conduction is not that significant due to the fact that the Bi-Polar method has twice the switching loss compared to that of the HPWM method.

**Driving Loss**

Driving loss is attributed to basically turning on and off the MOSFET. The way this happens is by applying a charge across $V_{gs}$. To apply and take away this charge takes some power therefore a loss in efficiency. However, the amount of loss associated with the driving loss is very small but it is constant across the entire power range. This constant power loss is insignificant during the high power operation but during low power draw, this small constant power loss becomes one of the key factors for low efficiency. EQ. 16 gives the power lost that is associated with driving loss.

$$P_{Driving} = \frac{1}{2} \cdot C_{eff} \cdot f_s \cdot V_{gs}^2$$

(16)

From EQ. 16 the driving loss main component for power loss is the switching frequency because the effective capacitance is relatively small. Therefore, if there is a way to bring down the switching frequency the loss can be also be reduced. As stated earlier for the Bi-Polar method all four switches are being switched at the switching frequency, but for the HPWM method, two of the four switches are being switched at the switching frequency and the other two are being
switched at twice line frequency. Therefore, the HPWM has lower overall switching frequency. This means that the driving loss has also been lowered for the HPWM compared to that of the Bi-Polar method.

<table>
<thead>
<tr>
<th></th>
<th>HPWM</th>
<th>Bi-Polar</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>835</td>
<td>835</td>
</tr>
<tr>
<td>B</td>
<td>835</td>
<td>835</td>
</tr>
<tr>
<td>C</td>
<td>2</td>
<td>835</td>
</tr>
<tr>
<td>D</td>
<td>2</td>
<td>835</td>
</tr>
</tbody>
</table>

Table 2 shows the amount of time each MOSFET has been switched over a single line period. The overall effective switching frequency for the Bi-Polar is 50 kHz while the HPWM has an effective switching frequency of approximately 25 kHz. This lowered effective switching frequency reduces the driving loss by half. Also with the switching frequency being lowered for some of the HPWM MOSFETs their lifetime has been extended thus making the HPWM more reliable and more efficient, but the increase in reliability is insignificant.

Overall Efficiency

The overall second stage inverters efficiency was measured; excluding auxiliary power supplies that were required to power up the DSP that was used to create the SPWM and the power used for driving the MOSFET. Also since the closed loop was not being tested the sensors where not powered up. Driving and control power losses will all be considered separately when
considering the over-all system efficiency. Using the equations above and other loss equations were added to achieve a more accurate model to estimate the system efficiency. The loss equation that was added was the resistance of the wire used to create the inductor (ESR of the inductor).

![Efficiency curve and Power loss](image)

**Figure 17 Theoretical Efficiency and Power Loss (using HPWM w/ f_s=50 kHz)**

From Figure 17, the major areas that power is lost can be seen. Such as for low power level the major power loss component is the MOSFET switching loss. While in the higher power levels the key power loss is due to the MOSFETs conduction loss. Figure 17 can be utilized to increase peak efficiency, choose best operating frequency, and flatten out the efficiency curve so that a constant efficiency can be achieved across the higher power levels. However, Figure 17 does not match the actual efficiency curve (Figure 18) exactly. This mismatch may be due to the non-idealities of the core loss from the inductors core along with other non-idealities that are
unforeseen at this time. The core loss was not taken into consideration at this time due to the intensive math along with the limited understanding of the losses associated with the core such as eddy and core loss.

![Efficiency Curve](image)

**Figure 18 Efficiency Curve (using HPWM w/ \( f_s = 50 \text{ kHz} \))**

The overall efficiency was measured; a major problem occurred trying to achieve this goal, which was achieving accurate readings. The accuracy problem was fixed by placing an inductor before the input to the inverter (basically an input filter). This inductor enables the input current to be sinusoidal rather than discontinuous allowing the input power to be calculated easier and more actually. In addition, the input inductor reduced the harmonics seen on the input current. As a result, a more accurate value of the input DC current was attainable and no longer needed to calculate the value in the oscilloscope which is bad due to the error of the scope. The
next significant modification to measuring the power came from the understanding of the scope that was being used. What was found out about the scope was that all functions on it were calculated graphically. That means that if the scope was extremely zoomed in, out, or parts of the plot were off the screen, then the voltage and current readings became inaccurate, thus the power readings became inaccurate.

**Experimental Results**

A 1 kW prototype was built for experimental testing. The prototype was successfully tested at above the rated power level as can be seen in Figure 19. The 60 Hz output sine wave has near unity power factor that also can be seen by Figure 19. The prototype was also successfully tested and passed for Bi-directional capability seen by Figure 20. The Bi-directional test was a purely inductive load that also can be seen by the 90-degree phase shift between the output current and voltage (waveforms 1 and 2 respectively in figure).
From Figure 19 the completed prototype experimental results can be seen. Also, the efficiency can be determined at full load which is 96.7% efficient. Also, the output current and voltage waveforms are near unity power factor due to being in phase and having basically only the fundamental harmonic in the waveform.
Figure 20 Experimental Results Purely Inductive Load

Output Current “yellow”

Output Voltage “red”

Input Voltage “blue”

Input Current “green”
From Figure 21 the achievement of soft switching on one of the four switches is seen. This achievement is seen by the voltage across the drain to source of the MOSFET goes to zero before the switch is turned on. This achievement of soft switching, as stated earlier, lowers the switching loss, increases efficiency, lowers the needed heat to be dissipated, and increase the reliability of the switch and the system as a whole.
CHAPTER 3: PRIMARY STAGE

Introduction

The primary stage (or first stage) in the Two Stage approach is to take the varying input voltage and convert that to a constant DC bus voltage, through a transformer for galvanic isolation which provides safety and the ability to create an additional voltage gain. The purpose of this constant DC bus is to enable the second stage to be more easily designed and optimized. If this constant DC bus was not created the second stage design complexity will increase which could lower efficiency of the second stage as well as increase component count and cost.

However, the varying input makes the primary stage harder to design/optimize, because the worst case scenario must always be taken into account (or hardest design parameters must be satisfied). The varying input increases the design complexity because the gain needed from the transformer to create the appropriate output voltage must be determined at the lower input voltage so that the DC bus voltage is achievable across the entire input range. The reason the concern is mainly on the transformer is due to the fact that the converter’s gain is there only to tweak the final overall gain of the system. The converters gain should not be meant to be the gain of the system due to the increased stresses and also the smaller the operating range the duty cycle would have to be.

Once this gain from the transformer is found for the lower input voltage it is constant regardless of the input voltage. So when the higher input voltage is applied to the transformer the output rectifying diodes of the transformer will have a higher voltage stress than the DC bus voltage. This higher voltage stress that the diodes will be blocking is due to the gain of the
transformer which multiples the peak input voltage. So, if the highest input voltage is twice the lowest input voltage the voltage stress that the rectifying diodes will have when the highest input voltage is applied will be at least twice that of the DC bus voltage. Also, any non-idealities such as leakage inductance of the transformer will have some adverse effect on the whole output range but the effects are sometimes greater at the lower input voltage so the design must take that into account. Which usually means the turn’s ratio must be increased to achieve the desired output gain.

**Topology Selection**

**Secondary Stage Topology**

As in all designs, topology selection is a key issue for increased efficiency and reliability as well as decreased cost and component count. With the secondary stage a buck or buck-boost topology is needed and because of the zero crossings that are required to make the sine wave which means that a boost topology can not be used. The bi-direction capability and 120 Hz ripple attenuation is achieved on the secondary stage through the input bulk capacitance by the energy that the capacitor stores.

\[ E_{cap} = \frac{1}{2} C V^2 \] (17)

From EQ. 17 to increase the amount of energy stored (i.e. increase the bi-directional capability and decrease the 120 Hz ripple) by the capacitor the capacitance or voltage must be increased. From EQ. 17 it can be seen that there is a linear dependence on the capacitance and a non-linear dependence on the voltage. This means that the best way to increase the capability of the capacitor to store energy and to keep component count and size down is to increase the bus
voltage. This in turn means that a buck topology is the better topology to choose for the second stage based purely on the increased energy storage and decreased 120 Hz ripple. The Buck-Boost would not be as well suited as the Buck topology because the duty cycle for the Buck-Boost topology would have to be limited to values below a half, for the Buck-Boost topology to have the same amount of energy storage that the Buck has.

Whereas the Buck topology can contain all the possible duty cycle values, this means that the Buck topology would have a wider duty cycle range. This wider duty cycle range helps with the MOSFETs current stress by allowing the energy a longer time window to flow through. Assuming that the DC bus voltage is the same in both Buck and Buck-Boost to achieve the same 120 Hz ripple attenuation. The current stress would have to be higher in the Buck-Boost than that of the Buck because the energy flowing in both is the same however the Buck-Boost MOSFETs conduction time will be shorter than that of the Bucks.

\[ E = P \cdot dt \Rightarrow E = V \cdot I \cdot dt \] (18)

Looking at EQ. 18 the voltage and energy that is being transferred in both buck and buck-boost is the same so the current stress difference between the two is proportion to the amount of time difference that the two topologies are conducting. The longer the one topology is conducting than the other the lower the current stress of that topology. Since the maximum time that the buck-boost is on is only half that of the buck that means the buck will have a lower current stress than that of the buck-boost. That is why the Buck topology is chosen for the second stage.
Primary Stage Topology

Now for the primary stage a topology must be chosen buck, boost, or buck-boost. Comparing the voltage stresses on the secondary side of the transformer a boost type topology is desirable, this is due to the fact that most of the voltage gain that is needed is achieved through the converter itself rather than the transformer unlike the buck derived topologies. When the low input voltage is applied to the input of the primary stage a gain of approximately seven times is needed to yield the correct output voltage. Now if a buck topology is used the only way to achieve this gain is through a transformer with at least that much or higher number of a turns ratio. However, as stated earlier when the high input voltage is applied that means a much higher output voltage stress will be applied to the rectifying diodes due to that constant voltage gain of the turn’s ratio.

Now with a boost type topology the voltage gain that is required can be achieved through the circuit itself and a little through the turns ratio to lower the needed duty cycle which will enable a lower voltage stress and keep a more constant voltage stress on the rectifying diodes as compared to the buck derived topology. So the diodes don’t have to be overrated based only on the highest input voltage rather the voltage stress would be more uniform across the diodes, thus the diode will not be overrated most of the time. A buck-boost derived topology can lower the voltage gain needed from the transformer compared to that of the buck, however, depending on the design the voltage stress on the diode still could be larger than that of the boost type topology. Also, as stated earlier the Buck topology will have the worst case of the voltage stress on the diodes.
The next analysis that is done is the primary sides’ voltage stress; here it will be helpful if there are some assumptions made. The assumptions are that over a single switching cycle the energy storage devices (i.e. capacitor and inductor) are large enough that they can be considered as sources. This means that a capacitor can be replaced by a voltage source in the circuit while an inductor is replaced by a current source. The first topology that is examined is the boost. The boost topology transforms the input from a voltage source to a current source when the above assumption is applied.

This change of the input source type affects the voltage stress due to the non-idealities of the transformer that the input is feed into also seen in Figure 22. The affects of the non-idealities of the transformer for the voltage stress will be analyzed from the leakage inductance point of view. This leakage inductance causes a much higher voltage stress because the current through the leakage inductance must change quickly due to the input being a current source now. This high change in current causes a high voltage stress across the primary side MOSFET’s because the voltage seen across an inductor is proportional to the rate of change of the current.

The buck topology is the same as the boost topology but in the other direction, so the input of a boost would be the output of a buck. That means that the problem of the input current

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Figure 22 Boost Topology w and w/o Assumption

The buck topology is the same as the boost topology but in the other direction, so the input of a boost would be the output of a buck. That means that the problem of the input current
source of the boost on the primary side is no longer there. However, one might think that the problem that was on the primary side of the transformer will be transferred to the secondary side. This is true, however, if the rectification of the second side of the transformer was correctly chosen i.e. a full wave rectification. The transformer’s current could slowly ramp up to the output sources current which would keep the voltage stresses low. Also, diodes are a bit more resilient than MOSFETs are when it comes to voltage stress and diodes can be selected to have a much higher breakdown voltage than a MOSFET for a much cheaper price. So for the buck the main voltage stress concern is due to amplification of the highest input voltage through the turn’s ratio calculated for the lowest input voltage.

Next is the buck-boost topology to be analyzed. The buck–boost topology unlike the buck or the boost can have the input and output both be modeled as voltage sources or current sources or a combination of the two. This means the voltage stress that comes from the non-idealities of the transformer is no longer as much of a concern when the input and output both are modeled as voltage sources. Also the buck-boost allows the turn’s ratio of the converter to be optimized at the center of the input voltage range rather than at one of the end points which what must be done with the buck and boost topologies. This optimization at the center input voltage range allows for a more optimized converter because the converter will be operated in the center of the input voltage range most of the time allowing the converter to be running in the most optimized point the longest.

**Converter**

There are several buck-boost type converters such as SEPIC, Zeta, and Cuk to name a few. The converter being used is seen in Figure 23 and will be a combination of an active clamp
with voltage doubler as the rectifier. The voltage doubler rectifier will enable another form of
gain like the transformer, this gain will be only twice the voltage applied, however, this gain
further reduces the needed turn’s ratio. Therefore, now the turn ratio that is needed will be
approximately three instead of the seven times that is needed for the buck type. Also there are a
couple of key features of this converter, the first is that the non-idealities of the transformer are
utilized, it enters both first and third quadrants of the BH curve of the transformer, the primary
sides MOSFET’s can be switched at ZVS, if the secondary side diodes are replaced by
MOSFET’s they to can be switched at ZVS and can allow the converter to be bi-directional, and
lastly the converter is self power limiting.

![Figure 23 Active Clamp w/ Voltage Doubler](image)

**Figure 23 Active Clamp w/ Voltage Doubler**

**Modes of Operation**

There are two basic modes, however the two basic modes repeat in one period to yield
four main modes of operation for the active clamp voltage doubler. The first two modes switch 1
will be on and the last two modes the high sides’ switch, switch S₂ will be on.
Mode 1

During this mode switch S₁ is just turned on under ZVS conditions and diode D₁ is on. The diode D₁ is on during this mode because the series inductor still has some energy stored in it from the previous mode and the current will continue to flow in the negative direction until the inductor is fully discharged.

![Figure 24 Mode 1](image)

The current directions in the primary and secondary are shown as the thick black arrows in Figure 24. The positive reference for the voltage across the capacitors and the current directions through the series inductance is also shown and will be kept the same for all modes below.

\[
\begin{align*}
-V_c + V_{in} \cdot N + V_{c1} &= 0 \\
-i_L(t) &= \frac{V_{in} \cdot N + V_{c1}}{L} \cdot t + i_L(0^-) \quad 0 \leq t < t_i
\end{align*}
\]

(19)

During this mode the amplitude of the inductor current is being decreased so that the current will begin to flow in the positive direction. The duration of this mode is only a fraction of the fully on time of the switch S₁. This mode will end when the current in the inductor discharges down to
zero, knowing that the time that this mode last can be calculated from EQ. 19 by setting \( i_L(t) \) to zero. The amount of time that this mode actually lasts is given in EQ. 20.

\[
0 = \frac{V_{in} \cdot N + V_{c1}}{L} \cdot t_1 + i_L(0^-) \Rightarrow \\
\Delta t_1 = t_1 = -\frac{i_L(0^-) \cdot L}{V_{in} \cdot N + V_{c1}}
\]  

(20)

Mode 2

During this mode the switch \( S_1 \) is still on however the current in the series inductance has changed directions from the previous mode so now the diode \( D_2 \) is now conducting as shown in Figure 25.

![Figure 25 Mode 2](image-url)
This mode ends with switch $S_1$ turning off and then switch $S_2$ turning on. The end of this mode is somewhat similar to the end of mode four except the current directions are reversed. The end of this mode is the peak positive current that the series inductor will be, given by Eq. 22.

\[
i_L(D \cdot T_s) = i_L^+ = \frac{V_{in} \cdot N - V_{c2}}{L} \cdot (D \cdot T_s - t_1)
\]  

(22)

Mode 3

This mode begins with the switch $S_1$ turning off and switch $S_2$ turning on with ZVS while the diode $D_2$ is still conducting.
\[ V_c \cdot N + V_{c2} + V_L = 0 \implies i_L(t) = -\frac{(V_c \cdot N + V_{c2})}{L} \cdot (t - D \cdot T_s) + i_L(D \cdot T_s) \quad D \cdot T_s \leq t < t_2 \] \hspace{1cm} (23)

This mode ends when the current on the secondary side goes to zero much like mode 1.

\[ \Delta t_2 = t_2 - D \cdot T_s = \frac{i_L(D \cdot T_s) \cdot L}{V_c \cdot N + V_{c2}} \hspace{1cm} (24) \]

**Mode 4**

Same as mode 2 this mode starts when the current switches direction turning diode D2 off with ZCS and turning the diode D1 on with ZCS as well. This mode will end when the switch S2 is turned off which will be the end of the period and the modes will start over again.

\[ -V_c \cdot N + V_{c2} - V_L = 0 \implies i_L(t) = -\frac{(V_c \cdot N - V_{c1})}{L} \cdot (t - t_2) \quad t_2 \leq t < T_s \] \hspace{1cm} (25)

As stated earlier there are two basic modes of operation. This mode is similar to that of mode 2 such that the end of this mode yields a peak series inductance current. However, this mode
differs from the mode 2 by instead of the peak being a positive value it is a negative value. The peak negative current can be calculated from EQ. 25 and is given by EQ. 26

\[ i_L(T_s) = i_{L*} = -\frac{(V_L \cdot N - V_{cs})}{L} \cdot (T_s - t_2) \]  \hspace{1cm} (26)

The current in the series inductor, secondary side diodes and when the switches are turned on over the entire switching period can be seen in Figure 28.
Figure 28 Current Waveforms
Mathematical Analysis

**Gain**

The gain of the converter can be found by using two of the above four modes. By combining two of the modes together (one with two and three with four) yields EQ. 27 and EQ. 28 either of which can be use to calculate the gain.

\[
\frac{D \cdot T_s}{L} = \frac{\dot{i}_L}{V_{in} \cdot N + V_{c1}} + \frac{\dot{i}_L}{V_{in} \cdot N - V_{c2}}
\]

(27)

\[
\frac{(1-D) \cdot T_s}{L} = \frac{\ddot{i}_L}{N \cdot V_c + V_{c2}} + \frac{\ddot{i}_L}{N \cdot V_c - V_{c1}}
\]

(28)

The only point that the gain of the converter can be calculated without a recursive solution or intensive math computation is with a duty cycle of 50 percent. At this point of a duty cycle of 50 percent allows for several math simplifications such as \(i_L^+\) to equal \(i_L^-\), \(V_c\) to equal \(V_{in}\), and for \(V_{c1}\) to equal \(V_{c2}\) which is also equal to half \(V_o\). From these simplifications and from the knowledge of series inductance current (that \(i_L = 4*I_o\)) a gain equation can be derived for the converter at a duty ratio of 50 percent. Through the simplifications and the knowledge of the series inductance current the voltage gain can by determined by EQ. 29.
\[ V_o = 2 \cdot \sqrt{V_{in}^2 \cdot N^2 - \frac{16 \cdot I_o \cdot V_{in} \cdot N \cdot L_k}{T_s}} \]  

(29)

**Figure 29 Output Power vs. Output Current**

Using EQ. 29 and entering parameters for the turns ratio N, input voltage, series inductance, and switching frequency (N=5, \( V_{in} = 45V \), \( L_k = 10uH \), and \( F_s = 100 \text{ kHz} \)) Figure 29 was created. From Figure 29 it can be seen that the converter is self power limiting and depending on the above listed parameters the peak power and to a lesser extent the location of the peak can be modified.

**Stress Analysis**

As stated for the gain equation the analysis is only valid for the duty cycle of 50 percent. This restriction allows equations to be found providing valuable insight into converter operation
and analysis instead of using recursive solutions to find the answers only and not the equations. The current stress for both the clamping Capacitor C and its switch $S_2$ is given by EQ. 30.

$$I_{s2rms} = I_{crms} = \sqrt{\frac{1}{2} \left( \frac{N^2 \cdot I_L^2}{3} - N \cdot I_L \cdot I_{DC} + I_{DC}^2 \right) + \frac{2 \cdot N \cdot \Delta t \cdot I_L \cdot I_{DC}}{T_s}}$$  (30)

The DC current that is on the primary side of the transformer ($I_{DC}$) is equal to the power that is being transferred to the output divided by the input voltage. The $\Delta t$ in the above and below equations is actually a simplification of the length of times of modes 1 and 3 which are equal due to the duty cycle simplifications which are shown in EQ. 20 and EQ. 24. The rms current rating of the output capacitors $C_1$ and $C_2$ are both approximately 1.3 times that of the output current while the rectifying diodes average current stress is just the output current or one fourth the peak current. Also the current stress of the series inductance on the secondary side and therefore the current stress on the secondary side of the transformer is approximately 2.3 times the output current. The last two current stresses are the primary MOSFET and the transformers primary side current stress is given by EQ. 31 and EQ. 32 respectively.

$$I_{s1rms} = \sqrt{\frac{1}{2} \left( \frac{N^2 \cdot I_L^2}{3} + N \cdot I_L \cdot I_{DC} + I_{DC}^2 \right) - \frac{2 \cdot N \cdot \Delta t \cdot I_L \cdot I_{DC}}{T_s}}$$  (31)

$$I_{prim} = \sqrt{\frac{16 \cdot I_a^2 \cdot N^2}{3} + I_{DC}^2}$$  (32)

While the voltage stress across both MOSFETs is given by the input voltage divided one minus the duty or the same as a boost converter.
Draw Backs

There are a couple key draw backs that this topology has. The main draw back is that this topology has a large DC circulating current on the primary side of the transformer. This large circulating current is a function of the power level and input voltage given by EQ. 33.

\[ I_{\text{circ}} = \frac{P_{\text{over}}}{V_{\text{in}}} \]  

The higher the power level of the converter and/or lower the input voltage is, the higher the circulating current will be on the primary side. This large circulating has several adverse effects on the converter; one is that the converter transformer size will need to be increased to handle the large circulating current. Another is that the converter is not suited to high power similar to that of a flyback or single ended forward. Also, this circulating current will increase conduction losses, but the conduction loss could be lower than the switch loss that the circulating decreases.

Simulation

The active clamp forward voltage doubler has been simulated in both P-Spice as well as in PLECS (which is a simulation package that is used with MatLab’s Simulink). Both simulation software tools agreed with the mathematical analysis.
CHAPTER 4: SINGLE STAGE INVERTER

Introduction

In order for the consumer to achieve maximum profit from their solar array, the array must produce as much usable power as possible. For the solar array to produce as much usable power as possible two main goals must be met. The first goal is that the solar array must produce its maximum power at all times. While the second goal is that the power must be in the required form (60 Hz, 120 V\textsubscript{rms} when grid connected). However, in order to achieve the second goal and not have an adverse effect on the first, power electronics will be utilized.

In order to create as much power for a solar array as possible MPPT (maximum power point tracking) will be used. Also, increasing the efficiency of the overall inverter system that is converting the input power into the required output form will further increase the consumer’s profit margin. That is a reason for the single stage approach. The single stage approach will be able to achieve higher efficiency due to the lower overall seen switching frequency.

However, the name behind the single stage approach is deceiving. This is because one would believe from the name that there is only one converter, however, this is not true. In fact, there is the same number of converters in the single stage as the two stage approach as can be seen from Figure 30.
The reason behind the name is not due to the number of converters but the number of high frequency switching converters. With the one stage approach, one converter is switching at the high switching frequency while the second stage is only switching at twice line frequency or 120 Hz.

The reason for this is because the high switching frequency stage or the first stage will take the constant DC input voltage and create a rectified sine wave output through isolation for safety. While the line switching or Unfolding Stage will then take the rectified sine wave and unfold it into a sine wave thus the name Unfolding Stage. While this approach does not save on component count it will increase efficiency due to the lower overall switching frequency of the system as stated above. From this increase in efficiency there will be lower losses and thus a smaller heatsink requirement. This smaller heatsink requirement yields a smaller converter which in turn yields a high power density, while reducing the weight and cost of the converter.

**Basic Single Stage**

The block diagram for the Basic Single Stage converter is given in Figure 30. The Basic Single Stage is similar in topology to the Two Stage as stated above. One difference between the
Basic Single Stage and the Two Stage design is how both the isolated and non-isolated stages are controlled. The high frequency DC to Rectified AC stage can have the same topology as the Two Stage Isolated DC-DC stage, one difference is the control. Also, the Unfolding Stage can be the same as the Two Stage’s Inverter Stage with a slight modification.

This modification arises from the zero switching loss in the Unfolding Stage. The reason that there is zero switching loss in the Unfolding Stage is because this stage is slow switched and the point at which the device is switched assuming a purely resistive load is at the zero crossings of the outputted sine wave. Furthermore, the switching speed of the Unfolding Stage is at twice the line frequency. This slow switching speed and zero switching loss allows for the modification of the use of IGBTs instead of MOSFETs in the Unfolding Stage, whereas for the Inverter Stage on the Two Stage approach MOSFETs would be the switching device of choice. However, in [8] the Unfolding Stage switching device was MOSFETs not IGBTs (due to the power level) and the paper also shows that the isolation transformer can output a rectified sine wave without saturating the core.

The reason that the Unfolding Stage is allowed to be slow switched is through the control of the DC to Rectified AC Stage. The control of the DC to Rectified AC is that instead of the bus being held constant at some voltage as with the Two Stage approach the bus voltage will vary the same way as a rectified sine wave. Because of this varying voltage on the bus, there can no longer be a bus capacitor only a filter capacitor in the Basic Single Stage. The bus capacitor in the Two Stage method is used as energy storage to attenuate the 120 Hz. ripple as well as handle bi-directional power flow. Since there is no bus capacitor in the Basic Single Stage the 120 Hz. ripple now must be attenuated by the low voltage input capacitors.
Also, because the rectification on the output of the Basic Single Stage isolated stage is done by diodes and in conjugation with the fact that there is no bus capacitor this converter is no longer capable of bi-directional power flow. Several problems arise from the fact that the Basic Single Stage does not have the bus capacitors. As stated earlier the system is no longer bi-directional, the 120 Hz. ripple now must be attenuated by the input capacitors which itself causes some problems, and the entire system has double power peaks which cause the Basic Single Stage converter to be overrated to handle the double power peaks.

The reason for these double power peaks comes from EQ. 6. As can be seen from EQ. 6 the product of the two amplitudes will be halved due to this equation. So, in order to obtain the needed average output power the converters peak power must be twice that of the average power. This means that for the Two Stage approach the Inverter Stage must be overrated to handle the peak power while for the Basic Single Stage the entire system must be overrated to handle this peak power. The other problem with having the 120 Hz. ripple on the low voltage input is that the capacitance that is needed is based off of worst case conditions, however, since the capacitance is on the input the worst case condition is not the same as with the Two Stage method.

The reason for the difference in worst case conditions is that with the Two Stage method the impedance that is since going into the capacitor can be held by the Isolated DC-DC. While the impedance seen by the input capacitors on the Basic Single Stage is from the solar array panels and can not be held constant. This variable impedance increases the needed energy storage, while also the 120 Hz. ripple must be attenuated enough so that it does not interfere with the MPPT algorithm. Since the capacitance is on the low input voltage it will require higher
capacitance just to equal the same amount of energy storage that the Two Stage method has with the bus capacitance not to mention the increased capacitance that is needed for the worst case scenario.

**Proposed Modification for Bi-Directional Power Flow**

In order for a fair comparison to be made between the Single Stage and the Two Stage approaches the Single Stage method must be able to handle bi-directional power flow. In order to achieve this several approaches can be done. Some of the approaches are adding a parallel converter, synchronous rectification, and an active bus conditioner each of which will be expanded upon further. The Single Stage method could be compared to the Two Stage approach, without having bi-directional power flow and just citing that as a disadvantage for the Single Stage method. However, the Single Stage approach then could not have a stand alone mode and must always be connected to the grid or nothing at all. This becomes inconvenient when the utility grid goes down. Because the time that power is needed to be delivered from the inverter no power can be delivered due to utility grid being down.

**Parallel Converter**

One method of obtaining bi-directional power flow is using a parallel converter. The block diagram of the Parallel Converter approach is given in Figure 31. The two parallel primary input stages as seen from Figure 31 are both uni-directional.
However, the direction that each stage processes power is opposition to one another. This opposition allows for the bi-directional power flow. Adding this parallel converter was proposed in [7].

The Parallel Converter method is basically as the name states a converter is added in parallel to the DC to Rectified AC stage. This parallel converter will then process the bi-directional power back to the low voltage input side where it is stored. Once the load requires the bi-directional power then the DC to Rectified AC stage will process that extra power that was stored on the input side. The Parallel Converter method for the Single Stage approach enables this approach to be capable of achieving bi-directional power flow. As with the Basic Single Stage the Parallel Converter has the same low switching frequency Unfolding Stage and the unidirectional DC to Rectified AC stage. However, as stated above with the addition of the paralleled input the Paralleled Converter enables the ability of bi-directional power flow.
Since the paralleled stage only needs to be able to handle the bi-directional power the paralleled stage does not need to be rated for the same power level as the forward power stage. So, for higher power levels there can be multiple forward power stages for only one reverse or bi-directional power handling stage in the Parallel Converter method. The Parallel Converter method for the Single Stage has all the benefits of the Basic Single Stage with the added benefit of the bi-directional power flow. However, the Parallel Converter method for the Single Stage approach still has all the problems that the Basic Single Stage has except for the ability to process reactive (or bi-directional) energy, while also adding an increase in component count, and the reactive energy will double processed through an isolation stage decreasing efficiency.

**Synchronous Rectification**

![Figure 32 Synchronous Rectification](image)

As with the Parallel Converter method the Synchronous Rectification method is used to achieve the bi-directional power flow. As apposed to the Parallel Converter method the Synchronous Rectification achieves the bi-directional power capability through the DC to Rectified AC stage without the introduction of another converter as can be seen by Figure 32. The Synchronous Rectification like the Parallel Converter method has the same drawbacks as the
Basic Single Stage except for the bi-directional power ability. Also, the Synchronous Rectification has two more drawbacks which are that the rectification is now done by MOSFETs and as stated earlier the rectification must be able to handle high voltage stress and will need driving circuitry (so a slightly increased component count over the Basic Single Stage). Another method that can be considered under the Synchronous Rectification method is the Cyclo-Converter Approach described below.

**Cyclo-Converter Approach**

Using a Cyclo-converter a single stage inverter system can be achieved as shown in [6]. However, the Cyclo-converter is more of a stepping stone to the single stage approach. This is due to the high number of switches that are needed to achieve both the sine wave output while being capable of bi-directional power flow. Depending on the switching scheme the rectification stage can be switched at low frequencies. However, this usually involves the body diodes of the switches to conduct which will decrease efficiency. This is due to how poor body diodes of switches are with reverse recovery as well as the voltage drop across the diode itself. As seen from Figure 33 there can be four to six high side switches that all require high side driving. Each high side driven switch will require an increased component count which leads to a decrease in reliability and power density.
In Figure 33 the top Cyclo-converter will have the same amount of semiconductor devices conducting at any given time as compared to if the rectification and unfolding were done in two separate stages such as in Figure 30. Now with the Cyclo-converter as with most single stage approaches the 120 Hz. ripple will be processed from the input of the converter itself, rather than from a DC link bus. This ripple that is propagated from input to output will cause higher stress on all components (meaning that a 1 kW system must actually be rated for 2 kW assuming purely resistive load) rather than just the Inverter Stage as with the Two Stage approach.
Since the ripple is being supplied from the low voltage input side to achieve the same energy storage as with the two stage approach the input capacitance must be larger. However, unlike the two stage approach the energy stored by the input capacitor must be larger than that of the two stage approach. The reason for this increase is because ripple on the input will hinder MPPT of the solar array, the capacitors must be sized for worst case scenario (due to the impedance fluctuating unlike two stage approach which is able to keep the impedance constant), and the capacitance must be sized for the lowest input voltage but rated to handle the highest input voltage.

**Active Bus Conditioner**

The Active Bus Conditioner method was proposed in [9] then modeled in [10] for the Two Stage approach with multiple Inverter Stages for multiple loads. In [9] and [10] the Active Bus Conditioner was shown to attenuate the 120 Hz. ripple, which is what is needed for the Single Stage approach. The Active Bus Conditioner is similar in layout to the Parallel Converter; however, instead of the parallel converter being tied to the input it is floating at a higher voltage as seen by its block diagram in Figure 34.
The circuit of the energy storage network is given in Figure 35. The capacitor $C_{\text{bulk}}$ in the Energy Storage Network is used to replace the loss of the bus capacitor of the Two Stage approach. Since the Energy Storage Network is a synchronous boost off of the rectified bus line this network is capable of handling the reactive (or bi-directional) energy as well as the 120 Hz. ripple.

Due to the fact that the Energy Storage Network is a synchronous boost off of the line then the energy being stored in $C_{\text{bulk}}$ will have to be at a higher voltage than what is across the
This means that less capacitance is needed to store the same amount of energy as the Two Stage approach due to the energy being stored at a higher voltage. As stated above if the Energy Storage Network is carefully controlled it can attenuate the 120 Hz. ripple. Therefore the input capacitors no longer have to be oversized as much as with the other Single Stage approaches.

The amount of attenuation that the Energy Storage Network achieves on the 120 Hz. ripple means that the network must be sized to handle that increase in power flow along with the bi-directional power flow. Consequently the reduction of the input capacitor increases the size of the Energy Storage Network.

**Table 3 Comparison between Single Stage Approaches**

<table>
<thead>
<tr>
<th>Component</th>
<th>Count</th>
<th>Bi-Directional</th>
<th>120 Hz. Ripple</th>
<th>Input Capacitor</th>
<th>Control Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Single Stage</td>
<td>Lowest</td>
<td>No</td>
<td>Input</td>
<td>Oversized</td>
<td>Lowest</td>
</tr>
<tr>
<td>Parallel Converter</td>
<td>Highest</td>
<td>Yes</td>
<td>Input</td>
<td>Oversized</td>
<td>Medium</td>
</tr>
<tr>
<td>Synchronous Rectification</td>
<td>Medium</td>
<td>Yes</td>
<td>Input</td>
<td>Oversized</td>
<td>Medium</td>
</tr>
<tr>
<td>Active Bus Conditioner</td>
<td>Medium</td>
<td>Yes</td>
<td>High Voltage</td>
<td>Correctly Sized</td>
<td>Highest</td>
</tr>
</tbody>
</table>

As stated above there are trade offs to each of the proposed approaches to achieve the Single Stage methods, such as with the Basic Single Stage having no bi-directional capability.

Table 3 shows at a glance some of the benefits and disadvantages of the discussed Single Stage methods. From the comparison the Basic Single Stage does not have the capability for reactive energy and therefore should not be used as a comparison against the Two Stage
approach. Between the proposed bi-directional power approaches the Parallel Converter has the highest component count and thus not be the best choice for the comparison. While the Synchronous Rectification still has the 120 Hz. ripple and bi-directional power being stored on the low voltage input side as compared to the Active Bus Conditioner which does not. Also the Synchronous Rectification method must have MOSFETs instead the rugged diodes used for the rectification of the isolation transformer. From the comparison of the different Single Stage approaches the Active Bus Conditioner is the best method of choice for a comparison against the Two Stage approach.
CHAPTER 5: CONCLUSION

There are advantages and disadvantages to both the Single Stage and Two Stage approach for grid-tie inverters. Some of the advantages and disadvantages between the two approaches can and will change dependant on the design parameters. So if one design parameter changes the advantages and disadvantages for that approach may also change. The Single and Two Stage approaches each have their own merit. All of the Single Stages methods have been compared to one other to determine the best overall Single Stage approach to be compared to the Two Stage approach (using HPWM and to a lesser degree modified HPWM). There are several key issues when comparing different converters. Some of these key issues are cost, size, reliability, component count, stresses, and efficiency.

Table 4 Comparison between Two Stage and Active Bus Conditioner

<table>
<thead>
<tr>
<th></th>
<th>Bi-Directional</th>
<th>Component Count</th>
<th>Efficiency</th>
<th>Reactive energy and 120 Hz. ripple</th>
<th>Output Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two Stage</td>
<td>Yes</td>
<td>Depends on power level</td>
<td>Higher @ low to medium power levels and densities</td>
<td>Not double processed</td>
<td>Less rugged</td>
</tr>
<tr>
<td>Active Bus Conditioner</td>
<td>Yes</td>
<td>Depends on power level</td>
<td>Higher @ high power levels and densities</td>
<td>Stored at high voltage</td>
<td>More rugged</td>
</tr>
</tbody>
</table>

Table 4 shows a quick overview between the Active Bus Conditioner for the Single Stage and the Two Stage approach. With both approaches bi-directional capability is achieved,
however, to achieve this capability the Single Stage adds a parallel synchronous boost converter off of the rectified bus. This added converter increases component count but since the energy will now be stored at 600 V instead of at 200 V for the Two Stage the capacitance needed can be reduced by a factor of nine for the Active Bus Conditioner method. Thus less capacitors will be required to handle the bi-directional power. Also, the Active Bus Conditioner can reduce the capacitance needed on the input by attenuating some of the 120 Hz. ripple, also lowering the amount of capacitors needed on the input. The reason that only some of the the 120 Hz. ripple will be attenuated is because if all is attenuated this approach becomes the Two Stage method with the sine wave being generated by the Energy Storage Network. So by increasing the component count by the introduction of the Energy Storage Network there can be an overall decrease in size of the converter due to the reduction of the needed capacitance.

Increasing the power level will need an increase in the number of paralleled stages to be able to handle/distribute the stress to a tolerable level. For the increased power levels the Two Stage approach needs to parallel the entire system while the Active Bus Conditioner only needs to parallel the DC to Rectified AC converter up to a point. Assuming that the Energy Storage Network is only used to handle the bi-directional power flow and not attenuate the 120 Hz. ripple. The reason that the isolated stage is only needed to be paralleled to achieve higher power levels is because IGBT (which can handle higher current for the same package size as a MOSFET) can be used for the Unfold Stage.

Since the Energy Storage Network is only handling the bi-directional power which will not increase that much with increase in power level. The power level for the Energy Storage Network will stay relatively constant, thus, not needing to be paralleled for higher power levels.
However, another issue arises which is power density. As implied above the power density of the Active Bus Conditioner method will be higher than that of the Two Stage approach at higher power levels due to the fact that the Unfolding Stage and the Energy Storage Network not needing to be paralleled to handle the increased power level.

As for the efficiency the Active Bus Conditioner will have the bi-directional and 120 Hz. ripple double processed. This double processing will decrease the efficiency but this loss can be offset in the Unfolding Stage by using MOSFETs instead of IGBTs only for lower power levels though (the reason for this will be explained later). Additional the Inverter Stage for the Two Stage approach uses MOSFETs as apposed to the IGBTs that are used for the Unfolding Stage in the Active Bus Conditioner method. This difference in active devices allows the Two Stage approach to have a higher overall efficiency compared to the Active Bus Conditioner at low to medium power levels (taking the offset by using MOSFETs for the lower power levels) even though there is more switching loss in the Two Stage approach.

The reason MOSFET is a better choice at lower power than that of an IGBT is due to the low current being processed which is similar to one of the reasons for synchronous switching in VRMs (voltage regulated modules). However, the conduction loss in a MOSFET is exponential as opposed to linear conduction loss in IGBTs. So higher power levels means more conduction losses in MOSFETs than IGBTs. Also, the $R_{ds(on)}$ of a MOSFET increase with junction temperature while the IGBTs $V_{ce(sat)}$ decrease with higher junction temperature. This means the more the power processed the less conduction loss the IGBTs will produce as apposed to the MOSFETs. To offset the increased conduction losses parallel stages or parallel MOSFETs can be added; however, this will decrease the power density and increase cost. So, with higher power
levels and power densities the Active Bus Conditioner will begin to have better efficiency than that of the Two Stage approach.

Therefore, at higher power levels and power densities the Active Bus Conditioner for the Single Stage method will have a lower cost, high power density, higher efficiency, and a more rugged output stage (due to the Safe Operating Area of IGBTs) but more complex control. While the Two Stage approach will have a lower cost, better efficiency, and higher power density (due to the high input capacitance needed and Energy Storage Network for the Active Bus Conditioner method) at low to medium power levels and densities.
APPENDIX A: RIPPLE DIFFERENCE PLOTS MATLAB CODE
%ripple difference of HPWM & Bi-Polar

clear            %clearing memory
clc              %clearing the screen

%circuit specs
T=10e-6;         %switching period
L=500e-6;        %output inductor
Cap=5e-6;        %this is with the output voltage ripple of 0.5% (normalized)
Vbus=200;        %input bus voltage used to create output voltage

%sweeping through output voltage
Vo=0:.1:120*sqrt(2);

%calculations for current and voltage ripple
D=Vo/Vbus;       %determining duty cycle for HPWM
D1=.5+.5*Vo/Vbus; %determining duty cycle for Bi-Polar
DelI=(D*T.*(Vbus-Vo))/L;    %determining current ripple for HPWM
DelI1=(D1*T.*(Vbus-Vo))/L;  %determining current ripple for Bi-Polar
Vrip=((1-D).*D*(T^2)*Vbus)/(8*L*Cap);   %determining voltage ripple for HPWM
Vrip1=((1-D1).*D1*(T^2)*Vbus)/(4*L*Cap); %determining voltage ripple for Bi-Polar

%plotting current ripple
plot(Vo,DelI,'k',Vo,DelI1,'r'),xlabel('output voltage'),ylabel('current ripple'),title('Bi-Polar vs. HPWM driving');
legend('HPWM','Bi-Polar');

%plotting voltage ripple
figure;plot(Vo,Vrip,'k',Vo,Vrip1,'r'),xlabel('output voltage'),ylabel('voltage ripple'),title('Bi-Polar vs. HPWM driving');
legend('HPWM','Bi-Polar');
APPENDIX B: HPWM ANALYSIS MATLAB CODE
%Losses for HPWM

clear all
close all
clc

% circuit parameters
Vbus=200;       %input/bus voltage that is being bucked down and inverter to sine
Vo=120;         %output voltage in rms for the outputted sine wave
Rload=14.4;     %the load resistance (full power for 1Kw is 14.4 ohms)
Vrip=.005;      %this is with the output voltage ripple of 0.5% (normalized)
Irip=1.4;       %this is with a output current ripple of 1.4 A (not-normalized or put in terms of percentage)

%USED FOR CONDUCTION LOSSES
Rh=59e-3;       %Rds on resistance of high side the MOSFET being used
RL=Rh;          %Rds on resistance of low side the MOSFET being used
Tdelay=100e-9;  %dealy or dead time between high and low side switching on (for safety)
Vd=1;           %the MOSFETs body diode forward voltage drop

%USED FOR SWITCHING LOSSES
Trans=10e-9;    %the rise and fall time of the MOSFETs (i.e. the time between the MOSFET being fully on or off)

%USED FOR DRIVING LOSSES
Vg=10;          %the MOSFETs gate drive voltage
Qg=247e-9;      %the MOSFETs gate charge

% define radian vector
w=0:pi/10000:pi;
% sweep frequency
f=20e3:.1e3:120e3;

%initializing the conduction, switching, and driving losses
P_cond=zeros(1,length(f));
P_switch=zeros(1,length(f));
P_drive=zeros(1,length(f));

for i=1:length(f)

    Per=1/f(i);                     %determining the switching period
    Ddt=Tdelay*f(i);                %determining the dead time with
    respect to duty cycle
    D=Vo*sqrt(2)*sin(w)/Vbus;      %determining the duty cycle for
    the different radians

    %calculating the output components such as output capacitance and inductance
    L(i)=sum(D*Per.*(Vbus-Vo*sqrt(2)*sin(w))/Irip)/length(w);
    Cap(i)=sum((1-D)/(8*L(i)*(f(i))^2*Vrip))/length(w);

    % peak to peak inductor ripple current
    delI=D/f(i).*(Vbus-Vo*sqrt(2)*sin(w))/250e-6;
    delII=D/f(i).*(Vbus-Vo*sqrt(2)*sin(w))/L(i);
    current_ripple(i)=sum(delI)/length(w);

    % rms values for currents:
Ic = delI/(2*sqrt(3)); % switching frequency component
Icl = delIl/(2*sqrt(3)); % switching frequency component

Io = Vo*sqrt(2)*sin(w)/Rload; % line frequency component
IL = sqrt(Io.^2+Ic.^2); % total rms current (switching and line combined)
Il1 = sqrt(Io.^2+Ic1.^2); % total rms current (switching and line combined)

% calculating the conduction losses
P_cond(i) = sum((Rh+RL).*IL.^2.*D ... 
+ 2*RL.*IL.^2.*(1-D-2*Ddt) ... 
+ (Vd*IL+RL.*IL.^2)*2*Ddt )/length(w);
P_cond1(i) = sum((Rh+RL).*Il1.^2.*D ... 
+ 2*RL.*Il1.^2.*(1-D-2*Ddt) ... 
+ (Vd*Il1+RL.*Il1.^2)*2*Ddt )/length(w);

% calculating the switching losses
P_switch(i) = sum(Trans.*IL*Vbus*f(i)/6) /length(w);
P_switch1(i) = sum(Trans.*Il1*Vbus*f(i)/6) /length(w);

% calculating the driving losses
P_drive(i) = f(i)*Vg*Qg;

end

plot(f,P_cond+P_switch+P_drive),xlabel('Freq in Hz'),ylabel('Loss in Watts'),title('Power Loss in MOSFET vs. Freq. w/ const inductance');
figure; plot(f,P_cond1+P_switch1+P_drive),xlabel('Freq in Hz'),ylabel('Loss in Watts'),title('Power Loss in MOSFET vs. Freq. w/ constant output I rip');
figure; plot(f,Cap),xlabel('Freq in Hz'),ylabel('Capacitance in Farads'),title('Capacitance needed for constant output V ripple vs. Freq');
figure; plot(f,L),xlabel('Freq in Hz'),ylabel('Inductance in henry'),title('Inductance needed for constant output I ripple vs. Freq');
figure; plot(f,current_ripple),xlabel('Freq in Hz'),ylabel('Current in Amps'),title('output I ripple vs. Freq w/ const inductance');
APPENDIX C: BI-POLAR ANALYSIS MATLAB CODE
%Losses for Bi-Polar

clear all
close all
clc

circuit parameters

Vbus=200;       %input/bus voltage that is being bucked down and inverter to sine
Vo=120;         %output voltage in rms for the outputted sine wave
Rload=14.4;     %the load resistance (full power for 1Kw is 14.4 ohms)
Vrip=.005;      %this is with the output voltage ripple of 0.5% (normalized)
Irip=1.4;       %this is with a output current ripple of 1.4 A (not-normalized or put
in terms of percentage)

%USED FOR CONDUCTION LOSSES
Rh=59e-3;       %Rds on resistance of high side the MOSFET being used
RL=Rh;          %Rds on resistance of low side the MOSFET being used
Tdelay=100e-9;  %dealy or dead time between high and low side switching on (for
safety)
Vd=1;           %the MOSFETs body diode forward voltage drop

%USED FOR SWITCHING LOSSES
Trans=10e-9;    %the rise and fall time of the MOSFETs (i.e. the time between the
MOSFET being fully on or off)

%USED FOR DRIVING LOSSES
Vg=10;          %the MOSFETs gate drive voltage
Qg=247e-9;      %the MOSFETs gate charge

% define radian vector
w=0:pi/10000:pi;
% sweep frequency
f = 20e3:.1e3:120e3;

% initializing the conduction, switching, and driving losses
P_cond = zeros(1, length(f));
P_switch = zeros(1, length(f));
P_drive = zeros(1, length(f));

for i = 1:length(f)
    Per = 1/f(i); % determining the switching period
    Ddt = Tdelay*f(i); % determining the dead time with respect to duty cycle

    D = .5 + .5*Vo*sqrt(2)*sin(w)/Vbus; % determining the duty cycle
    for the different radians

    % calculating the output components such as output capacitance and inductance
    L(i) = sum(D*Per.*(Vbus-Vo*sqrt(2)*sin(w))/Irip)/length(w);
    Cap(i) = sum((1-D)/(8*L(i)*(f(i))^2*Vrip))/length(w);

    % peak to peak inductor ripple current
    delI = D/f(i).*(Vbus-Vo*sqrt(2)*sin(w))/250e-6;
    delII = D/f(i).*(Vbus-Vo*sqrt(2)*sin(w))/L(i);
    current_ripple(i) = sum(delI)/length(w);

    % rms values for currents:
Ic=delI/(2*sqrt(3));    % switching frequency component
Ic1=delI1/(2*sqrt(3));  % switching frequency component

Io=Vo*sqrt(2)*sin(w)/Rload;  % line frequency component
IL=sqrt(Io.^2+Ic.^2);   % total rms current (switching and line combined)
IL1=sqrt(Io.^2+Ic1.^2);  % total rms current (switching and line combined)

%calculating the conduction losses
P_cond(i)= sum( (Rh+RL).*IL.^2.*D ... 
+ 2*RL.*IL.^2.*(1-D-2*Ddt) ... 
+ (Vd*IL+RL.*IL.^2).*2*Ddt ) /length(w);

P_cond1(i)= sum( (Rh+RL).*IL1.^2.*D ... 
+ 2*RL.*IL1.^2.*(1-D-2*Ddt) ... 
+ (Vd*IL1+RL.*IL1.^2).*2*Ddt ) /length(w);

%calculating the switching losses
P_switch(i)=2*sum( Trans.*IL*Vbus*f(i)/6 ) /length(w);

P_switch1(i)=2*sum( Trans.*IL1*Vbus*f(i)/6 ) /length(w);

%calculating the driving losses
P_drive(i)=f(i)*Vg*Qg;

end

plot(f,P_cond+P_switch+P_drive),xlabel('Freq in Hz'),ylabel('Loss in Watts'),title('Power Loss in MOSFET vs. Freq. w/ const inductance');
figure; plot(f, P_cond1 + P_switch1 + P_drive), xlabel('Freq in Hz'), ylabel('Loss in Watts'), title('Power Loss in MOSFET vs. Freq w/ constant output I rip');
figure; plot(f, Cap), xlabel('Freq in Hz'), ylabel('Capacitance in Farads'), title('Capacitance needed for constant output V ripple vs. Freq');
figure; plot(f, L), xlabel('Freq in Hz'), ylabel('Inductance in henry'), title('Inductance needed for constant output I ripple vs. Freq');
figure; plot(f, current_ripple), xlabel('Freq in Hz'), ylabel('Current in Amps'), title('output I ripple vs. Freq w/ const inductance');
APPENDIX D: MATH DERIVATIONS
• EQ. 27 is derived from EQ. 20 and EQ. 22

\[ t_1 = \frac{-i_L(0^-) \cdot L}{V_{in} \cdot N + V_{c1}}, \quad i_L(0^-) = -i_L, \quad \Rightarrow t_1 = \frac{\ddot{i}_L \cdot L}{V_{in} \cdot N + V_{c2}} \]

\[ i_L^+ = \frac{V_{in} \cdot N - V_{c2}}{L} \left( D \cdot T_s - t_1 \right) \Rightarrow \frac{i_L^+}{V_{in} \cdot N - V_{c2}} + \frac{t_1}{L} = \frac{D \cdot T_s}{L} \]

Combining the above two equations yields:

\[ \frac{D \cdot T_s}{L} = \frac{i_L^+}{V_{in} \cdot N - V_{c2}} + \frac{V_{in} \cdot N + V_{c1}}{L} \]

\[ = \frac{i_L^+}{V_{in} \cdot N - V_{c2}} + \frac{i_L^-}{V_{in} \cdot N + V_{c2}} \]

• EQ. 28 is derived in a similar fashion using EQ. 24 and EQ. 26.

\[ \Delta t_2 = t_2 - D \cdot T_s = i_L(D \cdot T_s) \cdot \frac{L}{V_c \cdot N + V_{c2}}, \quad i_L(D \cdot T_s) = i_L^+, \quad \Rightarrow t_2 = \frac{i_L^+ \cdot L}{V_c \cdot N + V_{c2}} + D \cdot T_s \]

\[ i_L^- = \frac{-(V_c \cdot N - V_{c1})}{L} \left( T_s - t_2 \right) \Rightarrow \frac{i_L^-}{(V_c \cdot N - V_{c1})} + \frac{t_2}{L} = \frac{T_s}{L} \]

Combining the above two equations yields:

\[ \frac{(1 - D) \cdot T_s}{L} = \frac{i_L^-}{V_c \cdot N - V_{c1}} + \frac{i_L^+}{V_c \cdot N + V_{c2}} \]

• EQ. 29 is derived by taking either equation 27 or 28 and setting D to one half. With D set to one half \( V_c \) is equal to \( V_{in} \), the peak \( i_L \) currents are equal to \( 4 \cdot I_o \), and \( V_{c1} \) is equal to \( V_{c2} \) which is also equal to half of \( V_o \).
Using EQ. 27 and setting D = .5 yields

\[ i_L^+ = i_L^- = 4 \cdot I_o, \quad V_{in} = V_c, \quad V_{cl} = V_{c2} = \frac{V_o}{2} \]

\[ \frac{D \cdot T_s}{L} = \frac{i_L^+}{V_{in} \cdot N - V_{cl}} + \frac{i_L^-}{V_{in} \cdot N + V_{cl}} \]

\[ \Rightarrow \frac{.5 \cdot T_s}{L_s} = i_L^+ \cdot \left( \frac{1}{V_{in} \cdot N - V_{cl}} + \frac{1}{V_{in} \cdot N + V_{cl}} \right) = i_L^+ \cdot \left( \frac{V_{in} \cdot N + V_{cl} + V_{in} \cdot N - V_{cl}}{(V_{in} \cdot N - V_{cl}) \cdot (V_{in} \cdot N + V_{cl})} \right) \]

\[ \Rightarrow \frac{.5 \cdot T_s}{L_s} = i_L^+ \cdot \left( \frac{2 \cdot V_{in} \cdot N}{(V_{in} \cdot N)^2 + V_{in} \cdot N \cdot V_{cl} - V_{in} \cdot N \cdot V_{cl} - (V_{cl})^2} \right) = i_L^+ \cdot \left( \frac{2 \cdot V_{in} \cdot N}{(V_{in} \cdot N)^2 - (V_{cl})^2} \right) \]

\[ \Rightarrow \frac{.5 \cdot T_s}{L_s} = i_L^+ \left( \frac{2 \cdot V_{in} \cdot N}{(V_{in} \cdot N)^2 - \left( \frac{V_o}{2} \right)^2} \right) \Rightarrow .5 \cdot T_s \cdot \left( (V_{in} \cdot N)^2 - \left( \frac{V_o}{2} \right)^2 \right) = i_L^+ \cdot 2 \cdot V_{in} \cdot N \cdot L_s \]

\[ \Rightarrow (V_{in} \cdot N)^2 - \left( \frac{V_o}{2} \right)^2 = \frac{i_L^+ \cdot 2 \cdot V_{in} \cdot N \cdot L_s}{.5 \cdot T_s} \Rightarrow \frac{(V_o)^2}{2} = (V_{in} \cdot N)^2 - \left( \frac{i_L^+ \cdot 2 \cdot V_{in} \cdot N \cdot L_s}{.5 \cdot T_s} \right) \]

\[ \Rightarrow \frac{(V_o)^2}{2} = (V_{in} \cdot N)^2 - \left( \frac{16 \cdot I_o \cdot V_{in} \cdot N \cdot L_s}{T_s} \right) \Rightarrow \frac{V_o}{2} = \sqrt{V_{in}^2 \cdot N^2 - \frac{16 \cdot I_o \cdot V_{in} \cdot N \cdot L_s}{T_s}} \]

\[ V_o = 2 \cdot \sqrt{V_{in}^2 \cdot N^2 - \frac{16 \cdot I_o \cdot V_{in} \cdot N \cdot L_s}{T_s}} \]

- EQ. 30

The current going through the capacitor is equal to \( I_{Prim} \) in Figure 28 during the (1-D) period or when switch \( S_2 \) is on.
First Part = \frac{1}{T_s} \left( \int_0^{T_s} \left( -\frac{i^+_L \cdot N}{t_1} \cdot x + I_{Lmag} + I_{Series} \cdot N \right)^2 \cdot dx \right) \Rightarrow

\frac{1}{T_s} \left\{ \int_0^{T_s} \left[ \frac{(i^+_L)^2 \cdot N^2}{t_1^2} \cdot x^2 - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N)}{t_1} \cdot x + (I_{Lmag} + i^+_L \cdot N)^2 \right] \cdot dx \right\} \Rightarrow

\frac{1}{T_s} \left\{ \left[ \frac{(i^+_L)^2 \cdot N^2}{t_1^2} \cdot x^3 \right]_{0}^{T_s} - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N)}{t_1} \cdot \frac{x^2}{2} + (I_{Lmag} + i^+_L \cdot N)^2 \cdot x \left| _0^{T_s} \right. \right\} \Rightarrow

\frac{1}{T_s} \cdot \left\{ \left[ \frac{(i^+_L)^2 \cdot N^2}{t_1^2} \cdot T_s \cdot \frac{T_s}{3} \right] - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N) \cdot T_s}{2} + (I_{Lmag} + i^+_L \cdot N)^2 \cdot T_s \right\} \Rightarrow

\frac{1}{T_s} \cdot \left\{ \left[ \frac{(i^+_L)^2 \cdot N^2}{t_1^2} \cdot T_s \cdot \frac{T_s}{3} \right] - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N) \cdot T_s}{2} + (I_{Lmag} + i^+_L \cdot N)^2 \cdot T_s \right\} \Rightarrow

\frac{1}{T_s} \cdot \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{T_s/2}^{T_s} - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N)}{T_s/2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

\frac{1}{T_s} \cdot \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{T_s/2}^{T_s} - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N)}{T_s/2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

\frac{1}{T_s} \cdot \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{T_s/2}^{T_s} - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N)}{T_s/2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

\frac{1}{T_s} \cdot \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{T_s/2}^{T_s} - \frac{2 \cdot i^+_L \cdot N \cdot (I_{Lmag} + i^+_L \cdot N)}{T_s/2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

Second Part = \frac{1}{T_s} \cdot \int_0^{T_s/2} \left( -\frac{i^+_L \cdot N}{T_s/2 - t_1} \cdot x + I_{Lmag} \right)^2 \cdot dx \Rightarrow

\frac{1}{T_s} \cdot \int_0^{T_s/2} \left( \frac{(i^+_L)^2 \cdot N^2}{(T_s/2 - t_1)^2} \cdot x^2 - \frac{2 \cdot i^+_L \cdot N \cdot I_{Lmag}}{(T_s/2 - t_1)^2} \cdot x + I_{Lmag}^2 \right) \cdot dx \Rightarrow

\frac{1}{T_s} \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{(T_s/2 - t_1)}^{T_s/2} - \frac{2 \cdot i^+_L \cdot N \cdot I_{Lmag}}{(T_s/2 - t_1)^2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

\frac{1}{T_s} \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{(T_s/2 - t_1)}^{T_s/2} - \frac{2 \cdot i^+_L \cdot N \cdot I_{Lmag}}{(T_s/2 - t_1)^2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

\frac{1}{T_s} \left\{ \left[ (i^+_L)^2 \cdot N^2 \right]_{(T_s/2 - t_1)}^{T_s/2} - \frac{2 \cdot i^+_L \cdot N \cdot I_{Lmag}}{(T_s/2 - t_1)^2} \cdot \left[ \frac{x^2}{2} + I_{Lmag}^2 \cdot x \right] \left| _0^{T_s/2} \right. \right\} \Rightarrow

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\[
\frac{1}{T_s} \left[ \left( \frac{T_s}{2} - t_1 \right) \cdot \left\{ \frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 - (i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2) \right\} \right] \Rightarrow
\]

Combining the first and second
\[
\frac{1}{T_s} \left[ \left( \frac{T_s}{2} - t_1 \right) \cdot \left\{ \frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 - i_L^+ \cdot N \cdot (I_{Lmag} + i_L^+ \cdot N) + (i_L^+ \cdot N)^2 \right\} \right] + t_1 \cdot \left( -\frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right) +
\]
\[
\frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 - i_L^+ \cdot N \cdot (I_{Lmag} + i_L^+ \cdot N) + (i_L^+ \cdot N)^2 \Rightarrow
\]
\[
\frac{1}{T_s} \left[ \left( \frac{T_s}{2} - t_1 \right) \cdot \left\{ \frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 - i_L^+ \cdot N \cdot (I_{Lmag} + i_L^+ \cdot N) + (i_L^+ \cdot N)^2 \right\} \right] + t_1 \cdot \left( 2 \cdot N \cdot i_L^+ \cdot I_{Lmag} \right)
\]
\[
\left[ \frac{1}{2} \cdot \left\{ \left( \frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 \right) - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} \right] + \frac{t_1 \cdot \left( 2 \cdot N \cdot i_L^+ \cdot I_{Lmag} \right)}{T_s}
\]

Now the square root must be taken to find the rms value
\[
\sqrt{\left[ \frac{1}{2} \cdot \left\{ \left( \frac{1}{3} \cdot (i_L^+)^2 \cdot N^2 \right) - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} \right] + \frac{t_1 \cdot \left( 2 \cdot N \cdot i_L^+ \cdot I_{Lmag} \right)}{T_s}}
\]

- **EQ. 31**

The current going through the switch S1 is equal to \( I_{\text{Prim}} \) in Figure 28 during the D period.

First part = \( \frac{1}{T_s} \cdot \int_{t_1}^{t_1} \left( i_L^+ \cdot N \cdot x + \left(-i_L^+ \cdot N \cdot I_{Lmag} \right) \right)^2 \cdot dx \Rightarrow
\]
\[
\frac{1}{T_s} \cdot \int_{t_1}^{t_1} \left( \frac{(i_L^+ \cdot N)^2}{t_1} \right) \cdot x^2 + \frac{2 \cdot i_L^+ \cdot N \cdot (i_L^+ \cdot N \cdot I_{Lmag})}{t_1} \cdot x + \left(-i_L^+ \cdot N \cdot I_{Lmag} \right)^2 \cdot dx \Rightarrow
\]
\[
\frac{1}{T_s} \cdot \left( \frac{(i_L^+ \cdot N)^2}{t_1} \cdot \frac{x^3}{3} + \frac{2 \cdot i_L^+ \cdot N \cdot (i_L^+ \cdot N \cdot I_{Lmag})}{t_1} \cdot \frac{x^2}{2} + \left(-i_L^+ \cdot N \cdot I_{Lmag} \right)^2 \cdot x \right) \bigg|_{t_1}^{t_1} \Rightarrow
\]
\[
\frac{1}{T_s} \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} \cdot t_1 + \frac{i_L^+ \cdot N \cdot (-i_L^+ \cdot N \cdot I_{Lmag})}{1} \cdot t_1 + (-i_L^+ \cdot N \cdot I_{Lmag})^2 \cdot t_1 \right) \Rightarrow \\
\frac{1}{T_s} \cdot [t_1 \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} \right) - (i_L^+ \cdot N)^2 + i_L^+ \cdot N \cdot I_{Lmag} + \left( i_L^+ \cdot N \right)^2 + I_{Lmag}^2 - 2 \cdot I_{Lmag} \cdot i_L^+ \cdot N] \Rightarrow \\
\frac{1}{T_s} \cdot [t_1 \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right)] \\
\]

The second part = \[
\frac{1}{T_s} \cdot \int_0^{\frac{T_s}{2} - t_1} \left( \frac{i_L^+ \cdot N}{T_s} \cdot x + I_{Lmag} \right)^2 \cdot dx \Rightarrow \\
\frac{1}{T_s} \cdot \int_0^{\frac{T_s}{2} - t_1} \left( \frac{i_L^+ \cdot N}{T_s} \cdot x^2 + \frac{2 \cdot i_L^+ \cdot N \cdot I_{Lmag}}{T_s} \cdot x + I_{Lmag}^2 \right) \cdot dx \Rightarrow \\
\frac{1}{T_s} \cdot \left[ \left( \frac{T_s}{2} - t_1 \right)^{\frac{(i_L^+ \cdot N)^2}{3}} + \frac{2 \cdot i_L^+ \cdot N \cdot I_{Lmag}}{T_s} \cdot \frac{T_s}{2} - t_1 \right] \Rightarrow \\
\frac{1}{T_s} \cdot \left[ \frac{T_s}{2} - t_1 \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} \cdot I_{Lmag} \right) + \left( i_L^+ \cdot N \cdot I_{Lmag} \right) + I_{Lmag}^2 \right] \Rightarrow \\
\]

Combining first and second parts
\[
\frac{1}{2} \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} + (i_L^+ \cdot N \cdot I_{Lmag}) + I_{Lmag}^2 \right) + \frac{1}{T_s} \cdot \left[ -t_1 \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} \right) + (i_L^+ \cdot N \cdot I_{Lmag}) + I_{Lmag}^2 \right] 
\]
\[ t_1 \cdot \left( \frac{(i_L^+ \cdot N)^2}{3} - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right) \Rightarrow \]

\[ \frac{1}{2} \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} + (i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} = \frac{1}{T_s} \cdot [t_1 \cdot (2 \cdot i_L^+ \cdot N \cdot I_{Lmag})] \Rightarrow \]

\[ \frac{1}{2} \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} + (i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} - t_1 \cdot \frac{2 \cdot i_L^+ \cdot N \cdot I_{Lmag}}{T_s} \]

Now the square root must be taken to find rms value

\[ \sqrt{\frac{1}{2} \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} + (i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} - t_1 \cdot \frac{2 \cdot i_L^+ \cdot N \cdot I_{Lmag}}{T_s}} \]

- EQ 32

Since EQ 30 and 31 each are half of EQ 32, so you can add the above two equations and then you will achieve this EQ.

EQ 30

\[ \sqrt{\left[ \frac{1}{2} \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} + \frac{t_1 \cdot 2 \cdot N \cdot i_L^+ \cdot I_{Lmag}}{T_s} \right]} \]

EQ 31

\[ \sqrt{\frac{1}{2} \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} + (i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} - \frac{t_1 \cdot 2 \cdot i_L^+ \cdot N \cdot I_{Lmag}}{T_s}} \]

EQ 30 plus 31

\[ .5 \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} - i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} + \frac{t_1 \cdot 2 \cdot N \cdot i_L^+ \cdot I_{Lmag}}{T_s} + \]

\[ .5 \cdot \left\{ \frac{(i_L^+ \cdot N)^2}{3} + (i_L^+ \cdot N \cdot I_{Lmag} + I_{Lmag}^2 \right\} - \frac{t_1 \cdot 2 \cdot i_L^+ \cdot N \cdot I_{Lmag}}{T_s} \Rightarrow \]

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\[ \sqrt{\frac{(i_L^+)^2 \cdot N^2}{3}} + I_{Lmag}^2 \Rightarrow \text{From the property that } i_L^+ = 4 \cdot I_o \]
\[ \sqrt{\frac{16 \cdot I_o^2 \cdot N^2}{3}} + I_{Lmag}^2 \]

- The way to obtain the secondary side of the transformers current stress is by using the above equation, EQ. 32. This is due to the fact the secondary has the same current stress as the primary except no DC current and is reduced by the turns ratio.

EQ.32
\[ \sqrt{\frac{16 \cdot I_o^2 \cdot N^2}{3}} + I_{Lmag}^2 \]
now removing DC and relating the current to secondary side
\[ \sqrt{\frac{16 \cdot I_o^2}{3}} \approx \frac{4 \cdot I_o}{\sqrt{3}} \approx 2.3 \cdot I_o \]

- The current stress for the output capacitor is given by:

The first part
\[ \frac{T_s}{2} \int_0^{\frac{T_s}{2}} I_o^2 \cdot dx = I_o^2 \cdot \frac{T_s}{2} \]

The second part
\[ \frac{T_s}{2} \int_0^{\frac{T_s}{2}} (I_o - \frac{8 \cdot I_o}{T_s} \cdot x)^2 \cdot dx = \frac{T_s}{2} \int_0^{\frac{T_s}{2}} \left( I_o^2 - \frac{16 \cdot I_o^2}{T_s} \cdot x + \frac{64 \cdot I_o^2}{T_s} \cdot x^2 \right) \cdot dx \Rightarrow \]
\[
(I_o^2 \cdot x - \frac{16 \cdot I_o^2 \cdot x^2}{T_s \cdot 2} + \frac{64 \cdot I_o^2 \cdot x^3}{T_s \cdot 3}) \bigg|_{0}^{T_s/2} = I_o^2 \cdot T_s \cdot (\frac{1}{2} - 2 + \frac{8}{3}) = \frac{7}{6} \cdot I_o^2 \cdot T_s
\]

Combining the first and second part

\[
\frac{I_o^2 \cdot T_s}{2} + \frac{7}{6} \cdot I_o^2 \cdot T_s
\]

Now taking the root and mean of the squared terms.

\[
\sqrt{\frac{1}{T_s} \left( \frac{I_o^2 \cdot T_s}{2} + \frac{7}{6} \cdot I_o^2 \cdot T_s \right)} = \sqrt{\frac{I_o^2}{2} + \frac{7}{6} \cdot I_o^2} = \sqrt{\left( \frac{1}{2} + \frac{7}{6} \right) \cdot I_o^2} = I_o \sqrt{\frac{5}{3}} \approx 1.3 \cdot I_o
\]

The DC current stress for the diodes are equal to that of the output current because no DC current can go through capacitors. So, the only way for the output current to flow is through the diodes.
REFERENCES


[12] Steve Mappus, “Designing for High Efficiency with the Active Clamp UCC2891 PWM Controller” Texas Instruments Application notes, April 2004