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NEGATIVE BIAS TEMPERATURE INSTABILITY AND CHARGE TRAPPING EFFECTS ON ANALOG AND DIGITAL CIRCUIT RELIABILITY

by

YIXIN YU
B.S. University of Science and Technology of China, 2003

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2007

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ABSTRACT

Nanoscale p-channel transistors under negative gate bias at an elevated temperature show threshold voltage degradation after a short period of stress time. In addition, nanoscale (45 nm) n-channel transistors using high-k (HfO_2) dielectrics to reduce gate leakage power for advanced microprocessors exhibit fast transient charge trapping effect leading to threshold voltage instability and mobility reduction. A simulation methodology to quantify the circuit level degradation subjected to negative bias temperature instability (NBTI) and fast transient charge trapping effect has been developed in this thesis work. Different current mirror and two-stage operation amplifier structures are studied to evaluate the impact of NBTI on CMOS analog circuit performances for nanoscale applications. Fundamental digital circuit such as an eleven-stage ring oscillator has also been evaluated to examine the fast transient charge transient effect of HfO_2 high-k transistors on the propagation delay of ring oscillator performance.

The preliminary results show that the negative bias temperature instability reduces the bandwidth of CMOS operating amplifiers, but increases the amplifier's voltage gain at mid-frequency range. The transient charge trapping effect increases the propagation delay of ring oscillator. The evaluation methodology developed in this thesis could be extended to study other CMOS device and circuit reliability issues subjected to electrical and temperature stresses.

To remember my dear Grandma C. Y. Wang

ACKNOWLEDGMENTS

First of all, I would like to express my deep and sincere gratitude to my supervisor, Professor Jiann. S. Yuan. His wide knowledge and his logical way of think have been of great value for me. His understanding, encouraging and personal guidance have provided a good basis for the present thesis. I am pleasure to be one of his students. During the last two years, I learn from him both in academic and in life attitude, which will influence on my following whole life.

I am deeply grateful to my thesis committee members, Dr. Kalpathy B. Sundaram and Dr. Lee Chow for their valuable time and constructive comments.

I wish to express my sincere thanks to my classmate, Mr. Hongwei Jia for his friendly help. His valuable advices and extensive discussions around my work have been very helpful for this study.

I also wish to thanks my colleagues, Dr. Chuanzhao Yu, Ms. Lin Shen, Mr. Jun Ma and Ms. Hongxia Tang, for their kind help.

My final and most heartfelt acknowledgment must go to my father Weizhen Yu, my mother Yongfang Tang, and my husband Qiu Dai. Their support, encouragement and love have

turned my journey through graduate school into a pleasure. For all that, and for being everything I am not, they have my everlasting love.

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LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
BD	Breakdown
CMOS	Complementary Metal Oxide Semiconductor
C-V	Capacitance versus Voltage
CVS	Constant Voltage Stress
DC	Direct Current
DUT	Device-Under-Test
FOM	Figure of Merit
HBD	Hard Breakdown
HC	Hot Carrier
HCI	Hot Carrier Injection
HF	High Frequency
IC	Integrated Circuit
I-V	Current versus Voltage
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability

NF	Noise Figure
NMOSFET	N-type MOS Field Effect Transistor
PBTI	Positive Bias Temperature Instability
PMOSFET	P-type MOS Field Effect Transistor
RF	Radio Frequency
SILC	Stress Induced Leakage Current
SOC	System on Chip
SPCT	Single Pulse Chare Trapping
TDDB	Time Dependent Dielectric Breakdown

CHAPTER ONE: INTRODUCTION

1.1 Motivation

Complementary Metal Oxide Semiconductor (CMOS) has become the dominant technology in the electronic industry for the past several decades, and it is expected to stay in such position for the next years. Before the end of 2003, microprocessors were able to produce 90 nm processes, and now production on 45 nm and below is coming out. However, the scaling of CMOS technology into deep submicron regimes has brought about new reliability challenges in MOSFET device such as hot carrier Injection (HCI), Negative Bias Temperature Instability (NBTI) [1,2], Time Dependent Dielectric Breakdown (TDDB), radiation induced damage, etc., which can pose a limit to the device scaling, and cause circuit performance degradation.

When integrate circuits work for long time, especially for today's CMOS technology, heat of chips will increase significantly. For this reason, one of the dominant reliability issues - Negative Bias Temperature Instability (NBTI) in PMOS transistors will be studied in this work. NBTI impact gets even worse in scaled technology due to higher operation temperature and the usage of ultra thin oxide (i.e., higher oxide field).

In order to reduce the high gate leakage current in ultra thin regime, High-k dielectrics are used to replace the traditional SiO_2 material or combine with it to use. However High-k dielectrics still have many problems. One of the demonstrated issues is charge trapping effect. All of the high-k dielectrics contain large amounts of fixed charge compared to SiO_2, regardless of the high-k film deposition technique. The fixed charges are freely to move from the interface to gate oxide and back again. Those fixed charges within the bulk of high-k film change the threshold voltage. As the gate oxide thickness continues to shrink, it is very promising to use high-k dielectrics to reduce high leakage voltage. Consequently, it is very desirable to study the circuit reliability performance with high-k dielectrics.

1.2 Thesis Outline

This thesis is organized to 5 chapters. Two reliability issues -Negative Bias Temperature Instability (NBTI) and charge trapping effect are presented in chapter 2, including the physical explanation models, mathematics models, and popular measurements, which work already has been done by numbers of other groups. MOSFET structures and I/V characteristics are also introduced in this chapter in order to highly understand reliability induced circuit performance.

In Chapter 3, analog circuit performance degradation due to NBTI is analyzed. A simple current mirror, cascode current mirror, wide-swing current mirror and an unbuffered two stage operation amplifier are employed to study. After briefly introduction, those circuits are designed to analyze NBTI impact by using Cadence Spectra simulation tool.

In Chapter4, digital circuit performance degradation due to charge trapping effect and NBTI is analyzed. Firstly, Inverter and Ring Oscillator are briefly introduced, and then those digital circuits are designed in Cadence Spectra simulation environment to analyze the circuit degradation due to charge trapping and NBTI. Finally, summary about these two phenomena effect on digital circuits are given.

In the last Chapter 5, general conclusion of this thesis work will be concluded.

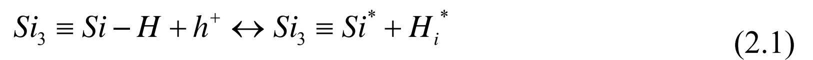
CHAPTER TWO: RELIABILITY ANALYSIS

2.1 Negative Bias Temperature Instability

2.1.1 Introduction

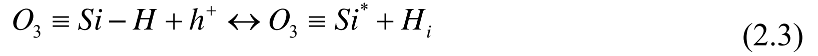
One of the major temperature-induced reliability issues for p-channel metal-oxide semiconductor field effect transistors (pMOSFETs) is the negative bias temperature instability (NBTI), which is caused by stressing negative gate bias at elevated temperatures. A positive charge builds up at the channel interface of pMOSFETs under negative bias and high temperature conditions. The typical temperature conditions for NBTI effects are in the range of 100 ~ 250 $^{\circ}C$, and the oxide electric fields should be below 6MV/cm [46].

During NBTI–induced device degradation, the holes in the inversion layer react with the hydrogen-silicon bonds (Si-H) at the Si/SiO_2 interface and then release the hydrogen species (atom, molecule or ion) by breaking the Si–H bonds, because the two-electron Si-H covalent bond is weakened. Once a hole is captured and this weakened bond is easily broken at relatively moderate temperature. The electrochemical reactions at the SiO_2/Si interface are given as follows [3, 4, 5, 6]:



$$Si_3 \equiv Si - H + h^+ \leftrightarrow Si_3 \equiv Si^* + H_i^* \quad (2.1)$$

$$Si_3 \equiv Si - H \overset{h^+}{\leftrightarrow} Si_3 \equiv Si^* + H_i \quad (2.2)$$



$$O_3 \equiv Si - H + h^+ \leftrightarrow O_3 \equiv Si^* + H_i \qquad (2.3)$$

$$(H^*, H_i)_{interface} \leftrightarrow (H^*, H_i)_{bulk} \qquad (2.4)$$

Both trivalent silicon dangling bonds ($S_{i_3} \equiv S_i^*$) and fixed oxide charges ($O_3 \equiv S_i^-$) can form interface states N_{it} , which are generated by the impact of hot holes on the hydrogen-terminated Si bonds and are responsible for the increase of threshold voltage, temporarily decrease of the off-state current, reduce in transconductance and drain saturation current.

2.1.2 Physics Mechanism and Models

The classical Reaction–Diffusion (R–D) model, a physical mechanism, has been used to interpret NBTI-induced degradation in pMOSTETs by several groups [7, 8, 9]. It is assumed that the NBTI effect results from hole-assisted dissociation of weak Si-H bonds into the charged Si dangling bonds and atomic H at the Si/SiO_2 interface.

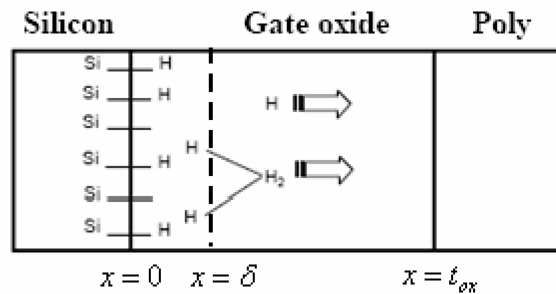


Figure 1: Reaction-Diffusion Model for NBTI

The related equations for this physical model and details of explanation are given in [10,11], which indicated that the NBTI degradation mainly results from depassivation of Si-H bonds at the Si/dielectric interface and resultant diffusion of hydrogen species into gate dielectric and poly-Si.

The direct effect of NBTI on device degradation is the shift of the threshold voltage $\Delta V_t(t)$, which presents a fractional power law characteristic $\Delta V_t(t) \propto t^n$ with $n \sim (0.15 - 0.3)$, and the typical value of n is 0.25 [7, 11, 12]. In most NBTI experimental work, the fractional value of n predicts a saturation behavior at long time ($t_{stress} > 10 - 100s$). It has been reported that the V_t shift is exponentially related with voltage and temperature, which are modeled by $\Delta V_t(t) \propto \exp(\beta V_G)$ [13, 14, 17], $\Delta V_t(t) \propto \exp(-E_a / kT)$ [5, 7, 15], and

$$\Delta V_t(t) \propto \exp(\beta V_G)\exp(-E_a / kT) \text{ [16].} \tag{2.5}$$

According to [18], the NBTI-induced threshold voltage instability is caused by the increase of positive fixed charge $\Delta N_f(t)$ and the generation of donor type interface traps $\Delta N_{it}(t)$, which are resulted from the dissociation of Si-H bonds.

$$\Delta N_{it}(E_{ox}, T, t, t_{ox}) = 9\times10^{-4} E_{ox}{}^{1.5} t^{0.25} \exp(-0.2 / kT) / t_{ox} \tag{2.6}$$

$$\Delta N_f(E_{ox}, T, t) = 490 E_{ox}{}^{1.5} t^{0.14} \exp(-0.15 / kT) \tag{2.7}$$

where C_{ox} is the oxide capacitance, E_{ox} is oxide electric field, t_{ox} is oxide thickness, k is Boltamann's constant, T is temperature and t is stress time. According to this condition, the threshold voltage shift equation is expressed as following [6]:

$$\Delta V_t(\Delta N_{it}, \Delta N_f) = B_1[1-\exp(-t/\tau_1)] + B_2[1-\exp(-t/\tau_2)] \tag{2.8}$$

Where B1 and B2 can be related to equation (9) and (10) respectively, and τ_1 and τ_2 are the reaction limiting time. However, it is assumed in R-D model that threshold voltage degradation is mainly due to interface trap generation. In additional, the threshold voltage degradation is also mainly dominated by interface state generation at relatively lower gate voltage during analog condition. It is reasonable to believe that threshold voltage degradation caused by interface trap N_{it} is able to be expressed as following equation [11]:

$$\Delta V_t(t) \propto \frac{q\Delta N_{it}(t)}{C_{ox}}, \text{ where } C_{ox} = \varepsilon_{ox}/t_{ox}. \tag{2.9}$$

Additionally, according to silicon-hydrogen bond density the other NBTI-induced threshold voltage instability model has been reported, which is given as follows [19, 20]:

$$\Delta V_t(t) = \Delta V_{\max}[1-e^{-(t/\tau)^\beta}] \tag{2.10}$$

where $\Delta V_{\max}$, τ and β are three model parameters. The parameter $\Delta V_{\max}$ is the maximum $\Delta V_t(t)$ shift that would occur when all the interfacial Si-H bonds have been depassivated. β is used to measure the dispersion of hydrogen diffusion and it decreases from 1 to 0 with the increases of dispersion. β is able to increase with the increase of temperature and be independent on stress oxide field. The term τ is the time to measure the NBTI-induced degradation rates when $\Delta V_t(t)$ reaches 63% of $\Delta V_{\max}$ [46].

Additionally, there also have been several efforts to study the NBTI-induced degradation under AC stress condition [21, 22]. It has been reported that NBTI-induced degradation under AC stress is smaller than that of DC stress condition, and the ratio of AC to DC NBTI degradation is frequency independent at least for low frequencies (<10–100 kHz).

2.1.3 Device Degradation Measurement Methods

To measure the NBTI characteristic of a PMOS transistor, a constant negative bias is applied to the gate electrode at high temperatures, with source, drain, and substrate grounded. Both V_t (extracted by $I_d - V_g$ measurement) and N_{it} (extracted by DCIV measurement) were measured [23, 24, 26]. During each interruption of stress for measurement, the negative gate voltage is reduced (for $I_d - V_g$ measurement), or even turned positive (for DCIV or CP measurement). The interface trap density reduces at this moment due to passivation of interface traps. The measured values of and are therefore underestimated. The passivation effect is more pronounced during the long measurement than during the short measurement, because of the longer measurement time and the more positive bias employed. The schematic cross-sectional diagram of the NBTI stress setup is shown in Figure.

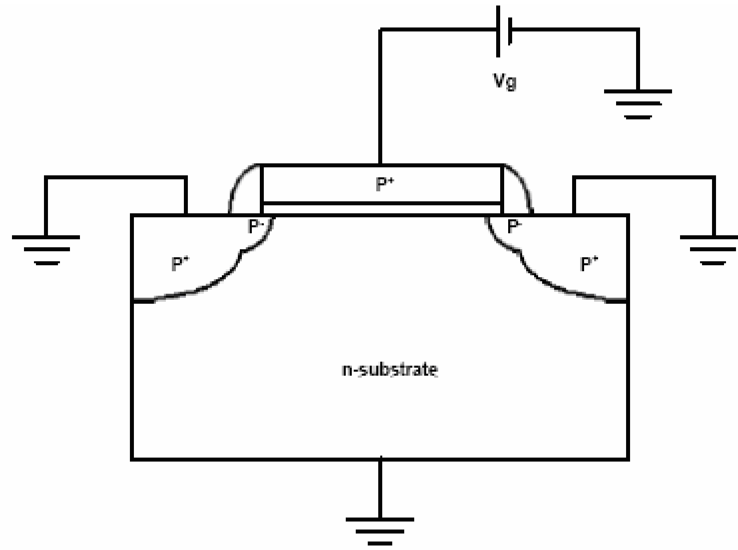


Figure 2: Experimental arrangement for NBTI stress

Recently, there're some circuit simulation methods to measure NBTI effect in SPICE environment at the sub-circuit level. For example, a new simulation method for NBTI analysis in HSPICE environment studied [10]. In this method, the increase of threshold voltage is modeled as a voltage controlled voltage source, which leads to decrease in V_{gs} (compared to V_{GS}) and subsequently decreases in the drain current. The decrease in the drain current emulates the NBTI effect. Another new Maryland Circuit reliability –Oriented SPEICE simulation method was studied by [26]. For this circuit model simulation, a gate resistance R_G was added between original gate biasing point G and the pMOSFET immediate gate terminal $G^{'}$. A gate leakage current tunneling from gate to drain and gate to source goes through R_G and increase the pMOSFET effective gate voltage at point $G^{'}$. The voltage dropping on R_G presents the threshold voltage shift due to NBTI. Gate tunneling

current was modeled with two voltage controlled current sources, which follow the form of a power law relation as: $I = KV^p$. This NBTI circuit model structure is shown on Figure 3.

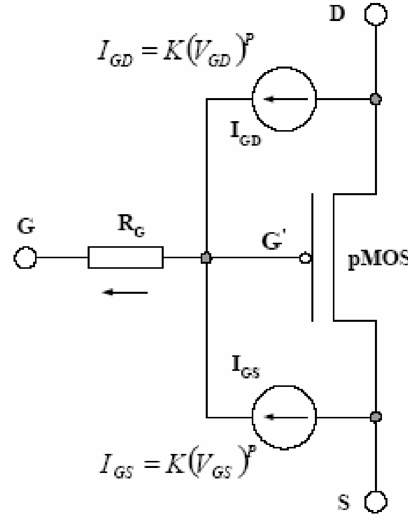


Figure 3: MaCRO NBTI circuit model

In this model, R_G is a voltage dependent resistance due to the fact that gate leakage currents are dependent on the voltage. R_G is also a time dependent resistance because voltage drop across R_G at any specific *t*, which is related to time-dependent threshold voltage shift $\Delta V_t(t)$. According to [27], both gate to drain leakage current and the gate to source leakage current are able to expressed as $I_{GD} = K(V_{GD})^p$ and $I_{GS} = K(V_{GS})^p$ respectively, where p is set to 5, and the default value of K is 3×10^{-6}. From this circuit model, we can get the PMOSFET threshold voltage shift due to NBTI effect by the following equations:

$$V_{R_G}(t) = V_{G'} - V_G = \Delta V_G(t) = (I_{GD} + I_{GS})R_G \tag{2.11}$$

$$R_G = \frac{\Delta V_{max}}{KV_{GD}{}^p + KV_{GS}{}^p}[1 - e^{-(\frac{t}{\tau})^\beta}] \quad (2.12)$$

$$\Delta V_G(t) = \Delta V_t(t) \quad (2.13)$$

The details of how to apply this NBTI circuit model in SPICE simulation environment are given in [26].

2.2 Charge Trapping Effect

2.2.1 Introduction

It is well known that the current leakage through the silicon dioxide layer of a gate increases exponentially with the decrease of layer thickness. When the thickness of gate dielectric is very thin, specifically oxide thickness (t_{ox}) below 1.6 nm, the transistor leakage current increases remarkably [28]. This condition causes the transistor to change from totally "on" and "off" state to "on" and "leaky off" behavior. While high κ materials (mostly Hf-, Zr-, and Al-based) can help solve gate leakage problems with leading-edge processes to retain the standard MOSFET design. They have a moderately high dielectric constant (~8 to 30), depending on Hf content. But, there still are some remaining challenges [28, 29]. Firstly, significant hysteresis is a result of transient threshold voltage instability, which contributed from fast charging and discharging of the trapped carriers causes. This prevents high-frequency switching operations. Second, threshold voltage instability due to comparatively

stable trapping is a serious concern for the long-term operational performance of MOS devices. Third, trapping has the most detrimental effect on the degradation of the channel carrier mobility in high-k MOSFETS. Fourth, bulk trapping distorts the internal electric field and modifies threshold voltage and leakage characteristics. Fifth, defects responsible for trapping also assist in tunneling, which gives rise to the high gate current and inversely affects the advantages of high-k oxides. Sixth, charging at trap levels, specifically near the metal gate electrode/high-k interface, modifies the gate Fermi level. This gives rise to gate Fermi level pinning, which results in higher threshold voltage. Therefore, it is obvious that studying the charge-trapping-induced degradation of the high-k gate stacks is a key to understand its reliability as it is the ultimate limiting factor for its long-term performance. One important factor attributed to those issues is trapping of charges in the pre-existing traps inside the high-k gate dielectrics [30]. For high-k gate stacks, in good agreement with the observations were made by Yong of charge trapping occurring mostly within high-k film rather than only at the interface [31]. When the transistor is turned on, some of the channel carriers will be accumulated in the gate dielectric due to the vertical electrical field, resulting in a shift of threshold voltage and a reduction in drain current. Charge-trapping characteristics can also be investigated by hot carrier stress (HCS), positive/negative bias temperature instability (PBTI/ NBTI), stress-induced leakage current (SILC), etc. [27]. As far as high-k gate stacks are concerned, this can be achieved by understanding the atomic structure and electronic properties of the defects within the high-k dielectrics, electronic structure of the

gate stacks, and carrier transport and kinetics under different oxide electric field conditions in conjunction with the critical analysis of the results observed from the electrical experiments. It is, therefore, the key to understand the source of channel mobility degradation and device reliability issues by fully understanding the charge-trapping mechanism.

2.2.2 Charge Trapping Phenomena and Models

After the transistor is turned on, the threshold voltage of the transistor increases as a result of interface charges trapped in the gate dielectric. Therefore, channel mobility slows down, the drain current decreases. Figure 4 illustrates charge trapping at the SiO_2/HfO_2 interface and in the bulk of high-k film.

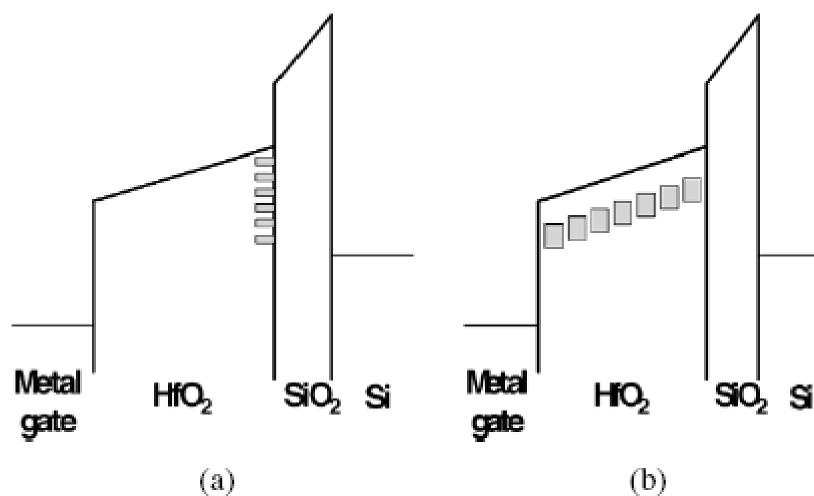


Figure 4: Charge Trapping (a) at the SiO_2/HfO_2 interface or (b) in the bulk of high-k film

It has been reported that both charge trapping and de-trapping times strongly depend on the composition of gate stacks, physical thickness of the interfacial SiO_2 layer and high film, as well as process techniques [32]. The time scale varies from less than a microsecond to tens of milliseconds [33]. The de-trapping of the charges is also strongly dependent on both gate voltage and polarity. The wide dynamic range of charge trapping and the voltage dependent trapping and de-trapping make it very difficult to use one type of characterization technique, especially DC techniques, to get a complete picture of what is going on inside the stacked gate dielectric. A faster measurement technique is desirable to capture the dynamic nature of the charge-trapping behavior.

As mentioned before, the main charge trapping induced device instability issue is threshold voltage shift, which follows a logarithmic dependence with time. Assuming the interface traps have continuous distribution, the threshold voltage modeled as a function of time is given by [34, 35]:

$$\Delta V_t(t) = \Delta V_{\max}(1 - \exp(-(t - \tau_0)^{\beta})) \tag{2.14}$$

where $\Delta V_{\max}$ is the maximum shift in threshold voltage. τ_0 is the peak of continuous distribution time. β is a measure of the distribution width.

Assuming a Fermi-derivative energy distribution of the traps, the simple exponential model of ΔV_t is [35]:

$$\Delta V_t(t) = \frac{\Delta V_{max}}{1 + (\frac{t}{\tau})^{\frac{-kT}{\sigma_{E_a}}}} \tag{2.15}$$

where ΔV_{max} is the maximum shift in threshold voltage, τ corresponds to the characteristic detrapping time, k is the Boltamann constant, T is the temperature and σ_{E_a} is the standard deviation of the activation energy.

2.2.3 Measurement Techniques

Currently, there are two methods to characterize the charge trapping and de-trapping effect. One is DC Characterization Techniques, and another is the Dynamic measurements, which contains Single-Pulsed Technique, Multiple-Pulse Technique and Charge pumping Technique.

For DC Characterization Techniques, there are several ways to detect charge-trapping phenomena. An easy and commonly used method is to use a double sweep gate voltage in either DC $I_d - V_g$ or C-V measurements. These techniques involve ramping gate voltage back and forth while drain current or gate capacitance is measured. Charge trapping inside the gate stacks can be clearly indicate, as hysteresis is seen on the resulting I-V or C-V curves. However the problem of these techniques is that the hysteresis is strongly dependent on measurement time, which is not easy to control in real operation due to its strongly

instrumental dependence. Even if test speed is controlled, there is still no model to quantify how much charge is really trapped in the gate during the test. Furthermore, most fast transient trapping will be lost in the DC measurement.

Another frequently cited DC measurement for quantifying trapped charges is to inject charges intentionally into the gate using DC stress, then measure the flat band voltage or threshold voltage shift using the C-V or I-V method [37]. The problem with this technique is that there is a typical transition period when there is no applied voltage between DC stress and I-V or C-V, or the voltage is very low in comparison with the stress voltage condition. As we know, when the stress voltage is off, the charges trapped in the gate can de-trap in as few as tens to hundreds of microseconds. In this case, only a fraction of the total trapped charges are measured due to relaxation during the transition between the stress and measure intervals, even though the DC characterization is quickly to screen the charge trapping effects on the characteristics of MOS device.

Overall, a static technique is not applicable to fast transient, and the dynamic measurement techniques are introduced to study the threshold voltage shift at shorter time scale in the following content. When the faster pulse is used, hysteresis is eliminated due to insufficient response time during charges trapping.

Over the past few years, many other methods have been developed [34, 35, 38, 39] for capturing the fast transient behavior of charge trapping. One of the most popular measure methods is Single Pulse Chare Trapping (SPCT) measurement. There are two different test configurations for a SPCT measurement shown in Figure 5. In each measurement setup, a single pulse is put to the gate of the transistor and its drain is biased at a certain voltage. The drain will shift caused by charge trapping effect between the gate pulse rise up and gate pulse fall down. This change in drain current, resulting from the gate pulse, appears on the digital oscilloscope.

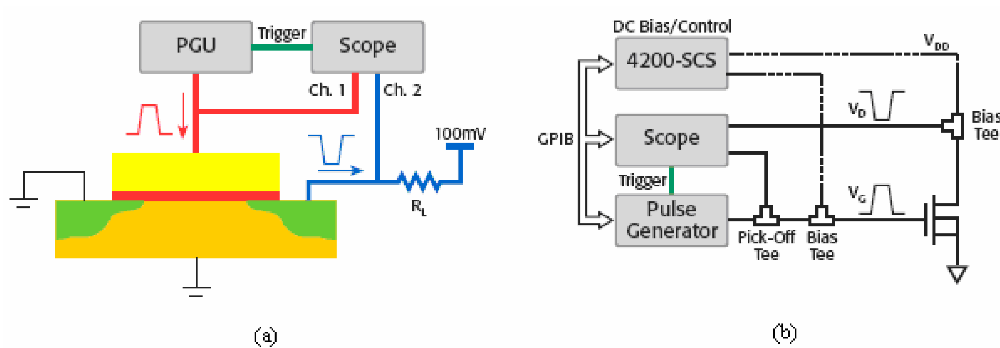


Figure 5: Two different pulse *I-V* test setups to study transient charge trapping inside high gate stack

The difference between these two configurations is that the one in Figure 5b has much higher bandwidth than the one in Figure 5a. Therefore, it can capture much faster pulse responses

(down to tens of nanoseconds). Figure 6a and 6b shows an example of a pulse I-V measurement results with using setups from Figures 5a and 5b respectively.

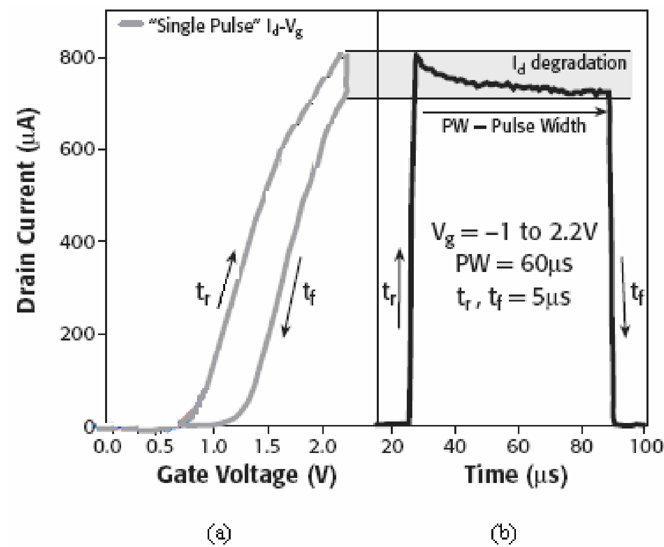


Figure 6: Single Pulse Charge Trapping measurements: a) the ultra-short ramped pulse I_d-V_g and slow "single pulse" pulse with hysteresis (DC result is shown as a reference), and b) corresponding slow pulse versus time illustrating an alternative approach to determine the degradation of I_d

It's clearly to see in Figure 6a that two traces in the t_r and t_f portions are not parallel, it is difficult to define the point at which hysteresis is measured. When the charge-trapping effect is significant, the more legitimate method is to use a fast pulse with short rise and fall times. Therefore, slower pulse measurements should only be used for high-ķ devices with relatively

low charge-trapping effects. However, in Figure 6b, the pulse I_d versus time to be plot, and an evaluation of the pulse width portion of I_d (where I_d degrades) can be used to quantify trapped charge [36, 40]. This measurement method produces $I_d - V_g$ values by using a single pulse per point of less than 100ns.

A well-configured single pulse is applied to the gate of transistor for charge trapping and de-trapping behavior is given in Figure 7.

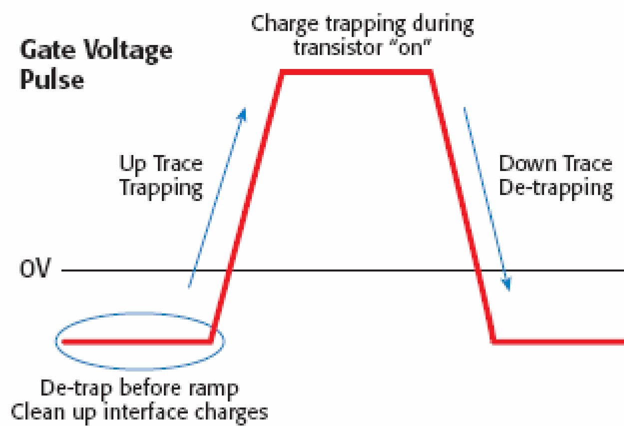


Figure 7: Trapping and de-trapping in single gate voltage pulse

Normally, the gate pulse starts in a position which discharges the gate capacitor before the voltage ramp begins. This is to clean up any residual charges that might be trapped in the gate. Then, during the rise time of the voltage ramp, the corresponding drain current response is captured, allowing a $I_d - V_g$ curve to be formed. During the plateau of the pulse, the

transistor is turned on, and some of the channel carriers might be trapped in the gate, which changes the threshold voltage and causes the drain current to drop. During the fall time of the pulse, another $I_d - V_g$ curve is formed. The shift of the two $I_d - V_g$ caused by charge-trapping effect will be formed. However, if the pulse rise time is fast enough so that there is no charge trapping, then the $I_d - V_g$ curve represents the intrinsic behavior of the transistor.

From these transient analyses methods, it is expected that the interface states trapping and the resulting degradation may be negligible under a high-speed circuit operation condition.

2.3 MOSFET –Devices

2.3.1 Introduction

Since NBTI is for pMOSFETs, and charge trapping effect is for nMOSFETs (high-k dielectrics) to talk in this thesis, it's necessary to introduce some basic MOSFET knowledge firstly.

2.3.2 MOS Structure

Figure 8 shows a simplified structure of the n-channel and p-channel MOSFET devices. The gate was once made of metal but is now made of heavily doped polysilicon, which is separated by a thin dielectric from the substrate. Normally, the thin dielectric layer is made of

silicon dioxide. The current runs between drain and source through an inversion channel created when a voltage is put on the gate that is greater than the threshold voltage (for PMOS the gate source voltage is sufficiently negative). When inversion occurs electrons (or holes for PMOS) from the bulk are attracted to the gate, the inversion layer constitutes a conductive path ("channel") between drain and source. The value of V_g for the transistor turn on is called threshold voltage.

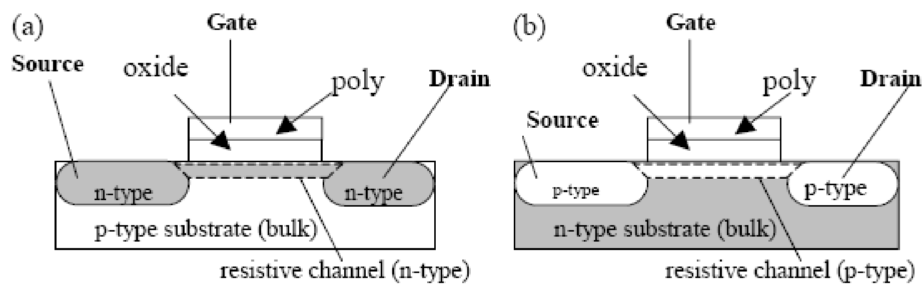


Figure 8: (a) Structure of a NMOS device (b) Structure of a PMOS device

2.3.3 MOS I/V Characteristics

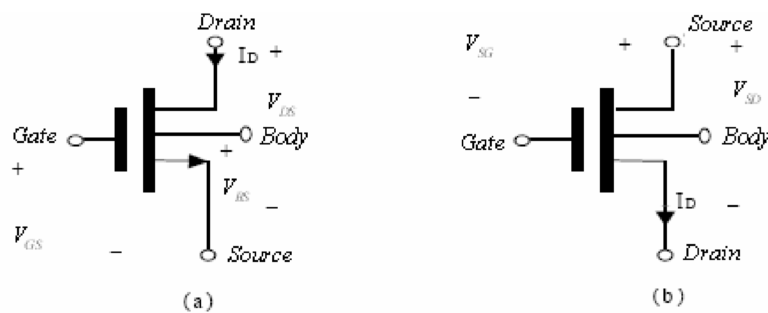


Figure 9: (a) Symbol for NMOS device (b) Symbol for PMOS device

MOSFETs can operate as current sources. And the current can be calculated in the two different work regions. According to the symbols shown in Figure 9, the equations of current are given by:

Drain current in linear region ($V_{DS} \le V_{GS} - V_{TH}$):

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{2.16}$$

Drain current in saturation region ($V_{DS} > V_{GS} - V_{TH}$):

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.17}$$

where μ, C_{ox}, W, L are the device mobility, the oxide capacitor, channel width and channel length respectively. These equations are the same for PMOS transistors but the polarity is changed for the variables.

CHAPTER THREE: NEGATIVE BIAS TEMPERATURE INSTABILITY IMPACT ON ANALOG CIRCUITS

3.1 Introduction

For NBTI degradation, the dominating work has been focused on the discrete transistor rather on the circuit performance degradation [6, 7, 9, 11]. Recently, more and more interest has been elevated to the impact of NBTI degradation effect on digital, analog and RF circuit performance degradation [15, 31, 41]. In the following section current mirrors and a two stage operation amplifier are employed to study NBTI induced analog circuit degradation.

Because the most serious NBTI effect is the PMOSFET threshold voltage shift, we sweep the threshold voltage parameter from -0.4056452 V (V_{tp0}) to -0.4556452V in p-channel device model under the Cadence Spectra simulation environment. The model of the devices simulated in those circuits is TSMC 0.18µm.

3.2 NBTI Effect on Current Mirror Circuits

3.2.1 MOSFET Current Mirror circuits

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current

constant regardless of loading, which is a basic block in CMOS IC design and has been used extensively in analog integrated circuit design. Conceptually, an ideal current mirror is an simple ideal current amplifier with unity current gain [43]. Figure10 shows a simple NMOSFET current mirror structure.

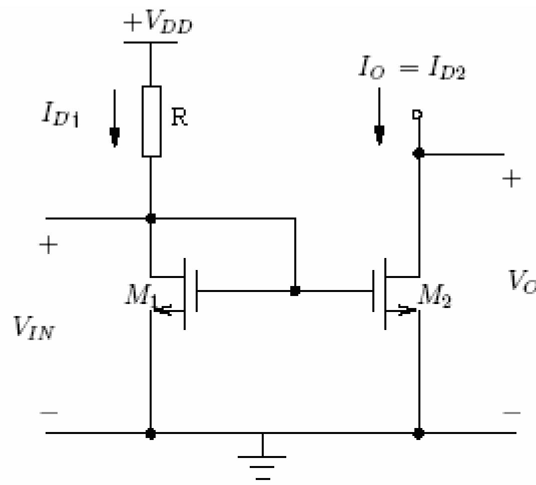


Figure 10: The basic current mirror schematic and symbol

The biasing current, I_{D1} and output current, I_o equation are given by:

$$I_{D1} = \frac{V_{DD} - V_{GS}}{R} = \mu_n C_{ox} \frac{W_1}{L_1}(V_{GS1} - \Delta V_{TH}) \quad (3.1)$$

$$I_{D2} = I_o = \frac{(W_2 / L_2)}{(W_1 / L_1)} I_{D1} \quad (3.2)$$

The output resistance of the current source is simply the output resistance of M_2, or defined by $r_{o2} = \frac{1}{\lambda I_o} = \frac{1}{\lambda I_{D2}}$, where λ is the sum of the mobility modulation and channel length

modulation parameters for n- and p- channel MOSFETs, and the value is approximately $0.06V^{-1}$. For analog design, it's extremely important to keep the output resistance as high as possible. It is also desirable to reduce the effects of channel length and mobility modulation. Normally, the design rule is to set the length of the MOSFETs used in analog applications as 2~5 times the minimum draw gate length. If we assume and design for a specific gate-source voltage V_{GS} (or V_{SG} for the p-channel), it's simplify to design the analog circuit. Setting V_{GS} close to the threshold voltage results in very large devices, while setting V_{GS} significantly larger than the threshold voltage causes the transistor to enter the triode region too early. An acceptable difference between V_{GS} and V_{TH}, sometimes referred to as the excess gate voltage, ΔV, is several hundred millivolts. The V_{GS} is normally adjusted to obtain a desired characteristic, such as minimum voltage across the current source [43]. The cascode connection of basic current mirror is show in Figure 11.

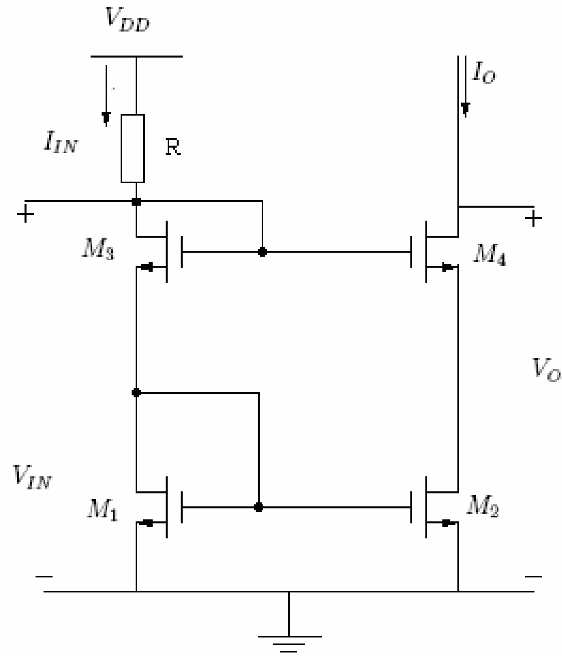


Figure 11: Cascode current source, showing that the minimum voltage output is $2\Delta V + V_{TH}$. M1 and M3 are wired as diodes and each have a voltage drop of $\Delta V + V_{TH}$ across the drain-source junction

This configuration is used to increase the output resistance of a current source. The output resistance of the cascode current mirror can be determined using the small-signal models, and which equation is given by $R_o = r_o(1 + g_m R) + R \approx (1 + g_m R)$, where $r_o = r_{o2} = r_{o4}$, $g_m = \sqrt{2\beta I_D}$ [43].

3.2.2 Simulation Methods, Results and Discussion

As mentioned before, current mirror is a constant current biasing scheme. Drifts in the bias currents can cause a significant deviation in the performance of an analog circuit. In this section three different current mirror constructions with pMOSFETs are presented to analyze their NBTI performance. In all three sample circuits, the biasing currents are designed with 200 μA, all the transistors are worked in the saturation region, and the value of V_o in each circuit is adjusted to pull a current equal to I_{bias}.

The circuit in Figure 12 is a simple current mirror circuit, which is used in applications where a very high-output resistance is not deeded. Figure 13 shows the simulation results.

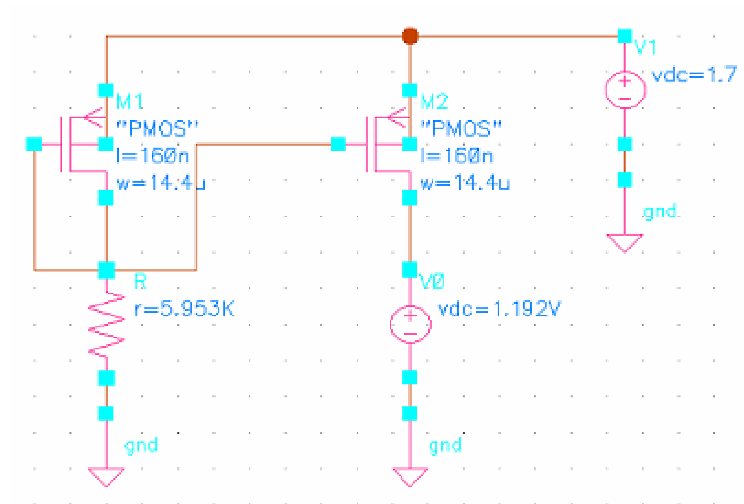


Figure 12: Simple current mirror circuit with values

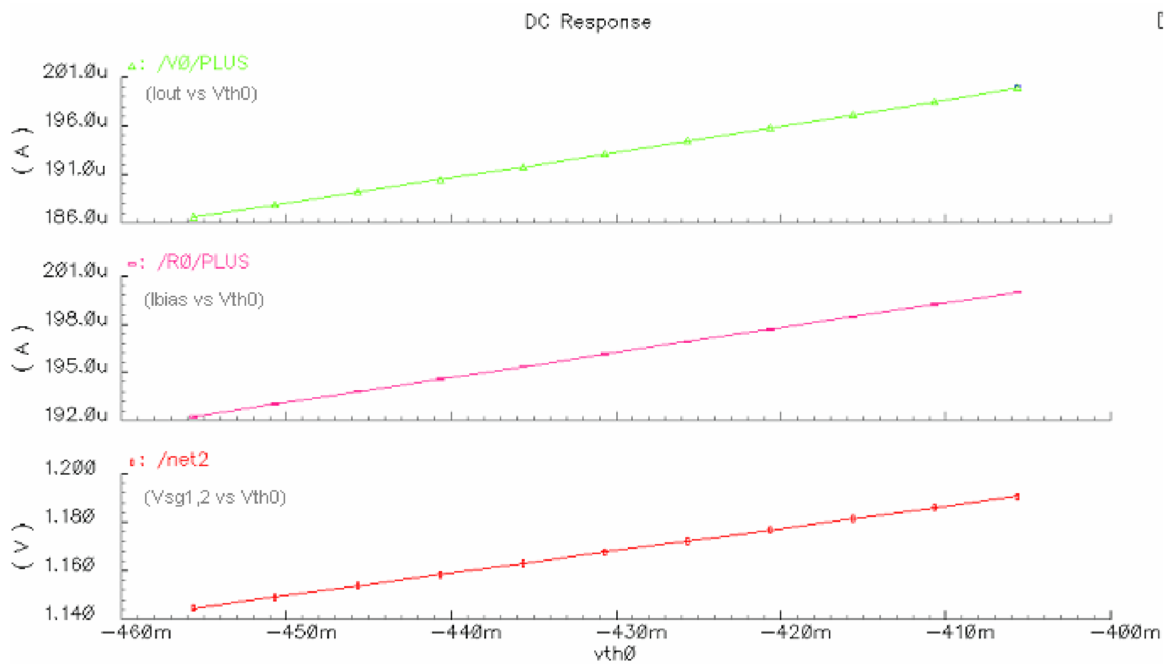


Figure 13: DC sweep simulation results

In Figure 12 as the two transistors M1 and M2 undergo identical gate stress voltage, ΔV_{tp} will vary identically for both of them. Shown in Figure 13 the output voltage, biasing voltage and the gate voltage of M1 and M2 are all decreased along with the absolute value of threshold voltage increase in the pMOSFETs.

Figure 14 shows a cascode current mirror with higher output impedance.

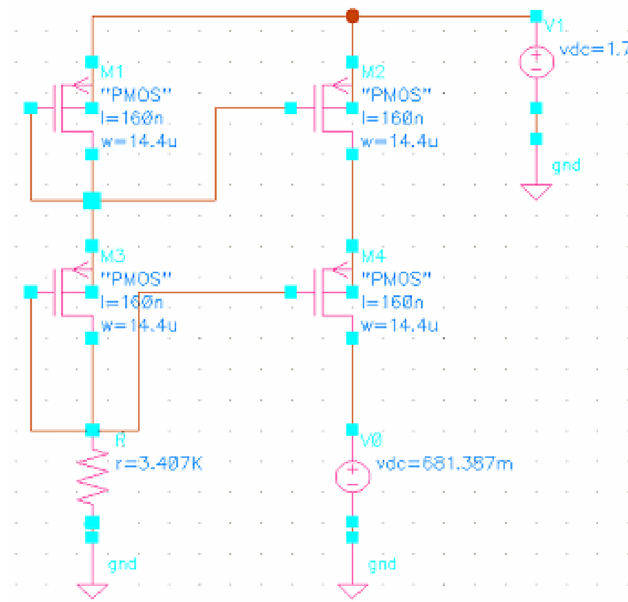


Figure 14: Cascode current mirror circuit with values

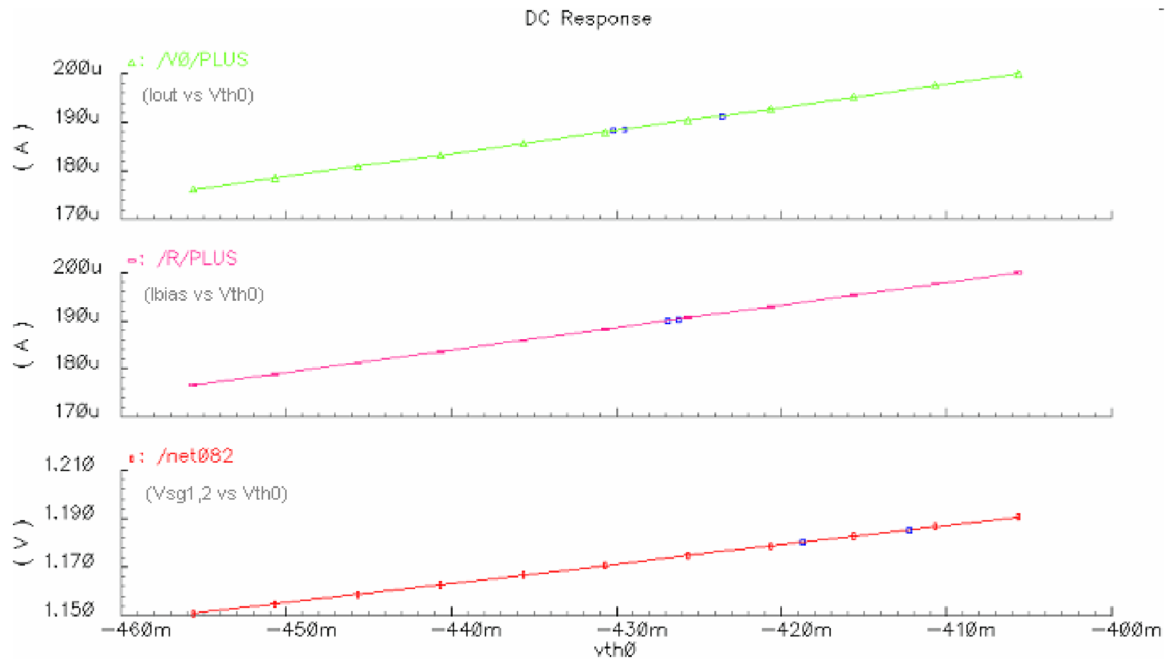


Figure 15: DC sweep simulation results of cascode current mirror circuit

In Figure 14 as the four transistors undergo identical gate stress voltage, ΔV_{tp} will vary identically for M1~M4. Similarly, after simulation, Figure 15 shows that the output voltage, biasing voltage and the gate voltage of M1~M4 are all decreased along with the absolute value of threshold voltage increase in the pMOSFETs also.

A wide-swing current mirror biasing circuit and the simulation results are showed in Figure 16 and Figure 17 respectively.

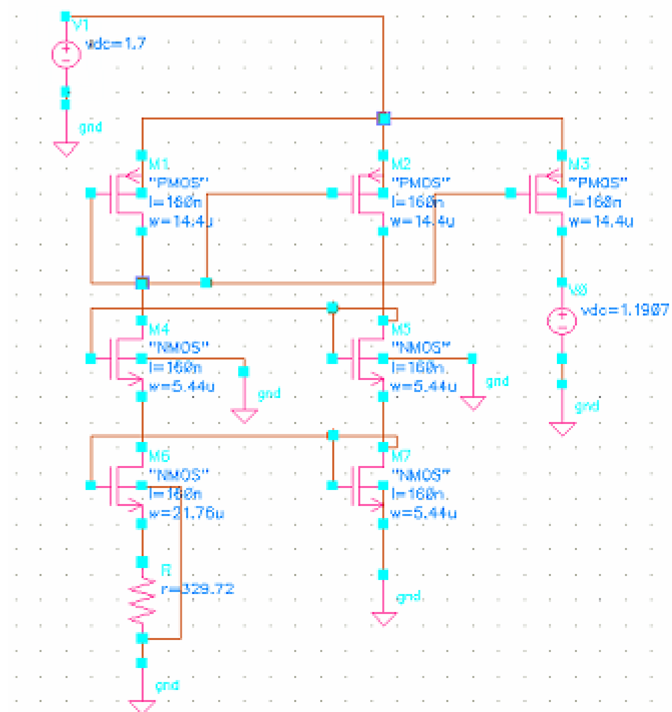


Figure 16: Wide-swing current mirror with values

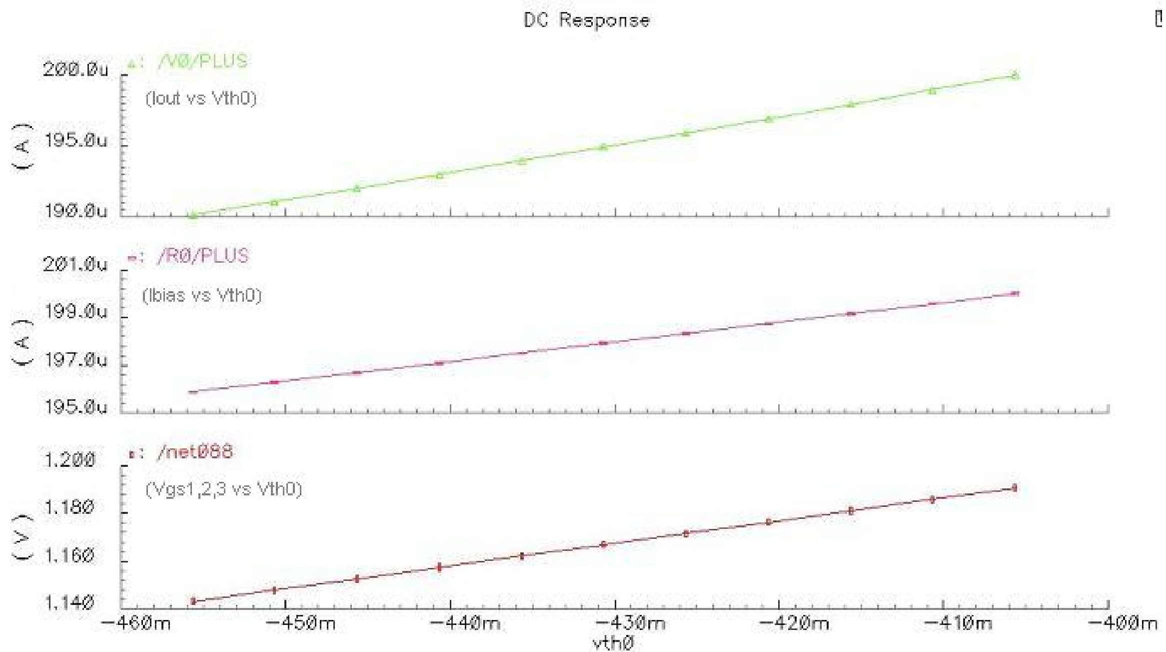


Figure 17: DC sweep simulation results of wide-swing current mirror

The circuit in Figure 16 is a wide-swing current mirror with a constant g_m biasing circuit. It is used in applications which the stable feedback transconductances are required [44]. In this circuit, a positive feedback is always maintained to match all the transconductances to the conductance of a resistor. Because of this reason, as long as the resistance is constant, the bias currents are maintained at a constant value irrespective of the variations in threshold voltage, temperature, and supply voltage.

Figure 17 presents the variation of currents and gate voltage in the current mirror circuits [shown in Figure 16] as a function of NBTI-induced threshold voltage increase. Similar with

the preceding two current mirror simulation results, output current, biasing current and output voltage are decreased. In Figure 17, ΔV_{tp} will vary identically for M1~M3.

Figure 12, Figure 14 and Figure 16 show that the output current, biasing current and gate voltage of p-channel devices in the three current mirrors shown in Figure 13, Figure 15 and Figure 17 respectively are all shift due to NBTI induced threshold voltage degradation. Those above simulation data are summarized in the Table1.

Table 1 Experimental data of output current, biasing current, and p-channel device gate voltage degradation due to NBTI effect in three different current mirror circuits

ΔV_{tp} (V)	simple current mirror shown in Figure 12			Cascode current mirror shown in Figure 14			Wide-swing current mirror shown in Figure 16		
	I_{out} (μA)	I_{bias} (μA)	$V_{sg1,2}$ (V)	I_{out} (μA)	I_{bias} (μA)	$V_{sg1,2}$ (V)	I_{out} (μA)	I_{bias} (μA)	$V_{sg1,2,3}$ (V)
-0.4056452	200	200	1.191	200	200	1.191	200	200	1.191
-0.4106452	198.5	199.2	1.186	197.6	197.6	1.187	199	199.6	1.186
-0.4156452	197.1	198.5	1.181	195.2	195.3	1.183	197.9	199.2	1.181
-0.4206452	195.8	197.7	1.177	192.8	192.9	1.179	196.9	198.7	1.176
-0.4256452	194.4	196.9	1.172	190.4	190.6	1.175	195.9	198.3	1.172
-0.4306452	193.1	196.1	1.168	188	188.2	1.171	194.9	197.9	1.167
-0.4356452	191.8	195.4	1.163	185.6	185.9	1.167	194	197.5	1.162
-0.4406452	190.5	194.6	1.158	193.3	183.5	1.163	193	197.1	1.157
-0.4456452	189.2	193.8	1.154	180.9	181.2	1.159	192	196.7	1.153
-0.4506452	187.9	193	1.149	178.5	178.9	1.155	191.1	196.3	1.148
-0.4556452	186.6	192.2	1.144	176.2	176.6	1.151	190.1	195.9	1.143

In Figure 18 we compare the output current instability performance of the three different types of current mirror circuits shown in Figure 12, Figure 14 and Figure 16. As shown in Figure 18, the simple current mirror [Figure 12] shows the middle drift (6.7%) in the output

current due to NBTI-induced degradation, for the same amount of NBTI-induced degradation , the cascode current mirror [Figure 14] shows the maximum drift (11.9%) in the output current, while the constant biasing circuit [Figure 16] shows the least degradation (4.95%). Those drift data can also be calculated from Table1. The highest degradation in the cascode current mirror can be explained by considering that there are two diode connected transistors in series and the change in voltage across the biasing resistor is a result of change in the threshold voltage of two transistors (M1 and M3). The least degradation observed in the constant biasing circuit is a result of the positive feedback, which takes care of the variation due to NBTI.

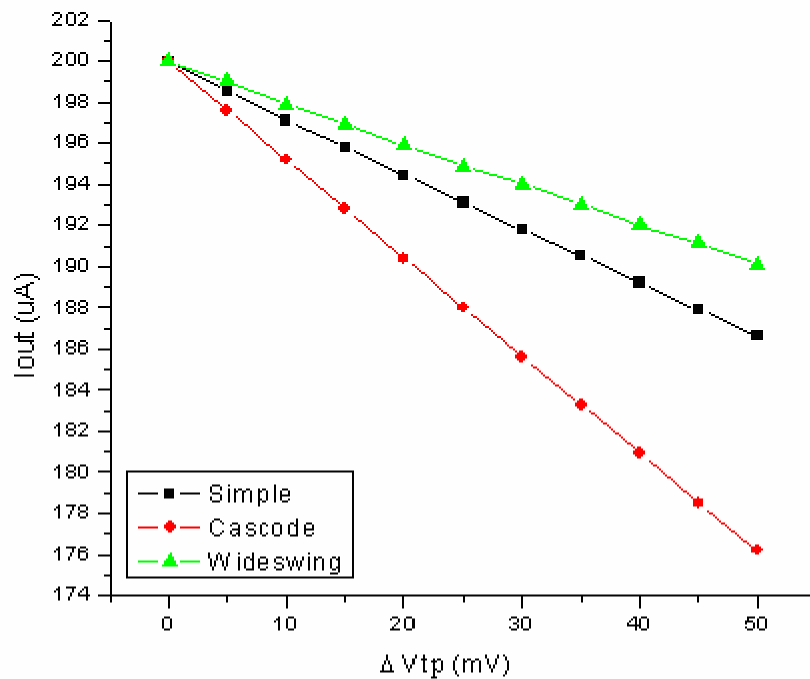


Figure 18: Comparison showing the drifts in output currents as a function of ΔV_{tp}

Figure19 shows the operating current (including output current and bias current) variation of those three different current mirror circuits under the same amount of NBTI-induced threshold voltage degradation.

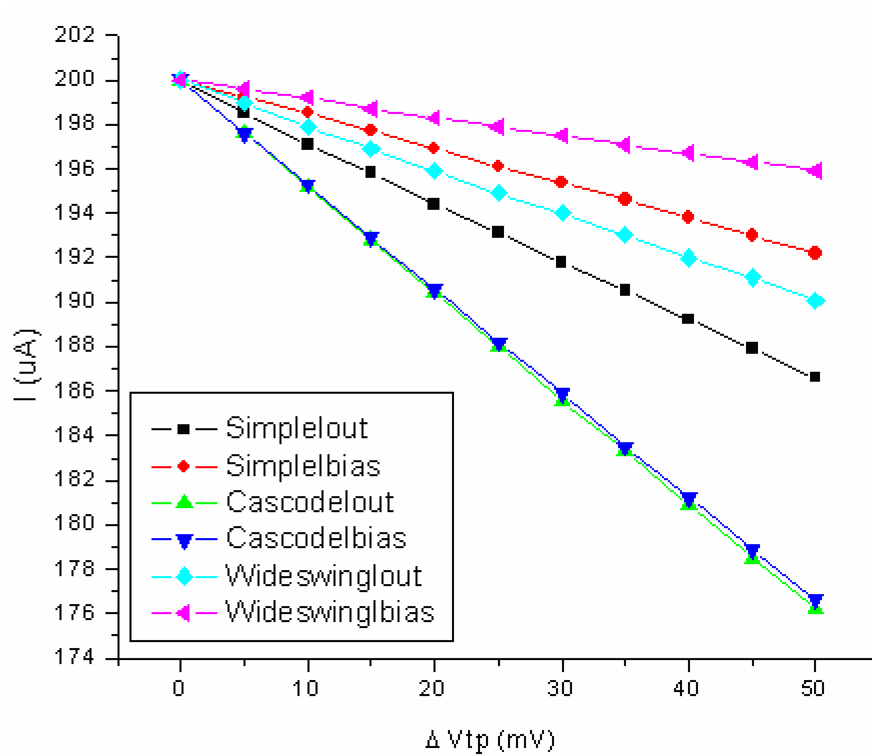


Figure 19: Drifts in operating currents

Shown in Figure 19, variation in the biasing currents can cause drift in the output characteristics, which agreed with the current mirror definition introduced before. And, it's clearly to see that under the same amount of variation due to NBTI, different current mirror configurations behave differently and hence must be chosen depending on the application.

3.3 NBTI Effect on Operation Amplifier

3.3.1 Two Stage Operation Amplifier Circuit without Buffer

The operation amplifier (op-amp) is a fundamental building block in analog integrated circuit. The first stage of a two stage operation amplifier is a differential amplifier, which is followed by another gain stage, and then an output buffer. If the op-amp drives a small purely capacitive load, the output buffer is not used. Otherwise, if the op-amp is intended to drive a resistive load or a large capacitive load or both of them, the output buffer is used. The op-amps without buffer is also called an operational-transconductance amplifier or OTA since the output resistance typically is very high. Compared to unbuffered op-amp, the output resistance of buffered op-amps is low [43].

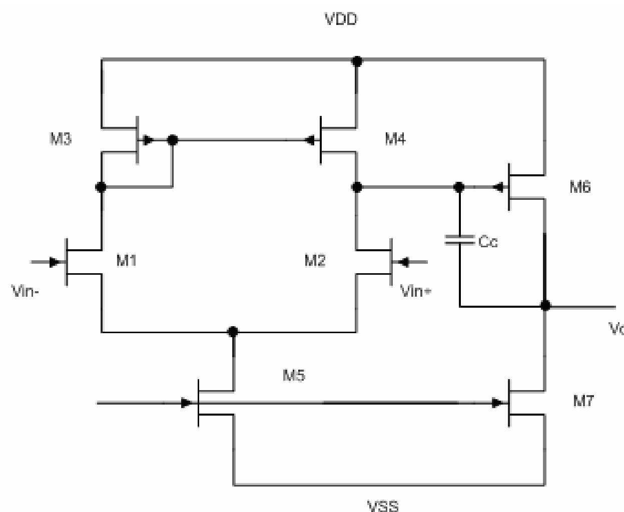


Figure 20: Schematic of an unbuffered CMOS two stage-op amp with n-channel input pair, which combines the two stages – the differential stage and inverting stage

In Figure 20, based on the balanced quiescent conditions, transistor M1 and M2 must be hmatched, and M3 and M4 must also be matched. If the input is balanced, then the current that flows in M5 is split equally through M1 and M2. That is $W_1 / L_1 = W_2 / L_2$, $W_3 / L_3 = W_4 / L_4$ and $i_1 = i_2 = i_5 / 2$. The current that flows in M5 is mirrored to the output by the ratio of the sizes of M7 to M5, just as the current in M4 is ratioed to the output by the ratio of M6 to M4. This results from our assumption of perfectly balanced conditions, which means that the drain voltages of M4 and M3 are equal. Since the gate and drain of M3 are tied together, the drain voltage of M4 is essentially the gate voltage of M3, thus the current i_4 is mirrored to i_6 by the ratios of sizes of M6 to M4. The qualitative analysis leads to the following relationships: $i_7 = i_5[(W_7 / L_7)/(W_5 / L_5)]$, $i_6 = i_4[(W_6 / L_6)/(W_4 / L_4)]$. For balanced conditions, it is desired that $i_7 = i_6$, and from previous discussion, we know that $i_5 / i_4 = 2$, therefore $(W_6 / L_6)/(W_4 / L_4) = 2(W_7 / L_7)/(W_5 / L_5)$ [45].

For this desired balanced condition, the channel-length modulation effects are not accounted. In the real design when we consider the channel-length modulation issue, there will be some error in the output resulting from current mismatches. This error at the output is then reflected back to the input as a systematic offset. Certainly, there are other important consideration in the design of circuits, such as common-mode input range, gain etc..

Those important concepts and definitions for op-amps are explained below. Based on the unbuffered two stage op-amps circuit shown in Figure 20, some related equations are also given in the following section [43, 45]:

1. Gain. For practical op-amps, the voltage gain is finite. Typical range of gain for low frequencies and small signals is from 10^3 to 10^5 (60 to 100 dB). For linear relation between input and output voltage, the gain $A = V_o / (V_{in+} - V_{in-})$, which limited by V_o. The total gain for this op amp is multiply the differential-stage gain by the current-source inverter gain, which is $A_v = \frac{g_{m6}}{g_{ds6} + g_{ds7}} \times \frac{g_{m2}}{g_{ds2} + g_{ds4}} = \frac{2 g_{m2} g_{m6}}{I_5(\lambda_2 + \lambda_4) I_6(\lambda_6 + \lambda_7)}$. When designing the gain, the size and current in M1 (M2) have been fixed by other constraints, so the terms that can be designed to achieve proper gain are I_6 and W_6 / L_6.

2. Slew Rate (SR). Simply speaking, rate is a voltage rate limit of output, but normally slew rate is limited by the current-source capability of the first stage, which is generally determined by the maximum current available to charge or discharge a capacitance. For typical CMOS op-amp, slew rates range is 1 to 20V/µs. Here, the definition equation for the example circuit is $SR = I_5 / C_c$.

3. Offset Voltage. For an ideal op-amp, when $V_{in+} = V_{in-}$, $V_o = 0$. However, in real circuits, $V_{o,off} \neq 0$ will happen at the output for shorted inputs. Because V_o is related gain directly, it's conveniently described in terms of the input offset voltage $V_{in,off}$, defined as the differential input voltage needed to restore $V_o = 0$ in the real circuit. For MOS op-amps, the typical value of $V_{in,off}$ is ±2 to 10 mV. This effect can be modeled by a voltage source of value $V_{in,off}$ in series with one of the input leads of the op-amp.

4. Common-mode rejection ratio (CMRR), which is defined as A_D / A_C in linear units, or $20\log_{10}(A_D / A_C)$ in logarithmic units, where A_D is the differential gain and A_C is the common mode gain. $A_C = V_o / V_{in,c}$, where $V_{in,c} = (V_{in+} + V_{in-})/2$, which is common mode input voltage. $A_D = V_O / (V_{in+} + V_{in-})$, which is gain of op-amp. The typical values of CMMR for CMOS op amps are in the range of 60 to 80 dB. It's the larger the better, because the CMMR values decide how much noise op-amps can suppress.

5. Gain-bandwidth, $GB = \frac{g_{m2}}{C_C}$.

6. Unity gain Frequency (f_T). That is the frequency where the voltage gain of an op amp is 1 ($0\,dB$). It indicates the highest usable frequency. If the phase at f_T is larger than -180°, the system will be stable.

7. Phase Margin, which is defined as 180 plus the phase at f_T. The larger phase margin, the more stable the circuit. Usually, the phase margin is 60°.

In the real design, if the gain is too low or the power dissipation is too high, some design components should be adjusted. Each adjustment may require another pass through this design procedure in order to insure that all specifications have been met. Table 2 shows a best way to adjust circuit components to match requirement [45]. It shows the effects of various device sizes and currents on the different parameters generally specified.

Table 2 Dependence of the Performance of Figure 20 upon DC Current, W/L Ratios and the Compensating Capacitor

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Comp. Cap.
	I_5	I_7	W/L	L	W	L	(W_6/L_6)	W_7	L_7	C_C
Increase dc Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$				$(\uparrow)^{1/2}$			$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$								$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\uparrow$

3.3.2 Simulation Methods, Results and Discussion

The simulation structure of two stage CMOS operation amplifier with values is shown in Figure 21. And, the design parameter specifications of this two stage operational amplifier are listed in Table 3.

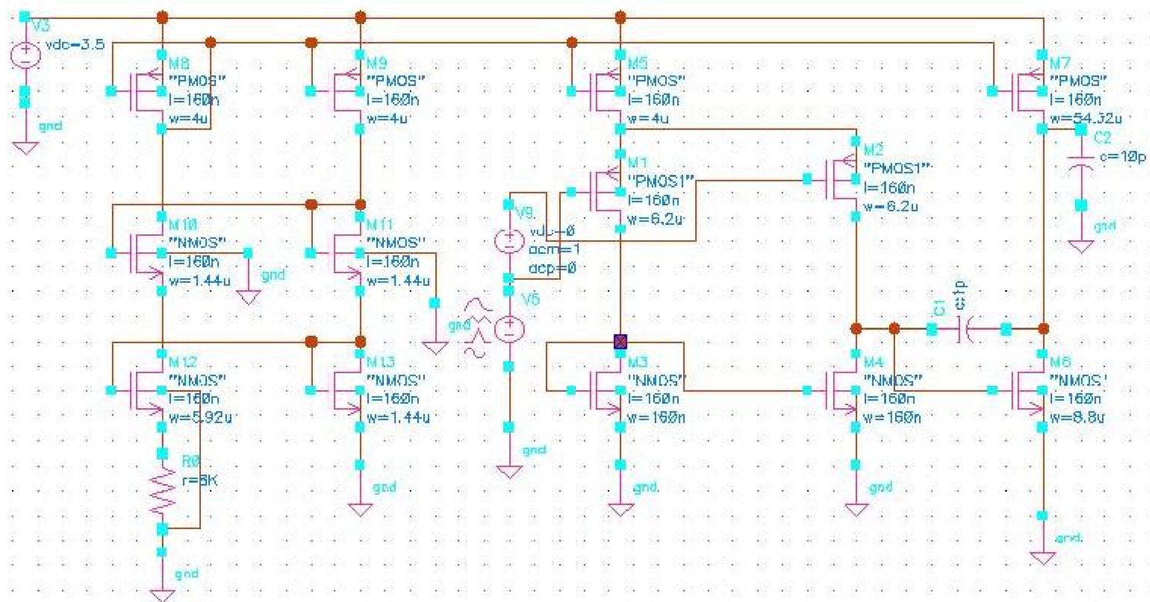


Figure 21: Two-stage CMOS operation amplifier structure with values

Table 3 Two stage CMOS operation amplifier parameter specifications. The circuit schematic is shown in Figure 21

Parameters	Value
DC Gain (A_{vo})	43.55dB
Unity Gain Frequency (f_T)	26.81MHz
Phase Margin	56.2°
ICMR	0.4-3.5V
Slew Rate	$23V/\mu s$

In this circuit, transistors M1 and M2 worked as input transistors. Since the transistors M8, M9, M5 and M7 undergo identical gate voltage stressing, during the simulation threshold voltage for them degrades identically. Figure 22 and Figure 23 show the Gain (A_{vo}) and Unity Gain Frequency (f_T) variations due to the NBTI-induced threshold voltage degradation respectively.

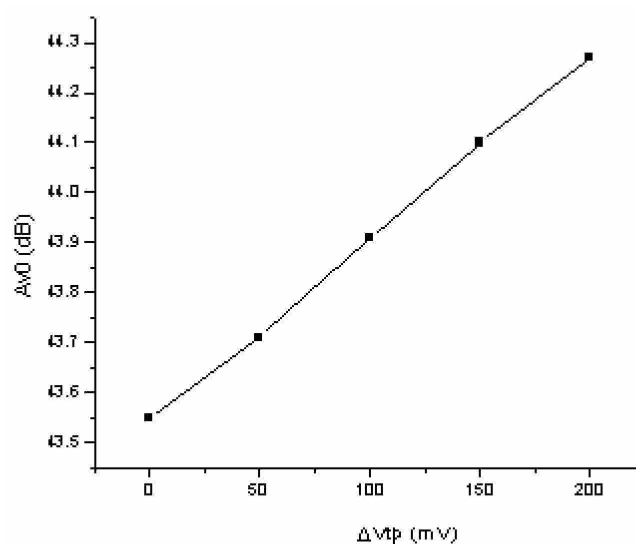


Figure 22: Variation in DC gain A_{vo} due to ΔV_{tp} degradation for the two stage operation amplifier shown in Figure 21

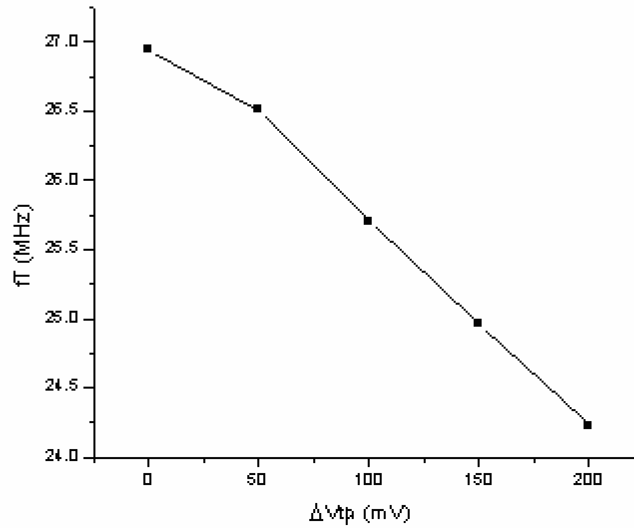


Figure 23: Variation in unity gain frequency f_T due to ΔV_{tp} degradation for the two stage operation amplifier shown in Figure 21

Table 4 Experiment data of DC Gain (A_{vo}) and Unity Gain Frequency (f_T) variance

Threshold voltage V_{tp} (V)	DC Gain $A_{vo}(dB)$	Unity Gain Frequency $f_T(MHz)$
-0.4056452	43.55	26.95
-0.4556452	43.71	26.51
-0.5056452	43.91	25.71
-0.5556452	44.1	24.96
-0.6056452	44.27	24.23

When threshold voltage changes from -0.4056452 V (V_{tp0}) to -0.6056452 V, the DC gain slightly increase 1.65%, and the Unity Gain Frequency decrease 10.09% following gain increase, which changes are not obvious. An increase in A_{vo} can be explained by equation $A_{v0} \propto \frac{1}{V_{sg} - V_{tp}}$ [43]. f_T is decreased according to the increase in A_{vo}, which can be explained by the definition of f_T introduced before.

In order to observe output current variations, a 1.75 V DC voltage (half of the V_{dd}) is put in the drain of M7. $I_{out} = 364.5\mu A$ at $V_{tp0} = -0.4056452V$, which there's no NBTI effect. When NBTI-induced threshold voltage degradation took place on the circuit, the variation curve of I_{out} is plotted in Figure 24.

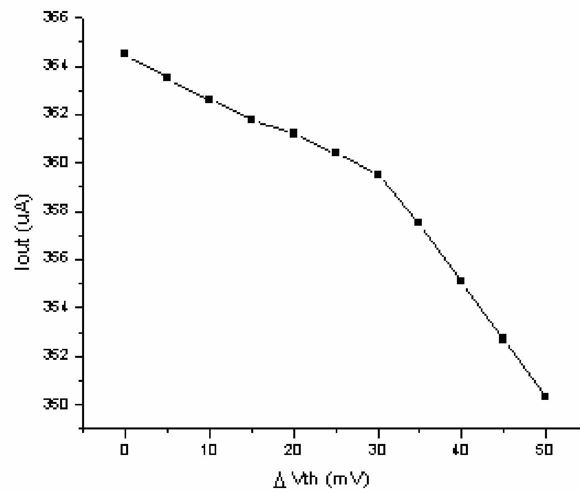


Figure 24: Variation in output voltage I_{out} due to ΔV_{tp} degradation for the two stage operation amplifier shown in Figure 21

When $V_{tp} = -0.4556452V$, I_{out} decreased to $350.3\mu A$. The rate of I_{out} degradation is only 3.84%, which resulted from the fact that wide-swing current mirror biasing circuit used in the op-amp keeps the biasing currents constant, according to adjust the gate voltage during the NBTI-induced threshold voltage shift. The experimental data are summarized in Table 5.

Table 5 The experiment data of Output Current (I_{out}) variance

Threshold voltage $V_{tp}(V)$	Output Voltage I_{out} (μA)
-0.4056452	364.5
-0.4106452	363.5
-0.4156452	362.6
-0.4206452	361.8
-0.4256452	361.2
-0.4306452	360.4
-0.4356452	359.5
-0.4406452	357.5
-0.4456452	355.1
-0.4506452	352.7
-0.4556452	350.3

3.4 Conclusion

In this chapter, we studied the analog circuits –three different current mirrors and one two-stage operation amplifier degradation due to NBTI induced threshold voltage instability. NBTI decreases the output and biasing currents of current mirrors. The output current of the two-stage operation amplifier decreases, and the DC gain of the operation amplifier increases, but the unity frequency gain decreases. Different analog configurations different degradation behavior and hence must be chosen depending on the application.

CHAPTER FOUR: CHARGE TRAPPING AND NBTI EFFECS ON DIGITAL CIRCUITS

4.1 Introduction

All the high-k dielectrics contain large amounts of fixed charge compared to SiO_2. The charge trapping responsible for the fixed charge are likely to occur within the bulk of the high-k film as well as at the interfaces of the high-layer with the gate electrode and the interfacial layer. The fixed charge within the high-k film shifts threshold voltage. Solving threshold voltage instability issue is a key to use high-k gate dielectric. Many researchers have reported the effects of charge trapping in high-k dielectrics and trapped charge induced threshold voltage instability [30, 31, 32].

In the following section, we will report the fast transient charge trapping effects in high-k devices on inverter and ring oscillator circuit operation. Later on, the same digital circuits are used to study NBTI effect. Before simulation, the converter and ring oscillator concept will be introduced briefly. The propagation delay will be used to characterize charge trapping effect and NBTI induced circuit degradation. Here, we are going to talk about charge trapping effect in high-k nMOSFETs, and NBTI in pMOSFTs. The model of the devices used in those circuits is TSMC 0.18µm. As mentioned before, both charge trapping effect and NBTI could cause the threshold voltage increase and mobility degradation.

4.3 Charge Trapping Effect on Inverter

4.2.1 Inverter

The CMOS inverter is a basic building block for digital circuit design. As Figure 25 shows that the inverter performs as a logical circuit of A to $\overline{A}$.

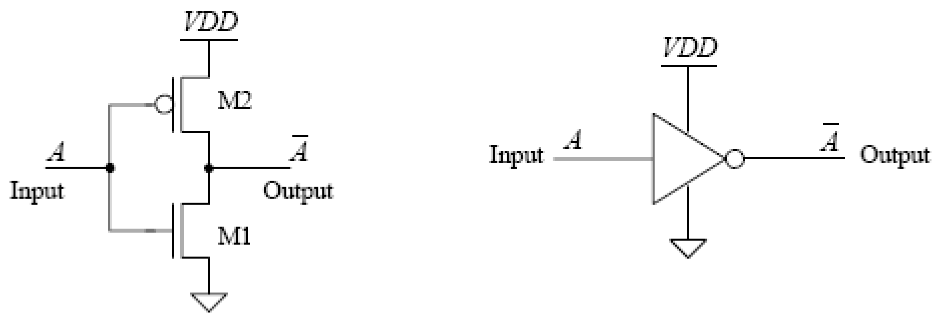


Figure 25: The CMOS inverter, schematic, and logic symbol

When the input to the inverter is connected to ground, the p-channel transistor M2 is open and n-channel transistor M1 is close, and the output is pulled to V_{DD} through M2. When the input to the inverter is connected to V_{DD}, the n-channel transistor M1 is open and p-channel transistor M2 is close, and the output is pulled to ground through M1. This CMOS inverter transfer characteristics is shown in Figure 26.

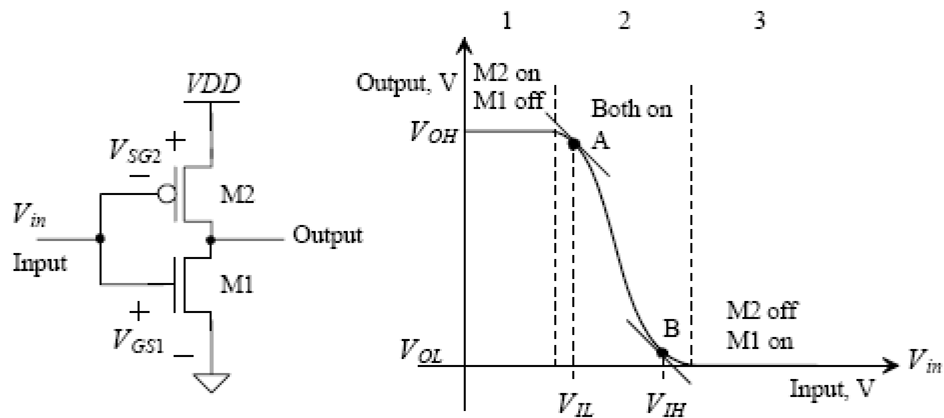


Figure 26: The CMOS inverter transfer characteristics

During the input from ground to V_{DD}, both of M1 and M2 are turn on. Ideally, this time should be zero. So, the input voltage between V_{IL} and V_{IH} do not define a valid logic voltage level. The time contributes inverter delay. And, the total intrinsic propagation delay of an inverter is given by $t_d = t_{PHL} + t_{PLH}$, which shown in Figure 27.

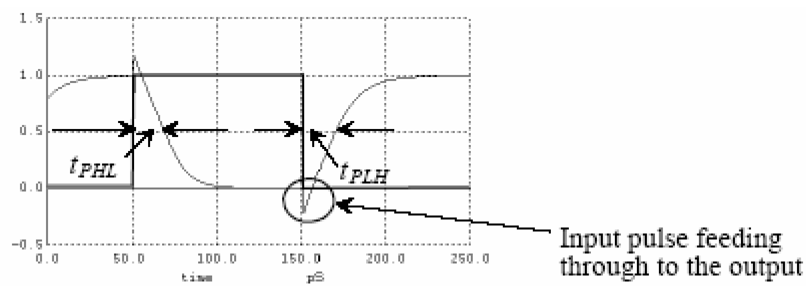


Figure 27: Intrinsic inverter delay

4.2.2 Simulation Methods, Results and Discussion

As mentioned before, the main instability caused by charge trapping effect is threshold voltage instability, which caused mobility degradation. In order to detect the circuit degradation due to charge trapping effect, we change the threshold voltage and mobility parameter in n-channel device model respectively during the simulation process. Here, $V_{tn0} = 0.3074534V$, and $\mu_{n0} = 270.095849 cm^2/Vs$. The propagation delay t_d is employed to qualify circuit degradation due to charge trapping. The inverter structure with values shown in Figure 28 is simulated using Cadence Spectra simulation tool.

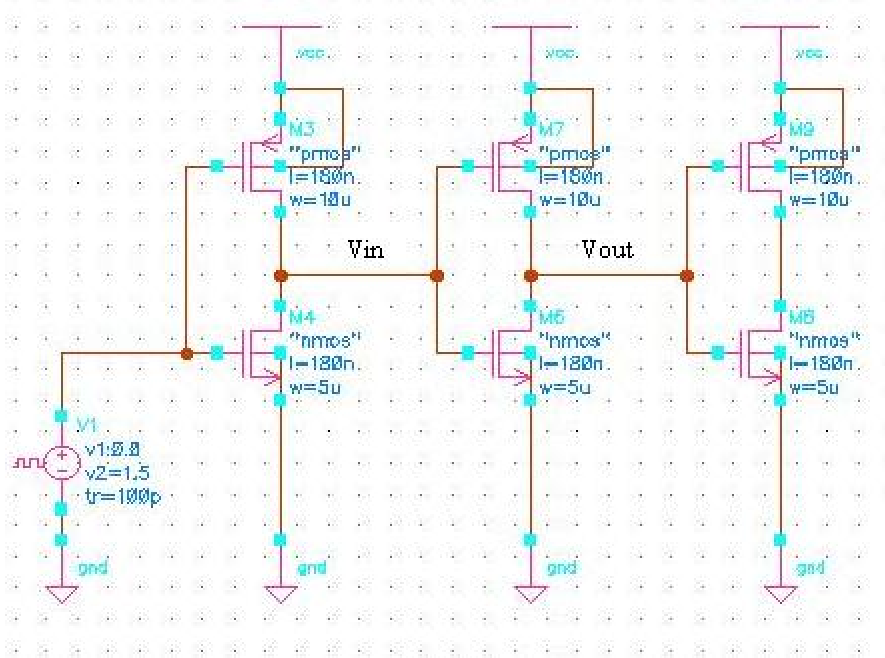


Figure 28: CMOS inverter structure with values used to simulate. $V_{dd} = 1.5V$, $V_{tno} = 0.3074534V$, $V_{tpo} = -0.4056452V$, $L = 180nm, W_n = 5\mu m, W_P = 10\mu m$. The values of pulse voltage source are $t_r = t_f = 100 ps, t_w = 2ns$.

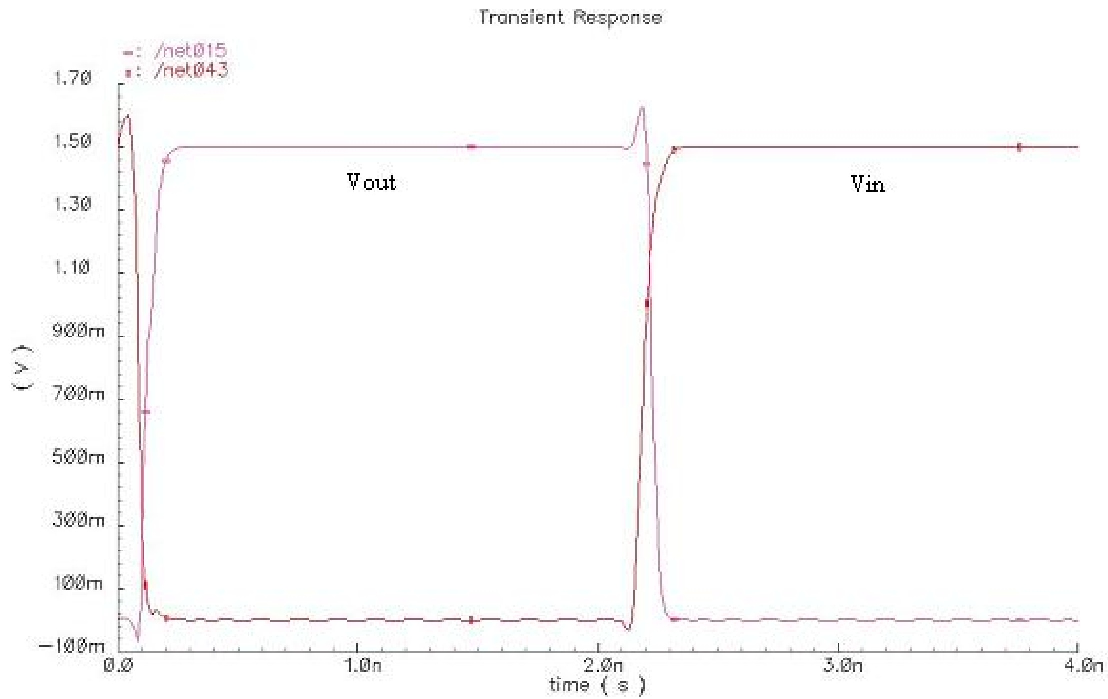


Figure 29: Simulation results of Inverter

Along with the threshold voltage of n-channel device increase, the time of inverter turn on and turn off is delay. When the mobility of nMOSFET decreased, the time is also delay. The experimental data are summarized in Table 6.

Table 6 The propagation delay of inverter due to Charge Trapping effect induced threshold voltage and mobility instability

$\Delta V_{tn}(mV)$	0	25	50	75	100
$t_d\ (ps)$	57.74	59.46	61.28	63.1	64.89
$\Delta\mu_n(cm^2/Vs)$	0	-15	-30	-45	-60
$t_d\ (ps)$	57.74	59.65	60.78	61.83	62.88

4.3 Charge Trapping Effect on Ring Oscillator

4.3.1 Ring Oscillator

There are two major types of implementation for CMOS oscillators: LC oscillators and ring oscillators. Here, we will introduce the ring oscillator shown in Figure 30, which consists of the odd numbers (*n*) of inverters in a positive feedback closed loop, and it's a self-start circuit.

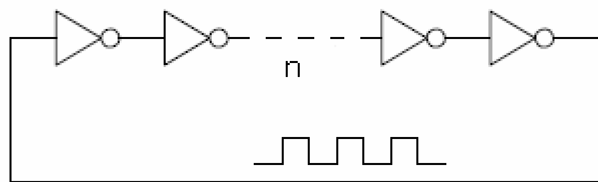


Figure 30: An *n* stage single-ended ring oscillator

Since each is an inverter it will just delay the signal with time t_d, and hence it will be referred to as a delay cell. The oscillation frequency is given by

$$f_{osc} = \frac{1}{n \cdot t_d} \qquad (4.1)$$

Where *n* denotes the number of stages used, and

$$t_{osc} = 1/f_{osc} = n \cdot t_d \qquad (4.2)$$

In general, the ring oscillator frequency is dependent on W (MOSFET channel Width), even much less than one would expect.

4.3.2 Simulation Methods, Results and Discussion

In this section, an 11 stage ring oscillator is used to analyze charge trapping effect induced circuit degradation. The simulation structure and results are shown in Figure 31 and Figure 32 respectively.

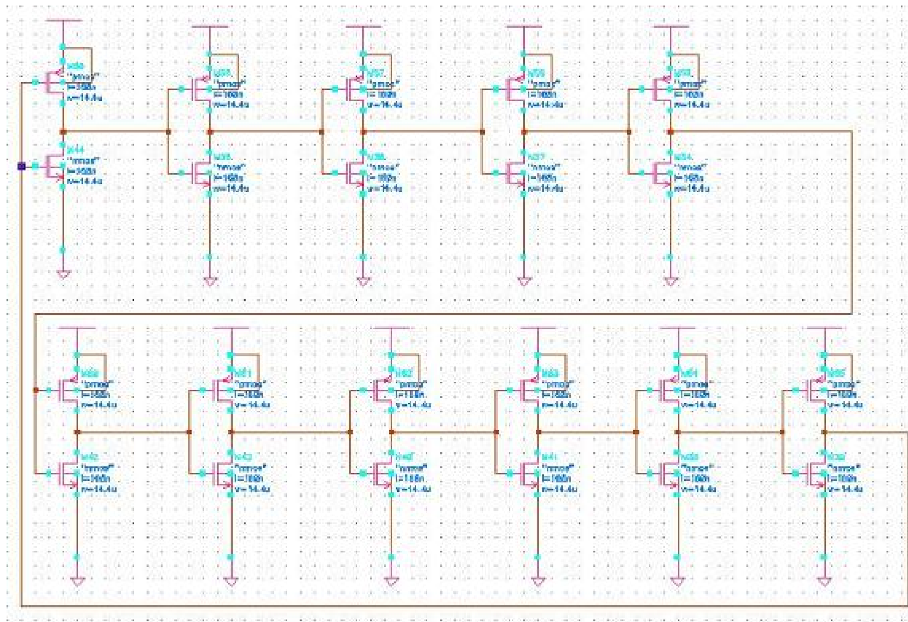


Figure 31: Schematic of the 11 stage ring oscillator. $V_{dd} = 1.5V$, $V_{tn0} = 0.3074534V$, $V_{tp0} = -0.4056452V$, $L = 180nm, W_n = 5\mu m, W_P = 10\mu m$.

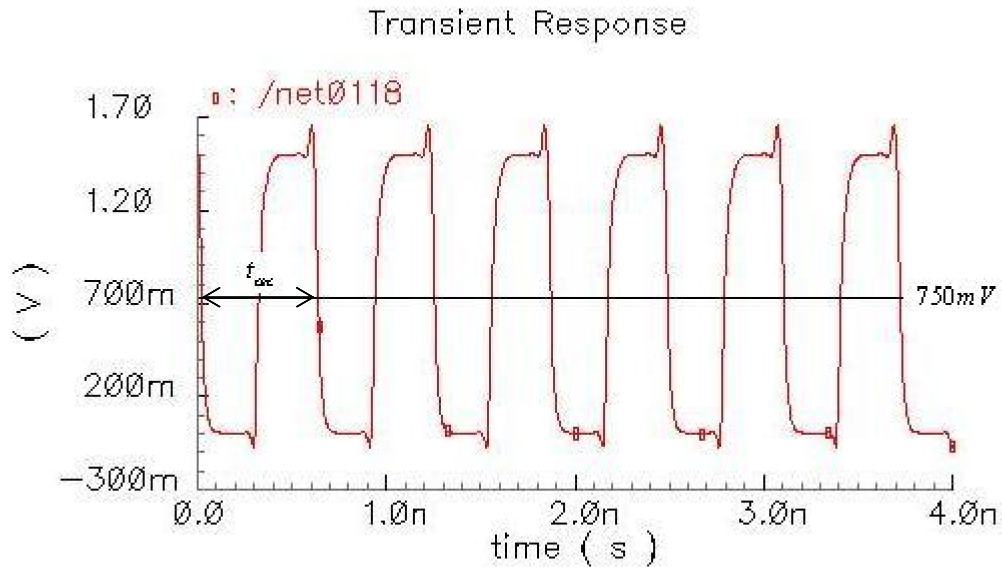


Figure 32: Simulation results of 11 stage Ring Oscillator

When the threshold voltage of n-channel device increase or the mobility of NMOSFET decreased, the period of ring oscillator, t_{osc} is also delay. The experimental data are summarized in Table7.

Table 7 The period delay of 11 stage Ring Oscillator due to Charge Trapping effect induced threshold voltage and mobility instability.

$\Delta V_{tn}(mV)$	0	25	50	75	100
$t_{osc}\ (ps)$	618.88	632.26	648.82	665.76	684.03
$\Delta\mu_n(cm^2/Vs)$	0	-15	-30	-45	-60
$t_{osc}\ (ps)$	618.88	626.65	637.58	649.64	663.08

Actually, Ring oscillator circuits are not suitable for the study of charge trapping mechanism because of its closed-loop cascade connection, because we cannot vary the input signal shape and frequency [47].

4.4 Comparison of Simulation Results

The same devices are used to build the single inverter and 11 stage ring oscillator. So, according to equation (4.1, 4.2), the ratio between t_{osc} and t_d should be 11. By calculating the simulation results of single inverter and the stage ring oscillator, we get the data presented in Table8.

Table 8 The ratio between t_{osc} and t_d under the same threshold voltage increase or same mobility decrease

$\Delta V_{tn}(mV)$	0	25	50	75	100
t_{osc}/t_d	10.72	10.63	10.59	10.55	10.54
$\Delta\mu_n(cm^2/Vs)$	0	-15	-30	-45	-60
t_{osc}/t_d	10.72	10.51	10.49	10.51	10.55

Seen from the Table that when the threshold voltage is increased from 0 to 100mV, or mobility is decreased from 0 to 60, the ratios between t_{osc} and t_d are all close to 11, which is agreed with theory.

4.5 NBTI Effect on Inverter and Ring Oscillator

Since NBTI is a reliability concern for p-channel transistors, we changed the threshold voltage and mobility parameters in the pMOSFET model to study the NBTI induced circuit degradation in the Cadence Spectra simulation environment. The device model is also TSMC 0.18 μm. The same inverter and ring oscillator structures (shown in Figure 28 and Figure 31) are used to study this phenomenon. The experiment data are summarized in Table 9.

Table 9 The experiment data of NBTI induced inverter and 11 stage ring oscillator degradation

$\lvert\Delta V_{tp}\rvert\ (mV)$	$t_d\ (ps)$	$t_{osc}\ (ps)$	t_{osc}/t_d
0	57.74	618.88	10.71
25	59.65	625.15	10.48
50	60.78	634.13	10.43
75	61.83	643.4	10.41
100	62.88	652.95	10.38
$\Delta\mu_p$	$t_d\ (ps)$	$t_{osc}\ (ps)$	t_{osc}/t_d
0	57.74	618.88	10.71
-15	61.02	654.63	10.73
-30	64.97	701	10.84
-45	69.08	775.06	11.21
-60	77.52	882.72	11.38

t_d is the propagation delay of the single inverter. t_{osc} is the period of the 11 stage ring oscillator. Both of them are increased along with NBTI induced $\lvert\Delta V_{tp}\rvert$ increase or $\Delta\mu_p$ degradation. Ideally, the ratio between the period of the 11 stage ring oscillator and the single

inverter should be equal to 11. The experiment data show that under the same degradation they are always keep around 11, which perfectly agree with theory.

CHAPTER FIVE: CONCLUSIONS

In this work, a simulation methodology is used to quantify the degradation at circuit level due to NBTI and charge trapping. The results in threshold voltage increase and the mobility decreases over time causing circuit instability and performance degradation

We study the analog circuits –three different current mirrors and one two-stage operation amplifier degradation due to NBTI induced threshold voltage instability. NBTI decreases the output and biasing currents of current mirrors. The output current of the two-stage operation amplifier decreases, and the DC gain of the operation amplifier increases, but the unity frequency gain decreases.

And, we also study the digital circuits –single inverter and 11 stage ring oscillator degradation due to charge trapping and NBTI induced threshold voltage increase or mobility decrease. The propagation delays of a single inverter and 11-stage ring oscillator are increased due to NBTI and charge trapping effect.

The general framework proposed in this thesis can also be extended for mapping other device-level reliability to the circuit performance degradations.

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