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DESIGN, CHARACTERIZATION AND COMPACT MODELING OF NOVEL SILICON CONTROLLED RECTIFIER (SCR)-BASED DEVICES FOR ELECTROSTATIC DISCHARGE (ESD) PROTECTION APPLICATIONS IN INTEGRATED CIRCUITS

by

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Major Professor:
Juin J. Liou
ABSTRACT

Electrostatic Discharge (ESD), an event of a sudden transfer of electrons between two bodies at different potentials, happens commonly throughout nature. When such even occurs on integrated circuits (ICs), ICs will be damaged and failures result. As the evolution of semiconductor technologies, increasing usage of automated equipments and the emerging of more and more complex circuit applications, ICs are more sensitive to ESD strikes. Main ESD events occurring in semiconductor industry have been standardized as human body model (HBM), machine model (MM), charged device model (CDM) and international electrotechnical commission model (IEC) for control, monitor and test. In additional to the environmental control of ESD events during manufacturing, shipping and assembly, incorporating on-chip ESD protection circuits inside ICs is another effective solution to reduce the ESD-induced damage. This dissertation presents design, characterization, integration and compact modeling of novel silicon controlled rectifier (SCR)-based devices for on-chip ESD protection.

The SCR-based device with a snapback characteristic has long been used to form a $V_{SS}$-based protection scheme for on-chip ESD protection over a broad range of technologies because of its low on-resistance, high failure current and the best area efficiency. The ESD design window of the snapback device is defined by the maximum power supply voltage as the low edge and the minimum internal circuitry breakdown voltage as the high edge. The downscaling of semiconductor technology keeps on squeezing the design window of on-chip ESD protection. For the submicron process and below, the turn-on voltage and sustain voltage of ESD protection
cell should be lower than 10 V and higher than 5 V, respectively, to avoid core circuit damages and latch-up issue. This presents a big challenge to device/circuit engineers. Meanwhile, the high voltage technologies push the design window to another tough range whose sustain voltage, 45 V for instance, is hard for most snapback ESD devices to reach. Based on the in-depth elaborating on the principle of SCR-based devices, this dissertation first presents a novel unassisted, low trigger- and high holding-voltage SCR (uSCR) which can fit into the aforesaid ESD design window without involving any extra assistant circuitry to realize an area-efficient on-chip ESD protection for low voltage applications. The on-chip integration case is studied to verify the protection effectiveness of the design. Subsequently, this dissertation illustrate the development of a new high holding current SCR (HHC-SCR) device for high voltage ESD protection with increasing the sustain current, not the sustain voltage, of the SCR device to the latchup-immune level to avoid sacrificing the ESD protection robustness of the device.

The ESD protection cells have been designed either by using technology computer aided design (TCAD) tools or through trial-and-error iterations, which is cost- or time-consuming or both. Also, the interaction of ESD protection cells and core circuits need to be identified and minimized at pre-silicon stage. It is highly desired to design and evaluate the ESD protection cell using simulation program with integrated circuit emphasis (SPICE)-like circuit simulation by employing compact models in circuit simulators. And the compact model also need to predict the response of ESD protection cells to very fast transient ESD events such as CDM event since it is a major ESD failure mode. The compact model for SCR-based device is not widely available. This dissertation develops a macromodeling approach to build a comprehensive SCR compact model for CDM ESD simulation of complete I/O circuit. This modeling approach offers
simplicity, wide availability and compatibility with most commercial simulators by taking advantage of using the advanced BJT model, Vertical Bipolar Inter-Company (VBIC) model. SPICE Gummel-Poon (SGP) model has served the ICs industry well for over 20 years while it is not sufficiently accurate when using SGP model to build a compact model for ESD protection SCR. This dissertation seeks to compare the difference of SCR compact model built by using VBIC and conventional SGP in order to point out the important features of VBIC model for building an accurate and easy-CAD implement SCR model and explain why from device physics and model theory perspectives.
To my husband Zhongyan, my parents Dingyuan and Xiuying
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TABLE OF CONTENTS

LIST OF FIGURES .......................................................................................................................... xii
LIST of TABLES ............................................................................................................................... xvi
LIST of ACRONYMS ....................................................................................................................... xvii
CHAPTER 1. INTRODUCTION ......................................................................................................... 1
  1.1. What is ESD ...................................................................................................................... 1
  1.2. How is ESD Relevant to Semiconductor Industry .......................................................... 1
  1.3. ESD Failure Modes on ICs and ESD models ............................................................... 2
  1.4. Characterization of ESD performance in ICs ............................................................... 6
    1.4.1. Human Body Model (HBM) ................................................................................... 6
    1.4.2. Machine Model (MM) .......................................................................................... 7
    1.4.3. Charged Device Model (CDM) ........................................................................... 8
    1.4.4. System-Level ESD Standard IEC 61000-4-2 ....................................................... 9
    1.4.5. Transmission Line Pulse (TLP) ............................................................................ 12
  1.5. Commonly Used ESD On-Chip Protection Circuits .................................................... 13
    1.5.1. The Qualities of Good ESD Protection ............................................................... 14
    1.5.2. ESD Protection Schemes ..................................................................................... 15
    1.5.3. Power Supply Clamp Design .............................................................................. 18
  1.6. Dissertation Outline ........................................................................................................ 22
CHAPTER 2. DESIGN AND INTEGRATION OF LOW VOLTAGE ESD PROTECTION DEVICES FOR AREA-EFFICIENT ON-CHIP ESD PROTECTION ........................................... 24
  2.1. Introduction .............................................................................................................. 24
  2.2. Device Principle and Device Structure .................................................................... 26
  2.3. Experimental Results and Discussions .................................................................... 32
  2.4. On-Chip Integration ................................................................................................. 36
  2.5. Chapter Summary .................................................................................................... 38

CHAPTER 3. DEVELOPMENT OF HIGH HOLDING CURRENT SCR FOR HIGH VOLTAGE ESD PROTECTION APPLICATIONS ......................................................... 39
  3.1. Introduction .............................................................................................................. 39
  3.2. Holding Current of SCR Devices ............................................................................ 43
  3.3. Device Structure, Experimental Results and Discussions ....................................... 46
  3.4. Chapter Summary .................................................................................................... 52

CHAPTER 4. COMPREHENSIVE COMPACT MODELING OF SCR DEVICES FOR CDM ESD SIMULATION OF COMPLETE I/O CIRCUITS .................................................. 53
  4.1. Introduction .............................................................................................................. 53
  4.2. SCR Compact Model Development ......................................................................... 55
    4.2.1. Equivalent Circuit of SCR ....................................................................................... 56
    4.2.2. Substrate Parasitic Modeling ................................................................................ 58
    4.2.3. Substrate Resistance Modeling ............................................................................. 59
    4.2.4. Negative Characteristic Modeling ........................................................................ 59
    4.2.5. Avalanche Current Modeling ............................................................................... 60
LIST OF FIGURES

Figure 1.1 Illustrations of the three basic failure mechanisms: (a) oxide failure, (b) metallization burnout, and (c) junction damage or burnout................................................................. 4

Figure 1.2 The simplified lumped circuit representation for ESD HBM model. ...................... 7

Figure 1.3 The simplified lumped circuit representation for ESD MM model. ....................... 8

Figure 1.4 Simplified CDM lumped circuit representation. ..................................................... 9

Figure 1.5 The negative (a) and positive (b) IEC zapping on a system board which has a off-chip IEC protection device. ................................................................. 10

Figure 1.6 Superposed waveforms obtained from the standard component level ESD models. Waveforms are generated from SPICE simulation................................................. 12

Figure 1.7 The V_{DD}-based ESD protection scheme............................................................... 17

Figure 1.8 The V_{SS}-based ESD protection scheme............................................................... 17

Figure 1.9 A simplified transient supply clamp, consisting of a capacitor, a resistor and a MOSFET.................................................................................................................. 18

Figure 1.10 The ESD design windows for (a) diode-chain-based, and (b) snapback-device-based supply clamps......................................................................................... 20

Figure 2.1 Device cross-section view of the uSCR, showing the locations of the L_n and L_p regions and the dimensions associated with the device characteristic................................. 26

Figure 2.2 The equivalent circuit of the SCR device................................................................ 30

Figure 2.3 Schematic diagram showing the different cases of L_n+L_p. L_x always keeps at 1\mu m. . 31
Figure 2.4 Measured TLP I-V characteristics of the four uSCR devices listed in Table 2.1. ...... 34
Figure 2.5 Measured TLP I-V characteristics of the four uSCR devices listed in Table 2.2. ...... 35
Figure 2.6 (a) Scheme of the on-chip ESD protection realized with the uSCR device. (b) Equivalent circuit schematic diagram of the layout showed in (a). It shows the discharge current loops under the different HBM and CDM zaps. ........................................................................................................... 37
Figure 3.1 The comparison of generic characteristics of the high holding current and the high holding voltage snapback ESD protection cells within the ESD design window defined by the supply voltage (V_{DD}), V_{max} and the latchup-immune current (I_{LU}). ................................................................. 42
Figure 3.2 The device cross-section view of the conventional SCR structure. ...................... 43
Figure 3.3 The equivalent circuit of the SCR device, showing the directions of all electron and hole current components after the both PNP and NPN transistors turn on. ......................................................... 46
Figure 3.4 The top view of the SCR devices. (a) Strip topology of conventional SCR, (b) segmented topology of high holding current SCR (HHC-SCR), (c) modified HHC-SCR with a well tie removed from each strip with an interval of every two well ties, and (d) modified HHC-SCR with a well tie removed from each strip with an interval of every well tie. .................. 47
Figure 3.5 The illustration of the segment topology of the SCR device reported in reference [83]. ................................................................................................................................................. 49
Figure 3.6 TLP measurement results of the conventional SCR, the SCR presented in [83] and HC-SCR devices with different D3=D4. .................................................................................................................. 50
Figure 3.7 TLP measurement results of the HHC-SCR device and the two modified HHC-SCRs shown in Figure 3.4(c) and (d). ............................................................................................................. 51
Figure 4.1 (a) Cross-section view of the HH-LVTSCR and (b) equivalent circuit of the HH-LVTSCR. ........................................................................................................................................................................ 56

Figure 4.2 Schematic of the HH-LVTSCR macromodel with all model elements included, showing the detailed connections of all internal nodes. ............................................................. 57

Figure 4.3 Different terminal configurations for the parameter extraction of different transistor models. ........................................................................................................................................................................ 67

Figure 4.4 Simulated and measured TLP I-V characteristics of the HH-LVTSCR........................... 70

Figure 4.5 (a) Simulated and measured time-dependent pad voltages and (b) simulated and measured pad currents right after the SCR triggering. ................................................................. 71

Figure 4.6 The simulated pad voltage under VFTLP pulse at a steady-state current of 1A. ....... 71

Figure 4.7 Simulated (a) base-emitter and collector-emitter voltages of the PNP and NPN transistors and (b) emitter, base and collector currents of the PNP and NPN transistors............. 73

Figure 4.8 Current waveforms of CDM pulses generated by the calibrated CDM equivalent circuit (insert) with the small target ................................................................. 74

Figure 4.9 (a) Schematic of on-chip ESD protection realized with SCR devices and (b) schematic showing the discharge current paths of the ESD protection in (a) under the positive and negative CDM zaps. ........................................................................................................................................................................ 76

Figure 4.10 Simulated transient voltage and current at the input-only pin under a positive 500 V CDM stress................................................................................................................................. 78

Figure 4.11 Simulated transient voltage and currents at the output-only pin under a positive 1 kV CDM stress................................................................................................................................. 79

Figure 5.1 The model circuit of the SPICE Gummel-Poon bipolar transistor model.............. 84
Figure 5.2 (a) The equivalent sub-circuit of VBIC bipolar transistor model and (b) the model circuit network. ........................................................................................................................................... 84
Figure 5.3 (a) Cross-section view of the HH-LVTSCR and (b) equivalent circuit of the HH-LVTSCR when the macromodel is using VBIC model to describe the NPN transistor......... 86
Figure 5.4 (a) Cross-section view of the HH-LVTSCR and (b) equivalent circuit of the HH-LVTSCR when the macromodel is using SGP model to describe the NPN transistor......... 86
Figure 5.5 Schematic of the HH-LVTSCR SGP-based macromodel with all model elements included, showing the detailed connections of all internal nodes.............................................. 87
Figure 5.6 Measured and Simulated TLP I-V characteristics of the macromodels built with VBIC and SGP models................................................................................................................ 88
Figure 5.7 (a) The measured and simulated time-dependent pad voltages and (b) pad currents by VBIC-based macromodel right after the SCR triggering. (c) The simulated time-dependent pad voltages and (d) pad currents by SGP-based macromodel right after the SCR triggering. .......... 89
Figure 5.8 Simulated (a) base-emitter and collector-emitter voltages of the PNP and NPN transistors and (b) emitter, base and collector currents of the PNP and NPN transistors in the SGP-based macromodel........................................................................................................ 92
Figure 5.9 The Gummel-Poon plots and output characteristics of VBIC and SGP model of NPN transistor under normal model extraction conditions......................................................... 95
Figure 5.10 The Gummel-Poon plot of VBIC and SGP model of NPN transistor when the macromodels is in conduction mode with a voltage of 10.85 V at Anode......................... 97
Figure 5.11 The output characteristics of VBIC and SGP model of NPN transistor when the macromodels is in conduction mode with a voltage of 10.85 V at Anode......................... 98
LIST OF TABLES

Table 1.1 The comparison of different standard component level ESD models. .......................... 12

Table 2.1 Lateral dimensions and TLP measurement results of the four uSCR devices with different \( L_n + L_p \). .......................................................................................................................... 33

Table 2.2 Lateral dimensions and TLP measurement results of uSCR-T3 devices with different D5 ........................................................................................................................................ 35

Table 4.1 Comparison of waveforms simulated from the calibrated CDM equivalent circuit in Figure 4.8 vs. JEDEC specifications ......................................................................................................................... 74
### LIST OF ACRONYMS

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATE</td>
<td>Automatic Test Equipment</td>
</tr>
<tr>
<td>BiCMOS</td>
<td>Bipolar Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>BSIM3v3</td>
<td>Berkeley Short Channel IGFET 3v3</td>
</tr>
<tr>
<td>CDM</td>
<td>Charged Device Model</td>
</tr>
<tr>
<td>DHVSCR</td>
<td>Dynamic Holding Voltage Silicon Controlled Rectifier</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>ESDA</td>
<td>Electrostatic Discharge Association</td>
</tr>
<tr>
<td>HBM</td>
<td>Human Body Model</td>
</tr>
<tr>
<td>ggNMOS</td>
<td>grounded gate N-type MOSFET</td>
</tr>
<tr>
<td>HHC-SCR</td>
<td>High Holding Current SCR</td>
</tr>
<tr>
<td>HH-LVTSCR</td>
<td>High-Holding Low-Voltage Triggering SCR</td>
</tr>
<tr>
<td>IC-CAP</td>
<td>Integrated Circuit Characterization and Analysis Program</td>
</tr>
<tr>
<td>ICs</td>
<td>Integrated Circuits</td>
</tr>
<tr>
<td>IEC</td>
<td>International Electrotechnical Commission</td>
</tr>
<tr>
<td>JEDEC</td>
<td>Joint Electron Device Engineering Council</td>
</tr>
<tr>
<td>LIGCSCR</td>
<td>Latch-Up-Immune Gate-Coupled LVTCSR</td>
</tr>
<tr>
<td>LOCOS</td>
<td>Local Oxidation of Silicon</td>
</tr>
<tr>
<td>LVTSCR</td>
<td>Low-Voltage Triggering SCR</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
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<tr>
<td>MLSCR</td>
<td>Modified Lateral SCR</td>
</tr>
<tr>
<td>MM</td>
<td>Machine Model</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>MOS Field Effect Transistor</td>
</tr>
<tr>
<td>NESD</td>
<td>N-type ESD</td>
</tr>
<tr>
<td>PLDD</td>
<td>P-type Lightly-Doped Drain</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SCR</td>
<td>Silicon Controlled Rectifier</td>
</tr>
<tr>
<td>SGP</td>
<td>SPICE Gummel-Poon</td>
</tr>
<tr>
<td>SPDT</td>
<td>Single Pole Double Throw</td>
</tr>
<tr>
<td>SPICE</td>
<td>Simulation Program with Integrated Circuit Emphasis</td>
</tr>
<tr>
<td>TCAD</td>
<td>Technology Computer Aided Design</td>
</tr>
<tr>
<td>TDDB</td>
<td>Time-Dependent Dielectric Breakdown</td>
</tr>
<tr>
<td>TLP</td>
<td>Transmission Line Pulse</td>
</tr>
<tr>
<td>uSCR</td>
<td>un-Assisted Low-Trigger and High Holding Voltage SCR</td>
</tr>
<tr>
<td>VFTLP</td>
<td>Very-Fast TLP</td>
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<tr>
<td>VBIC</td>
<td>Vertical Bipolar Inter-Company</td>
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</table>
CHAPTER 1. INTRODUCTION

1.1. What is ESD

Electrostatics, or static electricity, is an excess of deficiency of electrons on a surface. It is as old as the time itself. Static electricity is caused by contact and separation of 2 dissimilar materials including solids, liquids and gas. The very first documented observation of static electricity generation is back to 600 B.C. when Greeks rubbed amber with a piece of fur and observed attraction of lightweight objects to the amber. Electrostatic discharge (ESD) is the transfer of electrons between two bodies at different static potentials. The three mechanisms being responsible for generating the potential difference are triboelectrification, induction and conduction. The famous experiment is Franklin’s kite test in 1952 showing lightening is an ESD event [1].

Back to our everyday’s life, no one could hardly experience some kind of ESD events, like experiencing the shocking sparks when touching a door handle of a car. The damages caused by ESD should never been overlooked.

1.2. How is ESD Relevant to Semiconductor Industry

The ESD problem became a real issue after World War II as highly insulating polymeric materials found widespread usage where substantial static charge accumulation might cause machinery shut downs. However, the devastating ESD damage problem was not taken into serious consideration until the modern microelectronics technologies took the role in our
everyday life, which is how ESD failure problem became relevant to semiconductor integrated circuits (ICs) technologies [1]-[3].

Only a half century after the development of ICs was initiated, ICs have become ubiquitous. Modern computing, communications, manufacturing and transport systems, including Internet, all depend on the existence of integrated circuits. Technological innovation in the semiconductor industry has never slowed down. The evolution in the downscaling of the physical dimensions is considered a main factor in obtaining lower cost, while achieving better performance and more compact ICs, all of them keys for today’s demanding applications [4].

ESD failure is a profound reliability problem to ICs and poses a grand challenge to the semiconductor industry [5]. The impact of the invisible ESD phenomena became materialized with the invention of semiconductor transistor in 1947 and the development of metal-oxide semiconductor (MOS) technologies in the 1960s. The electronic device and system failures due to ESD events in the semiconductor industry escalated almost exponentially in the 1970s [1]. As the semiconductor ICs technologies keep on downscaling, ICs parts become increasingly susceptible to ESD damages [6]-[9]. Statistics indicated that up to 30% of all ICs failure might be attributed to ESD [10]. The actual cost of ESD damage to the electronics industry is running into the billions of dollars annually [11]. And ESD protection has become a topic of major interest and discussion [12]-[14].

1.3. ESD Failure Modes on ICs and ESD models

ESD damage to electronic devices can occur at any point from manufacture to field service. Damage results from handling the devices in uncontrolled surroundings or when poor
ESD control practices are used. Generally damage is classified as either a catastrophic failure or a latent defect.

The catastrophic failure causes immediate ICs malfunction. There are mainly three failure modes for permanently damaging semiconductor devices due to ESD events [15]-[16] and they can be described as followings:

1. **Oxide failure**: oxide may have void formation, vaporization and filament formation, leading to shorts or opens [17], as shown in Figure 1.1(a).

2. **Metallization burnout**: metal and contacts may melt and vaporization may occur, leading to shorts and opens, as shown in Figure 1.1(b).

3. **Junction damage or burnout**: junction may melt and cross diffusion or lattice damage may occur. It is an important mechanism in bipolar junction transistor [18] and MOS devices [19]. In NMOS, this failure is often displayed by a high reverse leakage current, and it may be due to a redistribution of n-type dopants into the channel or due to lattice damage during the ESD event, as shown in Figure 1.1(c).

A latent defect is more difficult to identify. A device that is exposed to an ESD event may be partially degraded, yet continue to perform its intended function. However, the operating life of the device may be reduced dramatically. A product or system incorporating devices with latent defects may experience premature failure after the user places them in service. Such failures are usually costly to repair and in some applications may create personnel hazards.
Figure 1.1 Illustrations of the three basic failure mechanisms: (a) oxide failure, (b) metallization burnout, and (c) junction damage or burnout.

ESD damage is usually caused by one of three events: direct electrostatic discharge to the device, electrostatic discharge from the device or field-induced discharges. Damage to an ESD sensitive device by the ESD event is determined by the device’s ability to dissipate the energy of the discharge or withstand the voltage levels involved. This is known as the device’s ESD sensitivity.

*Discharge to the device.* An ESD event can occur when any charged conductor (including the human body) discharges to an ESD sensitive device. The most common cause of electrostatic
damage is the direct transfer of electrostatic charge from the human body or a charged material to the electrostatic discharge sensitive device. When one walks across a floor, an electrostatic charge accumulates on the body. Simple contact of a finger to the leads of a device or assembly allows the body to discharge, possibly causing device damages. The model used to simulate this event is the Human Body Model (HBM). A similar discharge can occur from a charged conductive object, such as a metallic tool or fixture. The model used to characterize this event is known as the Machine Model (MM).

Discharge from the device. The transfer of charge from an ESD sensitive device is also an ESD event. Static charge may accumulate on the ESD sensitive device itself through handling or contact with packaging materials, work surfaces, or machine surfaces. This frequently occurs when a device moves across a surface or vibrates in a package. The model used to simulate the transfer of charge from an ESD sensitive device is referred to as the Charged Device Model (CDM). The capacitance and energies involved are different from those of a discharge to the ESD sensitive device. In some cases, a CDM event can be more destructive than the HBM for some devices.

The trend towards automated assembly would seem to solve the problems of HBM ESD events. However, it has been shown that components may be more sensitive to damage when assembled by automated equipment. A device may become charged, for example, from sliding down the feeder. If it then contacts the insertion head or another conductive surface, a rapid discharge occurs from the device to the metal object.

Field induced Discharges. Another event that can directly or indirectly damage devices is termed Field Induction. As noted earlier, whenever any object becomes electrostatically charged,
there is an electrostatic field associated with that charge. If an ESDS device is placed in that electrostatic field, a charge may be induced on the device. If the device is then momentarily grounded while within the electrostatic field, a transfer of charge from the device occurs as a CDM event. If the device is removed from the region of the electrostatic field and grounded again, a second CDM event will occur as charge (of opposite polarity from the first event) is transferred from the device.

1.4. Characterization of ESD performance in ICs

Based on the three ESD damage events mentioned above, standard ESD models which simulate real ESD events have been constituted by ESD Association (ESDA) and Joint Electron Device Engineering Council (JEDEC) in order to characterize the susceptibility of an IC to ESD damage. ICs will be tested by stressing the device under test (DUT) with emulated ESD zaps of different models, a procedure called ESD zapping. The ESD models are represented as lumped circuit equivalents, so that testing is consistent and reliability can be defined as a quantitative attribute.

1.4.1. Human Body Model (HBM)

The HBM is intended to represent the electrostatic discharge from the fingertip of a pre-charged human being delivered to a device [20]-[21]. The discharge current levels can be 1-4 A with a rise time of 10 ns and a discharge time constant of 150 ns. The HBM lumped circuit model is represented as a capacitor discharging through a resistor, with the capacitance $C_{ESD} =$
100 pF, the inductance $L_{ESD} \approx 7.5 \, \mu\text{H}$, and the resistance $R_{ESD} = 1.5 \, \text{k ohm}$, as shown in Figure 1.2.

Figure 1.2 The simplified lumped circuit representation for ESD HBM model.

1.4.2. Machine Model (MM)

The MM is intended to represent the interaction of electrical discharge from a pre-charged conductive source, such as metallic tools or machine, to the component [22]-[23]. In Japan, this model is widely used in the automotive industry. The standardized waveform for the MM is obtained by the lumped circuit as in Figure 1.3, the capacitor $C_{ESD} = 200 \, \text{pF}$, the inductor $L_{ESD} \approx 1.5 \, \mu\text{H}$, and the resistance $R_{ESD} < 1 \, \Omega$. With essentially no series resistance in its path, the MM event has higher current levels than the HBM for the same charging voltage. The MM is a damped sinusoidal oscillating current waveform, and the time to the first current peak is typically 15ns with duration for the pulse of approximately 40ns. Although the pulse width appears to be less, the power dissipation in the IC is dominated by the time at the peak current level, and this is nearly the same for both HBM and MM. Hence, the failure currents for HBM
and MM will be approximately the same and the equivalent MM level to a 2000V HBM under the present ESD Association Standards is about 100V with a peak current of 1.7A.

![ESD MM model diagram](image)

Figure 1.3 The simplified lumped circuit representation for ESD MM model.

1.4.3. **Charged Device Model (CDM)**

The CDM represents the electrostatic discharge occurring from a chip via an external grounded element. Different from HBM and MM, in the CDM event it is the packaged integrated circuit that accumulates the charge on its package and/or die [24]-[25]. During a CDM event rapid discharge occurs with the resulting current levels in tens of amperes and very fast rise time (<500ps rise time). The resulting damage due to such direct pin discharge is normally gate oxide breakdown. Because of the widespread use of automated manufacturing and testing line, as well as thinner and thinner gate oxides in advanced technologies, the CDM model has gained importance in more recent years [26]-[27]. CDM levels are dependent on package type and hence the same protection scheme may give different levels from one product chip to another product chip. Note that while the ratio for HBM and MM equivalence is more than 20:1, i.e. a 100V MM threshold is the same as a 2000V HBM threshold, CDM thresholds are not directly
linked to HBM and MM thresholds. A typical CDM setup is shown in Figure 1.4, where the ESD sensitive DUT is placed upside down on a charge plate, charged by a high voltage source, and then discharge through a discharge head. There are two different means for charging up the DUT: direct charging and field induced charging. The former charges the DUT by direct contact. The latter, recommended by many test standards, charges the DUT through electric field induction. The CDM is the fastest of the ESD phenomena, and the equivalent lumped circuit typically includes, a capacitor $C_{ESD} = 6.8 \, \text{pF}$, an inductor $L_{ESD} < 1 \, \mu\text{H}$, and the resistance $R_{ESD} = 1 \, \text{ohm}$.

![Simplified CDM lumped circuit representation.](image)

1.4.4. System-Level ESD Standard IEC 61000-4-2

IEC stands for International Electrotechnical Commission. IEC 61000-4-2 is a widely accepted European standard which defines a system level ESD event that is meant to be tested on actual end equipments like PCs, PDAs, set top boxes, etc. In this standard two different test procedures are defined, the air-gap test and the contact test. Commonly, the air-gap test is less
repeatable than the contact test. In regular testing programs, circuits are tested powered up and powered down in order to guarantee functionality after stress, not only when the system is off but also during operation. This IEC standard defines an ESD event that is much stronger than a component level ESD event such as HBM, CDM. For instance, a level 4 IEC 61000-4-2 ESD event has a peak current of 30A, compared to a 2kV HBM peak current of 1.3 A.

Figure 1.5 The negative (a) and positive (b) IEC zapping on a system board which has a off-chip IEC protection device.
The pins which require IEC protection usually are transceiver pins such as USB pins, Ethernet pins or RS-232 pins. IEC testing is done from the protected connection to the system ground, both polarities. The IEC protection could be done off chip (on the board) or on chip. It is preferred to have IEC protection components off chip as shown below. In certain situations, it may be necessary to have on chip IEC protection, with little or no board-level protection. Figure 1.5 shows the positive and negative IEC strikes on a system board with an off-chip IEC protection diode.

Figure 1.6 and Table 1.1 compares the current waveforms for the different component level ESD models previously discussed. Note that, consistent with the previous discussion, the CDM rise time is considerably faster than the other ESD standards. Another important consideration is that for the case of the MM and CDM, the oscillating waveform results in high peaks of ESD current in both polarities, as a consequence, ESD structures designed to sustain the MM should be able to handle high dual-polarity peak of ESD current.
Figure 1.6 Superposed waveforms obtained from the standard component level ESD models. Waveforms are generated from SPICE simulation.

Table 1.1 The comparison of different standard component level ESD models.

<table>
<thead>
<tr>
<th>Model</th>
<th>HBM</th>
<th>MM</th>
<th>CDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Level</td>
<td>2 kV</td>
<td>200V</td>
<td>1 kV through small target</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>~ 150 ns</td>
<td>~ 40 ns</td>
<td>~ 1 ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>2 ~ 10 ns</td>
<td>10 ~ 15 ns</td>
<td>100 ~ 500 ps</td>
</tr>
<tr>
<td>Peak Current</td>
<td>1.33 A</td>
<td>~3.6 A</td>
<td>12 A</td>
</tr>
</tbody>
</table>

1.4.5. Transmission Line Pulse (TLP)

All the existing ESD test models, as discussed above, share one common disadvantageous feature that the ESD test methods developed upon them are destructive. Such ESD zapping tests provide results about ESD failure threshold of an ESD sensitive device.
However, they offer no insights into the possible failure mechanisms, which are critical to ESD protection design. Such information can be obtained by use of a transmission line pulse (TLP) technique. TLP technique has been increasingly accepted in practical ESD protection circuit design since it was introduced into ESD protection design [29]. Many TLP testing systems with different flavor exist [12], [30]. The principle for TLP test is that a piece of transmission line cable is charged by a voltage source, and the TLP system forces a trapezoidal current waveform into device under test, easier to control compared to that generated based on other ESD test standards [30]-[31]. The pulse width of the TLP is a function of the length of the transmission line and the propagation velocity of the transmission line. For this method, the standard choice of pulse width has been determined based on the HBM model, i.e., the TLP current level gives an estimated HBM level [30], [32]. This ESD characterization method allows for a closer estimation of the device conducting characteristics. It also provides an idea of the quasi-static behavior of the ESD device since reliable data can be taken during the 100 ns time frame of the pulse width, with having reduced effects of self-heating in the device. In this respect, the TLP curve below the second-breakdown point can be considered a good approach to a dc-simulated curve. However, it still represents the way the device responds to ESD stress because it reveals the operating points after the initial turn-on transient.

1.5. Commonly Used ESD On-Chip Protection Circuits

There are two general methods to reduce IC failure due to ESD. One consists of the usage of ionization apparatus, the proper handling and grounding of personnel and equipment during manufacturing, and the usage of safety packaged chips, i.e., to prevent ESD events from
occurring [33]. The other method is to incorporate effective on-chip protection circuitry inside ICs, which would shunt high currents to keep ESD strikes away from the internal circuitry and clamp high voltages during an ESD event [34]-[35]. A chip manufacturer has partial control over a customer’s handling of its product, but it is not possible to guarantee total ESD immunity. However, through the proper design of on-chip protection structures, the threshold of sustainable stress can be significantly increased, resulting in improved reliability of the ICs and electronics systems [12]-[14], [17].

1.5.1. The Qualities of Good ESD Protection

The capability of ESD protection circuitry can be determined by its performance in four categories: robustness, effectiveness, speed and transparency. Good ESD protection must function well in all of these areas [12].

Robustness – Robustness describes the ability of the ESD protection circuitry to handle the ESD current by itself. It is defined as the ESD level at which the ESD protection circuitry fails. For example, a protection circuitry that can withstand a peak current of 3 A on the HBM timescale has a robustness of 4.5 kV HBM. Robustness is usually, but not always, proportional to the width of the protection circuitry. Therefore, it is often convenient to measure the breakdown characteristics of a protection device with TLP or HBM testing and quantify its failure level in milliamperes per micrometer or HBM volts per micrometer.

Effectiveness – Effectiveness describes the ability of the protection circuitry to limit the voltage to a safe level such that circuits in parallel with the ESD protection do not fail. To
achieve higher protection levels, the voltage sustained across the ESD protection circuitry must decrease or the turn-on voltage of the failing elements must increase.

**Speed** – Speed is of particular importance for CDM events, with their subnanosecond rise time. Even robust and effective ESD networks must activate with enough speed to clamp the ESD event at a safe level without causing circuits in parallel to fail.

**Transparency** – Transparency requires that the ESD protection not interfere with the normal operation of the I/O circuit and of the chip itself. This includes the ESD clamp should not have so much capacitance that it violates the loading limits of the I/O signaling specification, the ESD clamp must not draw excessive current at either high or low input or output levels, the ESD clamp must be compatible with the normal sequence for applying power, and the ESD clamp has to be able to tolerate the over-voltage conditions.

### 1.5.2. ESD Protection Schemes

In ESD measurement practice of HBM and MM, ESD pulses zap through 2 pin combinations in different directions, i.e., zapping the I/O pin versus the power supply pin in both polarities, zapping the I/O pad to the ground pin in both polarities, zapping the I/O pin versus I/O pin in both polarities and zapping power supply pin versus ground pin in both polarities [20]-[23]. For the case of CDM, the whole component package will be charged positively and negatively then all pins will be grounded respectively. The discharge current will go into or come out of the package from the grounded pin to the substrate of the chip [24]-[25]. A good ESD protection network must provide a discharge path for all pin combinations and must limit the voltage across any sensitive devices. Most ESD solutions rely on shunting charge from an I/O pin to a power
supply. These solutions fall into two general categories: $V_{DD}$-based ESD protection for those that shunt current to the positive supply rail and $V_{SS}$-based ESD protection that shunt current to the negative supply rail [12], [36]-[39]. Figure 1.7 and Figure 1.8 are the $V_{DD}$-based ESD protection scheme and $V_{SS}$-based ESD protection scheme, showing the discharge current paths for different ESD zapping combinations. For $V_{DD}$-based protection, the clamp is usually a pnp emitter-base diode and there is no clamp to $V_{SS}$. For $V_{SS}$-based protection, the clamp between the I/O pad and $V_{SS}$ is usually a snapback device and there is no clamp to $V_{DD}$.

The difference between these two methods becomes apparent when examining the ESD discharge path under various pin combinations. For example, when zapping the I/O pin versus $V_{SS}$ positively, for the $V_{SS}$-based clamp, the ESD current flows directly through the clamp. No such direct path exists for the $V_{DD}$-based clamp. The current must flow onto the $V_{DD}$ rail and through the $V_{DD}$ power supply clamp to reach $V_{SS}$. In both cases, the discharge also appears in parallel across the nMOS output driver. The objective of ESD protection is to restrict the I/O pad voltage below the failure voltage of devices in parallel, in this case the nMOS output driver. Therefore, in the $V_{SS}$-based scheme, the primary clamp alone must hold the I/O pad voltage below this limit. In the $V_{DD}$-based scheme, the current discharge through the primary clamp to the $V_{DD}$ rail, then though the $V_{DD}$ supply clamp. Therefore, these two clamps in series must meet the same voltage-limiting criterion to protect the nMOS output driver. Which ESD protection scheme should be used depend on the technology, available ESD protection devices, the product application requirements and the cost.
Figure 1.7 The $V_{DD}$-based ESD protection scheme.

Figure 1.8 The $V_{SS}$-based ESD protection scheme.
1.5.3. Power Supply Clamp Design

For both ESD protection scheme, they all have primary power supply clamp. There are two types of supply clamp, the static supply clamp and the transient supply clamp. Transient supply clamp has been used widely in preventing ESD damage [40]-[41]. It has been proven to offer robust, scalable, portable and easily simulated [42]-[48]. The operation of transient clamps depends on both a trigger voltage and the rate at which that voltage is applied (dV/dt). Figure 1.9 shows a simple transient supply clamp circuit, which consists of a capacitor, a resistor and a MOS device, to illustrate basic concept of how the transient clamp works. When the microchip (i.e., circuit core) being protected is subjected to the ESD stress, the ESD pulse will be fed simultaneously to the external capacitor $C$ and drain terminal of the MOSFET in the ESD protection circuit. Such a pulse, which has a very high voltage, will give rise to a voltage drop in the external resistor $R$ and therefore will turn on the MOSFET within a very short period of time. A lot of transient supply clamp designs have been presented in literatures [42]-[48].

Figure 1.9 A simplified transient supply clamp, consisting of a capacitor, a resistor and a MOSFET.
In addition to the transient supply clamp, the static supply clamps are also being used widely. The static supply clamp can be diode chain which is only applicable for low voltage supplies or snapback-based devices (as shown in Figure 1.7 and Figure 1.8). The static supply clamp is designed to respond when a specific trigger voltage is exceeded. To realize the effective ESD protection without interfering with the normal operation of the protected circuit, the key considerations include (as shown in Figure 1.10): 1) the turn-on voltage or the trigger voltage \( V_T \) and the clamping voltage at the required ESD protection level have to be kept below the voltage of internal circuitry breakdown, 2) the sustain point (also called holding point) in the case of the snapback devices has to be larger than the power supply voltage \( V_{DD} \) to avoid latchup problems [49], 3) low leakage current at operating voltage \( V_{DD} \), 4) good robustness, i.e., high second breakdown current \( I_{B2} \) per unit area. In additional, for the static supply clamp using snapback-based device, if its clamped voltage is low enough and the robustness is high enough in reverse operation, the extra diode between supply and \( V_{SS} \) in supply ESD protection section (in Figure 1.7 and Figure 1.8) and the primary ESD clamp for negative strikes in signal ESD protection section (in Figure 1.8) can be removed to save area.
Figure 1.10 The ESD design windows for (a) diode-chain-based, and (b) snapback-device-based supply clamps.

Normally, there are three type of devices, bipolar junction transistor (BJT), MOS field – effect transistor (MOSFET) and silicon controlled rectifier (SCR) having been used to form the snapback-based power supply clamp and the primary ESD clamp for positive strikes, as shown
in Figure 1.7 and Figure 1.8. A BJT is actually the underlying building bricks of these advanced ESD protection networks. When BJT is used in ESD protection, [39], [50]-[51], the collector of the BJT is normally connected to the protected pad, the emitter to one of the power rails, and an additional resistor between the base and emitter is incorporated. When the ESD pulse appears in the protected pad, the BJT can go into the snapback mode and create a low impedance discharge path that guarantees the integrity of the protected circuit.

Another proven protection element more often used in CMOS technologies is the MOSFET. For example, the grounded gate N-MOSFET (ggNMOS) with minimum design channel length and gate-, source-, and bulk- contacts tied together to ground represents the key element of many ESD protection concepts. Beside its electrical properties, it is available at the beginning of the technology definition, characterized at the early stages of the development process, as well as area-effective.

The operation of the ggNMOS during an ESD event is mainly controlled by the embedded NPN BJT, formed by the drain (n+), bulk (p), and source (n+), lateral structure [12]. As a result, the ggNMOS goes into snapback [52] during an ESD event and can be often self-protected. A similar concept applies to the PMOS. A lot of design works have been done to use MOS device as ESD protection [53], for example, PNP-driven NMOS [53], substrate triggered NMOS [54], NMOS triggered NMOS [55], etc. A drawback of an ESD device with MOS gate is that it can suffer long-term reliability problems if the pad operating voltage is higher than the pre-established voltage rating, or if a relatively large electric field is applied at the gate during the ESD event [56].
Different SCR-based device designed for ESD protection have been proposed in the literature using an experimental approach [57]. The SCR-based devices are not standard structures optimized in CMOS or Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) processes, and even though these devices can be the most efficient structures in terms of ESD protection, it has been rather difficult to design functional SCR-based protection devices [58] and effective compact modeling techniques for this type of device are also required.

Although the SCR-type structures might serve as superior ESD protection components in CMOS/BiCMOS technologies, the embedded SCR in the CMOS/BiCMOS processes has been, instead, a cause of concern because of the latchup problem [49], [60]. Thus, the challenge in the ESD design using SCR-based structures is to maintain a safe operation in the circuit without a latchup problem, while obtaining the advantage of the deep snapback and high conductivity modulation for high ratio of ESD protection per unit area [59].

1.6. Dissertation Outline

The investigation presented in this dissertation provides a comprehensive study of the design, characterization and integration of the ESD protection using SCR-based structures and the development and implementation of compact models for the SCR-based structures to predict ESD protection level and evaluate the interaction of ESD cell with core circuitry at pre-silicon stage. The organization of the dissertation is as following.

Chapter 2 starts with design methodologies followed by presenting the design of a novel and robust un-assisted low-trigger and high holding voltage SCR (uSCR) for low voltage application and the implementation of such device into whole chips to realize optimized ESD
protection. Chapter 3 addresses a new high holding current SCR (HHC-SCR) for the ESD protection of high voltage applications. Chapter 4 describes the development of a simulation program with integrated circuit emphasis (SPICE) equivalent-circuit model for the SCR used for ESD protection applications, with emphasis being placed on the simulation of circuits subject to an fast-transient and highly destructive ESD event known as CDM. The framework developed includes the equivalent circuit, model components’ equations, and model parameter extraction. Chapter 5 assesses two SCR macromodels by using Vertical Bipolar Inter-Company (VBIC) model and SPICE Gummel-Poon (SGP) model respectively are presented and the simulations results of both macromodels are compared with measurements. Comparing with SGP model, the unique advanced features of VBIC model for building an accurate SCR macromodel have been pointed out and analyzed from device physics and model theory perspectives. Chapter 6 comes summary and conclusion of the dissertation.
CHAPTER 2. DESIGN AND INTEGRATION OF LOW VOLTAGE ESD PROTECTION DEVICES FOR AREA-EFFICIENT ON-CHIP ESD PROTECTION

2.1. Introduction

As processes are scaling down, the breakdown voltage of internal circuitry is lower and lower. Especially for the ultra-thin gate oxide, with the time-dependent dielectric breakdown (TDDB) continually decreasing. To cover both intrinsic and extrinsic gate oxide failure, the suggested maximum permissible voltage limit under Electrostatic Discharge (ESD) conditions is 10 V for deep submicron process and below [61]. When using the $V_{SS}$-based ESD protection scheme as shown in Figure 1.8, the trigger voltage of designed snapback-based ESD protection cells, which are sitting as the primary ESD clamp for positive strikes on I/O pad in Figure 1.8 and as the primary power supply clamp between supply and $V_{SS}$ in Figure 1.7 and Figure 1.8, should be lower than 10V. For a 3.3 V product application running on the feature size of 0.35 $\mu$m, taking into account the maximum transient voltage, the holding voltage of the ESD protection cells should be higher than 5 V and/or the holding current of ESD cell should be higher than the minimum latch-up current in order to avoid a latch-up issue [49]. Such a narrow ESD design window (refer to Figure 1.10) presents a big challenge to the device/circuit engineers.

SCRs also known as thyristors are used extensively in power device applications because of the capability to switch from very high impedance state to a very low impedance state. Such device has long been used as an on-chip ESD protection element to form snapback-based ESD clamp [62]-[63] over a broad range of technologies because of its low on-resistance, high failure
current and the best area efficiency for on-chip ESD protection [12], [62]-[64], but a conventional SCR’s trigger voltage is higher than 10 V and the transient-induced latch-up is still a major problem. Some SCR devices have been reported to have a low switching voltage, such as gate-coupled low-voltage triggering (LVTSCR) [65], grounded-gate NMOS triggered SCR [61], double-triggered SCR [66], smart triggered multi-finger SCR [67], etc., but those SCR devices have to be assisted by external trigger circuitry to reach such low trigger voltage. For latch-up, two methods were reported to solve this problem. One way is to increase the trigger current [68] or by increasing the holding current [69]. The former has to use trigger circuitry to insure low trigger voltage and the latter needs to shunt an external resistance and gate structure, which consume the layout area. Besides these, the highly latch-up-immune gate-coupled LVTCSR (LIGCSCR) [70] was also reported, but the properly designed control circuits need to be involved. In addition, the holding voltage of dynamic holding voltage SCR (DHVSCR) [71] has been shown to be not high enough.

This chapter presents the first un-assisted, low-trigger and high-holding voltage SCR (uSCR), which can simultaneously realize a trigger voltage as low as 7 V and a tunable holding voltage from 5 to 7.5 V without using any external circuitry [72]-[74]. The ESD robustness of the uSCR in both positive and negative operations are higher than 60 mA/μm, thus enabling excellent ESD protection levels of +/- 8 kV HBM and +/- 2 kV CDM based on JEDEC standard, when using uSCR as the primary ESD clamp for positive strikes on I/O pad and as the primary supply clamp between supply and VSS in the ESD protection scheme of Figure 1.8.
2.2. Device Principle and Device Structure

The device cross-section view of the uSCR is shown in Figure 2.1. The SCR device is a p-n-p-n structure which is a PNP-NPN coupled system. In Figure 2.1, the p-n-p-n corresponds to the P+/N-Well/P-Well/N+. The N-Well terminal is tied to P+ which is the emitter of the PNP transistor to form the outside anode and the P-Well terminal is tied to N+ which is the emitter of the NPN transistor to form the outside cathode. The equivalent circuit is shown in Figure 2.2. There are 3 junctions inside the SCR structure.

![Figure 2.1 Device cross-section view of the uSCR](image)

Figure 2.1 Device cross-section view of the uSCR, showing the locations of the L_n and L_p regions and the dimensions associated with the device characteristic.

When the anode of the device is biased positively with respect to the cathode, the P+/N-Well junction and the P-Well/N+ junction are forward biased while the center junction, P-Well/N-Well, is under reverse bias. Most of the forward voltage drops across the P-Well/N-Well junction. The current level is small at the beginning since the supply of electrons and holes to the
center junction is restricted by the reverse-biased junction on either side [75]. If holes are injected from P+ to N-Well and will recombine with electrons in N-Well region to maintain space charge neutrality, the supply of electrons in current situation is severely restricted since N-Well region is terminated in the reverse-biased P-Well/N-Well junction. It is the same thing to electrons injected from N+ to P-Well region. The P-Well/N-Well junction is the blocking junction. The supply of electrons and holes are from the thermal generation of electron-hole pairs at the center junction. As a result, the total current is approximately the reverse saturation current of the center junction and the SCR device is in forward-blocking state. The reverse saturation current passing through the center junction will be multiplied by the carrier multiplication due to impact ionization over a fairly broad range of the voltage. As shown in Figure 2.2,

\[ I_{C-PNP} = \alpha_{PNP} I_{E-PNP} + I_{co-PNP} \]  
\[ I_{B-PNP} = I_{E-PNP} - I_{C-PNP} = (1 - \alpha_{PNP}) I_{E-PNP} - I_{co-PNP} \]  

where \( \alpha_{PNP} \) is the current transport factor of PNP transistor and \( I_{co-PNP} \) is the collector-base reverse saturation current of PNP transistor, when multiplied by the multiplication factor, \( M \),

\[ I_{C-PNP} = M \cdot (\alpha_{PNP} I_{E-PNP} + I_{co-PNP}) \]  
\[ I_{B-PNP} = (1 - M \cdot \alpha_{PNP}) I_{E-PNP} - M \cdot I_{co-PNP} \]  

similarly,

\[ I_{C-NPN} = M \cdot (\alpha_{NPN} I_{E-NPN} + I_{co-NPN}) \]  

where \( \alpha_{NPN} \) the current transport factor of PNP transistor and \( I_{co-NPN} \) is the collector-base reverse saturation current of NPN transistor, assuming \( M_{PNP} = M_{NPN} \). Since
\[ I_{B-PNP} + I_{SUB-PNP} = I_{C-NPN} \]  \hspace{1cm} (2.6)

\[ I_{E-PNP} = I_A - I_{SUB-PNP} \]  \hspace{1cm} (2.7)

\[ I_{E-NPN} = I_A - I_{SUB-NPN} \]  \hspace{1cm} (2.8)

Replacing Equation (2.4), (2.5), (2.7), (2.8) in Equation (2.6), it will have:

\[ I_A = \frac{M(I_{co-PNP} + I_{co-NPN}) - M\alpha_{PNP}I_{SUB-PNP} - M\alpha_{NPN}I_{SUB-NPN}}{1 - M(\alpha_{PNP} + \alpha_{NPN})} \]  \hspace{1cm} (2.9)

When carrier multiplication happens in the center junction, many electrons are swept into N-Well region and holes into P-Well region. This process provides the majority carriers to these regions needed for increased injection by the emitter junctions. As derived in Equation (2.9), breakdown occurs at the center blocking junction when

\[ M(\alpha_{PNP} + \alpha_{NPN}) \rightarrow 1 \]  \hspace{1cm} (2.10)

When the bias voltage increases, the depletion region of the P-Well/N-Well junction will expand, which means the base widths of both PNP and NPN transistors will be narrowed. Since \( \alpha_{PNP} \) and \( \alpha_{NPN} \) increase as the base widths decrease, the device triggering can occur by the effect of base-width narrowing. And just moderate narrowing can increase the alphas enough to trigger the device with the contribution of avalanche multiplication. As \( M(\alpha_{PNP} + \alpha_{NPN}) \) approaches unity, many holes injected into N-Well region survive to be swept across center blocking junction into P-Well region. This helps to feed the recombination in P-Well region and to support the injection of holes into N+ region. Similarly, the electrons injected in to P-Well region and collected by N-Well will supply the injection of electrons into P+ region. The transfer of injected carriers across the center junction is regenerative which means a greater supply of electrons to N-Well allows a
greater injection of holes from P+ and this greater injection of holes further feeds P-Well by transistor action. The process continues to repeat itself to push the device to be triggered in the end.

From another point of view, when the bias voltage increases, the reverse saturation current will increase due to impact ionization. This current will flow through the two substrate resistances, $R_{N-Well}$ and $R_{P-Well}$ (see Figure 2.1 and Figure 2.2), to raise the base-emitter voltages of both transistors. As long as the voltage drop on the base-emitter junction is greater than about 0.7 V, the PNP emitter and the NPN emitter would be allowed to inject a large number of holes and electrons, respectively, and the positive feedback regenerative mechanism is then initiated and the SCR device becomes active. Both PNP and NPN transistors are working in forward active mode now.

When the avalanche multiplication happens in the center junction, the primary collector current, $I_{C-PNP}$ and $I_{C-NPN}$, are multiplied by $M$.

$$I_A = M \cdot I_{C-PNP} + M \cdot I_{C-NPN} = M \cdot (\alpha_{PNP} I_{E-PNP} + I_{co-PNP}) + M \cdot (\alpha_{NPN} I_{E-NPN} + I_{co-NPN})$$

Equation (2.11) can be rewritten as:

$$\frac{1}{M} = \alpha_{PNP} \frac{I_{E-PNP}}{I_A} + \alpha_{NPN} \frac{I_{E-NPN}}{I_A} + \frac{I_{co-PNP} + I_{co-NPN}}{I_A}$$

Equation (2.12) can also be expressed as [84]:

$$\frac{1}{M} = 1 - \left(\frac{V_{BC}}{V_{BRK}}\right)^n$$

$V_{BRK}$ is the breakdown voltage of the center junction which is also the base-collector junction of both PNP and NPN transistors, $V_{BC}$ is the voltage drop across this junction, and $n$ is typically
equal to 2. By equaling Equation (2.12) with Equation (2.13), the trigger voltage, $V_T$, will be obtained as:

$$V_T = V_{BC} = V_{BRK} \left(1 - \alpha_{P_{NP}} \frac{I_{E-P_{NP}}}{I_A} - \alpha_{N_{PN}} \frac{I_{E-N_{PN}}}{I_A} - \frac{I_{CO-P_{NP}} + I_{CO-N_{PN}}}{I_A}\right)^{-\frac{1}{n}}$$

(2.14)

Figure 2.2 The equivalent circuit of the SCR device.

As derived in Equation (2.14), the breakdown voltage of the blocking junction controls the trigger voltage. In a typical low-triggering SCR without an external trigger circuit [62], the blocking junction is the P-Well/N-Well junction whose breakdown voltage is fairly high. To reduce the trigger voltage, the modified lateral SCR (MLSCR) [62] shown in Figure 2.1 is made by adding an N+ diffusion across the P-Well/N-Well junction. In such a device, the N+/P-Well junction controls the trigger voltage. In order to develop the new uSCR for further reducing the
trigger voltage, the N-type ESD (NESD) and P-type lightly-doped drain (PLDD) regions (regions indicated with dashed lines in Figure 2.1) are added into the MLSCR through the LDD ion implant step. The lengths, \( L_n \) and \( L_p \), depict the NESD and PLDD region extensions. \( L_x \) is the distance between the N+ and P+ regions (see Figure 2.1) and the silicide blocking mask covers this region for the fully-salicided process. The variation of \( L_n \) and \( L_p \) is visualized in Figure 2.3. When these two NESD and PLDD regions touch or overlap with each other (i.e., \( L_n + L_p \geq L_x \)), the NESD/PLDD junction takes over the N+/P-Well junction and becomes the dominant blocking junction. The order of magnitude of doping levels for N+, P-Well, NESD and PLDD are approximately \( 10^{20} \text{cm}^{-3} \), \( 10^{17} \text{cm}^{-3} \), \( 10^{19} \text{cm}^{-3} \) and \( 10^{19} \text{cm}^{-3} \), respectively. Since the depletion-region width of the NESD/PLDD junction is much smaller than that of the N+/P-Well junction under the same reverse-biased voltage, the former can breakdown at a smaller voltage than the latter, which is able to make the SCR device triggered at much lower voltage.

Figure 2.3 Schematic diagram showing the different cases of \( L_n + L_p \). \( L_x \) always keeps at 1\( \mu \text{m} \).
A high and tunable holding voltage is desirable for latch-up immunity. On the phenomenological level, the holding voltage depends on the degree of space charge neutralization in the base regions of the p-n-p and n-p-n BJTs due to free carriers injected from the emitter regions of the two BJTs. Hence, the lateral dimensions associated with the neutralization area and injection area are the key parameters in designing the holding voltage. For the uSCR shown in Figure 2.1, the holding voltage is tunable by changing the dimensions D3, D5, D6 and D8.

For the negative characteristic of the uSCR device, the reverse breakdown and conducting capability will be different when N-Well electrode is connected in two different ways. Keeping the terminals, Emitter-NPN and P-Well, connected together as Cathode and tied to ground, when N-Well is connected to Anode, the reverse breakdown voltage will approximate the turn-on voltage of forward-biased p-n junction and the conduction current can be relatively high. When N-Well is left open, the reverse breakdown voltage is about equal to VCEO of the parasitic PNP BJT and the conducting capability is low. The normal operation of uSCR is to keep N-Well connected to Anode. The connection way of N-Well open can be used to form a dual direction SCR [63].

2.3. Experimental Results and Discussions

uSCR devices have been fabricated on a 0.35-µm fully-salicided BiCMOS process (see Table 1.1). Their TLP I-V characteristics are plotted in Figure 2.4. The devices all have a width of 100 µm and L_x of 1µm, while L_n and L_p are varied. The distance of anode to cathode keeps at a (a has a value of more than 10 µm).
The trigger voltage $V_T$ is decreased from 14.24 to 7.16 V when $L_n + L_p$ increases from 0 to $1.5L_x$. Note that the trigger voltage is reduced more significantly when $L_n + L_p$ is increased beyond $L_x$. The leakage current $I_L$ increases with increasing $L_n + L_p$, but all $I_L$ are lower than $10^{-8}$ A. The holding voltage $V_H$ also decreases with increasing $L_n$ and $L_p$. The change of $L_n$ and $L_p$ alters only slightly the slope of the on-state I-V curve. The negative characteristic of the uSCR devices is like a forward-biased diode. The $I_{T2}$ listed in Table 2.1 are the failure current levels of the four uSCRs in the positive operation regions. The ESD robustness of the uSCR in both the positive and negative operations is high then 60 mA/μm.

When designing a snapback-type device, one of the most important things is to verify the tolerance of the device for process variation. Even for the same process, the I-V characteristic of the devices from different lots, wafers and dies will vary. The design goal is to make the device function ESD protection correctly with the process variation. For the uSCR device, the low trigger voltage is realized by dimension variation of $L_n$ and $L_p$, whose tolerance for aligning $L_n$ and $L_p$ was +/-5% and among the uSCR devices fabricated on four different wafers, alignment-induced variability in the trigger voltage was with +/- 1.5%.

Table 2.1 Lateral dimensions and TLP measurement results of the four uSCR devices with different $L_n + L_p$.

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>$L_n$, $L_p$, $L_x$</th>
<th>Anode to Cathode (μm)</th>
<th>$V_T$ (V)</th>
<th>$I_T$ (mA)</th>
<th>$V_H$ (V)</th>
<th>$I_H$ (mA)</th>
<th>$I_L$ (nA)</th>
<th>$I_{T2}$ (mA/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>uSCR-T1</td>
<td>$L_n = L_p = 0$</td>
<td>a</td>
<td>14.24</td>
<td>56</td>
<td>6.5</td>
<td>488</td>
<td>0.1</td>
<td>$\geq 60$</td>
</tr>
<tr>
<td>uSCR-T2</td>
<td>$L_n + L_p = 0.5L_x$</td>
<td>a</td>
<td>13.4</td>
<td>55</td>
<td>6.15</td>
<td>490</td>
<td>0.1</td>
<td>$\geq 60$</td>
</tr>
<tr>
<td>uSCR-T3</td>
<td>$L_n + L_p = L_x$</td>
<td>a</td>
<td>8.6</td>
<td>48</td>
<td>5.01</td>
<td>297</td>
<td>1.0</td>
<td>$\geq 60$</td>
</tr>
<tr>
<td>uSCR-T4</td>
<td>$L_n + L_p = 1.5L_x$</td>
<td>a</td>
<td>7.16</td>
<td>42</td>
<td>4.77</td>
<td>306</td>
<td>8.0</td>
<td>$\geq 60$</td>
</tr>
</tbody>
</table>
By using the uSCR-T3 device as a benchmark, three additional uSCR devices with different D5 but the same Ln and Lp were fabricated and the results are listed in Table 2.2 and their TLP I-V characteristics are shown in Figure 2.5. It can be seen that the holding voltage can be tuned from 5.01 to 7.46 V, whereas the trigger voltage keeps almost the same when D5 increases from b to 2.5b (“b” has a value of a few microns). In addition, listed in Table 2.2 is the anode-to-cathode spacing that ranges from a to 1.3a. The reason for the increased holding voltage is twofold. First, increasing D5 increases the collector thickness (in n-well) and, thus, increases the collector resistance of the n-p-n BJT. Moreover, increasing D5 also increases the base thickness (in p-well) and, hence, decreases the current gain of the n-p-n BJT. It is also noticed that with D5 increasing, the turn-on resistance increases because the current path becomes longer and the robustness of the device...
begins to degrade ($I_{T2}$ in positive region decreases). A multi-finger layout can be a solution to minimize such a drawback [63]. It should be pointed out that changing D3, D6, and D8 will alter the holding voltage only slightly. As a result, it is possible to design and implement a uSCR with a trigger/holding voltage window to be around 1 V.

Table 2.2 Lateral dimensions and TLP measurement results of uSCR-T3 devices with different D5.

<table>
<thead>
<tr>
<th>Cell Name</th>
<th>$L_n$, $L_p$, $L_x$</th>
<th>D5 (μm)</th>
<th>Anode to Cathode (μm)</th>
<th>$V_T$ (V)</th>
<th>$I_T$ (mA)</th>
<th>$V_H$ (V)</th>
<th>$I_H$ (mA)</th>
<th>$I_L$ (nA)</th>
<th>$I_{T2}$ (mA/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>uSCR-T3</td>
<td>$L_n + L_p = L_x$</td>
<td>b</td>
<td>a</td>
<td>8.60</td>
<td>48</td>
<td>5.01</td>
<td>297</td>
<td>1.0</td>
<td>$\geq 60$</td>
</tr>
<tr>
<td>uSCR-D2</td>
<td>$L_n + L_p = L_x$</td>
<td>1.5b</td>
<td>1.1a</td>
<td>8.63</td>
<td>52</td>
<td>5.9</td>
<td>308</td>
<td>1.0</td>
<td>$\geq 60$</td>
</tr>
<tr>
<td>uSCR-D3</td>
<td>$L_n + L_p = L_x$</td>
<td>2b</td>
<td>1.2a</td>
<td>8.61</td>
<td>48</td>
<td>6.5</td>
<td>290</td>
<td>1.0</td>
<td>47.1</td>
</tr>
<tr>
<td>uSCR-D4</td>
<td>$L_n + L_p = L_x$</td>
<td>2.5b</td>
<td>1.3a</td>
<td>8.55</td>
<td>50</td>
<td>7.46</td>
<td>258</td>
<td>1.0</td>
<td>43.5</td>
</tr>
</tbody>
</table>

Figure 2.5 Measured TLP I-V characteristics of the four uSCR devices listed in Table 2.2.
2.4. On-Chip Integration

The uSCR devices were integrated into a low-voltage IC and Figure 2.6(a) shows its on-chip ESD protection scheme. This uSCR device is designed for the \( V_{SS} \)-based ESD protection scheme as shown in Figure 1.8. The anode terminals of the uSCR devices are all connected to the pads and their cathode terminals are all connected to the common ground bus of the chip. The TLP results show the ESD robustness of uSCR is as high as 60 mA/\( \mu \)m at both positive and negative operation regions, the extra diode between supply and \( V_{SS} \) in supply ESD protection section and the primary ESD clamp for negative strikes in signal ESD protection section (in Figure 1.8) can be removed to save area. The die size of the test chip is 1000*800 \( \mu \)m\(^2\) the package type is 10-lead MicroPAK. The total width of the uSCR devices employed in this IC chip are all 100 \( \mu \)m. Figure 2.6(b) is the equivalent circuit schematic diagram of the layout showed in Figure 2.6(a). It illustrates the discharging current loops under the different JEDEC-standard HBM and CDM zaps. The diode inside each uSCR cell denotes the device when it is working in the negative operation. It can be seen that some discharging currents have to go through positive- and negative-direction uSCR cells, for example, in the case of the HBM zap of I/O pin vs. \( V_{cc} \). The robustness of the uSCR in both directions can protect the chip up to +/- 8 kV HBM and +/- 2 kV CDM stresses. Due to the robustness of the uSCR itself and no any externally-assisted circuitry, each uSCR cell only consumes an area of about 2400 \( \mu \)m\(^2\).
Figure 2.6 (a) Scheme of the on-chip ESD protection realized with the uSCR device. (b) Equivalent circuit schematic diagram of the layout showed in (a). It shows the discharge current loops under the different HBM and CDM zaps.

The proposed uSCR in this chapter with a trigger voltage lower than 8 V, a holding voltage higher than 6 V, an ESD robustness higher than 60 mA/μm and an HBM as well as a CDM ESD-protection levels as high as +/- 8 kV and +/- 2 kV, respectively, is one of the most advanced ESD devices to date for low-voltage ESD-protection applications.
2.5. Chapter Summary

As technology advances, the requirement for the trigger and holding voltages of the ESD devices becomes more stringent. This chapter starts with discussion of the triggering mechanism of the SCR device then presents a novel low trigger-/high holding-voltage SCR devices, called uSCR, which have been successfully designed, fabricated and characterized on a 0.35 μm BiCMOS process. Experimental results have verified that the trigger voltage can be reduced to less than 8 V without using any external trigger circuitry and that the holding voltage can be increased to more than 6 V without sacrificing the ESD robustness. The ESD robustness of the uSCR device makes it be used as an area efficient ESD protection cell in VSS-based ESD protection scheme. The area efficiency is realized by three factors:

1. The uSCR device itself is robust, with a $I_{T2}$ higher than 60 mA/μm at both forward and reverse operation region.

2. When apply the uSCR device in VSS-based ESD protection scheme, the extra diode for negative ESD strike can be removed, with relaying on the uSCR device to dump the ESD current of negative strike.

3. Comparing with VDD-based ESD protection scheme, the VSS-based ESD protection scheme dose not have to involve an ESD clamp between I/O pad and VDD.
CHAPTER 3. DEVELOPMENT OF HIGH HOLDING CURRENT SCR FOR HIGH VOLTAGE ESD PROTECTION APPLICATIONS

3.1. Introduction

High voltage technologies have been developed by extending mature, less expensive CMOS technologies (0.18 μm and above) with new features for specific automotive or consumer electronics products, etc, which offers significant economical advantages in this competitive market segment [76]. The new features, such as equipping the MOS transistors with thick gate oxides and lowly doped drain/source implants to increase the voltage tolerance of the devices, allows driving the maximum operating voltages to the limits of the process technology. The ESD protection cells for the high voltage technologies need to be able to withstand the high voltages. However, these new technology features will significantly degrade the high current performance of conventional protection devices.

ESD related issues in high voltage technologies including: 1) Strong snapback. The additional feature in high voltage technology, low doping implants, will strongly impact the snapback behavior of conventional snapback ESD protection device, like ggNMOS. The holding voltage of the ggNMOS for high voltage technologies are far away below operation voltage, $V_{DD}$. This is due to Kirk effect [77]-[78]. Also, the ggNMOS shows the immediate degradation after snapback. 2) Intrinsic high voltage NMOS reliability issues due to high voltage and high current applications. 3) Multi-finger non-uniformly triggering. The Murphy’s law always prefers to turn on one MOSFET finger ahead of any other ones. The condition, $V_{T1}$ (the trigger voltage) < $V_{T2}$
(the thermal runaway voltage), needs to meet to make other fingers come to play together before the first-turn-on finger fails, especially for the silicide technologies. It is hard to make $V_{T1} < V_{T2}$ valid in high voltage technologies [79]. 4) Latchup risk. Due to the strong snapback, transient latchup may occur due to the low holding voltage of the ESD protection cell. 5) High series resistance, which is due to the increasing critical distance in high voltage technologies to avoid punch through when the lightly doped diffusions make the depletion region wider. 6) The triggering competition between the weak output driver and the parallel ESD clamp are tougher in high voltage technologies.

We have discussed in previous chapters that the SCR device has long been used as a robust and area-efficient on-chip ESD protection device. Its inherent regenerative feedback mechanism leads to a deep-snapback characteristic with a relatively small holding voltage [80]. This reduces the power dissipation in the SCR during the ESD event and makes the SCR device more robust than other ESD devices such as diodes and GGNMOS [81].

The SCR device is one of the good candidate devices to be used for high voltage ESD protection [76]. When using SCR devices for ESD protection of high voltage ICs, the transient trigger voltage needs to be tailored to meet high voltage application. Also, the small holding voltage will become problematic, especially for the case of a supply clamp. The $V_{DD}$ is much higher for high voltage applications than that when the technology is for CMOS low voltage application, for example, $V_{DD}$ can be from 5 V to 65 V and higher. The low holding voltage would allow the SCR to remain in its low conductive state after the ESD event dissipated if the holding voltage is smaller than the supply voltage. And the SCR-based devices with low holding
voltage would interfere with the normal circuit operation when accidentally triggered on by noise pulses, which is known as the ESD-induced latchup [49].

There are two solutions to avoid such kind of latchup. One is to increase the holding voltage ($V_H$) to be greater than the maximum voltage supply of $V_{DD}$ [82]-[83], which either has to stack several ESD protection devices by consuming a large layout area [82] or has to sacrifice the robustness [83] which is right the advantage of SCR-based devices due to the relatively low holding voltage. Another solution is to increase the triggering current [68] or the holding current of the SCR devices [69]. As shown in Figure 3.1, if the SCR device has an holding current ($I_H$) higher than certain latchup-immune current ($I_{LU}$), the latchup due to ESD device false triggering can be avoided during normal operation as well as under the overshooting and undershooting noise pulses. Additionally, since the requirement of $V_H > V_{DD}$ can be dropped, the failure current ($I_{T2}$) of the SCR device can be higher, comparing with the other latchup-immune solution which requires $V_H > V_{DD}$. By doing this way, the big advantage of high failure current of the SCR device due to deep-snapback can be utilized well. Literature [68]-[69] have reported such SCR devices with high $I_H$ for latchup-free solutions, but both cases have to involve ground-gate MOS devices which normally will incur serious reliability weakness issues for high voltage technologies [76].
In this chapter, we will present a new high holding current SCR (HHC-SCR) device with a holding current as high as 24 mA/μm and a high failure current, $I_{T2}$, for high voltage applications without involving any external circuitry or extra devices. The avalanche multiplication factor ($M$) and the current gains of PNP and NPN bipolar transistors coupled in SCR devices are two factors to determine the holding current of SCR devices. The SCR device presented in this paper perform a high holding current by realizing an optimized balance between current gains and $M$. 

Figure 3.1 The comparison of generic characteristics of the high holding current and the high holding voltage snapback ESD protection cells within the ESD design window defined by the supply voltage ($V_{DD}$), $V_{max}$ and the latchup-immune current ($I_{LU}$).
3.2. Holding Current of SCR Devices

Figure 3.2 shows the cross-section view of a conventional triple-well SCR structure. There is no local oxidation of silicon (LOCOS) between the N+ region under terminal N-Well and the P+ region under terminal Emitter_PNP. Also, there is no LOCOS between the N+ region under terminal Emitter_NPN and the P+ region under terminal P-Well. It is well known such SCR device is a PNP-NPN coupled system and triggered by the avalanche breakdown of the base-collector junction which is N-Extension/P-Well junction in Figure 3.2. The avalanche current going through the both substrate resistances, $R_{N-Well}$ and $R_{P-Well}$, will raise the base-emitter biases of the PNP and NPN transistors to turn on both bipolar transistors in the end. Then the SCR device is triggered and enter conduction mode. The high avalanche breakdown voltage of the N-Extension/ P-Well junction ensures the SCR device to be triggered higher than 45 V for high voltage application.

Figure 3.2 The device cross-section view of the conventional SCR structure.
The SCR device physics before triggering has been discussed in detail in Chapter 2. Here will discuss the state after the SCR device triggers. Figure 3.3 is the equivalent circuit of the SCR device, showing all the directions of electron and hole currents after the SCR triggers, which means both PNP and NPN transistors turn on. $I_{\text{gen}}$ is avalanche generation current. $I_{\text{gen}}$ is a function of the avalanche multiplication factor, $M$, in the high electrical field region. $I_{\text{gen}}$ due to an incident current $I_p$ is given by [84]:

$$I_{\text{gen}} = (M - 1) \cdot I_p$$  \hfill (3.1)

$M$ is also expressed as Equation (2.13). Before SCR device triggers, $I_p$ is solely due to thermal generation and minority carrier diffusion. $I_{\text{gen}}$ only supplies the $I_{\text{SUB-PNP}}$ and $I_{\text{SUB-NPN}}$. As both bipolar transistors turn on, $I_{\text{gen}}$ will also supply $I_{B-PNP}$ and $I_{B-NPN}$ in additional to $I_{\text{SUB-PNP}}$ and $I_{\text{SUB-NPN}}$. But the bipolar current, $I_{C-PNP}$ and $I_{C-NPN}$, now provide additional current sources for multiplication. Equation (3.1) can be rewritten as:

$$I_{\text{gen}} = (M - 1) \cdot (I_p + I_{C-PNP} + I_{C-NPN})$$ \hfill (3.2)

Thus, the value of $M$ required to sustain both bipolar devices in the on states can be reduced and voltage snapback is observed where the voltage at Anode drops to a sustaining level, $V_H$. $I_{C-PNP}$ and $I_{C-NPN}$ are functions of current gains of both intrinsic PNP and NPN transistors, $\beta_{\text{PNP}}$ and $\beta_{\text{NPN}}$. The requirement that the SCR device stays latched is given by [85]:

$$M \left( \frac{1}{1 + \frac{1}{\beta_{\text{PNP}}}} + \frac{1}{1 + \frac{1}{\beta_{\text{NPN}}}} \right) \geq 1$$ \hfill (3.3)

The holding voltage $V_H$ is reached by coming to a balance between $M$ and $\beta_{\text{PNP}}$ & $\beta_{\text{NPN}}$. If the $\beta_{\text{PNP}}$ and $\beta_{\text{NPN}}$ are bigger, which means $I_{C-PNP} + I_{C-NPN}$ (see equation (3.2)) will be bigger, the $M$
will be less resulting a smaller $V_H$, vice versa. The corresponding current when the SCR device reaches $V_H$ is the holding current, $I_H$, which can be expressed as (as shown in Figure 3.3):

$$I_H = I_{SUB-PNP} + I_{E-PNP}$$  \hspace{1cm} (3.4)

$$I_{SUB-PNP} = I_{gen} + I_{C-NPN} - I_{B-PNP}$$  \hspace{1cm} (3.5)

Since the $I_p$ is much smaller comparing with $I_{C-PNP}$ and $I_{C-NPN}$ after the device turns on, we can get the relationship:

$$I_{gen} \approx (M - 1) \cdot (I_{C-PNP} + I_{C-NPN}) = I_{gen}$$ \hspace{1cm} (3.6)

$$I_{E-PNP} = \frac{I_{C-PNP}}{\alpha_{PNP}}$$ \hspace{1cm} (3.7)

$$I_{B-PNP} = \frac{I_{C-PNP}}{\beta_{PNP}}$$ \hspace{1cm} (3.8)

By replacing (3.6), (3.7), (3.8) and (3.9) in (3.5), we finally have:

$$I_H = M \cdot (I_{C-PNP} + I_{C-NPN})$$ \hspace{1cm} (3.9)

As the aforementioned, an increasing of $I_{C-PNP} + I_{C-NPN}$ will normally cause $M$ decreasing. So the high holding current will be realized by designing a SCR structure with a maximal $M(I_{C-PNP} + I_{C-NPN})$, which means to find an optimized combination of $M$ and $\beta_{PNP}$ \\& $\beta_{NPN}$. 


Figure 3.3 The equivalent circuit of the SCR device, showing the directions of all electron and hole current components after the both PNP and NPN transistors turn on.

3.3. Device Structure, Experimental Results and Discussions

The top view of the proposed HHC-SCR device is shown in Figure 3.4(b). Figure 3.4(a) is the top topology of the conventional SCR device, corresponding to the cross section view in Figure 3.2. Its well tie and emitter tie for both PNP and NPN transistors are strips. Both devices shown in Figure 3.4(a) and (b) have D3=D4=8 micron and D1=D2=D5=D6= 1.6 micron. In order to realize high holding current, we have to increase the $\beta_{PNP}$ & $\beta_{NPN}$ while without decreasing $M$ that much. Comparing with the conventional SCR device (Figure 3.4 (a)), the
The proposed HHC-SCR device gets rid of the strips of N-Well tie and P-Well tie and inserts the well ties into the strips of emitter ties of both PNP and NPN transistors, realizing a pattern of intermittent well tie and emitter tie. By doing this, the lengths of base region of both transistors are reduced, which will result in the increased $\beta_{\text{PNP}}$ & $\beta_{\text{NPN}}$. Also, the intermittent pattern reduced the effective emitter areas of both transistors such that the emitter injection efficiencies are decreased. The impact ionization has to be more intensive to get enough $I_{\text{gen}}$, which will incur a higher $M$ and higher holding voltage, $V_H$.

![Diagram of SCR devices](image)

Figure 3.4 The top view of the SCR devices. (a) Strip topology of conventional SCR, (b) segmented topology of high holding current SCR (HHC-SCR), (c) modified HHC-SCR with a well tie removed from each strip with an interval of every two well ties, and (d) modified HHC-SCR with a well tie removed from each strip with an interval of every well tie.
Figure 3.6. shows the TLP I-V characteristic of the proposed HHC-SCR as well as the conventional SCR device and the SCR device reported in [83] with the segment ratio of 1:1. Test devices were fabricated on the BiCMOS 0.6 μm process and all have a total width of 100 μm. Figure 3.5 illustrates the segmented topology of the device in [83] for comparison. The device shown in Figure 3.5 also has D3=D4=8 micron and D1=D2=D5=D6=1.6 micron. The conventional SCR device triggers at 45 V. Its holding voltage is very low at 5.5 V which give the device the high IT2 which is higher than 50 mA/μm. From the conventional SCR to the SCR device in [83], the injection efficiency has been reduced significantly, so IC-PNP + IC-NPN has been reduced a lot while M has to increase significantly to maintain an enough Igen. As a compensation result, IH of the SCR device in [83] doesn’t change a lot but a high holding voltage of 45 V is reached. Comparing with the SCR device in [83], the proposed HHC-SCR keeps the same injection efficiency but has a higher βPNP and βNPN, which will give a higher IC-PNP + IC-NPN, which causes M dropping a little to realize a maximal M(IC-PNP+IC-NPN), which means the best combination of M and βPNP & βNPN to realize the highest high holding current (refer to Equation (3.9)). The HHC-SCR device has performed a holding current as high as 24 mA/μm, which can effectively avoid latch-up without having to increase the holding voltage higher than the maximum supply voltage when using a such device for ESD protection applications. Such a high holding current is much higher than those having been reported in [68] and [69]. The leakage current of the HHC-SCR device is at nA range and the turn-on resistance is pretty low. In additional, with a lower M, the HHC-SCR device has a lower holding voltage, 22 V, which gives a higher ESD robustness comparing with the device in [83]. The IT2 of HHC-SCR is 48.8 mA/μm
versus 28 mA/μm in [83] which relies on increasing $V_H$ to be higher than $V_{DD}$ to realize the latchup immunity. And the $I_{T2}$ of HHC-SCR is almost as good as that of the conventional SCR.

![Diagram](image)

Figure 3.5 The illustration of the segment topology of the SCR device reported in reference [83].

The further increasing of $\beta_{PNP}$ and $\beta_{NPN}$ are also performed to verify the maximal $M(I_{C.\text{PNP}}+I_{C-NPN})$ has been reached. Taking the proposed HHC-SCR in Figure 3.4(b) as a benchmark, which has a $D3=D4=8$ micron, $D3=D4$ is reduced from 8.0 micro to 2.0 micron, which cause $\beta_{PNP}$ and $\beta_{NPN}$ increasing. Figure 3.6 shows the TLP measurement results of HHC-SCR with different $D3$ and $D4$. It can be seen that when $D3=D4$ decrease, the lengths of base region of both transistors are reduced, which will result in the increased $\beta_{PNP}$ & $\beta_{NPN}$ then the increased $I_{C.\text{PNP}} + I_{C-NPN}$. However, the holding voltage decreases since $M$ has decreased. As the result, the overall holding current, which is the product of $M$ and $I_{C-\text{PNP}} + I_{C-NPN}$, drops from 24 mA/μm to
12 mA/μm. So the HHC-SCR with D3=D4=8 micron has a maximal $M(I_{C,PNP}+I_{C,NPN})$ to realize the highest holding current. One thing worthy to point out is that when D3=D4 decrease, the effective substrate resistances, $R_{N-Well}$ and $R_{P-Well}$, also decrease, which will require higher triggering current as well as holding current to turn on and to sustain the SCR on-state according to [68] and [69]. But the decreasing of $R_{N-Well}$ and $R_{P-Well}$ here has not been able to be a dominant factor to not to let holding current drop.

![Leakage Current (A) vs Voltage (V) graph](image)

Figure 3.6 TLP measurement results of the conventional SCR, the SCR presented in [83] and HC-SCR devices with different D3=D4.

Another important observation is that when getting rid of some blocks of well tie at both Anode and Cathode sides, the holding current and the holding voltage will also decrease. In
Figure 3.4(c), a well tie is removed with an interval of every two well ties. And in Figure 3.4(d), a well tie is removed with an interval of every well tie. Figure 3.7 shows their I-V characteristics versus the HHC-SCR device. From the HHC-SCR to the pattern Figure 3.4(c) and Figure 3.4(d), the effective well resistances, $R_{N-Well}$ and $R_{P-Well}$, increase. Consequently, less base current is required to reach forward bias of the corresponding emitter-base junctions, then a lower trigger current as well as a lower holding current result. Also, when getting rid of more and more well-ties, the $\beta_{PNP}$ and $\beta_{NPN}$ also increase. So $M$ will decrease and the holding voltage is reduced. The overall holding current drops.

Figure 3.7 TLP measurement results of the HHC-SCR device and the two modified HHC-SCRs shown in Figure 3.4(c) and (d).
3.4. Chapter Summary

Preventing latchup is an important issue in the design and realization of on-chip ESD protection solutions for high voltage integrated circuits. This can be achieved by using ESD devices having a high holding voltage and/or high holding current. To this end, a novel high holding current SCR (HHC-SCR) has been presented in this chapter for high voltage applications and test devices have been fabricated on the BiCMOS 0.6 μm process. The holding current of SCR device is dependent on the avalanche multiplication factor, $M$, and the current gains of the PNP and NPN transistors in SCR device. The TLP measurement results have shown that by reaching a maximal $M(I_{C,PNP}+I_{C,NPN})$, the HHC-SCR device has realized a holding current as high as 24 mA/μm to effectively avoid latch-up and a high failure current (48 mA/μm) for ESD robustness. Additionally, without involving any external circuitry or extra devices, the HHC-SCR device releases reliability weakness issues and accomplishes the minimum area consumption.
CHAPTER 4. COMPREHENSIVE COMPACT MODELING OF SCR DEVICES FOR CDM ESD SIMULATION OF COMPLETE I/O CIRCUITS

4.1. Introduction

The CDM ESD event has been discussed in Chapter 1. The first use of CDM test method was reported in by Bossard et al. in [86]. The increased usage of automated manufacturing and testing equipment has led to environments that are more likely to have the presence of the CDM ESD event, rather than the more well-known HBM. As such, the CDM is becoming more and more widely used for defining the ESD stress and reliability in the semiconductor industry. The CDM possesses pulses that can reach several Amps in a few tenth of nano second. In addition the waveform of the current associated with the CDM is oscillatory (see Figure 1.6). These issues make the development of an accurate and compact model for CDM ESD devices very difficult, but such a model is urgently needed in the research and development of effective and robust CDM ESD protection solutions for a wide range of integrated circuits.

Normally, the ESD protection SCR devices have been designed through simulations by using either technology computer aided design (TCAD) tools or through experimental approach, which is also called trial-and-error iterations. The former is normally time-consuming and it is difficult to include both ESD protection cells and the protected core circuits into the TCAD simulation. The latter way also has to wait the entire cycle of test chip to get results and cost more money to run more rounds of trial if the first round doesn’t succeed. Additionally, there is interaction between ESD protection cells and core circuits. On one hand, ESD protection cell
will incur adverse parasitic effects to core circuits, such as extra parasitic capacitance and noise, which is a disaster especially for high speed and radio frequency (RF) ICs. On the other hand, the performance of ESD protection cells will be impacted by core circuits. A working stand-alone ESD protection unit does not warrant chip level ESD protection. So comparing with device simulations and iterative experiments, design engineers prefer to employ compact models in a circuit simulator to get faster prediction of the ESD protection level of the whole chip and do co-design of the ESD and functional circuitry at the pre-silicon stage.

Even though SCR is one of the most important ESD protection devices, SCR compact model is not widely available since most available design tools, such as SPICE, do not contain the standard model of SCR and SCR devices for ESD protection operate in high-current and breakdown regimes which regular circuit models do not cover. A few SCR compact models have been reported in the literature. Juliano and Rosenbaum developed a model based on the Verilog-A coded behavior modeling to describe the SCR snapback [87]-[88], but a smoothing function has to be used to ensure continuity. Another model was built from a macromodel consisting of existing device models, but additional auxiliary current and voltage sources have to be added to properly describe the breakdown behavior in the SCR [89]-[90], an approach that is hard-coded in simulators and lacks flexibility when the technology is changed. Zhou et al. mentioned that an advanced BJT model can be used as the backbone for the SCR compact modeling [91]-[92]. This model doesn’t describe the CDM-relevant features, such as the device characteristics in negative operation and the substrate element modeling. Therefore it is not applicable for the simulation of I/O circuits subject to the CDM ESD stress.
In this chapter, we seek to develop a comprehensive compact model for the high-holding, low-triggering SCR (HH-LVTSCR) [93] used to provide CDM ESD protection at the I/O pin of CMOS circuits. Section 3.2 will focus on model development and model implementation, as well as the discussion of apposite model parameter extraction. Special attention is given to accurately describing the CDM-relevant operation states. This is followed by the presentation of the modeling results and verification for SCR operations based on TLP technique in Section 4.3. In order to achieve accurate simulation of CDM events, proper characterization of the CDM tester is just as critical as the device modeling. A JEDEC-standard CDM waveform created by a calibrated series RLC circuit is presented in Section 4.4. And this section will demonstrate the application of the new SCR model on a 0.35 μm CMOS circuit under the CDM stress, and the model will successfully explain as to why the input-only pins of the circuit have lower CDM robustness than the output-only pins [94].

4.2. SCR Compact Model Development

The cross section of a HH-LVTSCR is shown in Figure 4.1(a). The device is considered here to illustrate the model development, but the modeling approach applies generally to other SCR devices. The terminal connection of the HH-LVTSCR device in typical ESD applications is shown in Figure 4.1(a) as well. The N-Well and Emitter-PNP terminals are connected to the Anode. The Gate, Emitter-NPN, P-Well and Substrate terminals are tied together to be the Cathode.
Figure 4.1 (a) Cross-section view of the HH-LVTSCR and (b) equivalent circuit of the HH-LVTSCR.

4.2.1. Equivalent Circuit of SCR

Macromodeling will be used in this work, as it is highly suitable for modeling a device, like the SCR, having a complex structure that is difficult to describe with closed-form analytical equations.
The HH-LVTSCR is an NPN-PNP bipolar transistor coupled device and triggered by the avalanche breakdown of the NMOS-drain-bulk junction which is also the base-collector junction of the NPN and PNP transistors. In addition to the NPN and PNP BJTs, the SCR macromodel consists of a parasitic PNP BJT, an NMOS, a diode, and several resistors, as shown in Figure 4.1(b). The NPN BJT including the parasitic PNP BJT, PNP BJT, and NMOS are described by the vertical bipolar inter-company (VBIC), SPICE Gummel-Poon (SGP), and Berkeley short channel IGFET 3v3 (BSIM3v3) models, respectively. The reason for using the VBIC model for the NPN BJT is that it is more advanced and comprehensive than the conventional GP model, and includes a parasitic PNP component. The schematic of the macromodel is illustrating in Figure 4.2, showing the detailed connections of all internal nodes.

Figure 4.2 Schematic of the HH-LVTSCR macromodel with all model elements included, showing the detailed connections of all internal nodes.
4.2.2. Substrate Parasitic Modeling

The CDM testing requires that the substrate of the device under test is charged either directly or indirectly to the specified voltage. One of the input or output pins is then grounded, and the behavior of the device during the subsequent high current discharge determines its CDM ESD robustness [24][25].

The terminal connection of the HH-LVTSCR is as Figure 4.1(a). If the substrate of the SCR is positively charged and the anode is grounded, then the P-Substrate/N-Well junction is forward biased and current flows through the forward biased junction. Since the Emitter-NPN and P-Well terminals are also tied to the substrate, the current will also pass through the forward biased P-Well/N-Well junction. Additionally, the Emitter-NPN/P-Well junction is being reverse-biased and the NPN transistor can be turned on. The discharge current flows both laterally and vertically. On the other hand, if the device is negatively charged and the anode is grounded, the HH-LVTSCR triggers in the normal manner, where the junction breakdown followed by the base voltage raise of NPN and PNP transistors will result in the SCR being triggered [95].

Based on the above discussion, a diode, Dsub, is integrated into the macromodel schematic to model the P-Substrate/N-Well junction (see Figure 4.1). In addition, P-Well, N-Epi and P-Substrate also forms a substrate parasitic PNP transistor which has been included in the VBIC NPN model. The VBIC model includes an intrinsic NPN transistor and a parasitic PNP transistor. So no extra PNP transistor is needed to insert into the macromodel of Figure 4.1. This is one advantage of using VBIC to model the NPN transistor.
4.2.3. Substrate Resistance Modeling

The important factors for SCR triggering are the substrate resistance $R_{N\text{-Well}-1}$ and $R_{P\text{-Well}}$ (see Figure 4.1). Before device triggering, the reverse saturation current of the blocking junction mainly goes through these two resistances, as shown by dashed line in Figure 4.1(b). The current level is very low. After device is triggered, appreciable current is injected into the N-Well and P-Well from the terminal Emitter-PNP and Emitter-NPN to cause conductivity modulation. Little current passes by $R_{N\text{-Well}-1}$ and $R_{P\text{-Well}}$. The current path is as dotted line in Figure 4.1(b). So the resistance $R_{N\text{-Well}-1}$ and $R_{P\text{-Well}}$ can be assumed to be constant independent of bias. There are another two substrate resistances, $R_{N\text{-Well}-2}$ and $R_{\text{sub}}$ (Figure 4.1), which are associated with $D_{\text{sub}}$.

4.2.4. Negative Characteristic Modeling

The negative characteristic of the HH-LVTSCR is like a forward-biased diode, as the TLP measurements in Figure 4.4. With the terminal connection as in Figure 4.1, when under the reverse bias, the P-Well/N-Well and P-Substrate/N-Well junction diodes are forward biased and diode-mode conduction results. The P-Substrate/N-Well junction has been modeled by $D_{\text{sub}}$. The current path going through $D_{\text{sub}}$ under reverse bias is denoted as P1 in Figure 4.1(a). The P-Well/N-Well junction is the base-collector junction of the PNP transistor as well as the NPN transistor. It has been modeled within the respective SGP model and VBIC model. The current path going through P-Well/N-Well junction diode under reverse bias is denoted as P2 in Figure 4.1(a). There is one more current path going through the base-collector junction of the Parasitic-PNP transistor built in VBIC, denoted as P3.
The SGP model is normally sufficiently accurate for the PNP BJT. We have found that, if the GP model is used for the NPN transistor, which means there are only current path P1 and P2, the simulation results can not fit the TLP measurement results since the coupled PNP and NPN transistor models can not function correctly as a forward biased diode under reverse bias. If we add an extra diode parallel with $D_{sub}$ to fit the negative characteristic of the device, the added diode will double-model the P-Well/N-Well junction and the positive characteristic of the macromodel will be affected.

With the built-in parasitic PNP transistor, we have additional current path, P3, parallel with P1 and P2 to conduct more reverse current. The VBIC model parameters, $R_S$, $R_{BP}$ and $R_{CX}$ (see Figure 4.2) can be tweaked to make the model to fit the negative characteristic.

### 4.2.5. Avalanche Current Modeling

The avalanche breakdown mechanism controls the SCR triggering and SCR conduction after the snapback. In the conventional approach in which a SCR is modeled with two coupled PNP and NPN bipolar transistors using the SGP model, an avalanche generation current source has to be inserted in parallel with the base-collector junction, which is the $N^+/P$-Well junction in Figure 4.1(a), to properly characterize the junction breakdown [89]-[90]. A classical expression for such a current source $I_{BRK}$ is given by [96]:

$$I_{BRK} = I_F \cdot \left( \frac{1}{1 - \left( \frac{V_{BC}}{V_{BRK}} \right)^n} - 1 \right)$$

(4.1)

$V_{BRK}$ is the breakdown voltage of the base-collector junction, $V_{BC}$ is the voltage drop across this junction, $I_F$ is the leakage current, and $n$ is typically equal to 2. However, behavior languages or
special setups in CAD simulators are needed to implement such a current source, which could significantly lower the simulation speed and may cause convergence problems.

Our approach of integrating the VBIC and BSIM models has alleviated this shortcoming, as all the necessary avalanche current sources are imbedded in the equivalent circuit in Figure 4.2 [98]. In BSIM3v3 model, the substrate current $I_{sub}$ is given by [97]-[98].

$$I_{sub} = \left( \alpha_{i} \cdot \frac{\alpha_{0}}{L_{eff}} \right) (V_{ds} - V_{dseff}) \exp \left( -\frac{\beta_{0}}{V_{ds} - V_{dseff}} \right) I_{dss}$$  \hspace{1cm} (4.2)

Where $L_{eff}$ is the effective channel length of the MOS, $V_{dseff}$ is the effective drain-source voltage, $V_{dssat}$ is in the saturation drain-source voltage, $I_{dss}$ is the drain current without considering impact ionization, and $\alpha_{0}, \alpha_{i},$ and $\beta_{0}$ are fitting parameters associated with impact ionization coefficients and $I_{sub}$ scalability. The avalanche current of the base-collector junction of the BJT is available in the VBIC model given by [99]-[100]:

$$I_{ave} = (I_{cc} - I_{bc}) \cdot AVC1 \cdot V_{t} \cdot e^{-AVC2 \cdot V_{bci}}$$  \hspace{1cm} (4.3)

$$V_{t} = \frac{1}{2} \left[ \sqrt{(PC - V_{bc})^2 + 0.01 + (PC - V_{bc})} \right]$$  \hspace{1cm} (4.4)

where $I_{cc}$ is the forward transport current, $I_{bc}$ is the base/collector current shown as $I_{cc}$-NPN and $I_{bc}$-NPN current sources in Figure 4.2, $(I_{cc} - I_{bc})$ is the collector current without avalanche, $PC$ is the junction built-in potential, $MC$ is the junction grading coefficient, $V_{bci}$ is the intrinsic voltage drop over the junction, and $AVC1$ and $AVC2$ are fitting parameters.

These two parallel current sources in Equation (4.2) and Equation (4.3) correctly model the avalanche generation current during the device triggering. In addition, they have similar exponential voltage dependence and provide more fitting parameters to work with than using the
current source in Equation (4.1), which offer more control on the avalanche current to model the
snapback accurately. Moreover, without the need of any external current source, the
implementation of the macromodel is much simpler. In principle, the macromodel in Figure 4.2
can be implemented in any circuit simulator containing advanced MOS and BJT models. The
simplicity of this modeling approach offers advantages of higher simulation speed, more
flexibility, and less convergence issues.

4.2.6. High-Level Injection Modeling

After the device is triggered, considerable electrons and holes are injected from the
emitters of NPN and PNP transistor, and the SCR resistance is reduced significantly. The high-
level injection can also give rise to base pushout and conductivity modulation in the collector.
This effect is accounted for in the VBIC model with the quasi-saturation components. The quasi
saturation behavior is modeled with the resistor element $R_{ci}$ and charge elements $Q_{bc}$ and $Q_{bcx}$
(see Figure 4.2). The quasi-saturation model consists of the current in the intrinsic collector
region (N-Epi region in Figure 4.1):

$$I_{epi} = \frac{V_{rei} + \frac{kT}{q} \left[ K_{hei} - K_{hei} - \ln \left( \frac{K_{hei} + 1}{K_{hei} + 1} \right) \right]}{RCI}$$  \hspace{1cm} (4.5)

$$K_{hei} = \sqrt{1 + GAMM \cdot e^{qV_{rei} / kT}}$$  \hspace{1cm} (4.6)

$$K_{bcx} = \sqrt{1 + GAMM \cdot e^{qV_{bcx} / kT}}$$  \hspace{1cm} (4.7)

$$V_{rei} = V_{hei} - V_{bcx}$$  \hspace{1cm} (4.8)
RCI is the intrinsic collector resistance, GAMM is the epi doping parameter, and \( V_{bci} \) and \( V_{bcx} \) are equal to \( V_{bi} - V_{ci} \) and \( V_{bi} - V_{cx} \), respectively. The intrinsic collector resistance \( R_{ci} \) is not formulated explicitly. Instead, the current \( I_{rci} \) passing through \( R_{ci} \) is expressed as [99]-[100]:

\[
I_{rci} = \frac{I_{epio}}{1 + \left( \frac{I_{epio} \cdot RCI}{0.5 \cdot (V_{rci}^2 + 0.01)^{1/2}} \right) + \left( \frac{V_{bi} - V_{ci}}{HRCF} \right)}
\]

(4.9)

where \( V_{bi} \) is the epi drift saturation voltage and \( HRCF \) is the high current factor.

### 4.2.7. Capacitance Modeling

The principal dynamic behavior of the device is modeled by both the non-linear junction and diffusion capacitances. Correctly modeling those capacitances is important to make the SPICE simulation results predictable when running the transient simulation for the complete I/O circuit. This is especially crucial when the transient stress is CDM.

As shown in Figure 4.2, there are a bunch of capacitances within the macromodel. They have been modeled respectively by VBIC, SGP and BSIM3v3 and the associated model parameters are extracted through the standard extraction process of each model, but the correct “coupling” between the different capacitances has to be decided.

The base-emitter and base-collector junction charges of the PNP transistor are modeled by \( Q_{be-PNP} \) and \( Q_{bc-PNP} \) in the SGP model (see Figure 4.2). The parasitic capacitance of the base-substrate junction is taken care of by \( Q_D \) in the diode component \( D_{sub} \), and all the model parameters associated with the base-substrate capacitance in the SGP model are set to zero.
In the VBIC NPN transistor model, the base-emitter and base-collector dielectric overlap capacitances, CBEO and CBCO, originated from the double-poly BJT process, which is not applicable for the NPN transistor considered here. So these capacitances are set to zero. The base-emitter and base-collector junction charges are modeled by the intrinsic and extrinsic portions which are \( Q_{bc-NPN} \) and \( Q_{bex} \), and \( Q_{bc-NPN} \) and \( Q_{bex} \), respectively (see Figure 4.2). The PNP transistor and the NPN transistor share the same base-collector junction, so the base-collector junction charge should not be modeled twice by the VBIC and SGP models. Since the VBIC has more advanced base-collector capacitance model than the SGP, we keep the initially extracted model parameters for \( Q_{bc-NPN} \) and \( Q_{bex} \) the same, but set the model parameter CJC in the GP model to a very small value, say 0.1% of the original value. \( Q_{bc-NPN} \) and \( Q_{bex} \) in VBIC are given by [99]-[100]:

\[
Q_{bc} = Q_{jc} + TR \cdot I_{tri} + QCO \cdot K_{bci} \tag{4.10}
\]

\[
Q_{bex} = QCO \cdot K_{bex} \tag{4.11}
\]

\( Q_{jc} \) is the depletion charge and \( TR \cdot I_{tri} \) is the diffusion charge where \( TR \) is the reverse transit time and \( I_{tri} \) is the reverse transport current. The terms of \( QCO \cdot K_{bci} \) and \( QCO \cdot K_{bex} \) are not included in the SGP model and are used to describe the charge associated with the effect of high level injection, a dominant mechanism after the SCR device is triggered.

BSIM3v3 also has the sophisticated capacitance models as illustrated in Figure 4.2 [97]-[98]. All the model parameters associated with capacitances are kept the original extracted value in order to get the correct transient response of the generation current.
4.2.8. Parameter Extraction

Contacts for all the seven terminals, N-Well, Emitter-PNP, Drain, Gate, Emitter-NPN, P-Well and Substrate are made in order to carry out parameter extractions. Different terminals are used and biased for the parametric tests of different models, as illustrated in Figure 4.3. Industry standard software tool Integrated Circuit Characterization and Analysis Program (IC-CAP) is used for the parameter extraction of VBIC, SGP and BSIM3v3. The model parameters are extracted from the I-V and C-V characteristics measured by parameter analyzer with following the standard model extraction strategies in IC-CAP user manual and BSIM3v3 user manual [97], [101]-[103]. Special emphasis has been placed on the substrate current and the avalanche breakdown current. The parameters associated with the generation current, $a_0$, $\alpha_1$ and $\beta_0$ in BSIM3v3 as well as $AVC1$ and $AVC2$ in VBIC, are first extracted following the respective standard algorithm. Based on the forward output I-V characteristics in avalanche breakdown region (at high $V_{ce}$), we can carry out the extraction and optimization of the parameter $AVC1$ and $AVC2$. Then the two parameters are optimized to fit the curve of $I_c/g_0$ versus $V_{ce}$, $V_{ce}$. Subsequently, the above 5 fitting parameters are tweaked slightly to fit the measured snapback curves. An advantage of the macromodeling approach, especially for industry applications, is that it allows reusing of the already available accurate lumped models and parameter extraction for the non-ESD domain of device operation.

The parameter extraction of the parasitic PNP transistor was done concurrently during the standard VBIC model parameter extraction. $D_{sub}$, it is not suitable to use the 7-terminal structure in Figure 4.3 to do measurement for model extraction. However, P-Substrate/N-Well junction is one of the most important elementary junctions for the process. $D_{sub}$ comprises the parasitic
portion of the macromodels of the most valid devices. So it normally has been modeled for the standard devices by design a specific structure to extract the characterization of the P-Substrate/N-Well junction. The parameters are available to be used for the presented SCR mode.

The VBIC model parameters, RS, RBP and RCX (see Figure 4.2) will be tweaked to make the model to fit the ESD conduction in the negative direction.

The value of $R_{P-Well}$ can be extracted from the forward-bias slope of the diode curve obtained by grounding the Drain and Emitter-NPN terminals and biasing the P-Well terminal. For extraction of $R_{N-Well-1}$, the MEDICI TCAD tool is employed to calculate the sheet resistance, $R_s$, of the n-well segment of the SCR structure in Figure 4.1. The value of $R_{N-Well-1}$ is equal to $R_s$ times the length-to-width ratio. The other two substrate resistances $R_{N-Well-2}$ and $R_{sub}$ (Figure 4.1), which are associated with $D_{sub}$, can also be calculated by multiplication of the relevant sheet resistance with the length-to-width ratio.
Figure 4.3 Different terminal configurations for the parameter extraction of different transistor models.

4.3. TLP Results and Discussions

HH-LVTSCR devices as in Figure 4.1 with a width of 100 micron were fabricated in a 0.35-μm /3.3-V fully salicided BiCMOS process. Model parameters of VBIC, SGP, and BSIM models were extracted and adjusted. The macromodel was implemented into the industry standard Cadence SPICE, and simulations were carried out using pulses as the input. For
measurement, Barth-4002 TLP pulse generator was used, and the rise time and width of TLP pulses were 8 ns and 100 ns, respectively. The same pulses were also considered in simulations.

In Figure 4.4, an excellent match between the measured and simulated TLP I-V characteristic is obtained for both the forward and reverse directions. In the positive direction, the SCR triggers at 9.4 V and holds at 5 V, while the SCR turns on at 0.7 V and without snapback in the reverse direction. Figure 4.4 also shows the simulation result of the macromodel presented by Zhou et al. [92] with using the same model parameter set and the same setup of simulation deck as the presented SCR macromodel. In Zhou et al.’s model, the substrate terminal of the BJT is tied high to form the Anode of the SCR. Without adding a PNP transistor in his macromodel, Zhou et al. just used the parasitic PNP and the intrinsic NPN transistors to form the SCR. But VBIC model does not include a complete gummel-poon transistor for the parasitic PNP. The parasitic transport current $I_{\text{tcp}}$ (Figure 4.2) models the substrate current when the intrinsic transistor goes into saturation. It is given by [99]-[100]:

$$ I_{\text{tcp}} = \frac{(I_{\text{tfp}} - I_{\text{trp}})}{Q_{\text{bp}}} \tag{4.12} $$

$$ I_{\text{tfp}} = WSP \cdot ISP \cdot \left( e^{V_{\text{bep}}/(NFP \cdot \tau_t)} - 1 \right) + (1 - WSP) \cdot ISP \cdot \left( e^{V_{\text{bec}}/(NFP \cdot \tau_t)} - 1 \right) \tag{4.13} $$

$$ I_{\text{trp}} = ISP \cdot \left( e^{V_{\text{bec}}/(NFP \cdot \tau_t)} - 1 \right) \tag{4.14} $$

$$ Q_{\text{bp}} = \frac{1}{2} \left( 1 + \frac{1}{\sqrt{1 + 4Q_{2p}}} \right) \tag{4.15} $$

$$ Q_{2p} = \frac{I_{\text{tfp}}}{IKP} \tag{4.16} $$
$I_{tp}$ and $I_{rp}$ are the parasitic forward and reverse transport currents, $WSP$ is the portion of $I_{ccp}$ from $V_{bep}$, $ISP$ is parasitic saturation current, $NFP$ is parasitic forward emission coefficient, $Q_{bp}$ is parasitic normalized base charge, and $IKP$ is parasitic knee current. It can be seen that $Q_{bp}$ only includes high-level forward injection, not including the early effects and high-level reverse injection. However, the parasitic PNP in Zhou et al.’s model is working in reverse active mode which the parasitic model doesn’t model. So the model can not fit the measurement data in positive operation very well.

The configuration of Zhou et al.’s maromodel doesn’t have efficient current path to describe the device characteristic in negative operation. That’s why the negative characteristic is far away from the measurement data. Also, the simulation results show the major portion of the negative current comes from the impact ionization of source-to-bulk junction of the NMOS transistor built in the macromodel, not coming from the forward biased diode.

Figure 4.5(a) and (b) compare the measured and simulated transient responses of the TLP voltage and current, respectively, in the SCR right after triggering point. The pad voltage reaches a peak value of 9.42 V and then is decreased to 5.11 V (holding voltage) before it is turned off. The pad current, on the other hand, reaches a maximum value of 218 mA after the device turns on.
Figure 4.4 Simulated and measured TLP I-V characteristics of the HH-LVTSCR.

Figure 4.6 shows the simulation results of the transient response of the pad voltage using the presented SCR macromodel under very-fast TLP (VFTLP) condition with a rise-time of 250 ps at a current level of 1A. The waveform demonstrates a significant voltage overshoot at the beginning of the pulse.
Figure 4.5 (a) Simulated and measured time-dependent pad voltages and (b) simulated and measured pad currents right after the SCR triggering.

Figure 4.6 The simulated pad voltage under VFTLP pulse at a steady-state current of 1A.
Figure 4.7(a) and (b) show the simulated voltages and currents, respectively, versus the input voltage of the internal nodes of the PNP and NPN transistors. It can be seen in Figure 4.7(a) that, before the SCR triggers, the voltages between the emitter and collector of the both transistors increase with increasing input voltage and the base-emitter voltage is lower than the turn-on voltage (the typical value is 0.7 V). After the SCR turns on, the emitter-collector voltages reduce significantly and keep around 4 V while the base-emitter voltages are in the range of 1-2 V. Note that the base-emitter voltages of both transistors after the triggering are much higher than those of the BJT transistors under normal analog applications. This means the free-carrier injection level in the SCR is extremely high. For the current, we can see in Figure 4.7(b) that very little current goes through both transistors before triggering, while after triggering both transistors conduct the majority of the current associated with the ESD stress.
Figure 4.7 Simulated (a) base-emitter and collector-emitter voltages of the PNP and NPN transistors and (b) emitter, base and collector currents of the PNP and NPN transistors.

4.4. CDM Transient Simulation of I/O Circuit

4.4.1. CDM Pulse Circuit

The CDM event can be emulated using the equivalent circuit in Figure 4.8 consisting of a capacitance, inductance, resistance, and a JEDEC-specified small target made of a piece of metal with a resistance of about 45 ohm. The current waveform associated with the CDM discharge process depends on the values of the RLC and the charging voltage. In order to comply with the
JEDEC standard [24]-[25], we have calibrated the RLC values, as shown in Figure 4.8, and the simulated waveforms of two CDM voltages (500 and 1000 V) compare with the JEDEC specs listed in Table 4.1. The calibrated equivalent circuit in Figure 4.8 will be used to generate CDM pulses in the subsequent transient simulation.

Figure 4.8 Current waveforms of CDM pulses generated by the calibrated CDM equivalent circuit (insert) with the small target.

Table 4.1 Comparison of waveforms simulated from the calibrated CDM equivalent circuit in Figure 4.8 vs. JEDEC specifications.

<table>
<thead>
<tr>
<th>Test voltage (V)</th>
<th>Peak current Magnitude (A)</th>
<th>Rise time (ps)</th>
<th>Full width at half height (ns)</th>
<th>Undershoot (A)</th>
<th>Overshoot (A)</th>
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<tr>
<td></td>
<td>Ip</td>
<td>tr</td>
<td>Td</td>
<td>U-</td>
<td>U+</td>
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<tr>
<td>500 V</td>
<td>5.75 (±15%)</td>
<td>&lt;400</td>
<td>1.0±0.5</td>
<td>&lt;50%Ip</td>
<td>&lt;25%Ip</td>
</tr>
<tr>
<td>1 kV</td>
<td>11.5 (±15%)</td>
<td>&lt;400</td>
<td>1.0±0.5</td>
<td>&lt;50%Ip</td>
<td>&lt;25%Ip</td>
</tr>
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<td>0.888</td>
<td>-1.5</td>
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Small Target

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<td>Simulation</td>
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4.4.2. Experimental Results

The HH-LVTSCR devices with a width of 100 micron were integrated into a single pole double throw (SPDT) analog switch. Figure 4.9(a) shows its on-chip ESD protection scheme. The anode terminals of the SCR devices are all connected to the pads and their cathode terminals are all connected to the common ground bus of the chip. The die size of the test chip is 1000*800 μm², and its package type is 10-lead MicroPAK.

Figure 4.9(b) is the equivalent circuit schematic diagram of the layout showed in (a). In the SPDT analog switch, there are three types of pins: input-only pins, output-only pins and power supply pins. The ESD protection is provided by the SCR devices conducting current from pins to ground bus, which is VSS-based ESD protection scheme as shown in Figure 1.8. Figure 4.9(b) illustrates the discharging paths under the JEDEC-standard CDM zaps. The diode inside each SCR cell and the output NMOS denotes the device when it is working in the negative operation.

SPDT analog switch parts are stressed by Thermo KeyTek RCDM automatic tester from 250 V to 1 kV. The stress method is compliance with JEDEC standard [24]-[25]. Those parts are screened for pin leakage and functionality by automatic test equipment (ATE) before and after CDM zaps to identify the failure voltage level. The test results revealed that, with the SCR protecting devices at the pin, the input pins will fail after 500 V CDM zap and the SCR devices can protect output pins up to 1 kV CDM.
4.4.3. Simulation Results

During the CDM measurements, the substrate is charged to the required voltage and one of the pins is grounded for the discharge. In the simulations, the discharge is applied to the pin being tested. Hence, applying an initially positive CDM voltage to the I/O pin is equivalent to discharging the pin after negative charging of the substrate, and vice versa. Simulation decks are
created to simulate the response of the input-only and output-only pins under CDM stresses. The macromodel developed is used to model the SCR devices and the standard BSIM3v3 model is used to model the MOS transistors in the core circuit. The NMOS in output buffer for pull-down has the snapback modeling capability.

Figure 4.10 shows the simulated transient voltage and current characteristics of the input-only pin subjecting to a positive 500 V CDM stress (i.e., negative substrate charging). The maximum voltage at the input pad, which is also the maximum voltage stressed on the gate oxide of the input MOS, is as high as 35 V. Even though the oxide breakdown voltage for a 1-ns rise time CDM pulse is much higher than that for a dc stress [95], but the 35 V resulted from the CDM is very likely to be sufficiently large to damage the core circuit. The ATE testing showed the leakage current of the input pins increases significantly after the 500 V CDM stress, indicating the gate oxide of the input MOS has failed. This may stems from that fact that the HH-LVTCSR doesn’t trigger fast enough to discharge the CDM stress current, as evidenced by the current waveform lagging the voltage waveform during the positive portion of the first cycle. The simulation results shown in Figure 4.6 also show the voltage overshoot. Ideally, if the SCR’s turn-on time is sufficiently fast, the maximum input pad voltage is the same as the SCR trigger voltage of 9.4 V. But in practice, the slow SCR turn-on leads to a voltage build up of about 35 V until the SCR can start to conduct a large current. In the negative portion of the first cycle, the maximum voltage is much lower because the current will discharge through the forward-biased P-Substrate/N-Well and P-Well/N-Well junction diodes. The diodes can turn on quickly enough to safely shunt the current. During the second cycle, the HH-LVTSCR follows the voltage response to turn on and conduct the current.
Figure 4.10 Simulated transient voltage and current at the input-only pin under a positive 500 V CDM stress.

Figure 4.11 shows the simulated transient voltage and current characteristics of the output-only pin subjecting to a positive 1 kV CDM stress. Three currents are shown: the total pad current $I_{\text{Total}}$, and $I_{\text{SCR}}$ and $I_{\text{Output-NMOS}}$ are the currents going through the HH-LVTSCR device and the output NMOS, respectively. The output driver of the I/O circuits is self protecting, i.e., it operates in snapback mode during ESD stress, and thus it can supply an additional path to discharge the ESD current. The output MOS usually has a higher trigger voltage than the SCR device (10.8 V vs. 9.4 V in this case). As can be seen in Figure 4.11, $I_{\text{Output-NMOS}}$ can follow the waveform of the pad voltage more closely than $I_{\text{SCR}}$ during the positive portion of the first cycle, implying the NMOS triggers faster than the SCR. On the other hand, once triggered, the SCR conducts a much larger current than the NMOS. The peak of the pad voltage is 24.4 V, which is much lower than that for the case of 500 V CDM on the input pin. In addition, there is no gate
oxide directly subjecting the ESD stress in the case of the output-only pin. As such, the CDM robustness of the output pin is higher than that of the input pin. During the negative portion, \( I_{\text{Output-NMOS}} \) will go through the forward-biased p-well/drain junction diode.

Figure 4.11 Simulated transient voltage and currents at the output-only pin under a positive 1 kV CDM stress.

The above simulation finding is consistent with the testing results that the input pins failed after a 500 V CDM stress and the output pins failed at a higher level of 1 kV CDM. While the output NMOS is self-protecting, the ESD protection device, like HH-LVTSCR considered, is still indispensable for the output pins. The total width of the output NMOS is not big enough to handle all the ESD current (the total width of the output NMOS in this presented case is 40 μm) and its area efficiency of ESD protection is lower than that of the SCR protection device.
In order to improve the CDM robustness of the pins, a clear way is to reduce the pad clamping voltage. A suggested way is to provide an alternate discharge path from pad to V_{SS} or to reduce the impedance of the existing path [104] or to design new ESD protection structures which can trigger fast enough to offer adequate CDM protection.

Thus, the model developed, together with the knowledge of pad voltage that can be applied to the I/O pin without damaging the core circuit, can be used to predict the I/O pin ESD protection level offered by the SCR protection devices.

4.5. Chapter Summary

In this chapter, we have presented a comprehensive compact model of SCR for the simulation of integrated circuits subjected to a pervasive ESD event called the charge device model (CDM). The work illustrated the useful and effective macromodeling approach of integrating the various industry standard models to describe the individual devices imbedded in the SCR. In addition, the modeling of the avalanche current sources, substrate parastics, and capacitances were discussed. The issue of parameter extraction was addressed as well. The macromodel has been implemented into Cadence SPICE, and TLP and transient simulations have been carried out. A 0.35-μm CMOS circuit subjecting to CDM stresses was also considered and tested in support of the modeling development.
CHAPTER 5. COMPARISON OF VBIC AND CONVENTIONAL GUMMEL-POON MODEL FOR ESD SCR COMPACT MODELING

5.1. Introduction

In Chapter 4, we have already discussed how important to build a predictable compact model for SCR devices for ESD protection design and what are the difficulties of building such model. Also, Chapter 4 presents a marcomodeling approach to build an accurate, stable and fast SCR compact model by taking the advantage of the advanced BJT model, VBIC. This modeling approach offers simplicity, wide availability and compatibility with most commercial simulators. In additional, this approach by using VBIC model can quickly adapted to technology scaling when new physical phenomena is updated into standard VBIC model for the latest state-of-art technologies by compact modeling community. Furthermore, the sophisticated capacitance modeling and the parasitical PNP in the advanced VBIC model ensure this macromodel approach can simulate the response of the SCR device to very fast transient stimulus such as CDM.

The macromodeling approach is to use the existing device model to build an equivalent sub-circuit to describe the characteristic of the device to be modeled. This approach is highly suitable for modeling a device whose behavior is hard to describe with a close-form analytical solutions. The SCR device is a PNP-NPN transistor coupled system. The straightforward idea to model this device is to consolidate a PNP and a NPN BJT to represent the SCR device. The question is what kind of model should be used for the PNP and NPN transistors in SCR sub-
circuit model to make the model accurate. SPICE Gummel-Poon (SGP) model has served the ICs industry well for over 20 years [105]-[106]. Some literatures have reported SCR sub-circuit models by using SGP model for the PNP and NPN transistors inside the models [89][90], but the models have to include the extra current/voltage source and the models can not describe the negative operation state and the response of the SCR device under very fast transient event. The SGP model is a three-terminal model and consists of three current sources, $I_{cc}$, $I_{bc}$ and $I_{be}$, as shown in Figure 5.1 which is a NPN-type model circuit. $I_{rc}$ and $I_{re}$ are the recombination current in base-collector depletion region and in base-emitter depletion region. The basic of all variants of the SGP model is the integral charge control model for the dc current $I_{cc}$ passing through the emitter and collector terminals. There are two capacitances, $Q_{bc}$ and $Q_{be}$, associated with the charges stored between the base and collector terminals and between the base and emitter terminals.

The Unlike the conventional SGP model, the VBIC is a four-terminal model comprising the base, emitter, collector and substrate which includes several features that make it distinct with the SGP model. Figure 5.2 shows the equivalent sub-circuit and complete model network of a NPN-type VBIC model. The main modeling enhancements of VBIC over SGP are:

1. *The improved early effect modeling*. The early effect in VBIC models via q1 term to cover the bias dependence of output conductance over a wide range of biases.

2. *Quasi-saturation modeling*, which models the conductivity modulation of the collector.
3. *Parasitic substrate transistor modeling.* VBIC model composes a intrinsic NPN transistor and a parasitic PNP transistor.

4. *Parasitic oxide capacitance modeling.*

5. *Avalanche current modeling.* VBIC models the base-collector avalanche current at high reverse bias when the device is in forward-active mode.

6. *Decoupling of base and collector current.* In the conventional SGP model, the base and collector currents are correlated with current gain while in VBIC model, there is no such direct connection between the two currents.

7. *Improved temperature dependence modeling.*

8. *Self heating modeling.*

9. *Capacitance continuous modeling.*

For ESD compact modeling purpose, are all the above advanced features benefit the sub-circuit model with using VBIC model to be a superior one and how these distinct features benefit the SCR compact model for ESD application? This chapter seeks to compare the difference of SCR compact model built by using VBIC and conventional SGP in order to point out the important features of VBIC model for building an accurate and easy-CAD implement SCR model and explain why from device physics and model theory perspectives. First, the development of SCR macromodels by using VBIC and SGP will be presented. The results calculated from the VBIC-based macromodel, calculated from SGP based macromodel and obtained from measurements will be compared. This will be followed by the discussion of what kind of unique features in VBIC model, comparing with SGP model, make the VBIC-based macromodel model SCR triggering and characteristics in conduction mode accurately.
Figure 5.1 The model circuit of the SPICE Gummel-Poon bipolar transistor model.

Figure 5.2 (a) The equivalent sub-circuit of VBIC bipolar transistor model and (b) the model circuit network.
5.2. Model Development by Using VBIC and SGP

A comprehensive SCR compact model for CDM ESD circuit simulation by using VBIC has been developed in Chapter 4. The HH-LVTSCR has been considered to illustrate the model development. Here we redraw Figure 4.1 as Figure 5.3 for comparison. The cross-section view and the terminal connection in ESD bias condition of the device are shown in Figure 5.3(a) and the sub-circuit of SCR macromodel is shown in Figure 5.3(b). The NPN bipolar transistor is using the VBIC model which includes a built-in parasitic PNP to model the substrate parasitics. The PNP BJT and NMOS are described by the SGP and BSIM3v3 models respectively. The schematic of the macromodel is illustrating in Figure 4.2, showing the detailed connections of all internal nodes.

Using this macromodel as a benchmark, another macromodel based on SGP is developed. As shown in Figure 5.4, the NPN BJT is now described with SGP model. The rest sub-circuit of the macromodel keeps the same in order to compare the performance of the macromodel when using VBIC and SGP to describe the NPN transistor. The Figure 5.5 shows the detailed internal nodes connection of the SGP-based macromodel.

Industry standard software tool IC-CAP is used for the parameter extraction. The model extraction follows the methods presented in Section 4.2.8. The terminals, N-Well, Emitter-NPN, P-Well and Substrate, are biased to extract the NPN VBIC model for VBIC-based macromodel while also used to extract the NPN SGP model for SGP-based one. The model extraction of NPN SGP also follows the standard strategies in IC-CAP user manual [101]. The rest model elements of both macromodels are using the same extracted model parameters.
Figure 5.3 (a) Cross-section view of the HH-LVTSCR and (b) equivalent circuit of the HH-LVTSCR when the macromodel is using VBIC model to describe the NPN transistor.

Figure 5.4 (a) Cross-section view of the HH-LVTSCR and (b) equivalent circuit of the HH-LVTSCR when the macromodel is using SGP model to describe the NPN transistor.
Figure 5.5 Schematic of the HH-LVTSCR SGP-based macromodel with all model elements included, showing the detailed connections of all internal nodes.

The two macromodel were implemented into the industry standard Cadence SPICE, and simulations were carried out using pulses as the input. HH-LVTSCR devices with a width of 100 micron were fabricated in a 0.35-μm/3.3-V fully salicided BiCMOS process for model validation. Barth-4002 TLP pulse generator was used to do the measurement, and the rise time and width of TLP pulses were 8 ns and 100 ns, respectively. The same pulses were also considered in simulations.
Figure 5.6 shows the comparison of the simulation results of the macromodel using VBIC as well as SGP and the measurement results for both forward and reverse directions. There is an excellent match between the measurements and the simulation of macromodel by VBIC. The simulation of SGP-based macromodel also shows snapback but the curve is far away from the measurements. In the positive direction, the VBIC-based macromodel triggers at 9.4 V and holds at 5 V, and the model turns on at 0.7 V without snapback in the reverse direction. However, the SGP-based macromodel snaps back at 10.54 V and holds at 10.13 V.

![Figure 5.6 Measured and Simulated TLP I-V characteristics of the macromodels built with VBIC and SGP models.](image)

Figure 5.7(a) and (b) have been redrawn from Figure 4.5 for comparison with SGP-based macromodel. They compare the current and voltage waveforms from the measurement and the
simulations by VBIC-based macromodel with a TLP pulse right after triggering point. As we discussed in Chapter 4, the pad voltage reaches a peak value of 9.42 V and then is decreased to 5.11 V (holding voltage) before it is turned off. The pad current, on the other hand, reaches a maximum value of 218 mA after the device turns on. Figure 5.7(c) and (d) show the current and voltage waveforms from the simulations by SGP-based macromodel with a TLP pulse also right after the triggering point of the model. The voltage initially is built up to 10.55 V then reaches 10.11 V (holding voltage) before it turns off. The current keeps at the low level of 21.9mA after the device is triggered.

Figure 5.7 (a) The measured and simulated time-dependent pad voltages and (b) pad currents by VBIC-based macromodel right after the SCR triggering. (c) The simulated time-dependent pad voltages and (d) pad currents by SGP-based macromodel right after the SCR triggering.
5.3. Model Analysis and Discussion

5.3.1. Triggering Region

As shown in Figure 5.7, the SGP-based macromodel does not snapback correctly since the macromodel doesn’t model correctly the avalanche breakdown current which is the most important components to determine the device triggering.

We have discussed in Section 4.2.5 that in the conventional approach in which a SCR is modeled with two coupled PNP and NPN bipolar transistors using the SGP model, an avalanche generation current source as Equation (4.1) has to be inserted in parallel with the base-collector junction to properly characterize the junction breakdown [89]-[90]. For the macromodel using VBIC, no extra current source is needed. All the necessary avalanche current sources are imbedded in the equivalent circuit in Figure 4.2, as described with Equation (4.2) and (4.3).

For the macromodel using SGP for NPN transistor, there is no avalanche breakdown model in SGP. The macromodel only has one current source imbedded in NMOS transistor described by BSIM3v3 (Equation (4.2)). $I_{sub}$ accounts for a big portion of the generation current in VBIC-based macromodel, so the SGP-based macromodel dose snapback even with this one current source. But without enough generation current generated by the model, the model will not triggered at the right voltage. Also, the model doesn’t work out the right holding voltage. Figure 3.3 shows the directions of all electron and hole currents after the SCR triggers which means both PNP and NPN transistors turn on. $I_{gen}$ is avalanche generation current. The two current sources, $I_{ave}$ (Equation (4.3)) and $I_{sub}$ (Equation (4.2)), compose $I_{gen}$ in the VBIC-based macromodel while in the SGP-based macromodel, there is only $I_{sub}$ who functions as $I_{gen}$. $I_{gen}$ is given by Equation (3.1). As discussed in Section 3.2, after both PNP and NPN bipolar transistors
turn on, \( I_{gen} \) will be described as Equation (3.2). Then the value of \( M \) will reduce and the voltage at Anode drops to \( V_H \). The value of \( V_H \) is dependent on the voltage at Anode required to maintain the base to emitter voltage at the level needed to sustain the bipolar current. Hence, \( V_H \) is a function of \( R_{N-Well}, R_{P-Well}, R_P, M \) and the gains of both intrinsic PNP and NPN transistors, \( \beta_{PNP} \) and \( \beta_{NPN} \). As shown in Figure 3.3,

\[
V_H = I_H \cdot R_P + V_{BC} + I_{SUB-PNP} \cdot R_{N-Well} + I_{SUB-NPN} \cdot R_{P-Well} 
\]

(5.1)

\[
I_{SUB-PNP} = I_H - I_{C-PNP} \cdot \left(1 + \frac{1}{\beta_{PNP}}\right) 
\]

(5.2)

\[
I_{SUB-NPN} = I_H - I_{C-NPN} \cdot \left(1 + \frac{1}{\beta_{NPN}}\right) 
\]

(5.3)

Replacing equations (5.2) and (5.3) in equation (5.1), we will get

\[
V_H = I_H \cdot (R_P + R_{N-Well} + R_{P-Well}) + V_{BC} - I_{C-PNP} \cdot R_{N-Well} \cdot \left(1 + \frac{1}{\beta_{PNP}}\right) - I_{C-NPN} \cdot R_{P-Well} \cdot \left(1 + \frac{1}{\beta_{NPN}}\right)
\]

(5.4)

\( I_H, I_{C-PNP} \) and \( I_{C-NPN} \) are functions of \( \beta_{PNP} \) and \( \beta_{NPN} \), and \( V_{BC} \), the voltage drop across base-collector junction, determines how big \( M \) will be. Since the SGP-based maromodel has only one current source, which requires higher \( V_{BC} \) to reach higher \( M \) in order to get enough \( I_{gen} \). So the model has not been able to hold at the right voltage. The \( V_H \) is much higher for SGP-based maromodel. The comparison results presented in Figure 5.7 shows that it is not efficient enough to model the SCR triggering when having the only one current source, \( I_{sub} \) in NMOS.

Extra current source needs to be added into the macromodel with NPN transistor described by SGP. In this way, behavior languages or special setups in CAD simulators are needed to implement such extra current source, which could significantly lower the simulation
speed and may cause convergence problems, while the implementation of the VBIC-based macromodel is much simpler. In principle, the macromodel in Figure 4.2 can be implemented in any circuit simulator containing advanced MOS and BJT models. The simplicity of this modeling approach offers advantages of higher simulation speed, more flexibility, and less convergence issues.

Figure 5.8 Simulated (a) base-emitter and collector-emitter voltages of the PNP and NPN transistors and (b) emitter, base and collector currents of the PNP and NPN transistors in the SGP-based macromodel.
Comparing with Figure 4.7, Figure 5.8(a) and (b) show the simulated voltages and currents, respectively, versus the input voltage of the internal nodes of the PNP and NPN transistors for the SGP-based macromodel. In Figure 5.8(a), the emitter-collector voltages of both transistors also increase with increasing input voltage. The trigger voltage of the macromodel by SGP model is higher than that of the one by VBIC model. After the SCR turns on, the emitter-collector voltages reduce little bit and keep increasing afterwards while the base-emitter voltages are in the range of 0.8-1.0 V. For the currents in Figure 5.8(b), very little current goes through both transistors before triggering, while after triggering the current conduction level of both transistors are low.

5.3.2. High Current Region

After the SCR device enters conduction mode, both PNP and NPN transistor turn on and work in forward active mode. The simulated shape of I-V curve in conducting state depends on the current level both PNP and NPN transistor models can work out. As shown in Figure 5.6, Figure 4.7 and Figure 5.8, the conduction current level of SGP-based macromodel is low after the model turns on while the VBIC-based macromodel can give the accurate conduction current. After the device is triggered, considerable electrons and holes are injected from the emitters of NPN and PNP transistor, and the SCR resistance is reduced significantly. As shown in Figure 4.7 and Figure 5.8, the base-emitter biases of PNP and NPN transistors in both macromodels are higher than those of the BJT transistors under normal analog applications, especially the biases in the VBIC-based macromodel. This means the free-carrier injection level in the SCR is extremely high. The high-level injection can also give rise to base pushout and
conductivity modulation in the collector. This effect is accounted for in the VBIC model with the quasi-saturation components described by Equation (4.5) to (4.9).

Additionally, the emitter-collector biases of PNP and NPN transistors in both macromodels are also high, especially the biases in the SGP-based macromodel. This means the reverse biases of base-collector junctions are high where effects of impact ionization become significant. This effect has been taken care of by avalanche current model in VBIC as described by Equation (4.3) to (4.4).

With aforesaid advanced features in VBIC model, the VBIC-based macromodel can simulate the SCR characteristic in conduction region very well. Figure 5.9 shows the forward Gummel-Poon plots (Figure 5.9(a)) and the output characteristics (Figure 5.9(b)) of VBIC and SGP models for the NPN transistor in both macromodels under normal model extraction conditions. Figure 5.9(a) is the forward Gummel-Poon plots when $V_{ce} = 2$ V. Since the NPN transistor is working under high $V_{be}$ bias for SCR modeling, so we focus on high $V_{be}$ region when doing the model extraction of VBIC and SGP for NPN transistor. We tried to make the SGP model can reach the same high current level as VBIC, sacrificing the low $V_{be}$ region. If we make the $I_b$ and $I_c$ of SGP model match the ones of VBIC model in low $V_{be}$ region, the both currents will drop much lower in the high $V_{be}$ region. In Figure 5.9(b), it can be seen that at different $V_{be}$, the $I_c$ increases as $V_{ce}$ increasing in VBIC model while it keeps almost the same in SGP model, which shows the capability of VBIC model to handle impact ionization.
Figure 5.9 The Gummel-Poon plots and output characteristics of VBIC and SGP model of NPN transistor under normal model extraction conditions.
When we applied the extracted VBIC and SGP models on NPN transistor for both macromodels, the bias voltages of base-emitter and emitter-collector junctions of NPN transistor in both macromodels are different after both macromodels enter conduction mode with the same bias at Anode. The characteristics of NPN transistor in both macromodels are studied when the voltage at Anode is 10.85 V, under which voltage both PNP and NPN transistors turn on, working in forward active mode. When voltage at Anode is 10.85V, the total current dumped by the VBIC-based macromodel is 288.8 mA while only 23.34 mA by SGP-based macromodel. In VBIC-based macromodel, $V_{be}$ and $V_{ce}$ are 1.15 V and 3.65 V respectively, and $I_{B-NPN}$ and $I_{C-NPN}$ are 75.7 mA and 213 mA respectively. In SGP-based macromodel, $V_{be}$ and $V_{ce}$ are 0.8 V and 9.47 V respectively, and $I_{B-NPN}$ and $I_{C-NPN}$ are 14.34 mA and 8.5 mA respectively. Figure 5.10 and Figure 5.11 show the comparison of forward Gummel-Poon plots and output characteristics for VBIC and SGP models under the above bias conditions. It can be seen there are about two orders of magnitude difference between the collector currents as well as the injected emitter currents of the NPN transistor in the VBIC-based macromodel and the SGP-based one when both macromodels are conducting ESD current even though the VBIC model and SGP model have been extracted in the way that they have almost the same current level under high $V_{be}$ region. Being lacking of features to model high level injection and avalanche breakdown, the macromodel using SGP for NPN transistor has not been able to model the current of the SCR device in conduction mode.
Figure 5.10 The Gummel-Poon plot of VBIC and SGP model of NPN transistor when the macromodels is in conduction mode with a voltage of 10.85 V at Anode.
5.3.3. Negative Operation Region

The negative characteristic of the HH-LVTSCR is like a forward-biased diode, as the TLP measurements in Figure 5.6. With the terminal connection as in Figure 5.3 and Figure 5.4, when under the reverse bias, the P-Well/N-Well and P-Substrate/N-Well junction diodes are forward biased and diode-mode conduction results. The P-Substrate/N-Well junction has been modeled by \( D_{\text{sub}} \). The current path going through \( D_{\text{sub}} \) under reverse bias is denoted as P1 in
Figure 5.3(a) and Figure 5.4(a). The P-Well/N-Well junction is the base-collector junction of the PNP transistor as well as the NPN transistor. It has been modeled within the respective SGP-PNP model and VBIC-NPN model in the VBIC-based macromodel, and SGP-PNP model and SGP-NPN model in the SGP-based macromodel. The current path going through P-Well/N-Well junction diode under reverse bias is denoted as P2 in Figure 5.3(a) and Figure 5.4(a). There is one more current path going through the base-collector junction of the Parasitic-PNP transistor built in VBIC, denoted as P3 (see Figure 5.3(a)).

For the SGP-based macromodel, there are only current paths P1 and P2, the simulation results can not fit the TLP measurement results since the coupled PNP and NPN transistor models can not function correctly as a forward biased diode under reverse bias. With the built-in parasitic PNP transistor, we have additional current path, P3, parallel with P1 and P2 to conduct more reverse current.

5.4. Chapter Summary

In this chapter, we presented two SCR macromodels by using VBIC model and SGP model respectively to describe the NPN bipolar transistor in the macromodel. The simulation results of the VBIC-based macromodel shows excellent match with measurements while those of the SGP-based macromodel do not. Comparing with SGP-based macromodel, the VBIC-based macromodel has one more current source, avalanche breakdown current, to contribute to the total generation current, which makes the macromodel predict the trigger and holding voltages correctly. In additional to the avalanche current model, the VBIC model models the quasi-saturation behavior to describe high level injection, which makes the VBIC-based macromodel is
accurate in conduction mode. Moreover, the parasitic PNP built in VBIC model supplies additional current path in negative operation, which make the simulation results of the VBIC-based macromodel fit the TLP measurements well in reverse direction. Being lack of the above advanced features, the SCR macromodel by using SGP for NPN transistor has not been a successful model.
CHAPTER 6. CONCLUSIONS

ESD failure is a stringent reliability problem to semiconductor industry. Up to one third of all ICs failure might be attributed to ESD. The dissertation firstly talks about how ESD events happen and how they related to failures of integrated circuits, which is followed by models of ESD events and characterization of ESD performance in ICs. Then the dissertation leads the topic to how to reduce ICs failures due to ESD. One of the most important ways is to incorporate on-chip ESD protection inside ICs. The main contributions of this dissertation are having designed and integrated the novel ESD protection devices for low- and high-voltage applications and having developed and implemented the accurate compact model of the ESD protection device in SPICE-like circuit simulator to optimize ESD design and predict ESD performance at pre-silicon stages.

A novel SCR device, called uSCR, has been presented in this dissertation for ESD protection applications of low-voltage ICs. This is the first time an SCR can possess a trigger voltage as low as 7 V without using any external triggering circuitry and a holding voltage as high as 6 V without sacrificing the ESD robustness, while at the same time consuming an area of only 2400 μm². The ESD protection robustness of the uSCR in both positive and negative operations exceeds 60 mA/μm, which enables ESD protection levels of +/- 8 kV HBM and +/- 2 kV CDM for a low voltage ICs.

For high voltage technologies, the first important issue the snapback-type ESD protection device has to face is how to avoid latch-up. Increase the holding current is an efficient solution.
The holding current of SCR device is dependent on the avalanche multiplication factor, $M$, and the current gains of the PNP and NPN transistors in SCR device. A novel high holding current SCR (HHC-SCR) has been developed in this dissertation for high voltage applications and test devices have been fabricated on the BiCMOS 0.6 $\mu$m process. The TLP measurement results have shown that by reaching a maximal $M(I_{C\text{-PNP}}+I_{C\text{-NPN}})$, the HHC-SCR device has realized a holding current as high as 24 mA/$\mu$m to effectively avoid latch-up and a high failure current (48 mA/$\mu$m) for ESD robustness. Additionally, without involving any external circuitry or extra devices, the HHC-SCR device releases reliability weakness issues and accomplishes the minimum area consumption.

In addition to the on-chip ESD protection design, this dissertation has presented a comprehensive compact model of SCR for the simulation of integrated circuits subjected to a pervasive CDM ESD event. The work illustrated the useful and effective macromodeling approach of integrating the various industry standard models to describe the individual devices imbedded in the SCR. In addition, the modeling of the avalanche current sources, substrate parastics, and capacitances were discussed. The issue of parameter extraction was addressed as well. This modeling approach offers simplicity, wide availability and compatibility with most commercial simulators by taking advantage of using the advanced BJT model, VBIC. The presented model is implemented into the industry standard Cadence SPICE to study the CMOS circuit response to CDM stress. Application to 0.35-$\mu$m technology SPDT analog switch I/O circuits demonstrates effectiveness in analyzing CDM response and quantitatively predicting withstand levels.
In the end, this dissertation compared two SCR macromodels by using VBIC model and SGP model respectively to describe the NPN bipolar transistor in the SCR macromodel. The simulation results of the VBIC-based macromodel shows excellent match with measurements while those of the SGP-based macromodel do not. The avalanche current model, the quasi-saturation model and the parasitic substrate transistor model built in VBIC model give the VBIC-based macromodel capability to predict the trigger and holding voltages correctly, to perform in conduction model accurately and to dump enough current in reverse operation region to fit the TLP measurement results. Being lack of the above advanced features, the SCR macromodel by using SGP for NPN transistor has not been able to be a successful model.
LIST OF REFERENCES


