Study Of Gate Oxide Breakdown And Hot Electron Effect On Cmos Circuit Performances

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STUDY OF GATE OXIDE BREAKDOWN AND HOT ELECTRON EFFECT ON CMOS CIRCUIT PERFORMANCES

by

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A dissertation submitted in partial fulfillment of requirements
for the degree of Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2009

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ABSTRACT

In the modern semiconductor world, there is a significant scaling of the transistor dimensions—The transistor gate length and the gate oxide thickness drop down to only several nanometers. Today the semiconductor industry is already dominated by submicron devices and other material devices for the high transistor density and performance enhancement. In this case, the semiconductor reliability issues are the most important thing for commercialization. The major reliability issues caused by voltage are hot carrier effects (HCs) and gate oxide breakdown (BD) effects. These issues are recently more important to industry, due to the small size and high lateral field in short-channel of the device will cause high electrical field and other reliability issues.

This dissertation primarily focuses on the study of the CMOS device gate oxide breakdown effect on different kinds of circuits performance, also some HC effects on circuit’s performance are studied. The physical mechanisms for BD have been presented. A practical and accurate equivalent breakdown circuit model for the CMOS device was studied to simulate the RF performance degradation on the circuit level. The BD location effect has been evaluated. Furthermore, a methodology was developed to predict the BD effects on the circuit’s performances with different kinds of BD location. It also provides guidance for the reliability considerations of the digital, analog, and RF circuit design. The BD effects on digital circuits SRAM, analog circuits Sample&Hold, and RF building blocks with the nanoscale device – low noise amplifier, LC oscillator, mixer, and power amplifier, have been investigated systematically. Finally 90 nm device will be used to study the HC effect on the circuit’s performance.
The contributions of this dissertation include: Providing a thorough study of the gate oxide breakdown issues caused by the voltage stress on the device – from device level to circuit level; Studying real voltage stress case – high frequency (950 MHz) dynamic stress, and comparing with the traditional DC stress; A simple, practical, and analytical method is derived to study the gate oxide breakdown effect including breakdown location effect and soft / hard breakdown on the digital, analog and RF circuits performances. A brief introduction and simulation for 90 nm device HC effect provide some useful information and helpful data for the industry.

The gate oxide breakdown effect is the most common device reliability issue. The successful results of this dissertation, from device level to circuit level, provide an insight on how the BD affects the circuit’s performance, and also provide some useful data for the circuit designers in their future work.
To my mother Wen Yan Yu
ACKNOWLEDGMENTS

I would like to express my gratitude to my advisor, Professor Jiann S. Yuan, for his help and support throughout my graduate studies. He contributed many suggestions to this work while offering the right direction on my research. His technical and editorial advice was essential to the completion of this dissertation and has taught me innumerable insights on the workings of my PhD research. His knowledge and philosophy will guide my future work.

My thanks also go to the members of my dissertation committee, Dr Chow Lee, John Z. Shen, Kalpathy B. Sundaram for your advice for my presentation and contents of this dissertation.

I am grateful to all my colleagues in the lab – Dr Chuazhao Yu, Yidong Liu, Hongxia Tang and Yixin Yu. In particular, Chuanzhao gives me a lot of help on the experiments, analysis, design, and implementation and so on. Also thanks for him allow me use some of our data and information in my paper.

Last, but not least, I would like to thank my wife Puiyan for her understanding and love during the past few years. Her support and encouragement were in the end what made this dissertation possible. My mother – Wenyan Yu, receive my deepest gratitude and love for her dedication and many years of support during my studies.
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<th>Definition</th>
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<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
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<tr>
<td>BD</td>
<td>Breakdown</td>
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<tr>
<td>BSIM</td>
<td>Berkeley Short-Channel IGFET Model</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>C-V</td>
<td>Capacitance versus Voltage</td>
</tr>
<tr>
<td>CVS</td>
<td>Constant Voltage Stress</td>
</tr>
<tr>
<td>DUT</td>
<td>Device-Under-Test</td>
</tr>
<tr>
<td>EOS</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrical Over-stress</td>
</tr>
<tr>
<td>HBD</td>
<td>Hard Breakdown</td>
</tr>
<tr>
<td>SBD</td>
<td>Soft Breakdown</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IGFET</td>
<td>Insulated-Gate Field-Effect Transistor</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input Third-Order Intercept Point</td>
</tr>
<tr>
<td>IM3</td>
<td>Third-Order Intermodulation Distortion</td>
</tr>
<tr>
<td>I-V</td>
<td>Current versus Voltage</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s Current Law</td>
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<tr>
<td>KVL</td>
<td>Kirchhoff’s Voltage Law</td>
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<tr>
<td>LCO</td>
<td>LC Oscillator</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>LCR</td>
<td>Inductance Capacitance Resistance</td>
</tr>
<tr>
<td>LF</td>
<td>Low Frequency</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LS</td>
<td>Large signal</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>NPR</td>
<td>Noise Power Ratio</td>
</tr>
<tr>
<td>NMOSFET</td>
<td>N-type MOS Field Effect Transistor</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
</tr>
<tr>
<td>PMOSFET</td>
<td>P-type MOS Field Effect Transistor</td>
</tr>
<tr>
<td>PSS</td>
<td>Periodic Steady State</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random access memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SS</td>
<td>Small Signal</td>
</tr>
<tr>
<td>TDDB</td>
<td>Time Dependent Dielectric Breakdown</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
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<tr>
<td>XF</td>
<td>Transfer Function</td>
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CHAPTER ONE: INTRODUCTION

1.1. Motivation

Due to the continuous downscaling of device size and increasing demands for high performance, the major reliability issue – gate oxide breakdown (BD) due to high vertical field in the oxide becomes even more important. Gate oxide breakdown results in performance degradation in digital, analog, and RF circuits. As the transistors become smaller in dimension for improving speed and functionality, they need more sophisticated management for reliability issues. Another important reliability issue is HC effect, which is caused by high lateral field in short-channel MOSFETs. Gate oxide breakdown and HC become important reliability issues and normally happen in the RF and most of the digital, analog circuit operations.

Much is known about the BD and HC effects on the device dc characteristics, but little is understood of the impact on digital analog and RF circuit’s performance, such as delay, noise, and linearity. The practical, normal, and dynamic stresses on the RFICs are investigated. BD location effect is also studied here. An impactful and accurate BD model to evaluate the circuits’ performance is very necessary.
1.2. Research Goals

The research presented here aims to the following issues:

1. Refining the gate oxide breakdown model for circuit simulation;
2. Examining the gate oxide breakdown location effect on circuit performances;
3. Improving the gate-source and gate-drain leakage current model for SPICE simulation;
4. Studying RF, mixed-signal, and digital circuit performances subject to gate oxide breakdown;
5. Studying RF circuit performance subject to HC effect;

1.3. Outlines

Chapter 2 presents the introduction of the wireless application and basic voltage reliability issues –BD and HC in MOSFETs. Device reliability and the breakdown model for a circuit’s simulation are given in chapter 3. The breakdown effect on the circuits’ performance such as SRAM, Sample & hold, LNA, PAs, and LC Oscillator are presented in chapter 4. The circuits performance degradation subjected on HC is given Chapter 5 and Chapter 6 suggests the future work and conclusions.
CHAPTER TWO: INTRODUCTION OF WIRELESS APPLICATION AND BSIM MODEL

2.1. Introduction of wireless application

In the modern world, wireless products are widely used in our daily lives, such as wireless local area networks (WLANs), RF identification systems, mobile phones, GPS, home satellite networks and so on. Even more, many wireless products are still on the way and people will rely on those products in the future. Fig. 2.1 shows the wireless application in today’s world.

![Wireless Communication Systems Today](image)

*Figure 2.1 Wireless Communication Systems Today*

Fig. 2.2 shows the basic RF circuits design flow. It consists of two major parts; the first one is the RF transmitter, and the second one is the RF receiver. For the RF transmitter, the signal
first goes to analog digital converter (ADC) and then goes to the modulation & DSP—those two steps are called digital baseband section and the main function is to compress, code, modulate, and shape the coming signal. After that, the signals go to the RF section, first to the digital analog converter, and then to the carrier which is the upconverter and modulator, finally the signals go to the power amplifier. And for the RF receiver is completely the opposite. The signals first go to the RF filter and then low noise amplifier, down the converter and ADC which form the RF section. For the digital baseband section, the signals go to the demodulator & DSP, DAC, and then go out.

Figure 2.2 RF Circuits Design Flow

The RFICs market grows faster and faster every year. Fig. 2.3 shows the entire IC market in 2007-2011 for the prediction. The picture shows that the electronic systems sales rise 5%,
growing $1.21 trillion in 2007. The new report forecasts an average annual increase of 7% for the worldwide electronics systems growth between 2006 and 2011, and the total will reach $1.6 trillion. Also in 2007, the fastest-growing electronics systems markets are video game consoles (58%) RFID (35%), smartcards (11%), wireless personal and local area networks (26%). Moreover, many new RFIC design companies have been built up in the last year all over the world, thus more and more money has been spent on the RFIC on the market.

![2007 Electronics Systems Markets](image)

Figure 2 3 2007 Electronics Systems Markets
2.2. BSIM Model

The BSIM model is a physics-based, scalable, and predictive SPICE model for circuit simulation in CMOS technology. It was developed by the BSIM Research Group of the Department of Electrical Engineering and Computer Science (EECS) at the University of California, Berkeley. The third iteration of BSIM3v3, which is considered as the first industry-wide standard was established by SEMATECH in December of 1996. BSIM3v3 has been widely used by most semiconductor companies for device modeling. The newest version for the BSIM model, which is the BSIM4 model, was developed by the BSIM Research Group in 2007.

2.3. An Equivalent Circuit Model

It is very important to improve the reliability of circuits, making it necessary to evaluate the performance degradation due to these effects during the circuit’s design phase before fabrication. Another important thing is to have an accurate model to predict the stressed MOS transistor behaviors. The BSIM3v3 model is extracted from DC characteristics. A model which represents the stressed device behaviors is developed and shown in Fig. 2.4. The equivalent circuit includes two inter-terminal resistances ($R_{gd}$, $R_{gs}$), the terminal resistances ($R_g$, $R_d$, $R_s$), substrate network equivalent resistances ($R_{db}$, $R_{sb}$, $R_{dsb}$), and junction capacitances ($C_{db}$, $C_{sb}$). The intrinsic transistor is a BSIM3v3 model, which is extracted from the fresh or stressed devices using BSIMpro computer tool at different kinds of temperatures. Agilent 4156B is used as the I-V
meter. $R_{gs}$ and $R_{gd}$ are used as the equivalent resistances between the gate and the source and between the gate and the grain, respectively. The resistances come from the $I_g-V_g$ curve data.

Other parameters – $C_{gs}$, $C_{gd}$, $R_g$, $R_d$, $R_s$, $C_{db}$, $R_{ds}$, $R_{db}$, are extracted from Y-parameters which were converted from measurement of S-parameters. $R_{bsd}$ and $C_{sb}$ are obtained by optimizing the entire model to get the S-parameters. In the BSIM3v3 model, the parameters are temperature dependent [8].

![Improved Model for RF simulation](image)

**Figure 2-4 Improved Model for RF simulation**

Other parameters are also extracted from Y-parameters that were converted from measured S-parameters.
CHAPTER THREE: DEVICE RELIABILITY AND BD MODEL FOR THE CIRCUITS SIMULATION

3.1. Introduction

In the modern semiconductor industry, the transistor size becomes smaller and smaller to improve the speed and performance, the power dissipation and reliability issue becomes more and more important to the designer. High speed and performance of silicon-on-insulator can have hot spots in a circuit design chip which will cause high electrical filed and too much power. In this case, the transistor most likely suffers from the gate oxide breakdown (BD) effect caused by high vertical electrical fields in the oxide and the HC effect caused by high lateral electrical field.

3.2. Hot Carrier Effects

The term ‘hot carriers’ refers to either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor (especially MOS) device [9]. Hot carrier usually injects into the gate oxide or substrate layers because of the high electrical field. A path of traps and charges will be created which will degrade the semiconductor device performance. Hot carries effects refers to device degradation or instability caused by hot carrier injection.
There are four types of hot electron injection mechanisms.

1) The channel hot electron injection;

Channel hot electron injection happens when both the gate voltage and drain voltage are higher than the source voltage, with $V_D \approx V_G$. Due to the high gate voltage, channel carriers sometimes are driven to the gate oxide before they reach the drain side.

2) The substrate hot electron injection;

Substrate hot electron injection usually happens when the substrate bias is very high such as, $|V_B| >> 0$. Substrate field drives the carriers to the Si-SiO2 interface under this condition. In the process the carriers gain a lot of kinetic energy from the high electrical field so that they could go into the surface depletion region. In the end, they overcome the surface energy barrier and inject into the gate oxide.

3) The drain avalanche hot carrier injection;

The drain avalanche hot carrier (DAHC) injection is shown in Fig. 3.1. This is the worst device degradation under normal operating temperature. This happens when a high voltage applied at the drain at the condition of $V_D > V_G$, the channel carriers will accelerate into the drain’s depletion region. The results show that the worst effects happen when $V_D = 2V_G$. This acceleration of channel carriers creates dislodged electron-hole pairs. The phenomenon is known as impact ionization, some electron-hole pairs gain enough energy to overcome the electric potential barrier between the gate oxide and the
silicon substrate. Then some of the electron and carriers inject into the gate oxide layer as well as the substrate layer where they are sometimes trapped. Hot carriers can be trapped at the Si-SiO2 interface or within the oxide itself, creating a space charge which will increase over time as more charges are trapped. These trapped charges change some of the device characteristics, for example the threshold voltage ($V_{th}$) and mobility. Injected carriers will not become gate current in the gate oxide. Meanwhile, most of the holes from the electron-hole pairs generated by impact ionization flow back to the substrate, comprising a large portion of the substrate’s current.

4) The secondary generated hot electron injection.

Secondary generated hot electron injection involves the generation of hot carriers from impact ionization involving a secondary carrier which was created by an earlier incident of impact ionization. This happens when a high voltage applied at the drain side or $V_D > V_G$. The back bias results in a field which tends to drive the hot carriers generated by the secondary carries to the surface region and get enough kinetic energy to overcome the surface energy barrier.

Hot carrier effects are mainly because the device dimensions were reduced without reduction of the operating voltage, resulting in high electric fields in the device. Hot carrier injection usually results in higher circuit current densities. Recently, a lot of studies were done to prevent hot carrier effects. Some method include: 1) n+ / n- double diffusion of sources and drains; 2) introduction of self-aligned n-regions between the channel and the n+ junctions to
create an offset gate; 3) use of graded drain junctions; 4) increase in channel lengths; 5) use of buried p+ channels; and 6) inject other materials in the gate oxide.

Figure 3.1 Mechanisms of Hot Carrier Effects
3.3. **Gate Oxide Breakdown Effect**

Oxide Breakdown [10] is defined as the destruction of the oxide layer (usually silicon dioxide or SiO2) in a semiconductor device. Oxide layers are used in many parts of the semiconductor device: such as the dielectric layer in capacitors; the gate oxide between the metal and the semiconductor in MOS transistors; the inter-layer dielectric to isolate conductors from each other, etc. Oxide breakdown is also considered as ‘oxide rupture’ or ‘oxide punch-through’.

In the modern world with the dimensions reductions of the transistor, one of the reliability issues called Oxide breakdown has been concerned by the industry. While the other features of the device are scaled down, the oxide thickness must be reduced. Oxides become more vulnerable to the gate to source and drain to source voltages when they get thinner. Right now the thinnest oxide layers in the world are already less than 30 angstroms thick. An oxide layer can break down easily at once at 8-11 MV per cm of thickness.

There are several classifications of the oxide breakdown base on different kinds of definition.

First, Oxide breakdowns could be classified as one of the following:

1) Early-life dielectric breakdown;

   Early-life dielectric breakdown refers to the breakdown happens in the early device life, such as within the first 1-2 years of the normal operation. Early life dielectric breakdown is mainly because of the presence of weak spots within the
dielectric layer arising from its poor processing or uneven growth. These weak spots or dielectric defects could be caused by: 1) radiation damage; 2) contamination, wherein particles or impurities are trapped on the silicon prior to oxidation; 3) the presence of mobile sodium (Na) ions in the oxide; and 4) crystalline defects

2) Time-dependent dielectric breakdown (TDDB);

Time-dependent dielectric breakdown refers to the breakdown happens after a longer use of time, such as 6-10 years, usually considers as the “wear-out stage”. However, the mechanism is the same as the early-life breakdown.

3) EOS/ESD-induced dielectric breakdown.

The third classification is self-explanatory, which is merely to gate oxide destruction due to the application of excessive voltage or current to the device.

Gate oxide breakdown could also divide into soft breakdown and hard breakdown. When breakdown just happens, it could be considered as the soft breakdown, and when breakdown happens in a long time it could be considered as hard breakdown. Usually soft breakdown does not degrade the device performance a lot, but hard breakdown could usually damage the device. As Fig. 3.2 shows, in (a) first the traps start to form in the gate oxide, but they do not overlap and conduct; in (b) as more and more traps are created, then the traps start to overlap and conduction path is created, as soon as the conduction path is created, the soft breakdown happens. After soft breakdown happens, in (c), the traps are overlapping, at this time thermal damage was happen.
Because conduction leads to heat, and heat leads to thermal damage. And finally in (d), hard breakdown happens, because the silicon in the breakdown spots melts and oxygen is released. Fig. 3.3 is several photographs of gate oxide breakdown [11]. The gate oxide breakdown could damage the device as shown in the photographs. That is why the gate oxide breakdown effect is very important.

Figure 32 Traps in the gate oxide when soft hard and hard breakdown happen
Figure 3.3 Photographs of gate oxide breakdown

- Breakdown region pictured through emission microscopy
- Photon emission at breakdown regions
- Dark region indicates area where Silicon has melted
- TEM Image of Breakdown Spot
- Substrate below Gate Oxide Breakdown
3.4. **Device Degradation due to Breakdown Stress**

3.4.1. **Experiment**

The tested devices are $0.15 \times 20 \ \mu\text{m}^2$ pFETs and $0.20 \times 20 \ \mu\text{m}^2$ nFETs with 30 amstron of HfO2 dielectrics, 10 amstron of SiO2 interfacial layers, and polysilicon gate. The wafer was tested in a Cascade 12000 Probe Station and Agilent 4156B Precision Semiconductor Parameter Analyzer was used for DC biasing and I-V characterization. The breakdowns are studied by the constant voltage stress (CVS). In the stress, the gate-source was set at 4.0 V for positive bias stress and -4.0 V for the negative bias stress. The source, drain, and bulk were grounded.

3.4.2. **Results and Discussions**

The study of the gate leakage current during the CVS for several p- and nFETs are shown in Fig. 3.4. The experimental data indicates that the negative bias stress is easier to trigger the gate breakdown than the positive bias stress for both p- and n-channel transistors. Additionally, nFET is more difficult to breakdown than pFET under the same stress. Under the gate injection, interface state creation and the high holes trapping rate indicate a fast degradation of the interfacial layer. While under the substrate injection, the trap creation occurs most likely in the bulk layer. For either n- or p-device, the breakdown under gate injection is much easier than under substrate injection.
3.5. **Breakdown Equation & Breakdown Model for Circuits Simulation**

A compact model to evaluate the stressed transistor is introduced in chapter 2.3. And the equivalent circuit model will include: substrate network resistances \( R_{db}, R_{sb}, R_{dsb} \), the terminal \( R_g, R_d, R_s \), junction capacitances \( C_{db}, C_{sb} \), overlap capacitances \( C_{gdo}, C_{gs0} \), and two internal resistances \( R_{gd}, R_{gs} \). The post-breakdown characteristics could be studied by using the two breakdown resistances \( R_{gs}, R_{gd} \) where extracted the BSIM3v3 model from fresh and stressed devices using BSIMPro software.

The breakdown position is defined as \( X = I_{GD}/(I_{GS}+I_{GD}) \), as shown in Fig. 3.5. when \( X = 0 \) indicates the BD location is at the source side, \( X = 1 \) indicates the BD location is at the drain side. Also the breakdown path is \( \Phi (V_{GS}, V_{DS}, and x) \) and the voltage across the breakdown path is \( V_{GS} - \Phi (V_{GS}, V_{DS}, and x) \). The currents which flows through the source \( (I_{GS}) \) and drain \( (I_{GD}) \) are derived. The equations are as:

\[
I_{GS} = K[V_{GS} - V_{FB} - \Phi_S(V_{DS}, V_{GS}, x)]^\alpha
\]

\( \text{(1)} \)

\[
I_{GS} = (1-x)K[V_{GS} - V_{FB} - \Phi_S(V_{DS}, V_{GS}, x)]^\alpha
\]

\( \text{(2)} \)

\[
I_{GD} = xK[V_{GS} - V_{FB} - \Phi_S(V_{DS}, V_{GS}, x)]^\alpha
\]

\( \text{(3)} \)

Equation (1) is the gate leakage current equation after the breakdown effect. Where \( K \) is the gate leakage saturation current, \( V_{FB} \) is the flat band voltage, \( x (=y/L) \) is the normalized position along the channel, \( \alpha \) is constants, and \( \Phi_S \) is the surface potential. Base on the definition of the
breakdown location, the gate to drain current and gate to source current were derived in equation (2) and equation (3).

The BD path is defined as the source or drain extension region, i.e., with \( x < 0.01 \) or \( x > 0.99 \). The gate current can be derived as \( KV_{GS}^a \) or \( KV_{GD}^a \). For small-signal excitation at a given voltage bias, one could use the two equivalent resistances, \( R_{GS} \) and \( R_{GD} \) to replace the current sources, \( I_{GS} \) and \( I_{GD} \). But for large-signal applications, equation (2) and (3) could be used to study post-breakdown behavior. A simple model equation for the voltage across the BD path is:

\[
V_{Cross} \approx V_{GS} - (aV_{DS} + b\sqrt{V_{DS}} + c)
\]

(4)

Where \( a, b, \) and \( c \) are fitting coefficients.

The equivalent circuit model for n-channel transistor after breakdown is shown in Fig. 3.6. There are two current sources from the gate side to the drain and source side respectively. Also a gate oxide resistor is used to study the post-breakdown effect. Based on the equation (4), another fitting equation (5) was derived to fit the experiment data.

\[
I_G = f(V_g, V_d) = M[V_g - (a * V_d + b * \sqrt{V_d} + c)]^a
\]

(5)

Fig. 3.7 shows leakage current for different kinds of n-and p-FETs after breakdown. In this figure, the lines show the model predictions which is based on equation (5) and the symbols show the experimental data. A good agreement between the measurement and simulation over a wide range of gate current is obtained. After breakdown, the gate leakage current density goes more than \( 10^4 \) A/cm\(^2\). While at high gate leakage, it is hard to obtain an accurate capacitance by using
the traditional C-V measurement or LCR meter. However for the Cadence SPICE circuit simulation tool, it doesn’t support the real square. The cadence simulation only supports the integer square, so in order to make the model more accurate, a new fitting equation (5) is developed using the integrator square, simply to say \( \alpha \) should be integer for the simulation not the real number. A polynomial equation was needed to fit the breakdown model. Here is the fitting result equation for the new breakdown model.

\[
\bar{I}_G = f(V_g, V_d) = M \times (a_1 V_g^n + a_2 V_g^{n-1} + \ldots + a_{n-1} V_g + b_1 V_d^n + b_2 V_d^{n-1} + \ldots + b_{n-1} V_d + c)
\]  

(6)

Fig. 3.8 shows the polynomial fitting breakdown model, although it has some differences, it is still very close to the experiment plot. And Fig. 3.9 is the BD models for the cadence circuit simulation. In Fig. 3.9 (a), it has two current sources for the circuit simulation, but it is not accurate enough due to only the BD effect cause by the gate-to-source voltage was considered in this case. In fact, the BD is a function of the gate-to-source voltage as well as the drain-to-source voltage. For the Fig. 3.9 (b), four current sources are added for simulation, which will make my BD model more accurate. For the latter circuit simulation in chapter 4, this cadence model is used in the simulation.
Figure 3.4 Gate leakage current during stress for (a) pFET and (b) nFET.

Figure 3.5 Schematic of breakdown path in MOS transistor.
Figure 3.6 Equivalent circuit model for the n-channel transistor after breakdown
Figure 3.7 (a)-(g) Characterizations of gate leakage current for n- and p-channel transistors after breakdown. Lines: modeling results using fitting coefficients; Marks: measurement data.

Figure 3.8 The left one is non polynomial fitting breakdown and the right one is the polynomial fitting breakdown model.
Figure 3.9 BD model for circuit simulation
4.1. **Digital Circuits Performance under BD-SRAM**

4.1.1. **Introduction**

SRAM is a common circuit in our daily life and is widely used in a lot of electronics, such as iPod, mp3, computer RAM, and so on. Simply SRAM includes many typical sub circuits such as, memory cell, precharge, peripheral control logic, sense amplifier cross-connected six-transistor (6-T) which is shown in Fig. 4.1. Also, for a typical system-on-chip (SOC) circuit, SRAM occupies more than 40% of the chip area; this ever-increasing integration of SRAM in embedded SOC indicates that the reliability of the modern VLSI systems depends on the reliability of memories. Therefore, SRAM is used to study the reliability issues and the key part is the cross-connected six-transistor (6-T), which was used as an example to study the gate oxide breakdown effect of SRAM here [12].

There are three kinds of distinct breakdown locations between gate and diffusions of the transistors in an SRAM cell, as shown in Fig. 4.1, the pass-gate breakdown, drain side breakdown and n-source breakdown. Two resistors are used to study the HBD effect on SRAM as shown in Fig. 4.2. Oxide HBD in their positions of the cell was simulated. It has been observed that oxide breakdown located between gate and source of one of the NFETs of the cell
has a greater influence on the SRAM performance, and breakdown happen in p-source does not have any influence on the performance [13-17].

4.1.2. Circuit Simulation

A. Write delay

One of the most important parameters for SRAM is write delay. The Oxide breakdown on the circuit performance for write delay was evaluated. Fig. 4.3 shows the write delay as a function of oxide HBD resistance in the pass-gate location of the SRAM cell. The write delay was measured between the 50% point of the world line signal and the left sense amplifier output during a read operation. Fig. 4.4 and 4.5 show the same write delay as a function of oxide HBD resistance in n-source and drain side respectively. As it shows when breakdown resistance is less than 1000 ohms, for all the three figures, the write process of the cell is completely damaged. However, for oxide HBD in the pass transistor of the cell, the write delay increases as the HBD conduction becomes higher although the write process is totally destroyed when oxide HBD is lower than 1000 ohms.

B. SNM

SNM is another important factor in SRAM circuit-reliability analysis. SNM stands for Signal Noise Margin, which indicates the gate performance under noise conditions [18] [19]. Based on the SPICE DC transfer analysis, the SNM simulation is shown in Fig. 4.6, which shows us the typical butterfly plots for different breakdown location. For the same breakdown resistant 40K, BD happening in drain affects the SRAM performance a lot compared to the p-source and
n-source. N-source and p-source breakdowns induce and asymmetry in the butterfly curve reducing the SNM. P-source breakdown is not a bad thing, because the NMOS is strong enough to combat the effects, while n-source BD results in decrease of SNM because the PMOS is weak and cannot deliver enough current to combat the extra leakage source. Drain BD also reduces the output swing of the SRAM, reducing its SNM. The switching state time for p-source BD is longer than n-source BD. But when BD happens, the SRAM performance will decrease substantially.

4.1.3. Conclusion

SRAM cells are a typical digital circuit subjected to the BD effects which people have studied. Here, SRAM cells are used to report some typical digital circuit performances subjected to BD effects.

Figure 4 1 6-T SRAM cell with possible BD leakage current paths corresponding the cell state.
Figure 4.2 Circuit to model the oxide HBD leakage current from gate to drain or gate to source in a transistor.

Figure 4.3 Breakdown happen in the pass transistor.
Figure 4.4 Breakdown happen in n-source side

Figure 4.5 Breakdown happen in drain side
Figure 4.6 Typical Butterfly plots illustrating the effect of breakdown at each location in the cell HBD, R=40K.
4.2. Analog Circuits Performance under BD-Sample-and-Hold circuit

4.2.1. Introduction

The sample-and-hold circuit is an important building block in analog integrated circuits, such as analog-to-digital data converter (ADC). The high-speed and high-resolution analog-to-digital data converter needs a high performance switched-capacitor circuit.

Gate oxide breakdown effects also highly happened in Sample-and-Hold circuits due to its own circuit operation. The detail circuit operation and simulation are reported below [20]-[27].

The operation cycle of the sample-and-hold circuit is divided into two distinct states, the sampling state and the holding state. In the sampling state, the analog signal is sampled, where the sample-and-hold circuit works something like a buffer. In the holding state, the sampled signal is kept fixed until the next sampling state, where the sample-and-hold circuit allows the voltage comparison of the signal. At this point, the time-continuous signal has been converted to a discrete time continuous signal.

The bootstrapped technique [28]-[32] is widely used in switched-capacitor circuits to improve the circuit performances when the supply voltage is relatively low. The bootstrapped technique is a signal NMOS transistor, and it operates on a two-state clock as shown in Fig. 4.8. The bootstrapped circuit operates based on a two-phase clock scheme. During the ‘on’ phase, the capacitor is switched across the gate-to-source nodes of the switch device. The voltage $V_{DD}$ between the gate and source nodes is used to provide the constant turn-on resistance of the
switch device. During the ‘off’ phase, the switch is turned off by grounding the gate. Simultaneously, the capacitor is charged to $V_{DD}$.

Fig. 4.7 shows the circuit schematic of a bootstrapped switched-capacitor circuit [33]. The operation cycle of the sample-and-hold circuit is divided into two phases. In the sampling phase, the analog signal is sampled, where the sample-and-hold circuit works as a buffer. In the holding phase, the sampled signal is kept fixed until the next sampling cycle. At this point, the analog (time-continuous) signal has been converted to a digital (discrete time) signal. The sample-hold circuit in Fig. 4.7 includes the main switch transistor $M_S$, secondary switches $M1$-$M5$, and capacitors $C_1$ and $C_2$. The CLK$_1$ and CLK$_2$ are the two non-overlapping clock signals. When the CLK$_1$ signal is low and the CLK$_2$ is high, the transistors $M1$ and $M4$ are on. The capacitance $C_1$ is charged to $V_{DD}$ and the transistor $M5$ is used to turn off the main device $M_S$. When the clock signal CLK$_1$ is high and CLK$_2$ is low, the transistors $M2$ and $M5$ make the capacitance $C_1$ in series with the input signal $V_{in}$ and connect to the gate of $M_S$ so that its gate-to-source voltage is equal to $V_{DD}$. The gate voltage of $M_S$ is then charged to $V_{in} + V_{DD}$. The capacitance $C_1$ must be larger to supply charge to the gate of $M_S$ and all parasitic capacitances in the charge path. The transistor $M6$ is used to reduce the maximum drain-to-source voltage of $M7$ for less oxide stress.

The sampling capacitance $C_2$ in the bootstrapped circuit is usually large. The time delay between the sampling network ($M_S$ and $C_2$) and the bootstrapped network ($M1$-$M5$, $M8$, and $C_1$) will induce the gate-oxide transient overstress across the gate-to-drain nodes of the switch $M_S$. The source node of the main switch is driven by an input signal $V_{in}$, and the drain node of $M_S$ is connected to a large sampling capacitor. When the input signal $V_{in}$ is biased to $V_{DD}$, the drain
voltage of $M_S$ is set to ground. As the switch device turns on, a voltage of approximately $2 \times V_{DD}$ will be generated at the gate of $M_S$ to keep the constant voltage $V_{DD}$ between the gate and source nodes of the switch device. Before a channel is formed and the sampling capacitor $C_2$ is charged to $V_{DD}$, excessive voltage greater than $V_{DD}$ may exist across the gate-to-drain terminals of $M_S$. Fig. 4.9 shows the input voltage and bootstrapped gate voltage of the sample-and-hold circuit. The increased gate voltage provides gate overstress, thus, potentially degrading the main switch transistor $M_S$ due to the gate oxide breakdown effect. Since the sample-and-hold circuit keeps switching on and off, the gate of the main switch device $M_S$ accumulates oxide damages over time.

4.2.2. Circuit simulation and result

Fig. 4.10 shows the output waveform versus the input waveform. In the sampling mode, the output waveform is the same as the input waveform, but in the holding mode due to the sampling capacitance $C_2$, the output will remain constant in the holding mode. When the soft breakdown happens, $M=30u$, the output waveform will slightly decrease but still functional, like Fig. 4.11. However, when the hard breakdown happens it will decrease the circuits’ performance a lot, especially when breakdown happens in the drain side which is shown in Fig. 4.12. This will cause the output to go down to almost zero in the holding mode. That is because when hard breakdown happens in the drain side, it causes the drain voltage to be almost equal to the gate voltage, which is almost zero, due to the seriousness of the breakdown phenomenon. When hard breakdown happens in the source side which is shown in Fig. 4.13, it decreases the circuits’ performance, but it is not as serious as the gate breakdown happens in the drain side.
As Fig. 4.11-13 shows, the breakdown will degrade the performance of sample-and-hold amplifiers. One very important design parameter in the sample-and-hold amplifier is the signal to noise plus distortion ratio (SNDR). The SNDR is defined as the ratio of the signal power at the fundamental frequency to the largest noise power at the harmonics. In Cadence circuit simulation, the transient simulation is performed to obtain the output voltage versus time. Discrete Fourier transform is then used to convert time response to frequency response. The SNDR is measured from the fundamental signal (at 2 MHz) to the peak noise signal (at 4 MHz) that takes place in the second harmonic. The simulated results are shown in Table 4.1. It is clear from Table 4.1 that the SNDR decreases after oxide stress. The soft breakdown has a minor effect, while the hard breakdown decreases the SNDR significantly, especially when the breakdown location is at the drain side of the MOS transistor. The SNDR changes from 35.1 dB to 27.1 dB when the breakdown resistance $R_{BD} (= 5 \text{ k}\Omega)$ is between gate and drain, and to 33.8 dB when the $R_{BD}$ is between gate and source [28]. Fig. 4.14 and 4.15 show the threshold voltage and mobility versus the SNDR. The SNDR decreases with the $V_{th}$ increase and SNDR increases with the increase of mobility, that is because when $V_{th}$ decreases or mobility increases the $R_{on}$ is decreased, which causes the noise power to increase, due to $SNDR = \frac{P_s}{P_D + P_N}$ SNDR will decrease.

### 4.2.3. Conclusion

Gate oxide soft breakdown and hard breakdown and breakdown location effect on the sample-and-hold mixed signal circuit are examined. The HBD located at the drain of the MOSFET degrades the mix-signal circuits under this study. The signal noise distortion ratio of the sample-and-hold circuit is sensitive to breakdown location as well. The SNDR decreases
significantly when the level of HBD damage at the drain side increases. However, the HBD at the source side has a relatively minor effect on the SNDR of the sample-and-hold circuit compared to that of the HBD at the drain side.

Figure 4.7 Schematic of Sample-and-hold circuit

Figure 4.8 Clock signal.
Figure 4.9 Gate Voltage of Switch M and input signal
Figure 4.10 Output Voltage vs. Time at fresh model.

Figure 4.11 Output Voltage vs. Time at NMOS4 model.
Figure 4.11 Output Voltage vs. Time using NMOS4 model

Figure 4.12 Output Voltage vs. Time at Drain side breakdown and breakdown current factor $M=0.05$
Figure 4.13 Output Voltage vs. Time when BD happen in source side M=0.05

Figure 4.14 SNDR vs. Threshold Voltage
Table 4.1 Simulated SNDR and $\Delta$SNDR/SNDR @ Different kinds of HBD position

<table>
<thead>
<tr>
<th>Device condition</th>
<th>Simulated SNDR (dB)</th>
<th>$\Delta$SNDR/SNDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fresh</td>
<td>35.1</td>
<td>0%</td>
</tr>
<tr>
<td>SBD</td>
<td>34.6</td>
<td>-1.4%</td>
</tr>
<tr>
<td>HBD @ drain/source ($R_{BD} = 30$ k$\Omega$)</td>
<td>32.2 / 34.4</td>
<td>-8.3% / 2.0%</td>
</tr>
<tr>
<td>HBD @ drain/source ($R_{BD} = 20$ k$\Omega$)</td>
<td>31.2 / 34.3</td>
<td>-11.1% / 2.3%</td>
</tr>
<tr>
<td>HBD @ drain/source ($R_{BD} = 10$ k$\Omega$)</td>
<td>30.7 / 34</td>
<td>-12.5% / 2.6%</td>
</tr>
<tr>
<td>HBD @ drain/source ($R_{BD} = 5$ k$\Omega$)</td>
<td>27.1 / 33.8</td>
<td>-22.8% / 3.7%</td>
</tr>
</tbody>
</table>
4.3. RF Circuits Performances under BD

4.3.1. Class-AB Power Amplifier

4.3.1.1. Introduction

Power amplifier is widely used in the RF transmitter and RF receiver. A Class-AB power amplifier is an important power amplifier which will be studied.

4.3.1.2. Circuit Analysis

A general class A, B, and C power amplifier circuit schematic is shown in Fig. 4.16 In this circuit, the dc blocking capacitor is used to isolate the dc and ac signal. The inductor and capacitor of the high-Q tank is used to shorten higher order harmonics at the fundamental frequency. The active n-channel transistor is biased to a quiescent point so that the conduction angle $\theta$ is at the right operation mode. For the class a power amplifier, the conduction angle is set to 360°. For the class B power amplifier $\theta$ equals 180°, while for the class AB amplifier $180^\circ < \theta < 360^\circ$. For the class C amplifier the conduction angle is less than 180°. The output power and drain efficiency for class A, B, and C power amplifiers are given as [34]

$$P_{out} = \frac{1}{2} (V_{DD} - V_{DSAT}) \frac{I_m}{2\pi} (\theta - \sin \theta) \quad (1)$$

$$\eta = \frac{V_m}{V_{DD}} \frac{\theta - \sin \theta}{4(\sin \frac{\theta}{2} - \frac{\theta}{2} \cos \frac{\theta}{2})} \quad (2)$$

Where $V_{DD}$ is the supply voltage, $V_{DSAT}$ is the knee voltage, $V_m$ is the maximum output voltage, and $I_m$ is the maximum current.
The maximum drain-source voltage $V_{DS}$ of the active transistor in a class A power amplifier could be as high as two times of $V_{DD}$ [35] due to symmetry of the sinusoidal waveform. The time-dependent drain-source voltage in fact is a function of input power level $p_{in}$. At high input power level, the drain-source voltage is distorted from the ideal sinusoidal waveform and $V_{DS}$ can be greater than $2 \times V_{DD}$ as evidenced by the Cadence Spectre simulation results in Fig. 4.17. In Fig. 4.17 the peak drain voltage reaches 3.6 V at $p_{in} = 0$ dBm, where the supply voltage $V_{DD} = 1.5$ V. The gate-source and drain-source waveforms at low input power level are sinusoidal. It is interesting to point out that at high input power level, when the drain voltage is beyond $2 \times V_{DD}$, the gate-source voltage could be less than 0 V (see Fig. 4.18). This provides a large drain-gate voltage for oxide over stress. At high input power level, the drain-source waveform is more like a class E switching than a class A current mode of operation. Also the time-dependent drain current in different input power is obtained in Fig. 4.19. In this figure the peak drain current changes from 0.035 A to 0.13 A when the input power increases from -20dBm to 0dBm. It is anticipated that the higher the input power level, the more gate oxide stress between the drain and the source. Consequently, more gate oxide breakdown damages will accumulate over time.

4.3.1.3. **Results and discussion**

A PA was used here for circuit simulation. The dc blocking capacitor is 7 pF. The inductor and capacitor of the high-Q tank used to short higher order harmonics at the fundamental frequency are 1nH and 30pF, respectively. The supply voltage is 1.5 V and the gate bias is 0.63 V. The device is biased to a quiescent point so that the amplifier is operated in the class-AB mode. The input drive level is adjusted so that the drain current swings between zero and a
predetermined maximum current. The biasing of the transistor corresponds to the measurement condition for the model extraction. The time-dependent drain current in high input power 0dBm under different gate oxide model is shown in Fig. 4.20. There is a slight increase as well as the phase change when breakdown becomes serious. Fig. 4.21 and 4.22 shows the output versus the input power, and the power added efficiency versus the input power in fresh model, no breakdown happens. When breakdown happens in the drain side the output power will increase and the efficiency will decrease, but when breakdown happens in the source side, the output power will decrease and the efficiency will increase as shown in table 4.2. That is because when breakdown happens in the gate to drain side, the drain current will increase and when breakdown happens in the gate to source side, the drain current will decrease.

The Cadence simulation results before stress (fresh device) and after stress (soft breakdown and different levels of hard breakdown) are given in table 4.2. Key BSIM3v3 model parameters used in Cadence simulation include $V_{TH0} = 0.345$, $K1 = 0.5869914$, $K2 = 416856E-3$, $K3 = 1E-3$, $U0 = 258$, and $VOFF = -0.089$. Also as seen in Table 4.2, the soft breakdown does not change the output power and power-added efficiency too much. When the hard breakdown becomes increasingly significant (a smaller breakdown resistance), the power-added efficiency decreases drastically while the breakdown damage location is at the drain side. $\eta_{add}$ changes from original 31.1% to 29.1%, 28.1%, 25.3%, and 20.8% when the HBD resistance is at 30 k$\Omega$, 20 k$\Omega$, 10 k$\Omega$, and 5 k$\Omega$, respectively. When the hard breakdown occurs at the source side, the power-added efficiency of the power amplifier surprisingly increases. This is because the reduction in $P_{DC}$ is larger than the decrease in $p_{out}$ when the HBD occurs at the source side. Using the partial
derivative, the change of drain efficiency can be normalized \((\Delta \eta/\eta \approx \Delta V_m/V_m + \Delta \theta f(\theta))[36]\). The normalized output power and drain efficiency for different breakdown damages are examined. The comparison between analytical equations above and Cadence SpectreRF simulation results is given in Table 4.3 and 4.4. As seen in these Tables, the degradation of drain efficiency is minimal after SBD. The drain efficiency decreases with the level of HBD at the drain side, but increases with the HBD at the source side as evidenced by a good agreement between the analytical predictions and Cadence simulation results.

4.3.1.4. Conclusion

Gate oxide soft breakdown, hard breakdown and breakdown location effect on the class AB power amplifier are examined. The SBD in the channel of the MOSFET does not affect the RF power amplifier and sample-and-hold circuit performances much. The HBD located at the drain of the MOSFET degrades the RF performance is under studied. The power-added efficiency and drain efficiency of the class AB power amplifier decrease with the increase in HBD oxide damages.
Figure 4.16 Schematic of Class-AB Power Amplifier

Figure 4.17 Drain Source Voltage vs. Time @ different Pin
Figure 4.18 Gate to source voltage vs. Time @ different Pin

Figure 4.19 Drain current vs. Time @ different Pin
Figure 4 20 Drain current vs. Time @ different degree of BD

Figure 4 21 Output power vs. Input power
Figure 4.22 Power Added Efficiency vs. Input power

Table 4.2 Output power and power efficiency vs. Breakdown Model

<table>
<thead>
<tr>
<th>Breakdown Model</th>
<th>Pout Power (dBm) Drain Side/Source side</th>
<th>Power Efficiency (%) Drain Side/Source Side</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fresh</td>
<td>11.15</td>
<td>31.1</td>
</tr>
<tr>
<td>Soft Breakdown (M = 30u)</td>
<td>11.21/11.12</td>
<td>29.63/32.25</td>
</tr>
<tr>
<td>Hard Breakdown R =30 kΩ</td>
<td>11.23/11.09</td>
<td>29.12/33.13</td>
</tr>
<tr>
<td>Hard Breakdown R =20 kΩ</td>
<td>11.26/11.04</td>
<td>28.12/33.45</td>
</tr>
<tr>
<td>Hard Breakdown R =10 kΩ</td>
<td>11.35/11.01</td>
<td>25.27/36.43</td>
</tr>
<tr>
<td>Hard Breakdown R =5 kΩ</td>
<td>11.54/10.85</td>
<td>20.8/39.5</td>
</tr>
</tbody>
</table>
Table 4 3 Output Power (Model Predictions vs. Simulation)

\[
\frac{\Delta P_{\text{out}}}{P_{\text{out}}} \approx \frac{\Delta I_m}{I_m} + \frac{\Delta \theta}{f_1(\theta)}
\]

\[
f_1(\theta) = \frac{\theta - \sin \theta}{1 - \cos \theta}
\]

<table>
<thead>
<tr>
<th>Model</th>
<th>Equation</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft Breakdown (M = 30 (\mu))</td>
<td>(\frac{\Delta I_m}{I_m} + \frac{\Delta \theta}{f_1(\theta)})</td>
<td>0.53 %</td>
</tr>
<tr>
<td>HBD (R = 30 k(\Omega))</td>
<td></td>
<td>0.74 %</td>
</tr>
<tr>
<td>HBD (R = 20 k(\Omega))</td>
<td></td>
<td>0.95 %</td>
</tr>
<tr>
<td>HBD (R = 10 k(\Omega))</td>
<td></td>
<td>1.75 %</td>
</tr>
<tr>
<td>HBD (R = 5 k(\Omega))</td>
<td></td>
<td>3.52 %</td>
</tr>
</tbody>
</table>

Table 4.4 Drain Efficiency (Model Predictions vs. Simulation)

\[ f_2(\theta) = \left( \frac{1 - \cos \theta}{\theta - \sin \theta} - \frac{\theta}{4} \frac{\sin \frac{\theta}{2}}{\sin \frac{\theta}{2} - \frac{\theta}{2} \cos \frac{\theta}{2}} \right)^{-1} \frac{\Delta \eta}{\eta} \approx \frac{\Delta V_m}{V_m} + \frac{\Delta \theta}{f_2(\theta)} \]

<table>
<thead>
<tr>
<th>BD level</th>
<th>Equation</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft BD (M = 30 u)</td>
<td>(\Delta V_m/V_m + \Delta \theta/f_2(\theta))</td>
<td>0.59 %</td>
</tr>
<tr>
<td>HBD (R = 30 kΩ)</td>
<td></td>
<td>1.08 %</td>
</tr>
<tr>
<td>HBD (R = 20 kΩ)</td>
<td></td>
<td>1.81 %</td>
</tr>
<tr>
<td>HBD (R = 10 kΩ)</td>
<td></td>
<td>3.92 %</td>
</tr>
<tr>
<td>HBD (R = 5 kΩ)</td>
<td></td>
<td>8.61 %</td>
</tr>
</tbody>
</table>
4.3.2. Class-E Power Amplifier

The advance CMOS technology for high-frequency applications has made it a natural choice for integrated, low cost RF power amplifiers (PAs) in wireless front-end products. With the smaller dimensions for improving speed and functionality, each successive generation of CMOS transistors in a deep sub-micrometer regime has resulted in major reliability issues such as channel hot electron effect [37] and gate oxide breakdown (BD) [38-39].

Recently, many papers on CMOS device and RF circuit performance degradations after hot electron and gate oxide breakdown effects were reported [40-43]. These RF circuits include low noise amplifiers [40-41], oscillators [42], and power amplifiers [43]. For the low noise amplifiers, the noise figure increases and power gain $S_{21}$ decreases after gate oxide breakdown [40]. For the oscillators, the phase noise increases and tuning range decreases after channel hot electron stress and gate oxide breakdown [42]. For the RF power amplifiers, the class-E amplifier degrades faster than the class-A amplifier due to a much higher level of stress in class-E amplifier during switching. In [40, 41, 43], however, the transistor model parameters were extracted after DC stress, not after RF stress for circuit operation.

In this work the RF stress on the power amplifier performance including effect of oxide breakdown location was evaluated. The class-E circuit topology was selected since the class-E power amplifier inherits large peak voltages and currents in RF operation, leading to higher probability of gate oxide breakdown [44]-[52]. Transistor model parameters were extracted after RF stress to account for the circuit operation condition. Analytical modeling of power efficiency
as a function of duty cycle and mobility is derived. The analytical predictions are compared with Cadence RF simulation results for model utility and accuracy.

4.3.2.1. **Reliability Effect on Class-E Power Amplifier Performance**

The analytical modeling of the reliability effect is now presented on the class-E power amplifier. Since the gate oxide breakdown results in the drain current degradation [53] [56] [57] [58], the degradation could be related to changes in mobility from the modeling prospective.

Fig. 4.23 depicts the basic Class-E amplifier [54] consisting of an n-channel MOS transistor, shunt capacitance ($C_1$), RLC series-resonant circuit ($L_2$ and $C_2$), RF choke (inductor $L_1$), and load resistor $R_L$. The MOSFET is operated as a switch with duty cycle ratio $D$ at the frequency of interest. The class-E circuit reduces losses by switching the MOSFET when the drain-to-source voltage is zero. This mode of operation is called zero-voltage switching (ZVS). Although the only requirement for ZVS is that the drain voltage be zero at switch closure, a nominal ZVS condition occurs when the class-E amplifier is designed such that both the drain voltage and the rate of change of drain voltage ($dV_d/dt$) reach zero at the instant when the MOSFET is switched on. This nominal ZVS condition is referred to as zero-derivative switching (ZDS).

For the ideal class-E power amplifier, the drain current and drain voltage are carefully designed to avoid any overlapping of drain current and drain voltage at a given time in the transient waveform. For example, $i_d = 0$ when $v_d$ rises and $v_d = 0$ when $i_d$ rises. Thus, the transistor power loss is equal to zero (i.e., $\int i_d (t) \times v_d (t) = 0$) and the drain efficiency is ideally 100%. However, due to finite channel resistance $R_{DS}$ and transistor switching speed, the
overlapping of \(i_d\) and \(v_d\) during switching transient cannot be avoided. The drain efficiency of the class-E PA is thus less than 100%. Using the boundary conditions of ZVS and ZDS at the instant of switching on, the power loss through \(R_{DS}\) is derived as

\[
P_{R_{on}} = R_{DS} \left( \frac{P_L}{V_{DD}} \right)^2 \left\{ 2 - D + \frac{\pi (1 - D)^2 \left[ 2 \pi D - \cos(2 \pi D + 2 \phi) \sin(2 \pi D) \right]}{\left[ \cos(2 \pi D + \phi) - \cos(\phi) \right]^2} \right\}
\]

(3)

Where \(P_L\) is the power delivered to the load resistance, \(V_{DD}\) is the supply voltage, and \(\phi\) is the phase angle given by [55]

\[
\phi = \tan^{-1} \left[ \frac{\cos(2 \pi D) - 1}{2 \pi (1 - D) + \sin(2 \pi D)} \right] + n \pi
\]

(4)

Taking into accounting the power loss in the MOS transistor, the efficiency is simply written as

\[
\eta = \frac{P_L}{P_L + P_{R_{on}}}
\]

(5)

Combining (3) and (5) yields

\[
\eta = \frac{P_L}{P_L + R_{DS} \left( \frac{P_L}{V_{DD}} \right)^2 \left\{ 2 - D + \frac{\pi (1 - D)^2 \left[ 2 \pi D - \cos(2 \pi D + 2 \phi) \sin(2 \pi D) \right]}{\left[ \cos(2 \pi D + \phi) - \cos(\phi) \right]^2} \right\}}
\]

(6)

In (6) the channel resistance may be approximated as

\[
R_{DS} \approx \frac{L}{\mu_n C_{ox} W (V_G - V_T)}
\]
Where $\mu_n$ is the electron mobility, $C_{ox}$ is the oxide capacitance per area, $W$ is the channel width, $L$ is the channel length, and $V_T$ is the threshold voltage. The power deliver to the load resistance is

$$P_L = 2V_{DD}^2 \frac{\sin^2(\pi D + \phi) \sin^2(\pi D)}{\pi^2 (1-D)^2 R_L}$$

(7)

### 4.3.2.2. Results and Discussion

The class-E RF power amplifier in Fig. 4.23 has the supply voltage of 1.5 V, the gate bias of 0.7 V, the inductors $L_1 = 900$ pH, $L_2 = 20$ nH, and the capacitors $C_1 = 1$ pF, $C_2 = 11$ pF. The transistor model parameters were extracted using BSIMPro after the gate and drain RF stress for 7200 seconds. The device used in the Cadence simulation has 0.16 $\mu$m of channel length and 800 $\mu$m of channel width. Each of 40 fingers is modeled by the extracted 0.16×20 $\mu$m$^2$ NMOS model for the fresh device as well as the stressed device. The transistor model including the gate oxide breakdown location effect is used in the class-E power amplifier simulation. Fig. 4.24 and 4.25 shows the drain current and drain voltage waveforms obtained from Cadence SPICE simulation. In Fig. 4.24 and 4.25 the solid line represents the fresh model and the lines with symbols represent the stressed devices with different breakdown locations. When the oxide breakdown occurs at the drain side, the overlapping of the drain current with respect to the drain voltage during rising and falling times in Fig. 4.24 and 4.25 increases. This may be due to an increase of the gate leakage current going through the gate-drain path. Fig. 4.26 displays the efficiency versus normalized breakdown location. $x = 0$ represents the breakdown at the source side and $x = 1$ represents the breakdown at the drain side. The Cadence simulation results in Fig. 4.26 show that the efficiency decreases with $x$. As seen in Fig. 4.26 more drain currents are overlapped with
non-zero drain voltage when the breakdown position is closer to the drain side. This results in more power loss in the active transistor and thus reduced power efficiency.

The drain efficiency as a function of duty cycle rate is simulated. The model predictions using (6) are compared with the circuit simulation results in Fig. 4.27. In Fig. 4.27 the solid line represents the model predictions and solid circles represent the Cadence simulation. The power efficiency increases with duty cycle for $D < 50\%$ and then decreases with duty cycle for $D > 50\%$. Good agreement between the analytical predictions and Cadence simulation is obtained. This demonstrates the model utility in (6) and its accuracy. The stress effect on the drain efficiency is evaluated. Fig. 4.28 shows the efficiency versus channel mobility. The gate voltage stresses decrease the mobility of the MOS transistor and thus the drain efficiency. In Fig. 4.28 the solid lines represent Cadence simulation results and symbols represent the model predictions. Good agreement between the model predictions and circuit simulation is obtained. Again, Fig. 4.28 indicates that the efficiency decreases after RF stress due to reduce channel mobility or drain current.
Figure 4.23 Schematic of Class-E power amplifier

Figure 4.24 Simulated drain current waveforms vs. time for fresh and stressed devices with different breakdown locations.
Figure 4.25 Simulated drain voltage waveforms vs. time for fresh and stressed devices with different breakdown locations.

Figure 4.26 Simulated efficiency vs. gate oxide breakdown location.
Figure 4.27 Predicted and simulated efficiency as a function of duty cycle rate.

Figure 4.28 Predicted and simulated efficiency as a function of mobility.
4.3.3. LC-Oscillator

4.3.3.1. Introduction

LC-oscillator is a common and widely used RF circuits because of the implementation of a cheap and reliable monolithic voltage-controlled oscillator (VCO) for the integrated SOC RF CMOS transceivers [59]-[61]. As the CMOS device size shrinks, the gate voltage is sustained across the thin gate oxide of the transistor for a time; the breakdown phenomenon is more likely to happen.

Typically there are two types of LC oscillators, as shown in Fig. 4.29 and 4.30. The first one is with two NMOS transistor, and the second one consists of two PMOS transistor and two NMOS transistors which are called complementary LC oscillators. Due to their special structure with PMOS transistor, it most likely subject to another reliability effect which is NBTI effect [62-67].

4.3.3.2. Circuit Performance-Important parameter

A. Drain To Source Voltage

In LC oscillators, a 2.4GHz frequency is used in Fig. 4.29; also it consists of two ideal inductors and an ideal capacitor. The amplitude of the oscillation is simulated for different kinds of supply voltage using cadence spectreRF circuit simulator. The inductors and capacitor are charging and discharging to supply additional voltage to the drain side during the on state, as shows in Fig. 4.31, the amplitude of the drain-source voltage could reach up to 5 volts, due to this high drain side voltage the breakdown effect likely happens in the
drain side. The models which were extracted in the modeling part of chapter 3 were used to study the different kinds of BD effects. As shown in the table 4.5, the drain voltage decreases when BD become serious. This is because when BD becomes worse and worse, it is almost like short circuit for the gate to drain side or gate to source side, so the drain source voltage will decrease. Also from the table, the BD most likely happens in the gate to drain side due to the high drain side voltage.

B. Oscillator Phase Noise

The mechanisms for phase noise have been reported in [68]-[70]. The phase noise of an LC oscillator at an offset frequency of $\omega_c$ from the frequency of oscillation $\omega_0$, normalized with respect to the carrier is given by:

$$\mathcal{Z}(\omega_c) = 10 \log \left[ \frac{4kTFR_{LC}}{V_m^2} \cdot \left( \frac{\omega_0}{2Q\omega_m} \right)^2 \right]$$

Where $F = 2 + \frac{8\gamma R_{eq}I_{tail}}{\pi V_m} + \gamma \frac{8}{9} g_{mhias} R_{eq}$. The three terms in F account for thermal noise for the tank resistance, differential pair and tail current source, respectively. The loaded quality factor $Q$ depends on the inductors and capacitors. Fig. 4.32 shows the phase noise of the oscillator for different numbers of BD models. As the amplitude of oscillation degrades as the gate oxide BD progress, the phase noise of the oscillator will increase. At a given offset frequency, the higher the number of finger BD, the higher the phase noise of the oscillator. [71]-[73].

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4.3.3.3. **Conclusion**

Overall the LC oscillator is likely to suffer from the gate oxide BD effect, two important parameters drain to source voltage and phase noise was studied.

![Figure 4 29 Schematic of LC-oscillator](image1)

![Figure 4 30 Complementary LC oscillator](image2)
Figure 4: Drain-to-source voltage vs. Time
Table 4.5 Voltage vs. Different kinds of BD Models

<table>
<thead>
<tr>
<th>MODEL</th>
<th>VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRESH</td>
<td>6.21</td>
</tr>
<tr>
<td>PMOS4</td>
<td>6.122</td>
</tr>
<tr>
<td>PMOS3</td>
<td>6.041</td>
</tr>
<tr>
<td>NMOS4</td>
<td>5.812</td>
</tr>
<tr>
<td>NMOS2</td>
<td>5.57</td>
</tr>
<tr>
<td>NMOS3</td>
<td>49</td>
</tr>
</tbody>
</table>

PMOS4  
X=1 \( f(V_g,V_d)=0.00003(V_g-0.9V_d) \)

PMOS3  
X=0.3 \( f(V_g,V_d)=0.00008(V_g^2+0.001V_g+0.05V_d^2+0.1V_d-0.12) \)

NMOS4  
X ALMOST 0 \( f(V_g,V_d)=0.0013(V_g) \)

NMOS2  
X ALMOST 0 \( f(V_g,V_d)=0.00042(V_g^2) \)

NMOS3  
X=0.8 \( f(V_g,V_d)=0.00015(0.2V_g^5+9V_g-V_d^3+V_d^2+2V_d-5) \)
Figure 4 32 Phase noise vs. Frequency
**4.3.4. Dual-Band Class-E Power Amplifier**

Currently, power and size are two key important factors for modern circuits design. Dual-Band circuits are beneficial to reduce the number of circuit components in modern wireless communication systems which have two frequency bands, such as dual-band LNA, dual-band mixer, and dual-band Pas. The dual-band class-E Power Amplifier [74] - [80] is studied in this chapter.

### 4.3.4.1. Dual-Band Class-E Power Amplifier Design

The circuit schematic for the dual-band power amplifier is shown in Fig. 4.33. It consists of a transistor acting as a switching shunt capacitor Cs and other components. The Class-E power amplifier has the inductors L1=2.635 nH, L2=5 nH, capacitors C1=20 pF, C2= 20 pF, and the supply voltage of 1.5 V. The MOS transistor of the power amplifier is biased at 1 V. The transistor SPICE model parameters were extracted by using BSIMPro after 10, 20, 40, 60, and 100 minutes of DC stress, respectively. The MOSFET used in the Cadence SpectreRF simulation has 90 nm of channel length and 800 um of channel width. The dual band class-E power amplifier is operating at 800MHz and 2.1GHz sin input signal.

### 4.3.4.2. Circuits Analysis and Simulation Results

The proposed dual-band class-E power amplifier was simulated using Cadence SPICE at cellular (800MHz) and (2.1GHz) frequency.
Fig. 4.34, 4.35, and 4.36 show the drain voltage, drain current and gate voltage changing with the input power at 800MHz frequency. From the pictures, once the input power increase, the Vds,Ids and Vgs increase too, for Vds the increment up to 6 volts when the input power is up to 10dBm, which will trigger the breakdown effect happen in the transistor.

The condition for Fig. 4.37, 4.38, and 4.39 is Pin up to 10dBm, T=25. The Vdd effect was studied also. It is well known that the input dc voltage is another important factor for circuit design. It was seen when the input voltage increases to 2.5 volts, the drain voltage could increase up to 9 volts, and the drain current could increase up to 400mA. But from Fig. 4.39, there is no change for the gate to source voltage which is because the gate to source voltage is only determined by the input power and dc biasing voltage; it has nothing to do with the dc voltage.

Overall two important factors for the circuits were studied: the input power, dc input voltage and the breakdown most likely happen for the dual-band class-E circuits. Fig. 4.40 is the new circuit schematic to study breakdown effect of the circuit. Two current sources were added from the gate to drain side and the gate to source side to model the breakdown effect. The two tables below show how the BD current influences the PAE and Pout. For table 4.6 the condition is Pin=10dbm Vdc=1.5 and the BD happens in the drain side. In this case, both PAE and Pout decrease with the increase of the BD current, which is because when BD happens in the drain side, Ids decrease. The condition for Table 4.7 is almost the same as table 4.6, but this time BD happens in the source side, surprisingly when breakdown happen in the source side, the output power decrease when breakdown become more serious, however, the efficiency increases. The reason is even though the output power decreases, the dc power decreases more than the output.
power. The proposed dual-band class-E power amplifier was simulated using cadence IC design tool at 800MHz and 2.1GHz. The transistor model used is TSMC0.18 technology.

Fig. 4.41-4.43 shows how the Pout and PAE change with Pin at different Vdd in 800MHz operation frequency. It can be seen that at the given input power, the output power will increase with an increase of the dc voltage, but PAE will decrease with an increase of dc voltage, because the Pout increases the dc power, more than the output power, which is shown in Fig. 4.43.

Fig. 4.44-4.47 shows the Pout and PAE versus Pin in different VDD at 2.1GHz operation frequency. The result is almost the same as 800MHz, but still slightly different. The difference is for the PAE, when operated at 2.1GHz the PAE increases with VDD at given Pin, because this time Pout increases more than dc power, which is shown in Fig. 4.47.

4.3.4.3. Circuits Study and Equation derivation

The series-resonant current is

\[ i = I_m \sin(\omega t + \phi) \]  

(1)

Applying KCL yields the relationship among switch current \( (i_s) \), shunt capacitor current \( (i_{c1}) \), dc input current \( (I_f) \), and series-resonant current \( (I_m) \)

\[ i_s + i_{c1} = I_f - I_m \sin(\omega t + \phi) \]

(2)
The switch remains closed during the interval $0 < \omega t \leq 2\pi D$ and is open during the interval when $2\pi D < \omega t \leq 2\pi$ therefore,

$$
\begin{align*}
  i_s(t) &= \begin{cases} 
    I_i - i - I_m \sin(\omega t + \phi), & \text{for } 0 < \omega t \leq 2\pi D \\
    0, & \text{for } 2\pi D < \omega t \leq 2\pi
  \end{cases} \\
  i_{c1}(t) &= \begin{cases} 
    0, & \text{for } 0 < \omega t \leq 2\pi D \\
    I_i - i - I_m \sin(\omega t + \phi), & \text{for } 2\pi D < \omega t \leq 2\pi
  \end{cases}
\end{align*}
$$

(3) (4)

The switch and shunt capacitance are in parallel with the switch closed during the interval from $0 < \omega t \leq 2\pi D$ and open during the interval from $2\pi D < \omega t \leq 2\pi$. Therefore, we obtain

$$
V_s = V_{c1} = \begin{cases} 
    0, & \text{for } 0 < \omega t \leq 2\pi D \\
    \frac{1}{\omega C_1} \int_{2\pi D}^{\infty} i_{c1}(\omega t) d(\omega t), & \text{for } 2\pi D < \omega t \leq 2\pi
  \end{cases}
$$

(5)

The switch closes when $\omega t = 2\pi$ and $V_s = 0$ (ZVS condition of class-E operation)

Base on the above equation, $V_{Rm}$ which is output the peak-to-peak load voltage could be derived.

$$
V_{Rm} = \frac{1}{\pi} \int_{2\pi D}^{2\pi} V_s \sin(\omega t + \phi) d(\omega t) = \frac{-2V_{dd} \sin(\pi D) \sin(\pi D + \phi)}{(1 - D)\pi}
$$

(6)

And the output power is

$$
P_L \approx \frac{V_{Rm}^2}{2R} \approx 2 \frac{V_{dd}^2 \sin^2(\pi D) \sin^2(\pi D + \phi)}{\pi^2(1 - D)^2 R}
$$

(7)
\[
PAE = \frac{P_L - P_{in}}{P_L + P_{loss}} \times 100\% \tag{8}
\]

\[
P_{loss} \approx ib \times V_{gd}^3 \quad \text{(BD in drain side)} \quad P_{loss} = ib \times V_{gs}^3 \quad \text{(BD in source side)} \tag{9}
\]

\[
P_{in} \approx \frac{V_{gs}^2}{Z} \tag{10}
\]

\[
V_{gs} \approx \sqrt{P_{in} \times Z} \tag{11}
\]

\[
\phi = \tan^{-1} \left[ \frac{\cos(2\pi D) - 1}{2\pi(1 - D) + \sin(2\pi D)} \right] + n\pi \tag{12}
\]

\[
P_L \approx \frac{V_{Rm}^2}{2R} \approx 2 \frac{V_{dd}^2 \sin^2(\pi D) \sin^2(\pi D + \phi)}{\pi^2(1 - D)^2 R} \tag{13}
\]

\[V_{Rm} \] is the peak-to-peak load voltage.

\[
V_{Rm} = \frac{1}{\pi} \int_{2\pi D}^{2\pi} V_s \sin(\omega t + \phi) d(\omega t) = -\frac{2V_{dd} \sin(\pi D) \sin(\pi D + \phi)}{(1 - D)\pi} \tag{14}
\]

\[
V_{ds} = \frac{V_{dd} \tan(\pi D + \phi) \sin(\pi D)}{(1 - D)\left[(1 - D)\pi \cos(\pi D) + \sin(\pi D)\right]} \left[\omega t - 2\pi D + \frac{2\pi(1 - D)\left[\cos(\omega t + \phi) - \cos(2\pi D + \phi)\right]}{\cos(2\pi D + \phi) - \cos(\phi)}\right] \tag{15}
\]

Frequency = 2.1GHz

Vdd=1.5

Pin=10dbm

\[
PAE \approx \frac{50}{150 + x \times ib \times V_{gd}^3} \times 100\% \quad \text{BD in drain side} \tag{16}
\]
$$PAE \approx \frac{50}{150 - x \times ib \times V_{gs}^3} \times 100\% \quad \text{BD in source side}$$

Equation 16 and 17 is the final PAE equation after BD happens in drain side and source side. $x$ is the fitting parameter, $ib$ is the gate leakage current, $V_{gd}$ is the gate to drain side voltage and $V_{gs}$ is gate to source current. From the equations, the basic idea of how the gate leakage current influences power efficiency was obtained.

### 4.3.4.4. Conclusion

Overall, $V_{dd}$ and $P_{in}$ effect were studied on the circuit performance. Some important circuit performance parameters such as $V_{gs}$, $V_{ds}$, $I_{ds}$, $P_{out}$ and $PAE$ were evaluated. Moreover, the breakdown location and soft/hard breakdown are studied, some circuit performance data was provided. And all those information is very useful for the dual-band class-E circuits design.

<table>
<thead>
<tr>
<th>BD CURRENT (A)</th>
<th>Efficiency (%)</th>
<th>Pout (dbm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRESH</td>
<td>33.48</td>
<td>17.33</td>
</tr>
<tr>
<td>1u</td>
<td>33.25</td>
<td>17.32</td>
</tr>
<tr>
<td>50u</td>
<td>25.38</td>
<td>17.32</td>
</tr>
<tr>
<td>100u</td>
<td>21.52</td>
<td>17.27</td>
</tr>
<tr>
<td>300u</td>
<td>14.57</td>
<td>17.09</td>
</tr>
<tr>
<td>500u</td>
<td>10.99</td>
<td>16.92</td>
</tr>
</tbody>
</table>
Table 4.7 BD happen in source side

<table>
<thead>
<tr>
<th>BD CURRENT (A)</th>
<th>Efficiency (%)</th>
<th>Pout (dbm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRESH</td>
<td>33.48</td>
<td>17.33</td>
</tr>
<tr>
<td>1u</td>
<td>33.72</td>
<td>17.29</td>
</tr>
<tr>
<td>50u</td>
<td>40</td>
<td>16.97</td>
</tr>
<tr>
<td>100u</td>
<td>42.61</td>
<td>16.74</td>
</tr>
<tr>
<td>300u</td>
<td>43.9</td>
<td>16.21</td>
</tr>
<tr>
<td>500u</td>
<td>45.2</td>
<td>15.94</td>
</tr>
</tbody>
</table>

Figure 4.33 Schematic of the dual-band power amplifier
Figure 4 34 Drain voltage vs. Time @ different Pin (800MHz)

Figure 4 35 Drain current vs. Time @ different Pin (800MHz)
Figure 4 36 Gate to source voltage vs. Time @ different Pin (800MHz)

Figure 4 37 Drain current vs. Time @ different VDD (800MHz)
Figure 4.38 Drain voltage vs. Time @ different VDD (800MHz)

Figure 4.39 Gate to source voltage vs. Time @ different VDD (800MHz)
Figure 4.40 Schematic of a dual band Class-E power amplifier with the breakdown current model.

Figure 4.41 Pin vs. Pout @ different VDD (800MHz)
Figure 4.42 Pin vs. PAE @ different VDD (800MHz)

Figure 4.43 Pin vs. Pdc @ different VDD (800MHz)
Figure 4.44 Pin vs. Pout @ different VDD (2.1GHz)

Figure 4.45 Pin vs. PAE @ different VDD (2.1GHz)
Figure 4.46 Pin vs. PAE @ different VDD (2.1GHz)

Figure 4.47 Pin vs. Pdc @ different VDD (2.1GHz)
CHAPTER FIVE: CIRCUITS PERFORMANCE UNDER HOT CARRIER EFFECT

In the previous chapter, hot carriers effect mechanism was introduced. Recently, many papers on CMOS-devices and RF-circuit performance degradations after hot-carrier effects were reported. These RF circuits include low noise amplifiers, mixer and PAs. For the low noise amplifiers, the noise figure increases and the power gain $S_{21}$ decreases after HCI stress. For oscillators, the phase noise increases after HCI stress [81]-[84]. For RF PAs, the power added efficiency will decrease after the HCI stress. Also different kinds of devices were studied under the hot electrons stress effect, such as High-K (HfO2, Al2O3 and Ta2O5) and SOI device. Here, the new device SiN380 and Tensile 700A were used to study the hot electron effect. The dual band class-E [85] and LNA-mixer [86]-[87] combination circuit are selected for evaluation the hot carrier effect. The transistor-model parameters were obtained after hot electron stress to account for the circuit-operation condition. The device performance such as the I-V characteristics was also studied.

5.1. **Device**

A. **Technology.**

As the gate length of CMOSFETs scales below 100 nm, it is very difficult to maintain high drive current density due to the degradation of carrier mobility in channel region. Therefore, high mobility technology is required to get a high performance device. One way is to modify the
thickness of high-tensile-stress contact etch stop layer, length of diffusion and gate width to control the tensile and compressive stresses in channel region to improve the channel mobility.

Gate material is 1.6 nm nitride oxide which was grown using rapid thermal oxidation in a NO ambient. Then, composite oxide/SiN spacers and source-drain junctions were formed using low-temperature processing and arsenic/boron ion implantations, respectively. Following, conventional SiN layer and tensile stress layer were down with furnace-deposited, SiN 380A and high tensile stress contact etch stop layer (CESL) 700A. High tensile CESL strain increases the device channel mobility and drain current.

The use of strain technique such as relaxed SiGe layer or epitaxial SiGe in the source and drain regions to improve mobility has become popular. One of the easy ways to enhance devices mobility without accompanying the increase of process steps is modifying the thickness of high-tensile-stress contact etch stop layer to control the tensile and compressive stresses in the channel region to improve the channel mobility. For a nMOSFET, for example, the tensile stress caused by HS CESL [88]-[95] in the direction parallel to the channel is the major factor for mobility improvement.

B. Experiment and data

Partially depleted (PD) SOI CMOSFETs were fabricated on <100> channel orientation SOI substrate based on advanced 90nm process with 200nm buried oxide layer (BOX) and 40nm SII layer using STI isolation technology. Device measurements and hot-carrier stressing were performed at the probe station using various drain voltage (VD=0-1.4V), and various gate voltages (Vg=0-1.4V) with up to 100 minutes hot-carrier stress time. Fig. 5.1 shows the ID-VD
characteristics of tensile 700A and SiN 380 device after 100min hot-carrier stressing. ID-VG characteristics of tensile 700A and SiN 380 device is shown in Fig. 5.2, the device’s Vt shifted after hot-carrier stressing and ID degrades after the hot-carrier stress. It is well known that the short-channel nMOS transistors were subjected to high electric field along the channel exhibit device degradation. The hot electron effect increases the threshold voltage (Vt) and decreases the mobility of the SiN380 and Tensile 700A device, which is shown in Fig. 5. 3 (a) and Fig 5. 3 (b). RF parameters such as power added efficiency, power gain, IP3 and noise figure are also degraded after channel hot-carriers stress. [97]

5.2. **Circuits Analysis and Simulation Results**

Power amplifiers are essential circuits for wireless communications. In several power amplifiers, the switched-mode class-E tuned power amplifiers with a shunt capacitor have found widespread application due to their simplicity design and high power efficiency. Concurrent dual-band operation is beneficial to reduce the number of circuit components in modern mobile systems requiring two frequency bands. The use of concurrent right/left-handed transmission lines allows for the manipulation of phase slope and phase offset at zero frequency for the design a dual-band class-E power amplifier [86].

Recently, RF circuit design has required less size and more function which will make the product smaller and smaller. Because of this, dual band and combination circuits are very popular around the world; here dual band class-E power amplifiers and LNA-mixer combination circuits are used as an example to study the performance subject to hot electron effect. The circuit schematic for the dual-band power amplifier is shown in Fig. 5.4 It consists of a transistor
acting as a switching shunt capacitor Cs and other components. The input source will provide the two different kinds of frequency, one is 800M Hz, the other one is 2.1G Hz sin input signal. C1, C2 and L2 composite output impedance matching network for dual band class-E power amplifier. The 5-GHz LNA-mixer combination of Fig. 5.5 was designed with a 90-nm transistor. The input matching network includes inductor Li and capacitor Ci for LNA part, and L1, C1, L2, C2 composite the mixer match part [96].

5.3. Results and Discussion

The dual band class-E PA shown in Fig. 5.4 has the supply voltage of 1.5 V, the gate bias of 1 V, the inductors L1= 2.635 nH and L2=5 nH, and the capacitors C1= 20 pF and C2=20 pF. The transistor-model parameters were extracted using BSIMPro after dc stress for 10, 20, 40, 60 and 100 minutes respectively. The device used in the cadence simulation has 90 nm of channel length and 800 μm of channel width. The mobility and Vt shift was shown in Fig. 5.3 (a) and Fig. 5.3 (b) for SiN 380 device and Tensile 700 device. The solid line represents the SiN 380 device and the line with symbols represents the Tensile 700 device. Mobility decreases and Vt increases after the hot electron stress for both of the two devices. Fig. 5.6 shows the drain-current and drain-voltage waveforms obtained from Cadence SPICE simulation. In Fig. 5.6, the solid line represents the fresh model for Tensile 700 device and the lines with symbols represent the fresh model for SiN 380 device while the dual band class-E PAs is operating at 800 MHz frequency with the input power of 0 dBm. The maximum voltage and current for the Tensile 700A device is slightly bigger than the SiN 380 device, which is because the model parameter Vt for Tensile 700A device is larger than SiN 380 device. Fig. 5.7 shows the efficiency and output
power obtained from Cadence SPICE simulation which the dual band class-E PAs is operating at 2.1 GHz frequency. Fig. 5.8 shows the power efficiency and output power versus hot electron stress time at 15 dBm input power for both Tensile 700A and SiN 380 device. The Cadence-simulation results in Fig. 5.8 show that the power efficiency increase and output decrease with the hot electron stress time is because of the Vt increase and mobility decrease after hot electron stress.

The LNA-mixer combination circuit in Fig. 5.5 has the supply voltage of 1.5 voltages, the inductors L1= 6.5 nH and L2=13.5 nH, and the capacitors C1= 1 pF and C2=2 pF. Fig. 5.9 shows the IIP3 versus hot electron stress time for both Tensile 700A and SiN 380 device at the fresh model. The cadence-simulation result in Fig. 5.9 show that IP3 will decrease with the hot electron stress time. Fig. 5.10 shows the noise figure waveforms at different kinds of stress time which is obtained from cadence simulation tool for both Tensile 700A device and SiN 380 device, but it only slightly changes for different kinds of stress time. The same thing happens for S21 and S11, which are shown in Fig. 5.11 and Fig. 5.12 for both Tensile 700A device and SiN 380 device. The S21 and S11 also slightly change with the stress time.

5.4. **Conclusion**

The Tensile 700A and SiN 380 device dc performances are examined experimentally. The hot electron effect on the dual band class-E PAs and LNA-mixer combination circuit performance has been examined using the model parameters extracted after DC stress. The efficiency decreases significantly after hot electron happens 100 minutes for the dual band class-E PAs circuit. IIP3 also decreases a lot but noise figure, S11, and S21 are slightly changed after
the hot electron stress for the LNA-mixer combination circuit. The decline in efficiency after stress is due to an increase threshold voltage and a decrease in the channel mobility or drain-current.
Figure 5.1 (a) $I_D - V_{DS}$ characteristics before and after hot-carrier stress for SiN 380 device.

Figure 5.1 (b) $I_D - V_{DS}$ characteristics before and after hot-carrier stress for Tensile 700A device.
Figure 5.2 (a) $I_D-V_{GS}$ characteristics before and after hot-carrier stress for SiN 380 device.

Figure 5.2 (b) $I_D-V_{GS}$ characteristics before and after hot-carrier stress for Tensile 700A device.
Figure 5.3 (a) Mobility versus stress time for both SiN 380 and Tensile 700A device.

Figure 5.3(b) Threshold voltage versus stress time for both SiN 380 and Tensile 700A device.
Figure 5.4 Schematic of a dual band Class-E power amplifier.

Figure 5.5 Schematic of a LNA-mixer combination circuit.
Figure 5.6 (a) Drain-source voltage and (b) drain current versus time at the fresh mode for both SiN 380 and tensile 700A device from cadence circuit simulation.
Figure 5.7 (a) Power added efficiency and (b) output power versus input power at fresh mode for both SiN 380 and tensile 700A device from cadence circuit simulation.
Figure 5.8 (a) Power added efficiency and (b) output power versus hot-carrier stress time for both SiN 380 and tensile 700A device from cadence circuit simulation.
Figure 5.9 IP3 versus hot-carrier stress time for (a) SiN 380 and (b) tensile 700Å device.
Figure 5.10 Noise figure versus frequency at different hot-carrier stress time for (a) SiN 380 and (b) tensile 700A device.
Figure 5.11 S11 versus frequency at different hot-carrier stress time for (a) SiN 380 and (b) tensile 700A device.
CHAPTER SIX: CONCLUSIONS

6.1. Achievement

This dissertation has studied the CMOS device reliability-gate oxide breakdown and HC effect in circuit’s performance. Deep understanding and study of gate oxide breakdown mechanisms are present; gate oxide breakdown leakage current equation was derivate. Gate oxide breakdown model for circuit simulation was developed here. The investigations of performance degradation due to gate oxide breakdown effect SRAM, Sample-and-hold, Class-AB power amplifier, Class-E power amplifier, and dual band class-E power amplifier are studied. HC effect on dual band Class-E power amplifier and LNA-mixer combination are also studied.

6.2. Future Work

The traditional CMOS technology was well studied in the past 20 years. Recently high-k device and LDMOS are more popular not only in the research but also in the real industry. Intel, AMD, and IBM spend a lot of money to do research on high-k devices, and real products already developed and sold in the market right now. The study of high-k devices is still not very well known by the industry, for the future work high-k device under gate oxide breakdown effect on circuit performance will be studied. Furthermore for high power devices, GaN device is another target. Consequently, more studies will be accomplished in my future research.
REFERENCES


[7] IC Insight


