Design And Modeling Of Radiation Hardened Lateral Power Mosfets

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DESIGN AND MODELING OF RADIATION HARDENED LATERAL POWER MOSFETS

by

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B.S.E.E University of Central Florida, 2008

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the School of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

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2009

Major Professor: Dr. Z. John Shen
ABSTRACT

Galactic-cosmic-rays (GCR) exist in space from unknown origins. A cosmic ray is a very high energy electron, proton, or heavy ion. As a GCR transverses a power semiconductor device, electron-hole-pairs (ehps) are generated along the ion track. Effects from this are referred to as single-event-effects (SEEs). A subset of a SEE is single-event burnout (SEB) which occurs when the parasitic bipolar junction transistor is triggered leading to thermal runaway. The failure mechanism is a complicated mix of photo-generated current, avalanche generated current, and activation of the inherent parasitic bipolar transistor.

Current space-borne power systems lack the utility and advantages of terrestrial power systems. Vertical-double-diffused MOSFETs (VDMOS) is by far the most common power semiconductor device and are very susceptible to SEEs by their vertical structure. Modern space power switches typically require system designers to de-rate the power semiconductor switching device to account for this. Consequently, the power system suffers from increased size, cost, and decreased performance. Their switching speed is limited due to their vertical structure and cannot be used for MHz frequency applications limiting the use of modern digital electronics for space missions.

Thus, the Power Semiconductor Research Laboratory at the University of Central Florida in conjunction with Sandia National Laboratories is developing a rad-hard by design lateral-double-diffused MOSFET (LDMOS). The study provides a novel in-depth physical analysis of the mechanisms that cause the LDMOS to burnout during an SEE and provides guidelines for making the LDMOS rad-hard to SEB. Total dose radiation, another important radiation effect, can cause threshold voltage shifts but is beyond the scope of this study. The
devices presented have been fabricated with a known total dose radiation hard CMOS process.

Single-event burnout data from simulations and experiments are presented in the study to prove the viability of using the LDMOS to replace the VDMOS for space power systems. The LDMOS is capable of higher switching speeds due to a reduced drain-gate feedback capacitance (Miller Capacitor). Since the device is lateral it is compatible with complimentary-metal-oxide-semiconductor (CMOS) processes, lowering developing time and fabrication costs. High switching frequencies permit the use of high density point-of-load conversion and provide a fast dynamic response.
Dedicated to my wife, Rhian, and my daughter, Sarinah,

whom both have been a wonderful gift from God.
ACKNOWLEDGMENTS

I would like to give my utmost thanks to God for giving me the opportunity to learn more about the world He designed. Next, I give gratitude to Dr. Z. John Shen of the University of Central Florida, who has always found a way to spur my interest in research while pushing me to work hard for my goals. Dr. Shen’s advice has been a well-embraced asset through my research. Patrick Shea has also been a great contributor to my research; without his tedious task of designing the optimal 25V LDMOS, this research would not be possible. Thank you to Sandia National Laboratories for providing the funding for this research, fabrication, and testing support.

Lastly, I would like to acknowledge my wife, Rhian, who has spent so much time taking care of our daughter while I pursue my dreams as a researcher.
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CHAPTER ONE: INTRODUCTION

1.1 Motivation

Space-bourn power semiconductor devices and power conversion topologies currently lag around ten years behind state-of-the-art commercial products. Electronics and instruments available for use in space systems are thus limited to older technologies where the power requirements are less stringent. There is a desire to use current-off-the-shelf components for mission cost reduction; however this is difficult due to the legacy power systems for space applications used today. Power Metal Oxide Field Effect Transistors (MOSFETs) for spacecraft are typically vertical double diffused MOSFETs (VDMOS). For over three decades, the VDMOS has dominated the field of power electronics only being replaced by the Insulated Gate Bipolar Transistor (IGBT) for some terrestrial applications. Some of these devices need to be de-rated from their breakdown voltage to qualify for space applications, increasing their cost, size, and decreasing switching performance. Nevertheless, new low voltage topologies used for state-of-the-art digital electronics and instruments require point-of-load conversion. Modern digital electronics need a fast switching power system to handle their dynamic load. Point-of-load conversion allows a spacecrafts power system to operate much more efficiently, by dropping the first stage power converter and only converting power at the load.

Power semiconductor devices with faster switching speeds are needed that retain low on-state resistance (RDS-ON) at low voltage. The faster switching speed will reduce the parasitic passive component power lose and size, while providing a good dynamic
response to changes in load. Excellent dynamic response is needed for more advanced electronics and instruments. This combined effect can make space missions cheaper and lighter.

The Lateral Double Diffused MOSFET (LDMOS or LDMOSFET) has a low-gate charge enabling high switching frequencies for point-of-load conversion applications. In addition the LDMOS is compatible with Complementary Metal Oxide Semiconductor (CMOS) process allowing a high integration density and reduced power system weight. This thesis presents advanced Technical Computer Aided Design (TCAD) simulations and experiments with the most destructive radiation effect a power semiconductor device can go through Single-Event-Burnout (SEB), and propose using a retro-p-body and p-epitaxial LDMOS for radiation hardness against SEB. A large amount of literature is available on the susceptibility of the VDMOS to SEB[1][2][3]. However, there is no known modeling into how SEB affects lateral power MOSFETs. Predicative modeling with experimental verification is needed to determine the mechanism of SEB on lateral Power MOSFETs before they can be used readily in space applications. This and more is addressed in this study.

1.2 Radiation Environment

For microelectronics the radiation environments range from terrestrial, Earth orbit, to outside Earth orbit (space). The sun at any given time ejects highly charges particles as its natural cycle. The incoming flux of charged particles is made up of highly energized electrons and protons. Typically, the Earth protects us with its magnetic field also called the “magnetosphere” Figure 1. Few of the suns highly charged
particles get through the magnetosphere. Radiation of concern on Earth is mostly from human generated sources like fission reactors in nuclear power plants. Conversely, cosmic radiation does get through made up from sixth and seventh generation interactions of galactic-cosmic rays and highly charged particles from the sun with greatly reduced energy [4]. Once in Earth orbit a spacecraft is exposed to more and more of the sun’s charge particles. Another concern for space craft are the Van-Allen radiation belts where trapped particles exist around the Earth. Highly charged neutrons exist in very low earth orbit, protons and electrons become more prevalent at higher Earth orbits. Once outside the Earth’s protective magnetosphere any spacecraft would be exposed to the full array of charged particles from the sun in addition to galactic-cosmic rays.

Figure 1: Earths Magnetosphere deflected cosmic radiation; After Nikkei Science, Inc. of Japan, by K. Endo, Prof. Yohsuke Kamide
Even greater threat than the sun lies outside the Earth orbit where very high energy heavy ions of unknown origin (also known as Galactic-cosmic rays) can transverse electronics and power semiconductor devices and cause Single-Event-Effects (SEEs) which includes SEB, Single-Event-Latchup (SEL), Single-Event-Upset (SEU), and more. At the Nuclear Space and Radiation Conference of 1975 Binder at al. [5] reported that communication satellites were getting digital errors from suspected single-event upset. Before then heavy ion radiation was consider a non issue because of the low total dose contribution of a few hundred rads [6]. The maximum energies of radiation types are given in Table 1. However, the ever shrinking size of microelectronics has created a new surge of interest in SEEs.

<table>
<thead>
<tr>
<th>Particle Type</th>
<th>Maximum Energy</th>
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<tr>
<td>Trapped Electrons</td>
<td>10s of MeV</td>
</tr>
<tr>
<td>Trapped Protons &amp; Heavy Ions</td>
<td>100s of MeV</td>
</tr>
<tr>
<td>Solar Protons</td>
<td>GeV</td>
</tr>
<tr>
<td>Solar Heavy Ions</td>
<td>GeV</td>
</tr>
<tr>
<td>Galactic Cosmic Rays</td>
<td>TeV</td>
</tr>
</tbody>
</table>
1.3 Radiation Effects

1.3.1. Ionizing Radiation

During ionizing radiation highly charged particles (electrons, protons, gamma rays etc) pass through a material they ionize the material generating electron hole pairs (ehps). Ionizing radiation that accumulates over time is referred to as Total Dose Effects (TDE) or Total Ionizing Dose (TID). Electron hole pairs generated in bulk semiconductor material will quickly be removed through typical recombination, drift, and diffusion mechanisms. However, in SiO₂ (the common gate oxide used for power semiconductor devices) charges can become trapped in interface and bulk states and overtime cause threshold voltage shifts and increased leakage currents. Rad is a material specific unit which is the amount of ionizing radiation required to transfer 0.1μJ of energy per gram of material.

EHPs generated in the oxide are driven to the interface by the work-function of the SiO₂/Si interface. For n-type devices holes move toward the Si/SiO₂ interface and get trapped in fixed oxide traps and interface traps, whose concentrations are given in terms of \( N_{ot} / N_{it} \) respectively. Figure 2 shows a physical picture of the transport and trapping in SiO₂ due to TID.
Trapped charge at the interface induces an inversion layer during the off-state that is responsible for increasing leakage current and threshold voltage shifts. Even the oxide that passivates/isolates semiconductor devices is susceptible to creating leakage paths. A back channel can be form for devices that use Silicon-on-Insulator (SOI) technology. TID will always remain a concern for space electronics and limit their life as long as SiO$_2$ gate dielectric is used. Besides the long term concerns of TID a short-term concern is single event burnout from heavy ions which can happen at any time and cause catastrophic failure.

1.3.2. **Single Event Effects**

Any type of radiation that causes a large amount of ionization to take place over a short period of time can cause a single event effects (SEE) a “soft-error” altering a digital state or a “hard-error” causing permanent damage can occur. The two most
common incidents for SEEs to occur are from galactic-cosmic-rays or a prompt dose event. Galactic-cosmic rays are made up primarily of energetic heavy ions such as iron; their origins cannot be traced. Prompt dose is similar to total ionizing dose, but occurs over a very short time span 1-5ns producing a near uniform electron hole pair generation. Events such as a nuclear detention that generates an electromagnetic pulse can deliver a prompt dose.

1.4 Power Device SEE Failure Modes

1.4.1. Single Event Burnout

As a heavy ion transverses semiconductor material it deposits charge along the ions track. The deposited charge can trigger the parasitic bipolar transistor and lead to burnout. There are two methods that charge is generated by heavy ions: the ion itself and secondary particles from nuclear interactions [7]. Charge deposition is given quantitatively by the Linear Energy Transfer (LET) measured in units of MeVcm$^2$mg$^{-1}$. In other words the energy loss per unit path (MeV/cm) length is normalized by the density of the material (mg/cm$^2$). Normalizing the energy loss allows the LET value to become independent of material; this is extremely useful for comparing devices of different materials.

1.4.2. Single Event Gate Rupture

A galactic-cosmic ray that strikes near the gate region of a semiconductor device can cause the SiO$_2$ oxide to electrically overstress. Afterwards gate leakage current increases dramatically. The electric field that was supporting the reverse blocking voltage is
removed and is redistributed near the gate and drain. Much research is still needed in the area of SEGR to determine the real cause. This type of event is referred to as single-event gate rupture.
2 CHAPTER TWO: REVIEW OF CURRENT AND PAST ART

Space power systems use vertical-double-diffused MOSFETs (VDMOS). The VDMOS is prone to SEEs by virtue of its structure. In 1985 T. F. Wrobe, F. N. Coppage, and G. L. Hash from Sandia National Laboratories published the first paper on burnout of the power VDMOS transistors [2]. The authors reported finding a correlation between a photo-ionization from radiation which induced avalanche at the epitaxial drain junction and caused burnout. A dose of 1x10 rads(Si) or greater was required to initiate the burnout. They split the burnout response into three sections Figure 3, the initial photo response, followed by avalanche, and then second breakdown. Most researchers believe that the initial charge collection is what activates the parasitic bipolar transistor.

![Typical Burnout Response](image)

Figure 3: High dose rate response of epitaxial transistors after [2] © 1985 IEEE

Typically SEB is thought to occur from the drift and diffusion of the deposited electrons and holes in VDMOS transistors [8]. A VDMOS is inherently weak to heavy ion strikes due to its vertical structure. As the ion passes through the device it creates an ion shunt. This can be thought of as an electrical short between any two points along the
ion track. Since the VDMOS shares a common drain on the bottom the probability of shorting the drain directly to the source is relatively high.

![Diagram of VDMOS and Parasitic BJT during a heavy ion traversing the device]

**Figure 4:** VDMOS and Parasitic BJT during a heavy ion traversing the device

Any electric field or spacecharge that exists along the ion track is eradicated by the electrical short from the ion. To maintain a state of quasi-equilibrium the electric field will redistribute itself sometimes referred to as the funneling effect. In essence the MOSFET drain becomes shorted to the base. The parasitic BJT is activated and the emitter begins to inject electrons across the p-body base. Avalanche then occurs due to the high level injection from the emitter. Impact ionization generates current near areas of heavy donor/acceptor concentrations. If the BJT gain is large enough with a relatively high base resistance and avalanche outpaces recombination then thermal runaway will result.
The VDMOS can be made rad-hard to SEB. Many papers suggest how to improve the SEB radiation response of the VDMOS [9,10]. Through various techniques the parasitic BJT can be squelched to prevent burnout. However, due to the common drain on the bottom SEGR is a concern and limits the operating area of the VDMOS.
3 CHAPTER THREE: PROPOSED LDMOS SOLUTION

3.1 Lateral Double Diffused MOSFET

The LDMOS is desired for space power applications due to its low gate charge; and TID hard CMOS fabrication process. Low gate charge allows for a high switching frequency (MHz). Therefore, LDMOS technology can provide the power switch for modern switching topologies such as point-of-load conversion. More sophisticated digital instruments and current-off-the-shelf parts could then be used on spacecraft reducing cost. Another benefit is a smaller footprint due to a high integration density and small inductor and capacitor requirements; further reduce the size of the power system. CMOS compatibility is another benefit the LDMOS provides making it have cheap production cost, faster development times, and a well the option to use well established total dose hard fabrication methods and processes. A 2D cross-section an LDMOS is shown in Figure 5.

![LDMOS 2D cross-section](image)

Figure 5: LDMOS 2D cross-section
3.2 Proposed Rad-Hard 25V Lateral Power MOSFET

Radiation hard by design is an effective alternative to de-rating power semiconductor devices for space applications. The Power Semiconductor Research Laboratory at the University of Central Florida with collaboration from Sandia National Laboratories is researching this topic and is developing an optimized design for SEB hardness. The LDMOS is designed to have a breakdown voltage of 25V.

For space applications the LDMOS design was modified to make it radiation resistant to SEEs. Initial theory from this research suggested that by adding a p-epi with a heavy p-type substrate that was grounded. Initial charge collection from a heavy ion would be sucked down by the substrate eliminating the hole current passing through the p-body and not trigger the inherent parasitic BJT. Results showed that the p+ substrate does help, but is secondary to the gain of the bipolar transistor. The SEB results were very poor. A 2D cross-section of the initial design without a p+ source contact is shown in Figure 6.

Figure 6: 2D cross-section of proposed LDMOS w/o p+ source contact
Figure 7 shows LDMOS w p+ source contact which was a design variation from the initial design lot. This design did just as poorly as the LDMOS w/o p+ source contact in SEB.

3.3 SEE Hardness of the LDMOS Compared to the VDMOS

In terms of SEE when the LDMOS is compared to the VDMOS the LDMOS fairs much better. There is a common drain on for the VDMOS on the bottom of the semiconductor device. Therefore, it is very probable a heavy ion to short the source to the drain. However, in the LDMOS with a p+ grounded substrate the probability is much smaller; this can be easily observed when looking at Figure 8.
Figure 8: 2D cross-sections of LDMOS and VDMOS
4 CHAPTER FOUR: METHODOLOGY

4.1 Introduction

Technical Computer Aided Design (TCAD) is a simulation tool that can quickly generate predictive results based on the given test conditions and the semiconductor device under test (DUT). First, a semiconductor device structure is defined and then electrically simulated in a Finite Element Analysis (FEM). These predictive simulations provide a good starting point for producing actual lots of semiconductor devices and can help define where design splits are needed. This thesis will present TCAD simulation data and experimental data to define the failure mechanisms of later power MOSFETs and provide design guidelines for making the LDMOS less prone to SEB.

4.2 Technical Computer Aided Design

An RDS$_{ON}$ VS BV optimized LDMOS was designed by the Power Semiconductor Research Laboratory at the University of Central Florida. Sentaurus device editor is used to define the structure, doping profile, and mesh. Then Sentaurus device carriers out an electrical simulation of the DUT in a mixed mode environment where the TCAD model is placed in a spice circuit model and solved together. Heavy ion simulation code is given in APPENDIX A: HEAVY ION SIMULATION CODE.

The physical models used for the SEB simulation include coupled Possion’s, electron, and hole current continuity equations. Mobility is handled with the lucent mobility model which is a comprehensive model that covers low field, high field, and parallel field mobility. For recombination and generation the default avalanche model,
Shottky-Reed-Hall recombination, and auger recombination. For the simulations the drain voltage was incremented by 1V until SEB occurred. Then the voltage was reduced by 1V and the test repeated.

### 4.2.1. TCAD Models

The models for power semiconductor devices were used to model SEB with an area factor of 0.1µm to limit the photocurrent generated to an accurate level. Drift and diffusion are accounted for by coupled electron hole continuity equations and the Poisson’s equation. The default avalanche model is R. van Overstreten avalanche model. Mobility is doping dependent Masetti model [10,11]. Auger recombination is included due to the high level of carriers injected during SEB. Schottky-Reed-Hall (SRH) recombination is also used for low current and steady-state modeling.

The Lucent mobility model was found to match the experiment results well and is compared with the default models in the modeling chapter. It is a combination of Philips unified mobility model, enhanced Lombardi model for mobility degradation at interfaces, Hänsch model is a high field saturation mobility model. By using a combination of these three models an accurate simulation of dynamic mobility changes from low to high fields can be accounted for.

A sweep of models for generation and recombination, mobility, and hydrodynamic was conducted to analysis how they affect SEB. Changes to the mobility model shown in Table 2 have a large impact on SEB. Parasitic base resistance is inversely proportional to mobility and as will be shown in the modeling section effects SEB greatly. Just because a model passed does not mean it was correct. For example a SEB test that passed might have failed when a model was turned on. The models pertaining to
mobility had the most impact of SEB simulation results. Hydrodynamic model is based off energy relaxation times and takes into account localized carrier heat generation. It was found that the transients are so short that no carrier heating occurs and the hydrodynamic simulation did not have an impact on heavy ion modeling.
Table 2: SEB TCAD Model Impact

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<tr>
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<th>Generation and Recombiantion</th>
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<tbody>
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Effect to SEB
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<th>BandGap Narrowing (OldSlotboom)</th>
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<th>SRH(Doping Dependence)</th>
<th>Mobility</th>
<th>HydroDynamic</th>
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</tbody>
</table>

- **Mobility**: Enormal, Tunneling, PhuMob, HighField Velocity Saturation, hHighField Saturation
- **HydroDynamic**
4.3 SEB Experiment Procedure

The experimental guideline used is the US Military specification MIL-STD-750 “Test Method Standard Test Methods for Semiconductor Devices.” Method 1080 is the procedure for conducting heavy ion irradiation for SEB and Single-Event Gate Rupture (SEGR). Figure 9 shows the SEB/SEGR circuit schematic.

![SEB/SEGR Circuit Schematic](image.png)

Figure 9: SEB/SEGR Text Circuit Schematic [13]

Testing is conducted by the following procedure. The DUT is biased at a $V_{DS}$ below breakdown. The gate voltage is set so that the LMDOS is in the off-state. Then the DUT is subjected to heavy ion irradiation at fluence up to 100,000ions/cm$^2$ under vacuum. If SEB/SEGR does not occur then the drain voltage is increased and again exposed to the heavy ion irradiation. This process is repeated until the semiconductor device fails or the BV is reached.
Figure 10: Simplified MIL-STD-750 Method 1080 SEB/SGER flowchart
5  CHAPTER FIVE: SINGLE EVENT BURNOUT MODELING

5.1 SEB Modeling Results

Simulated TCAD LDMOS structure for SEB modeling is the design variation with a p+ contact is shown in Figure 11. The applied drain voltage is 10V for the failing case.

A heavy ion strike causes a complicated mix of reactions and changes in a semiconductor device. Figure 12 and Figure 13 shows the mixed-mode transient snaps shots of a heavy ion strike for the electron and hole currents. Expansion and absorption of the excess electron and holes generated along the ion track are clearly visible. Sustained BJT operation is also observed in the $10^{-9} - 10^{-8}$ (s) which leads to single event burnout.
Figure 12: Simulated evolution of electron current in a LDMOS w p+ source contact during a heavy ion strike.
Figure 13: Simulated evolution of electron current in a LDMOS w p+ source contact during a heavy ion strike.
Electric field and the potential distribution reveal a telling story about the internal mechanism of SEB in a LDMOS. As a heavy ion generates electrons and holes the potential must expand to compensate since no voltage can be supported along the column of excess electrons and holes. The potential lines get closer at the top and taper out in the epi as shown in Figure 14. This effect is often referred to as the funnel effect.

Where ever the potential lines are closest are the areas of the most intense electric field which are referred to as hot spots in Figure 15. Hot spots are the areas where the electric field is most intense and therefore generate the most impact ionization as seen in Figure 16: Simulated impact ionization evolution of a LDMOS w p+ source contact during SEB
The breakdown field of Si is $3 \times 10^5$ V/cm. Impact ionization generates more current that must exit out the drain for electrons and the source for holes.
Figure 14: Simulated potential distribution of a LDMOS w p+ source contact during SEB
Figure 15: Simulated electric field evolution of a LDMOS w p+ source contact during SEB
Figure 16: Simulated impact ionization evolution of a LDMOS with p+ source contact during SEB
Figure 17 contains the internal snapshots of the 25V LDMOS with the p+ source contact. Lowering the voltage from 10V to 9V allowed this design to pass the heavy ion test. The LDMOS without the p+ contact fails at 9V and is shown in Figure 18.
Figure 17: Simulated passing case internal evolutions of a LDMOS w p+ source contact during a heavy ion strike that survives with $V_{DS}=9V$
Figure 18: Simulated failing case of a LDMOS w/o p+ contact internal evolution during SEB
As the drain voltage is increased the electric field intensity goes up due to more potential line crowding. It can be concluded that impact ionization gets larger for increasing drain voltage bias as shown in Figure 19.
Figure 19: Simulated SEB induced avalanche snapshots for 5, 15, and 25V
5.2 Novel SEB Failure Mechanism Developed for a Power LDMOS

There has no research into the failure mechanism of SEB in a power LDMOS. The study here will present a novel approach to the mechanism of SEB in an LDMOS for the first time. Failure due to SEB is a hard problem to study due to the picoseconds time scale on which the events take place.

LDMOS SEB failure mechanism can be defined when the heavy ion generated electron and hole plasma short out the electric field in the LDD region. Simultaneously the electric field has to redistribute itself and initially crowds near the gate on the drain side as shown in Figure 15; before bouncing back to the n+ drain/LDD junction. Hole current generated by the avalanche at this point exits out the source. Consequently, the avalanche generated hole current triggers the parasitic bipolar junction transistor. Once, the parasitic BJT is triggered the source (which is acting as the BJT emitter) injects a high level of electrons. Injected electron current exits VIA the drain and amplifies the impact ionization already taking place near the drain (Kirk Effect). Figure 20 contains a diagram of this discovered physical mechanism. Explosions represent impact ionization in the figure. Impact ionization at the substrate also enhances the drain impact ionization, but not to the level that the source injected electrons do.
In conjunction with the failure mechanism discovered a circuit schematic of the failure is developed shown in Figure 21. $R_{\text{ION}}$ goes from infinity to zero this forward biases the parasitic BJT. Once the BJT is forward biased $I_{\text{AVAL}}$ current source starts to feed current into the parasitic BJT base. $R_{\text{ION}}$ returns to infinity to represent the excess electron hole column being completely absorbed. $I_{\text{AVAL}}$ will keep the BJT forward biased as long as the voltage drop is around 0.6-0.7V. Greater than 0.6V and SEB will occur less and the LDMOS will survive.
5.3 LDMOS Design SEB Impact

Sentaurus Device Editor is used to generate the LDMOS model then heavy ion experiments were run in the electrical device simulator Dessis to obtain the sensitivity of LDMOS structure parameters. The parameters that are varied to determine the radiation tolerance to SEB are \( L_n \), \( t_{epi} \), \( N_{PB} \), \( N_{LDD} \), and \( N_{epi} \). Where \( L_n \) is the drift length of the drain extension, \( t_{epi} \) is the epitaxial layer thickness, \( N_{LDD} \) is the concentration in the drain extension, \( N_{PB} \) is the p-body carrier concentration, and \( N_{epi} \) is the epitaxial carrier concentration as shown in Figure 22.
Figure 22: LDMOS 2D cross-section

Table 3: LDMOS Structure Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_n$</td>
<td>Drain extension length</td>
</tr>
<tr>
<td>$N_{pb}$</td>
<td>p-body doping concentration</td>
</tr>
<tr>
<td>$t_{epi}$</td>
<td>Epitaxial thickness</td>
</tr>
<tr>
<td>$N_{epi}$</td>
<td>Epitaxial doping concentration</td>
</tr>
</tbody>
</table>

The SEB baseline test was a mixed mode electrical simulation with a heavy ion of 80 LET, with the substrate grounded. A normal ion strike with respect to the substrate is used and the strike location is the middle of the drain region (LDD). Too close to the gate risks SEGR and too close to the drain would short the drain to the grounded p-plus substrate.
5.4 LDMOS Design SEB Simulation Results

Design 2 is used for the heavy ion simulations. The drift length (Ln) is proportional to the breakdown voltage of the LDMOS. As Ln increases it spreads the electric field, thus increasing breakdown voltage. Intuition would suggest that as Ln increases it would harden the LDMOS to SEB; given the same drain voltage during the SEE. However, Simulation data in Figure 23 suggest there is not a strong trend that agrees with this theory. The Lucent model has a much smaller variation in failing \( V_{SEB} \) (the voltage where SEB occurred).

![Figure 23: Simulated SEB for increasing values of Ln](image)

Figure 23: Simulated SEB for increasing values of Ln
The N_{pb} doping is the p-body acceptor concentration. Using the default model revealed a trend where the higher the concentration the higher the V_{SEB} occurred. However, the over trend for the N_{PB} is relatively flat. One would assume that a higher p-body would reduce SEB because it would lower the base resistance. Increasing the N_{PB} also raises the threshold voltage.

Figure 24: Simulated SEB for increasing values of N_{pb}

Figure 25: Simulated SEB for increasing values of t_{e pi}
Figure 26: Simulated SEB for increasing values of $N_{epi}$

5.5 Secondary Effects

To determine if the p+ substrate has an impact on single event burnout heavy ion simulations were run with several resistances on the substrate contact. The results of the simulations are shown in Table 4.

Table 4: SEB Simulated LDMSO w p+ source contact varying substrate resistance @ Vds = 25V

<table>
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<tr>
<th>$R_{sub} \Omega$</th>
<th>Pass/Fail</th>
</tr>
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<tr>
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<td>Pass</td>
</tr>
<tr>
<td>13</td>
<td>Fail</td>
</tr>
<tr>
<td>18</td>
<td>Fail</td>
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<tr>
<td>23</td>
<td>Fail</td>
</tr>
<tr>
<td>75</td>
<td>Fail</td>
</tr>
<tr>
<td>9375</td>
<td>Fail</td>
</tr>
</tbody>
</table>

As the substrate resistance increases less hole current is directed towards the p+ substrate. If the resistance is high enough the substrate is more or less floating and
accepts no hole current. In terms of SEB the floating substrate did the worst while the substrate with the lowest resistance passed SEB simulations.

5.6 Summary of SEB in a LDMOS

Changing the structural parameters of the LDMOS does not significantly alter the radiation hardness to SEB. As the ion passes through the LDMOS and creates an ion shunt between the p-epi and drain the inherent bipolar base/collector junction becomes forward biased. Electrons begin to get injected from the n+ source/emitter and exit VIA the drain. The injected electrons aggravate avalanche already taking place at the drain by the redistribution of the electric field from the ion shunt. If the parasitic BJT gain and base resistance are high enough the regenerative avalanche (Kirk Effect) will continue and lead to thermal runaway; with the subsequent burnout of the power semiconductor device (SEB).
6 CHAPTER SIX: EXPERIMENTAL RESULTS

Heavy ion experiments were conducted at the Texas A&M Universities cyclotron facility by Sandia National Laboratories. LDMOS device variations with and without the p+ contact were tested. Table 5 contains the heavy ion results. If the power supply current increased SEB or SEGR was assumed to have occurred. Further, IV testing after that determined whether the failure is SEB or SEGR. An increase in gate leakage is a sign that SEGR has taken place. Results in the table just pertain to SEB events. Physical damage is noticeable when SEB occurs as shown in Figure 27. Both designed failed (SEB) at 7.5V experimentally.

The Lucent Model fits the experimental results the closest. This difference can be a result of the mobility for the models and contact resistance. Using the Default Models for heavy ion testing is not advised due to the very optimistic results and the larger variation in the drain voltage where SEB took place between designs.

Table 5: Single Event Burnout Experimental Results

<table>
<thead>
<tr>
<th>Design/LET</th>
<th>Experimental $V_{SEB}$</th>
<th>Default Model $V_{SEB}$</th>
<th>Lucent Model $V_{SEB}$</th>
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<tbody>
<tr>
<td>w p+ source contact/LET = 80</td>
<td>7.5</td>
<td>16</td>
<td>9</td>
</tr>
<tr>
<td>w/o p+ source contact/LET = 86</td>
<td>7.5</td>
<td>21</td>
<td>10</td>
</tr>
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</table>
Figure 27: Experimental LDMOS SEB die pictures with visible physical damage
An improved LDMOS design is proposed after testing our initial two designs and extensive results from TCAD simulations showed that suppression of the parasitic BJT is of paramount importance. The improved LDMOS developed utilizes a highly doped retro p-body implant shown in Figure 28. This design is found to have a far superior SEB hardness. The retro p-body reduces the base resistance of the parasitic BJT; requiring more current to forward bias the BJT. With the p-body grounded by a p-plus contact any electrical field disturbance could be reduced around the p-body while allowing holes a low resistance path.

Figure 28: Retro p-body radiation hardened 25V LDMOS 2D cross-section

Figure 29 contains an x-slice 1D cross-section of the doping concentration at the gate edge on the source side from all three designs discussed in the study. Two effects
can be extracted for the figure. One, the base resistance on the retro p-body design in the lowest due to the 1E18 boron/cm$^3$ and two the effective base width is increased lower the parasitic BJT gain. This addition results in a LDMOS less prone to SEB.

![Doping concentration at x-slice near gate edge source side](image)

**Figure 29:** Doping concentration at x-slice near the source side gate edge

### 7.1 Simulation Results of Improved Rad-Hard LDMOS

TCAD simulations of the retro p-body LDMOS increased to 24V at burnout. That is a 220% improvement over the initially proposed LDMOS. Simulated time evolutions of a heavy ion strike at 24V of the retro p-body LDMOS are shown in Figure 30. There in a increase in recombination due to the heavily doped retro p-body. Impact ionization is also shifted somewhat from the gate edge to the retro p-body front edge. Overall the
parasitic BJT is reduced to a very poor BJT hindering the regenerative avalanche mechanism that produces failure in lateral power MOSFETs.
Figure 30: Simulated retro p-body 25V LDMOS heavy ion strike (passed)
8 CHAPTER EIGHT: SUMMARY AND FUTURE WORK

8.1 Summary

A rad-hard LDMOS is developed at the University of Central Florida Power Semiconductor Research Laboratory in collaboration with Sandia National Laboratories. The VDMOS is prone to SEEs by virtue of its structure and common drain. A rad-hard LDMOS was proposed so a more modern power system could be used in space. The rad-hard LDMOS will allow modern digital electronics to be utilized for space missions. No research to date has been presented on the design and failure mechanism of a radiation hardened lateral power MOSFET. To design a rad-hard LDMOS a novel single event burnout failure model was developed by analysis of extensive heavy ion TCAD simulations and experiments. From the TCAD modeling it was determined that suppression of the BJT is of utmost importance. Thus, an improved rad-hard LDMOS is proposed utilizing a retro p-body implant, the retro p-body addition greatly increases the current needed to sustain that parasitic BJT. TCAD simulations predict a 220% improvement over the initially proposed rad-hard LDMOS.

8.2 Future Work

Future fabrication and heavy ion testing is already on schedule for the retro p-body LDMOS design for 2009. TCAD modeling of the total dose effects and single event gate rupture are also areas that need future study for the rad-hard lateral power MOSFET.
9 APPENDIX A: HEAVY ION SIMULATION CODE

Device LDMOS {
    Electrode{
        { Name="Gate"   Material = "PolySi"(N)    Voltage=0.0  }
        { Name="Drain"      Voltage=0.0  }
        { Name="Substrate"     Voltage=0.0  Resistance=@RSub@ }
        { Name="Source"  Voltage=0.0  }
    }
}

File{
    * Input Files
    Grid      = "@tdr@
    Plot      = "@tdrdat@
    Current   = "@plot@
}

Physics{
    AreaFactor=0.1
    * DriftDiffusion
    EffectiveIntrinsicDensity(
        BandGapNarrowing (OldSlotboom)
    )
    Mobility(
        *Using Lucent Mobility Model
        PhuMob EnormalDependence HighFieldSaturation(CaugheyThomas)
    )
    Recombination(
        SRH( DopingDep )
        Avalanche
        Auger
    )
    HeavyIon ( 
        Direction=(@Xvector@,@Yvector@)
        Location=(@Xion@,0)
        Time=1.0e-13
        Length=10
        Wt_hi=0.1
        LET_f=@LET@
        Exponential
        PicoCoulomb )
}
}
File {
    Output = "@log@"
}

Plot{
    *--Density and Currents, etc
    eDensity hDensity
    TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
    eMobility hMobility
    eVelocity hVelocity
    eQuasiFermi hQuasiFermi

    *--Temperature
    eTemperature Temperature * hTemperature

    *--Fields and charges
    ElectricField/Vector Potential SpaceCharge

    *--Doping Profiles
    Doping DonorConcentration AcceptorConcentration

    *--Generation/Recombination
    SRH Band2Band * Auger
    AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

    *--Driving forces
    eGradQuasiFermi/Vector hGradQuasiFermi/Vector
    eEparallel hEparallel eENormal hENormal

    *--Band structure/Composition
    BandGap
    BandGapNarrowing
    Affinity
    ConductionBand ValenceBand
    eQuantumPotential

    *--Heavy Ion
    HeavyIonChargeDensity
    HeavyIonCharge
}

System {
    Vsource_pset vds (3 0) {dc=0}
    Vsource_pset vgs (2 0) {dc=0}
}
Resistor_pset R1 (2 1) {resistance = 280}
Resistor_pset R2 (1 G) {resistance = 280}
Capacitor_pset C1 (1 0) {capacitance = 820p}
Capacitor_pset C2 (3 0) {capacitance = 0.25u}

LDMOS M1 ("Gate"=G "Drain"=3 "Source"=0 "Substrate"=0 )
 Plot "n@node@_Heavy_Ion" ( time ()
 v(1)
 v(2)
 v(3)
 i(M1,3)
 v(M1,3)
)
}
Math {
 Number_of_Assembly_Threads = 2
 Number_of_Solver_Threads = 2
 method=blocked
directcurrentcomp
Extrapolate
RelErrControl
ErRef(electron)=1.e13
ErRef(hole)=1.e13
Digits=4
Notdamped=50
Iterations=20
NoCheckTransientError
NewDiscretization
Derivatives
transient=BE
directcurrentcomp
RecBoxIntegration
}

Solve {
 *- Build-up of initial solution:
 Coupled{ Poisson Electron Hole Contact Circuit}

 Quasistationary(
  Goal{ Parameter=vds.dc Voltage=0 Vds2 } )
 ){ Coupled{ Poisson Electron Hole Contact Circuit} }

 NewCurrentFile="n@node@_Transient_
 Transient(
  InitialTime=0

53
FinalTime=1.5e-6
InitialStep=1e-16
Increment=2
MaxStep=5e-7
MinStep=1e-16
}

{ Coupled { Poisson Electron Hole Contact Circuit}
  Plot( FilePrefix = "n@node@_Xion@_Xion@_Ln@_Ln@_Vds@_Vds2@"
     Time=(5e-14; 1.0e-13; 1e-12; 1e-11; 5e-11; 1e-10; 1e-9; 5e-9; 1e-8; 1e-7; 1e-6; 1.5e-6)
     NoOverwrite)
}
}
10 REFERENCES


