Class-e Cascode Power Amplifier Analysis And Design For Long Term Reliability

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CLASS-E CASCODE POWER AMPLIFIER ANALYSIS AND DESIGN FOR LONG TERM RELIABILITY

by

KARAN KUTTY
B.S. University of Central Florida, 2008

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in the School of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

Summer Term 2010
ABSTRACT

This study investigated the Class-E power amplifier operating at 5.2 GHz. Since the operation of this amplifier applies a lot of stress on the switching transistor, a cascode topology was applied in order to reduce the drain-source voltage stress. Such an amplifier was designed and optimized in order to improve stability, power added efficiency, and matching. A layout for the said design was then created to be fabrication-ready using the TSMC 0.18 um technology.

Post-layout simulations were performed in order to realize a more realistic circuit performance with the layout design in mind. Long-term stress effects, such as oxide breakdown, on the key transistors were modeled and simulated in order to achieve an understanding of how leakage currents affect the overall circuit performance. Simulated results were compared and contrasted against theoretical understanding using derived equations.

Recommendations for future advancements were made for modification and optimization of the circuit by the application of other stress reduction strategies, variation in the class-E topology, and improvement of the driver stage.
To my parents
ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Jiann S. Yuan, for his continuous commitment to help and support me through my graduate career. His advice, technical and otherwise, has been valuable to my experience as a graduate student and a person. I would also like to thank my committee members, Dr. Kalpathy Sundaram and Dr. Xun Gong, for their support throughout my years at UCF.

My heartfelt gratitude goes out to all of my colleagues at the lab – Yidong Liu, Jun Ma, Smitha Krishnamurthy, Jason Steighner, Divya Narasimha Raju, Shuyu Chen, Yiheng Wang, Gigi Skaria, and Gabriel Vazquez.

Finally, I thank my parents for all that they have done and sacrificed to make this possible.
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<th>Description</th>
</tr>
</thead>
<tbody>
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<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DE</td>
<td>Drain Efficiency</td>
</tr>
<tr>
<td>DRC</td>
<td>Design Rule Checking</td>
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<td>KCL</td>
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<tr>
<td>NMOS</td>
<td>n-Channel Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
</tr>
<tr>
<td>PEX</td>
<td>Parasitic Extraction</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>TSMC</td>
<td>Taiwan Semiconductor Manufacturing Company</td>
</tr>
<tr>
<td>VCCS</td>
<td>Voltage-Controlled Current-Source</td>
</tr>
</tbody>
</table>
CHAPTER ONE: INTRODUCTION

The importance of fast and reliable communication has increased manifolds in the last decade. Starting all the way from cell phones that could only make phone calls, to now the hugely successful smart phones that have revolutionized the way in which consumers prefer to communicate. The growing demand for connectedness has driven the industry to continually expand its efforts to improve communication devices in terms of efficiency, range, and cost. The improvements have been made on both ends of the communication line: the base stations, and the communication devices.

An Introduction to RF Communications

At the end-user level, where cell phones and other communication devices are used, there has been significant improvement in the computing power, and as a result there has also been an increase in the quality of software. In addition, these devices have been provided even more bandwidth which has caused service providers to improve their services to meet additional demands. The base stations are what the communication service providers setup with large cell phone towers in order to receive and transmit wireless signals. A zoomed out view of the transmission-reception cycle is shown in Figure 1.1. This figure loosely represents either an end-user communication device, or the base station controlled by the service provider.

To understand this system, let us first take a look at the reception side of the system. The signal is received by an antenna, which could be a patch antenna in the case of a cell phone, or a parabolic, sector antenna, etc. in the case of a base station. Since this signal has travelled a large distance over which there is significant attenuation and noise added, it must first be conditioned. In order to do this, the signal is sent to a Low-Noise Amplifier (LNA). The LNA provides gain
by adding very little noise to the original signal and filters out any noise. The amplified signal is now sent to a mixer in order to shift it to a lower frequency. This is necessary as RF signals could be in the GHz range, much higher than the speed at which computers could process data. The signal is now converted to a digital signal using an analog-to-digital converter (ADC). The final digital signal is used by the on-board processor for any processing needs.

![Diagram of a transceiver circuit](image)

Figure 1.1: General overview of a transceiver circuit

On the transmission side, the bits of data coming from the processor are converted to an analog signal using a digital-to-analog converter (DAC), which is then shifted to a higher frequency using a mixer. The reason for shifting the signal is because the communication frequency is much higher than the frequency at which the digital information is output. The resulting signal is now amplified using a power amplifier, and transmitted using an antenna.
Power amplifiers are used just before the antenna since the power of the signal needs to be amplified manifold in order for it to travel a large distance and offset the attenuation.

**Motivation**

It is a continuous struggle for the service providers to provide a greater reception range so that the number of stations required can be reduced in order to cut operating costs. This range can be increased if the power of the output signal is increased, as it can now be received a larger distance away from the cell phone tower while still meeting the power and noise requirements. In order to do this, the supply voltage can be increased. However, for a Class-E amplifier, as it will be explained later in detail, this causes a large stress on the dielectric of the switching transistor. This stress can eventually cause the breakdown of the dielectric.

**Goals and Outline**

The ultimate goal of this research is to study the oxide breakdown effect in the cascoded Class-E power amplifier, model it, and finally compare it to the PA designed using ADS and Cadence simulation and layout tools.

In Chapter Two, the different power amplifier classes are explained in brief detail in order to provide the reader with some insight and comparison. This comparison is used to explain why the Class-E was picked, along with some of its advantages and disadvantages compared to the other classes. The remainder of that chapter will explain an ideal Class-E PA. Chapter Three will introduce the cascoded Class-E PA, the topology used for simulation and layout as part of this thesis, along with the reason why the cascoded topology is used. Chapter Four explains the model derivation of the cascoded Class-E PA using the analytical
understanding backed by fundamental equations describing circuit behavior. Chapter Five discusses the results by comparing and contrasting the waveforms obtained from the model and the simulations. Finally, in Chapter Six, the work is concluded and future work on this topic is proposed.
CHAPTER TWO: IDEAL CLASS-E POWER AMPLIFIER

When it comes to practical application, there are several different types of amplifiers that can be applied. Depending on the application and its requirements, different amplifier classes can be applied to achieve the design goals. Table 2.1 provides a comparison of the well known amplifier classes. From a first look at this table, it should be noted that the two most prominent ways of operating the switching transistor in all amplifiers is either as a current source, or as a switch. Additionally, the relationship between the conduction angle and the ideal maximum drain efficiency (DE) should be noted. Since the Class-A amplifier is on during the entire conduction cycle, the transistor is constantly dissipating power, hence the maximum drain efficiency is capped at 50%. As the duration for which the transistor is on during the conduction cycle reduces, the power dissipated during one cycle is reduced, and as a result the drain efficiency is increased. This change in the DE is reflected as the amplifier is progressively changed from class-A to class-C, where class-C can ideally attain a maximum efficiency of 100% when its conduction angle is very small. This principle of conduction angle controlling the efficiency of the amplifier governs class-A to C amplifiers.

Table 2.1: Power amplifier class comparison

<table>
<thead>
<tr>
<th>Class</th>
<th>Conduction Angle (%)</th>
<th>Ideal Max. Drain Efficiency (%)</th>
<th>Operation Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>100%</td>
<td>50%</td>
<td>Current Source</td>
</tr>
<tr>
<td>AB</td>
<td>50% – 100%</td>
<td>50 – 78.5%</td>
<td>Current Source</td>
</tr>
<tr>
<td>B</td>
<td>50%</td>
<td>78.50%</td>
<td>Current Source</td>
</tr>
<tr>
<td>C</td>
<td>&lt; 50%</td>
<td>100%</td>
<td>Current Source</td>
</tr>
<tr>
<td>D</td>
<td>50%</td>
<td>100%</td>
<td>Switch</td>
</tr>
<tr>
<td>E</td>
<td>50%</td>
<td>100%</td>
<td>Switch</td>
</tr>
<tr>
<td>F</td>
<td>50%</td>
<td>100%</td>
<td>Switch</td>
</tr>
</tbody>
</table>
Classes D through F make use of the transistors in their respective topologies as a switch, and are all ideally capable of attaining 100% DE. These class amplifiers are better performers in terms of efficiency, however, perform worse in terms of linearity. Even though the class-C amplifier is ideally able to obtain comparable DE, and is more linear, it does provide less output power compared to class-E amplifiers. Similarly, when considering classes D and F in comparison with class-E, additional filters are required for removing undesired harmonics and tuning different harmonics respectively. These additional filters require a lot more space than a class-E amplifier would since it does not have such stringent requirements.

On the down side, class-E amplifiers suffer from a high drain voltage due to the operating characteristics of the circuit (explained in more detail later in this chapter). While in comparison to classes D and F, the class-E occupies less area, it also is a downfall to its performance. As it will be explained later, the output inductor is shared by the filter and the impedance matching, causing the circuit to either attain maximum efficiency, or maximum matching based on that inductance value.

**Class-E Characteristic Equations**

As previously explained, the class-E operates its transistor as a switch, instead of a current source, which allows it to bypass the conduction angle and performance tug-of-war. Not only that, but this criterion is achieved without the added complexity of class-F amplifiers, or the inherent harmonic issues with the class-D amplifiers. The only downfall is that a class-E amplifier is most certainly a non-linear one, as it will not be able to reproduce every detail in the input waveform in the output.
A simple circuit configuration for a class-E can be seen in Figure 2. It should be noted that this circuit is unmatched for the characteristic impedance. In fact, $R_{\text{Load}}$, $L_S$, $C_S$, and $C_P$ are all derived through design equations. $L_D$, on the other hand is assumed to be large enough to allow only DC current through to the rest of the circuit. This allows for the further simplification of the design equations. Let it also be noted that the transistor is treated as an ideal switch in the derivations.

![Figure 2.1: Class-E power amplifier circuit](image)

Upon initial inspection of the circuit, it is realized that when the switch is on (or closed), the entire current pass through $S_1$ to ground, and $V_P$ is now zero. In the next case where $S_1$ is off (or open), there is no current flowing through the transistor and $V_P$ is some non-zero finite value; in this case the entire current flows into the capacitor $C_P$. This sequence where the switch conducts with zero voltage across it, and then stops conducting with a finite voltage across it allows for zero-voltage-switching operation. This is the fundamental reason why a class-E
amplifier is able to ideally achieve 100% drain efficiency. The current which flows into $S_1$ or $C_P$ at any given point in a cycle can be described by the following equations, the base of which was obtained from [1, 2], after which the pertinent results were obtained.

\[ i_{Total} = i_{DD} + i_{RF} \sin \theta \]  

(2.1)

\[ S_1 = \begin{cases} 
    i_{Total}, & \text{when } S_1 \text{ is on (closed)} \\
    0, & \text{when } S_1 \text{ is off (open)} 
\end{cases} \]  

(2.2)

\[ C_P = \begin{cases} 
    0, & \text{when } S_1 \text{ is on (closed)} \\
    i_{Total}, & \text{when } S_1 \text{ is off (open)} 
\end{cases} \]  

(2.3)

Given these equations, it can then be surmised that the voltage $V_P$ is now equal to the following.

\[ V_P = \begin{cases} 
    0, & \text{when } S_1 \text{ is on (closed)} \\
    \frac{1}{\omega C_P} \int_{\alpha}^{\theta} i_{Total} \, d\theta, & \text{when } S_1 \text{ is off (open)} 
\end{cases} \]  

(2.4)

When the switch is off, $V_P$ can be described as the voltage across the capacitor using the current flowing into $C_P$. The variables $\alpha$ and $\theta$ are the conduction angles at which the switching transistor turns off and on, respectively. The angle $\theta$ ranges from $\alpha$ to $\beta$, since that is the time period over which the voltage is non-zero. The graphs of the two currents and voltage can be found in Figure 2.2.

The principle of zero-voltage-switching can also be confirmed in these graphs as the product of $V_P$ and $I_{SW}$ is always equal to zero. In comparison to real-world applications, where power loss is unavoidable, the cause of this power loss is due to the overlapping of the voltage and current waveforms. This is often caused by parasitic capacitances caused by a variety of reasons, and these causes will be discussed in the chapters to come.
The next step is to find the output voltage; however, frequency analysis needs to be performed in order to obtain the voltage that is in and out of phase with the output current. The reason that both components are required is because the in-phase voltage is used to find the load resistance for a design current criterion, and a corresponding reactance is calculated to filter out the quadrature (out of phase) voltage.

\[ V_p = \frac{1}{\omega C_p} \int_{\alpha}^{\theta} i_{Total} \, d\theta, \quad \text{when } \alpha < \theta < \beta \]  

\[ V_p = \frac{1}{\omega C_p} [i_{DD}(\theta - \alpha) - (\cos \theta - \cos \alpha)], \quad \text{when } \alpha < \theta < \beta \]  

Figure 2.2: The waveforms for the current flowing through the switch, capacitor \((V_p)\), and the voltage \((V_p)\) during one conduction cycle.
Similarly, the quadrature component of the output voltage is $90^\circ$ out of phase from the in-phase voltage; therefore, the out-of-phase voltage can be derived as follows.

\[ V_{\text{quadrature}} = \int_{\alpha}^{\beta} V_p \cos \theta \, d\theta \]  

\[ \Rightarrow V_{\text{quadrature}} = \frac{1}{\omega C_p} \int_{\alpha}^{\theta} \left[ i_{DD}(\theta - \alpha) \right] \sin \theta \, d\theta \, d\theta \]

\[ \Rightarrow V_{\text{quadrature}} = \frac{i_{RF}}{2\pi \omega C_p} \sin \theta \left[ \frac{(\beta - \alpha) \cos \alpha}{2} + \sin \alpha - \sin \beta \right] \]  

(2.9)

The output power and drain efficiency (DE) can now be solved for easily using the following power and DE definitions.

\[ P_{\text{OUT}} = 10 \log_{10} \left( \frac{V_{\text{in-phase}} i_{RF}}{2} \right) \, dBm \]  

(2.13)

\[ DE = \frac{P_{\text{OUT}}}{P_{\text{DC}}} = \frac{V_{\text{in-phase}} i_{RF}}{2} \]  

(2.14)

Using the peak output current that was called $I_{RF}$ previously we can now calculate the output load and the additional reactance needed because of the quadrature component of the
output voltage. Additionally, the design frequency tuning can be done by changing the values of $L_S$ and $C_S$.

$$R_{Load} = \frac{V_{in-phase}}{I_{RF}}$$

(2.15)

$$\Delta X_S = \frac{V_{quadrature}}{I_{RF}}$$

(2.16)

$$\omega = \frac{1}{\sqrt{L_S C_S}}$$

(2.17)

These equations describe some of the more prominent aspects of the ideal class-E amplifier; however, more advanced effects can also be derived using the mean voltage and current through the capacitor $C_p$.

$$V_{mean} = \frac{1}{2\pi} \int_{\alpha}^{\beta} V_p d\theta$$

(2.18)

$$\Rightarrow V_{mean} = \frac{i_{RF}}{2\pi \omega C_p} \left[ \sin \alpha - \sin \beta + \frac{(\beta - \alpha)(\cos \alpha + \cos \beta)}{2} \right]$$

(2.19)

$$I_{C \ mean} = \frac{1}{2\pi} \int_{\alpha}^{\beta} I_c d\theta$$

(2.20)

$$\Rightarrow I_{C \ mean} = \frac{1}{2\pi} \left[ i_{DD}(\alpha + 2\pi - \beta) - i_{RF}(\cos \alpha - \cos \beta) \right]$$

(2.21)

The equations for the mean current and voltage, along with the previous equation sets, are a good starting point for all of those relationships as described in [1].

Design Issues for Class-E PA

The proof for the ideal class-E has been very straight-forward and pointed in proving that this class of amplifiers is indeed capable of attaining an ideal drain efficiency of 100%.
However, like every real engineering scenario, there is no free lunch. This class has its own pitfalls. As it can be seen in (2.6), $V_p$ is greatly dependent on $i_{RF}$. Even though in the previous derivations $i_{RF}$ was considered to be a design constant, for the sake of simplicity, this value is ultimately dependent on $V_{DD}$. It should be noted that increasing $V_{DD}$ corresponds to an increase in $i_{RF}$, and this in-turn increases $V_p$. This increase in $V_p$, in an ideal class-E amplifier is stipulated to follow the following equation.

While an increase in $i_{RF}$ can be seen as a good thing since the output power ($P_{OUT}$) is increased, it can also have various other consequences which can do more harm than good to the circuit. The following sub-sections will delve into these possibilities in detail.

_Hot Carrier Injection (HCI)_

There are three requirements for HCI to occur at a significant rate in order cause harm to a transistor. The first is that there should be a high voltage from drain to source, which causes a high electric field near the drain region. The second requirement is for there to be a significant amount of current passing through the transistor when there is a high electric field present.

The high electric field causes the carriers to travel at high speeds, which translates to a higher momentum in a physical sense. The high momentum allows the electrons to break the bonds in the oxide layer, causing trapped charges. This process occurs over the period of time and continues to create more trapped charges until a tunnel of trapped charges has been formed through the oxide layer, shorting the gate and drain. Around this point is when current begins to flow through the gate oxide. The problem mentioned here is not limited to just that however. The problem continues to deteriorate as the current also causes power dissipation through the
oxide, by heat, which breaks more bonds causing additional trapped charges. This negative feedback loop eventually destroys the device after throwing it into hard breakdown.

Since the class-E operates through the ZVS principle, the high voltage at the drain of the device does not occur when there is significant current passing through the transistor. Even in non-ideal cases when there is a voltage and current waveform overlap, the peak voltage (which causes the maximum E-field) occurs when the current is minimal, as will be shown later in simulation results. Therefore, the concern for damage by HCI can be neglected.

**Gate-Drain Oxide Breakdown**

A serious threat to the reliability and long-term performance of the circuit is the fact a high voltage across the drain and gate can eventually cause gate-drain oxide breakdown. The process requires a high electric field across the gate oxide, which occurs in this case. The high electric field causes weaker bonds to be broken introducing trapped charges in the gate oxide over a wide area. Up until this point, the occurrence of scattered trapped charges the transistor operation is not disrupted severely, but only mildly where the threshold voltage is mildly shifted.

Over time, these trapped charges tend to concentrate at more vulnerable areas and continue to stack one on top of another, as shown in Figure 2.3. Once these trapped charges form a connection from the drain to the gate, a conduction path is formed. From this point onwards, a negative feedback is created due to heat dissipated by the current that flows. The current breaks more bonds creating additional trapped charges and throwing the device into a freefall. At this point the transistor operation is severely affected and eventually will be destroyed.
This sort of high-stress operation is expected in a regular class-E amplifier due to the high drain voltage and oscillating gate voltage. Since the drain voltage can ideally reach a peak of $3.6V_{DD}$, the only remedy to such a situation would be if the gate voltage can be increased to reduce the voltage difference between the gate and drain. The cascode class-E amplifier would be such a solution and is examined in the next chapter.

References


CHAPTER THREE: CLASS-E CASCODE POWER AMPLIFIER

As explained previously, the high voltage differential across the drain and gate can cause gate oxide breakdown in the simple class-E PA. Such an effect can be drastically hurtful to the long-term performance of the circuit as the transistor will be destroyed during normal usage cycles. One method of improving circuit reliability is by reducing the voltage at the drain of the transistor. Since the relationship between \( V_P \) and \( V_{DD} \) is entirely linear, \( V_{DD} \) can be reduced. However, this results in a reduction of \( P_{OUT} \). Instead, of suffering a loss of \( P_{OUT} \), a cascode architecture can be applied, whose workings are explained in the next section.

Why Cascode?

The cascode structure allows the top transistor to have its gate oxide stress reduced by providing it a constant gate biasing. As seen in Figure 3.1, with \( V_G \) as a constant, \( 3.6V_P - V_G < V_{IN} \). Additionally, this method reduces the drain-source voltage both transistors. On the other hand, with a single transistor, the swing from \( V_{IN} \) will cause tremendous stress on the gate oxide.

![Figure 3.1: Comparison of standard versus cascode topology for stress reduction across the gate oxide](image)

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Ideal Cascode Class-E PA

The ideal cascode class-E PA operation is very similar to the non-cascode version. $S_1$ and $S_2$ are considered to be ideal switches and $C_p$ is considered to be the parasitic capacitances from $S_1$ lumped up into a general capacitor for the sake of simplicity. The remainder of the circuit is the exact same as from the non-cascode class-E PA, as seen in Figure 3.2.

![Ideal cascode class-E PA circuit](image)

Figure 3.2: Ideal cascode class-E PA circuit

The analysis of an ideal cascode class-E is very similar, and in-fact, the equations describing the operation of this circuit are identical to the non-cascode class-E. The only real differences are that the angles $\alpha$ and $\beta$ are slightly different due to the introduction of $S_2$. So it
can be said that the total current flowing into the transistor branch is always equal to the following.

\[ i_{Total} = i_{DD} + i_{RF} \sin \theta \] (3.1)

Additionally, going through the same steps as done previously, the output voltage in-phase with the output current can be surmised to be as follows.

\[ V_P = \frac{1}{\omega C_P} \int_{\alpha}^{\theta} i_{Total} \, d\theta, \quad \text{when } \alpha < \theta < \beta \] (3.2)

\[ V_P = \frac{1}{\omega C_P} [i_{DD}(\theta - \alpha) - (\cos \theta - \cos \alpha)], \quad \text{when } \alpha < \theta < \beta \] (3.3)

\[ V_{in-phase} = \int_{\alpha}^{\beta} V_P \sin \theta \, d\theta \] (3.4)

\[ \Rightarrow V_{in-phase} = \frac{1}{\omega C_P} \int_{\alpha}^{\theta} \left\{ i_{DD}(\theta - \alpha) \right\} \sin \theta \, d\theta \, d\theta \] (3.5)

\[ \Rightarrow V_{in-phase} = \frac{i_{RF}}{2\pi \omega C_P} \sin \theta \left[ (\beta - \alpha) \cos \alpha \frac{\alpha}{2} + \sin \alpha - \sin \beta \right] \] (3.6)

This equation can now be used to find the load resistance for an output current design criteria. Even though the sets of equations are similar to the non-cascode circuit, the angles \( \alpha \) and \( \beta \) will be different because of slightly modified circuit operation.

The operation of this circuit can be described based on simulated results. Originally, when the switch \( S_1 \) is off, the current \( i_{Total} \) flows through \( S_2 \), and into \( C_P \). As \( C_P \) charges, the voltage across the capacitor increases, and there resulting power dissipated by the switch \( S_1 \) is zero because of no current flow through that switch. Eventually this rising voltage reduces the gate-source voltage for the switch \( S_2 \) below the threshold and the transistor turns off. Although
this transistor may be off, there is still sub-threshold conduction which continues the charging of the capacitor $C_p$. Due to the high voltage across the top transistor, there is power loss introduced here due to the sub-threshold conduction. Later, transistor $S_2$ switches operation and $C_p$ discharges into the load through $S_2$, as explained in [1]. Immediately afterwards, $S_1$ turns on and the remainder of $C_p$ discharges through $S_1$ introducing some power loss. The voltage across both transistors drop as the current flow increases and power dissipated during this period is quite low in comparison.

**Real Cascode Class-E PA Design and Analysis**

The complete circuit for the cascode class-E PA was designed in ADS. The circuit used is illustrated in Figure 3.3. The various parts of the circuit are highlighted accordingly, starting from the input matching for the amplifier, the driver stage, the class-E PA, and finally the output matching. This PA was designed for operation at 5.2 GHz.

![Figure 3.3: Real cascode class-E circuit used for simulation and layout](image)
**Input Matching**

The circuit has been designed with a characteristic impedance \((Z_0)\) of 50\(\Omega\). This implies that the impedance seen from the input and output is equal to 50\(\Omega\). In order to do so a series capacitance, shunt capacitance, and series inductance was used to tune the impedance. The measurement of the input impedance in the simulation phase was done using the smith chart plot of the S11.

**Driver Stage**

Originally, when the circuit was designed, the performance characteristics of the amplifier such as the PAE and DE were really low. The cause of this issue was debugged back to the driver stage, and it was found that the DC power dissipation through the transistor from the driver stage was operating in the class-A region. As mentioned in the previous chapters, class A provides the greatest linearity, however, the worst efficiency as the transistor is on for the entire conduction cycle. The low performance can be seen in Figure 3.4, which illustrates the low PAE and DE for a class-A driver.

In order to solve this issue, the operation class of the driver needed to be changed to a class-B or C amplifier. This can easily be done by reducing the gate biasing for the driver, however, the stability of the circuit was directly linked to the class operation of the driver stage. For a high gate biasing, the entire circuit remained unconditionally stable, however, for a bias lower than 1\(V\) the circuit was conditionally stable. The stability graphs for the different classes of operation can be seen in Figure 3.5.
Figure 3.4: Performance summary of the entire circuit, including the output power, PAE, and DE, with a class-A driver
In order to de-couple this relationship between the stability factor of the PA and the operation type of the driver stage, a feedback resistor was added, as shown in Figure 3.3. The feedback resistor was able to de-couple this relationship, which allowed the gate bias for the driver stage to be reduced significantly, which in-turn allowed the DC power dissipation in the driver stage to drop. All this led to a higher operating efficiency of the entire circuit.

Class-E PA and Output Matching

The cascode class-E circuit is similar to the one shown in the previous section. The only new portion remaining is the output matching circuit. As it can be observed in Figure 3.3, there is an overlap region between the class-E PA and the output matching circuit. This overlap region shares an inductor which is used by the class-E PA (as seen in the previous diagrams), and also the output matching circuit. This is considered both, good and bad, for two main reasons. Sharing an inductor in design reduces the layout area used by the circuit. The reduction in layout area translates as reduced manufacturing costs. However, one drawback of this shared inductor
is that the matching for maximum $P_{OUT}$ and filter matching do not occur at the same inductance value. Due to this fact, there has to be a trade-off during the design phase, between picking better output matching and better performance.

Class-E PA Layout and Post-Layout

The simulations and post-layout simulations were performed in ADS, using the 0.18$\mu$m 6-Metal TSMC technology library, and Cadence was used in order to create the layout for the entire circuit; these can be found in Figure 3.6, Figure 3.7, and Figure 3.8.

Figure 3.6: ADS schematic for the cascode class-E PA
Figure 3.7: Circuit for the class-E PA in Cadence for the LVS procedure
The final layout size was measured to be 820 by 887 \( \mu m \). For the creation of this layout, a few changes were made to the circuit seen in Figure 3.3. Firstly, for the gate biasing for each transistor, a large resistance value was used between the voltage source and the gate. Later, the
gate biasing for the top transistor of the class-E PA was made to share its biasing voltage with the supply voltage for the driver. The reason for this was a shortage of connection pads. There were four available connection pads, and five DC voltages, since the gate voltage for the top transistor was very close to the supply voltage for the driver, the two were made to share that bias.

Finally, after circuit layout was complete, a post-layout metal-6 skeleton was prepared in order to analyze the parasitic resistive, inductive, and capacitive effects of the metal lines. The layout view and the circuit view can be seen in Figure 3.9 and Figure 3.10, respectively. Both of those figures have highlighted lines in red and blue which correspond with each other. These were the two metal-6 lines used for post-layout simulation. Initially the two lines were separated into two files, where each one was simulated using ADS Momentum in order to calculate their parasitic properties. After these simulations were completed, the dataset result files were used in the ADS simulation in place of the ideal wire connections. Once this was completed, the simulation was run in order to calculate the post-layout simulation results. These results and more are presented in CHAPTER FIVE: RESULTS.
Figure 3.9: Metal-6 skeleton created from the layout to be used for PEX, with highlighted interconnects representing lines used for parasitic extraction
Figure 3.10: Class-E PA circuit with the highlighted lines representing those used for post-layout simulation

References

CHAPTER FOUR: GATE OXIDE BREAKDOWN MODEL

Even though the cascode structure for the class-E PA is a solution for reducing the gate-drain electrical stress on the switching transistor, it isn’t a solution that entirely rids the circuit of the gate oxide breakdown problem. Designers can always increase the supply voltage $V_{DD}$ in order to achieve higher $P_{OUT}$. The realization from the earlier chapters is still valid, where an increase in $V_{DD}$ will result in a direct increase in $V_P$. If the gate voltage was increased along with $V_P$, then the oxide stress is shifted from the drain-gate region to the source-gate region as the source of the top transistor will swing all the way to ground. The transient waveforms indicating the drain-gate voltage across the top (red) and bottom (blue) transistors are shown in Figure 4.1.

![Figure 4.1](image-url)

Figure 4.1: The drain-gate voltage measured in simulation for the top (red) and bottom (blue) transistors
To further prove that the gate oxide breakdown effect is still highly relevant to this circuit, let it be noted that a $V_G > 10\, MV/cm$ (in the case of $SiO_2$) will definitely cause oxide breakdown over a certain period of time. The circuit designed for this work uses is measured to have a $V_{DG} = 4.2V$ at a supply voltage of $V_{DD} = 2.4V$. This implies that the stress on the oxide just barely meets the oxide breakdown criterion as follows.

$$\frac{V_{DG}}{tox} = 10.3\, MV/cm$$  \hspace{1cm} (4.1)

$tox$ is the thickness of the oxide layer, and is measured to be 4.1\,nm [1]. Therefore, for any $V_{DD} \geq 2.4V$, gate oxide breakdown is imminent. The rapid rise in the peak drain voltage for the top transistor can also be seen in Figure 4.2, with linearly increasing $V_{DD}$ values.

![Figure 4.2: Graph of $V_p$ during transient simulation with $V_{DD}$ sweeps](image)

Figure 4.2: Graph of $V_p$ during transient simulation with $V_{DD}$ sweeps
It is for this reason that the gate oxide breakdown needs to be modeled in order to accurately predict the circuit performance including the degradation factor introduced by the oxide breakdown.

**Gate Oxide Breakdown Model Derivation**

There are two major ways of applying the gate oxide breakdown in the circuit, one with a varying resistance between the drain and gate nodes of a transistor representing the resistance seen by either side, or one with a voltage-controlled current-source (VCCS). The main difference between the two is that the gate-drain resistance based model is a specific case of the VCCS model. This relation can be displayed by the following equations.

\[ V_{GD} = (V_G - V_D) \]  \hspace{1cm} (4.2)

\[ R_{GD} \text{ Model: } i_{\text{leakage}} = \frac{V_{GD}}{R_{GD}} \]  \hspace{1cm} (4.3)

\[ \text{VCCS Model: } i_{\text{leakage}} = g_0 + g_1 V_{GD} + g_2 V_{GD}^2 + g_3 V_{GD}^3 + \cdots \]  \hspace{1cm} (4.4)

It can be noted from equations (4.3) and (4.4), that the \( R_{GD} \) model is just the second term from the VCCS model. For this work, the \( R_{GD} \) model has been chosen due to its simplicity. As it will be explained in CHAPTER SIX: CONCLUSION, this work will later use the VCCS model for a generalized approach to such a problem.

**Gate-Drain Resistance Model Derivation**

As mentioned previously, the gate-drain resistance model will employ a resistance \( R_{GD} \), which will represent the severity of breakdown with a resistance value. This resistance is connected directly between the drain and gate of the transistor in simulations, which is intended
to create a short after the resistance value has been lowered significantly. This resistance and respective currents for the circuit are shown in Figure 4.3.

The analytical equation derivation process is again very similar to the one previously mentioned. However, in this derivation, two variations were included. For the first set of derivations, the current from the supply voltage, \( i_{DD} \), was assumed to be constant with a large enough inductor \( L_D \). This was done to arrive at a simple equation explaining the relationship of \( R_{GD} \) to the output power. A second, more realistic case, was then derived using a fluctuating current \( i_{DD} \) with a finite \( L_D \).

![Diagram of generalized cascode class-E PA circuit including the gate-drain leakage resistance](image)

Figure 4.3: Generalized cascode class-E PA circuit including the gate-drain leakage resistance

**Constant Supply Current Model Derivation**

We start out this derivation with KCL at the drain node. With the sum of the currents flowing in and out of a node set equal to zero, we can find the total current flowing into the capacitor \( C_P \) when the bottom transistor is turned off.
\[ i_{GD} + i_{DD} + i_{RF} \sin \theta + i(\theta) = 0 \quad (4.5) \]
\[ \Rightarrow \frac{V_G - V_D}{R_{GD}} + i_{DD} + i_{RF} \sin \theta + C_P \frac{dv_c}{dt} = 0 \quad (4.6) \]

The sum of these currents can then be used to derive the voltage across the capacitor as follows.

\[ V_p = v_c, \text{ when the top transistor is on} \quad (4.7) \]
\[ \Rightarrow - \frac{V_p}{R_{GD}} + \frac{V_G}{R_{GD}} + C_P \frac{dV_p}{dt} - i_{DD} + i_{RF} \sin \theta = 0 \quad (4.8) \]
\[ \Rightarrow \frac{dV_p}{dt} - \frac{1}{R_{GD}C_P} V_p = \left( i_{DD} + i_{RF} \sin \theta - \frac{V_G}{R_{GD}} \right) \quad (4.9) \]
\[ \Rightarrow V_p = \left( i_{DD} + i_{RF} \sin \theta - \frac{V_G}{R_{GD}} \right) \frac{1}{C_P} + \rho e^{-\theta} \quad (4.10) \]

Using this derived form for the drain voltage, the in-phase component of the output voltage can now be derived using frequency analysis.

\[ V_{in-phase} = \frac{1}{\pi} \int_{\alpha}^{\beta} V_p \sin \theta \, d\theta \quad (4.11) \]
\[ \Rightarrow V_{in-phase} = \frac{1}{\omega C_P \pi} \int_{\alpha}^{\beta} \left( i_{DD} - \frac{V_G}{R_{GD}} \right) \sin \theta \, d\theta \quad (4.12) \]
\[ + \frac{1}{\omega C_P \pi} \int_{\alpha}^{\beta} \sin^2 \theta \, d\theta + \frac{\rho}{\pi} \int_{\alpha}^{\beta} e^{-\theta} \sin \theta \, d\theta \]
\[ \Rightarrow V_{in-phase} = \frac{1}{\omega C_P \pi} \left( i_{DD} - \frac{V_G}{R_{GD}} \right) (\cos \alpha - \cos \beta) \]
\[ + \frac{1}{\omega C_P 2 \pi} (-\alpha + \sin \alpha \cos \alpha + \beta - \sin \beta \cos \beta) \quad (4.13) \]
\[ + \frac{\rho}{\pi} \left[ e^{-\theta} (n \sin \alpha + \cos \alpha) - e^{-\theta} (n \sin \beta + \cos \beta) \right] \frac{n^2 + 1}{n^2 + 1} \]
The derived in-phase output voltage can then be used to find the output power as done in the previous chapters.

\[
P_{\text{OUT}}(W) = \frac{V_{\text{in-phase}} i_{RF}}{\sqrt{2}} = \frac{V_{\text{in-phase}} i_{RF}}{2}\quad (4.14)
\]

This relation can be used to derive the change in power with a change in gate-drain resistance by substituting in the result for \(V_{\text{in-phase}}\) into the equation for output power.

\[
\Delta P_{\text{OUT}} = \frac{V_{\text{in-phase}}' i_{RF}}{2} - \frac{V_{\text{in-phase}} i_{RF}}{2}
\]

\[
= \frac{i_{RF}}{2} (V_{\text{in-phase}} - V_{\text{in-phase}}')\quad (4.15)
\]

\[
\Rightarrow \Delta P_{\text{OUT}} = \frac{i_{RF}}{2} \frac{V_{G}}{\omega C_p \pi} (\cos \alpha - \cos \beta) \left( \frac{1}{R_{GD}} - \frac{1}{R_{GD}'} \right)\quad (4.16)
\]

Thus, the change in output power can be seen as a function of changing \(R_{GD}\), and easily proven to correspond with the simulation data, as will be shown in the next chapter.

**Varying Supply Current Model Derivation**

In this subsection, the non-ideal case of a varying supply current is included for a more detailed analysis of the output power. The initial equation stating the KCL remain the same, however, the changes quickly become apparent as the supply current is varied as the equations quickly become much more complex.

\[
i(\theta) = i_{GD} + i_{DD} + i_{RF} \sin \theta \quad (4.18)
\]

In this case, the divergence in derivations begins with \(i_{DD}\) being defined as a voltage drop across the inductive impedance.
Our KCL equation can now be said to change as follows.

\[
i(\theta) = \frac{V_G - V_D}{R_{GD}} + \frac{V_{DD} - V_P}{\omega L_D} + i_{RF} \sin \theta
\]  

(4.20)

The voltage \( V_P \) can now be derived by integrating the current flow into the capacitor, as done in the previous derivations.

\[
V_P = \frac{1}{\omega C_P} \int_{\alpha}^{\beta} i(\theta) d\theta \quad \text{where } \alpha < \theta < \beta
\]

(4.21)

\[
= \frac{1}{\omega C_P} \int_{\alpha}^{\theta} \left( \frac{V_G - V_P}{R_{GD}} + \frac{V_{DD} - V_P}{\omega L_D} + i_{RF} \sin \theta \right) d\theta
\]

(4.22)

\[
= \frac{1}{\omega C_P} \left[ \left\{ \frac{V_G}{R_{GD}} + \frac{V_{DD}}{\omega L_D} \right\} (\theta - \alpha) - i_{RF}(\cos \theta - \cos \alpha) \right]
\]

(4.23)

\[
\Rightarrow V_P = \frac{1}{\omega C_P} \left[ \left\{ \frac{V_G}{R_{GD}} + \frac{V_{DD}}{\omega L_D} \right\} (\theta - \alpha) - i_{RF}(\cos \theta - \cos \alpha) \right]
\]

\[
1 + \left( \frac{1}{R_{GD}} + \frac{1}{\omega L_D} \right) \left( \frac{\theta - \alpha}{\omega C_P} \right)
\]

(4.24)

\[
\Rightarrow V_P = \frac{\left( \frac{V_G}{R_{GD}} + \frac{V_{DD}}{\omega L_D} \right) (\theta - \alpha) - i_{RF}(\cos \theta - \cos \alpha)}{\omega C_P + \left( \frac{1}{R_{GD}} + \frac{1}{\omega L_D} \right) (\theta - \alpha)}
\]

(4.25)

\[
V_P = \frac{(\omega L_D V_G + R_{GD} V_{DD})(\theta - \alpha) - i_{RF}(\cos \theta - \cos \alpha)\omega R_{GD} L_D}{\omega^2 R_{GD} L_D C_P + (R_{GD} + \omega L_D)(\theta - \alpha)}
\]

(4.26)

For the sake of simplicity in the latter stages of the derivation, the constant groups of terms have been grouped up into other variables. This allows for a simplified view of the final equations.

\[
\Rightarrow V_P = \frac{f(\theta - \alpha) - i_{RF}(\cos \theta - \cos \alpha)g}{h + k(\theta - \alpha)}
\]

(4.27)
Using this final representation of $V_p$, the output voltage that is in-phase with the output current can now be derived using frequency analysis.

\[
V_{\text{in-phase}} = \frac{1}{\pi} \int_{\alpha}^{\beta} V_p \sin \theta \, d\theta
\]

\[
= \frac{1}{\pi} \int_{\alpha}^{\beta} f(\theta - \alpha) - i_{RF}(\cos \theta - \cos \alpha)g \frac{h + k(\theta - \alpha)}{h + k}\sin \theta \, d\theta
\]

\[
\Rightarrow V_{\text{in-phase}} = \left[- \frac{f}{\pi k^2} \left\{ h \sin \left( \alpha - \frac{h}{k} \right) \text{Ci} \left( -\alpha + \theta + \frac{h}{k} \right) \right. \\
- h \cos \left( \alpha - \frac{h}{k} \right) \text{Si} \left( \alpha - \theta - \frac{h}{k} \right) + k \cos \theta \right\} \\
- \frac{i_{RF} g}{2\pi k} \left\{ \sin \left( 2\alpha - 2 \frac{h}{k} \right) \text{Ci} \left( -\alpha + \theta + \frac{h}{k} \right) \right. \\
+ \cos \left( 2\alpha - 2 \frac{h}{k} \right) \text{Si} \left( -\alpha + \theta + \frac{h}{k} \right) \right\} \\
+ \frac{i_{RF} g \cos \alpha}{\pi k} \left\{ \sin \left( \alpha - \frac{h}{k} \right) \text{Ci} \left( -\alpha + \theta + \frac{h}{k} \right) \right. \\
+ \cos \left( \alpha - \frac{h}{k} \right) \text{Si} \left( -\alpha + \theta + \frac{h}{k} \right) \right\} \beta
\]

Since the integral stated in (4.29) is impossible to solve completely analytically since its solution contains various complex integrals that remain eventually unsolvable, and [2] was used to aid in solving the entire equation analytically. The results that were adopted include $\text{Si}(\theta)$ and $\text{Ci}(\theta)$ functions which are defined as follows.

\[
\text{Si}(\theta) = \int_{x}^{\infty} \frac{\sin x}{x} \, dx
\]

\[
\text{Ci}(\theta) = \int_{x}^{\infty} \frac{\cos x}{x} \, dx
\]
These functions are later calculated numerically to evaluate the output voltage. It should also be noted that (4.30) is being evaluated from $\beta$ to $\alpha$. Since it was time consuming to derive the final analytical function, it is simply done so in numerical computations. The output power can be calculated using the same general equation as used previously.

**Temperature Variance Model for Circuit Performance**

An additional modification was made to the output power equation in order to account for temperature variance by supplying it with the SPICE equations used for modeling temperature effects. The equations used for the resistance, inductance, and capacitance are as follows.

$$R(T) = R_{TNOM}(1 + TC1_R \Delta T + TC2_R \Delta T^2) \quad (4.33)$$

$$L(T) = L_{TNOM}(1 + TC1_L \Delta T + TC2_L \Delta T^2) \quad (4.34)$$

$$C(T) = C_{TNOM}(1 + TC1_C \Delta T + TC2_C \Delta T^2) \quad (4.35)$$

These equations use certain empirical constants which are defined in the technology library SPICE files. With these temperature variance equations, the output power equation can be further modified by replacing the constant component values with temperature varying component values. The simplification variables $f$, $g$, $h$, and $k$ are now described as follows.

$$f = \omega V_G L_{TNOM}(1 + TC1_L \Delta T + TC2_L \Delta T^2)$$

$$+ V_{DD} R_{TNOM}(1 + TC1_R \Delta T + TC2_R \Delta T^2) \quad (4.36)$$

$$g = \omega R_{TNOM}(1 + TC1_R \Delta T + TC2_R \Delta T^2) L_{TNOM}(1 + TC1_L \Delta T$$

$$+ TC2_L \Delta T^2) \quad (4.37)$$

$$h = \omega^2 R_{TNOM}(1 + TC1_R \Delta T + TC2_R \Delta T^2) L_{TNOM}(1 + TC1_L \Delta T$$

$$+ TC2_L \Delta T^2) C_{TNOM}(1 + TC1_C \Delta T + TC2_C \Delta T^2) \quad (4.38)$$
\[ k = R_{TNOM} (1 + TC_{1R} \Delta T + TC_{2R} \Delta T^2) \]
\[ + \omega L_{TNOM} (1 + TC_{1L} \Delta T + TC_{2L} \Delta T^2) \]  

(4.39)

The variables \( f, g, h, \) and \( k \) are computed beforehand and later plugged into the entire equation for evaluation purposes.

References


CHAPTER FIVE: RESULTS

For the purpose of simulations, the ADS software suite was used in order to run circuit simulations for both, pre and post-layout. The simulations use the TSMC 6-Metal 0.18\( \mu \text{m} \) technology library. For resistances, the p+ poly without silicide resistors were used for higher resistance values. Inductors used are planar structures which sit on the top-most metal layer, and all of them have an inner radius of 30\( \mu \text{m} \), while the width of the inductor metal is 6\( \mu \text{m} \). All capacitors used were of the MIM type and classified as 2p0_wos. In order to adjust the capacitance value, the length and width of the capacitor dimensions were modified, both in simulations and in layout, and every capacitor used has square dimensions.

Class-E PA Pre-Layout Simulation Results

Firstly, to prove that the circuit is operating as a class-E amplifier, the transient waveforms for the top and bottom transistors are shown in Figure 5.1 and Figure 5.2. Next, the drain-source voltages across the two transistors are compared in Figure 5.3 and it should be noted that the \( V_{DS} \) for the two transistors are not equal as expected. This occurs because the top transistor turns off due to the rising voltage at the source due to the parasitic capacitance \( C_P \) seen in the previous chapter.

The input and output impedance matching for the entire circuit can be seen in Figure 5.4. As mentioned in the previous chapters, there is a trade-off between the impedance matching and the proper tuning of the circuit. This tuning tug-of-war can either increase the output power, or increase the matching performance of the circuit. Finally, the output power, PAE, and DE can be seen in Figure 5.5.
Figure 5.1: Transient waveforms, drain-source voltage (red) and drain current (blue), for the bottom transistor for the pre-layout simulation.

Figure 5.2: Transient waveforms, drain-source voltage (red) and drain current (blue), for the top transistor for the pre-layout simulation.
Figure 5.3: Comparison of the transient drain-source voltage across the top (red) and bottom (blue) transistors for the pre-layout simulation
Figure 5.4: Input (top) and output (bottom) matching for pre-layout simulations
Figure 5.5: Output power (top), PAE (middle), and DE (bottom) for the pre-layout simulation

Class-E Post-Layout Simulation Results

The post-layout simulations include the two highlighted strips shown in Figure 3.9 and Figure 3.10. These metal interconnects were later provided to ADS Momentum in order to
calculate its S-Parameters, and saved in a dataset file. The dataset files later replaced the ideal wires in ADS in order to achieve the post-layout simulation results. These interconnects were chosen because there is a significant amount of current passing through these relatively thinner interconnects. The parasitic resistance, inductance, and capacitances can significantly alter the circuit performance is shown in the following figures.

First and foremost, the class-E operation is still valid as the voltage and current graphs display in Figure 5.6 and Figure 5.7. A comparison of the drain-source voltages for both transistors can be seen after post-layout simulations in Figure 5.8. The input and output matching can be seen in Figure 5.9, where it should be noted that the output is better matched in the post-layout simulation. The reason for this is because during initial design, the output was left to be slightly capacitive, not only because better PAE and DE were achieved because of this, but also because it was predicted that inductance of the layout line would compensate the matching as seen on the Smith Chart. Unfortunately, the inductive compensation was underestimated which created a much better matching than had been originally expected. Finally, the output power, PAE, and DE can be seen in Figure 5.10.
Figure 5.6: Transient waveforms, drain-source voltage (red) and drain current (blue), for the bottom transistor for the post-layout simulation

Figure 5.7: Transient waveforms, drain-source voltage (red) and drain current (blue), for the top transistor for the post-layout simulation
Figure 5.8: Comparison of the transient drain-source voltage across the top (red) and bottom (blue) transistors for the post-layout simulation.
Figure 5.9: Input (top) and output (bottom) matching for post-layout simulation
Figure 5.10: Output power (top), PAE (middle), and DE (bottom) for the post-layout simulation
Oxide Breakdown Model Results Comparison

The oxide breakdown model that was derived in CHAPTER FOUR: GATE OXIDE BREAKDOWN MODEL, is numerically solved using Python. The entire calculation is broken up into several portions in order to increase speed and accuracy. The Python platform was chosen as it is often used for scientific computation purposes due to the ease in prototyping and accuracy in floating point calculations with several open-source numerical libraries. The comparison of the output power in $dBm$ from the simulation and analytical equation is shown in Figure 5.11.

![Figure 5.11: Output power variance with respect to the drain-gate resistance as seen in the simulation result from ADS (blue) and the analytical equations (red)](image)
Temperature Variance Results Comparison

Similar to the oxide breakdown model, the analytical equation for the temperature variation case was also numerically solved using Python. The comparison of the output power can be seen in Figure 5.12.

Figure 5.12: Output power variance with respect to the temperature as seen in the simulation result from ADS (red) and the analytical equations (blue)
CHAPTER SIX: CONCLUSION

This work has studied, and designed the cascode class-E power amplifier structure. Some key reliability issues were identified with the circuit, such as the gate oxide breakdown under high drain-gate stress. A layout for this circuit was later created and post-layout simulations were performed in order to verify design and layout. The effect of this stress was then reflected on the circuit performance using simulation results from ADS. Analytical equations describing the output power including a gate oxide breakdown model were derived and numerically solved. The results matched those from the simulation and the effect was verified. Additionally, the temperature dependence of the resistance, inductance, and capacitance values were taken into account with the analytical equations derived, and compared with the simulated results.
CHAPTER SEVEN: FUTURE WORK

The analytical equations derived in this work take into account a gate-drain resistance as seen from either side. This is a specific case of the VCCS option previously discussed in this document. It is planned to re-derive the output power equation as a function of the VCCS, which provides a much more realistic and general case equation. Secondly, since there is significant power loss due to sub-threshold conduction, it would make the model more accurate if a finite resistance was used in place of an ideal switch. As discussed earlier in this document, the driver stage contributes significantly to the overall efficiency of the circuit, so it would be more realistic to include the driver operation into the overall derivation somehow. Finally, a true check of all these simulated and analytically derived equations would be a real fabricated chip containing the designed circuit.