LDMOS Power Transistor Design and Evaluation using 2D and 3D Device Simulation

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LDMOS POWER TRANSISTOR DESIGN AND EVALUATION USING 2D AND 3D DEVICE SIMULATION

by

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B.S. University of Central Florida, 2016

A thesis submitted in partial fulfilment of the requirements for the degree of Master of Science in the Department of Electrical Engineering and Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

Spring Term
2017

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The benefit of the super-junction (SJ) technique and the use of a floating P layer for low voltage (30 V) laterally double-diffused metal oxide semiconductor (LDMOS) transistors are investigated in this thesis using Sentaurus TCAD simulation software. Optimizations to the SJ LDMOS were attempted such as adding a buffer layer to the device, but simulation and theoretical evidence point out that the benefits of the SJ technique are marginal at the 30 V application. A replacement for the SJ technique was sought, the floating P structure proved to be a good solution at the low voltage range due to its simpler cost effective process and performance gains achieved with optimization. A new idea of combining the floating P layer with shallow trench isolation is simulated yielding a low figure of merit (on state resistance × gate charge) of 5.93 mΩ-nC.
In the name of Allah, the most Beneficent, the most Merciful
ACKNOWLEDGMENTS

I would like to acknowledge my advisor Dr. Yuan for his assistance and guidance all throughout my graduate and undergraduate career. I would also like to acknowledge Dr. Kapoor and Dr. Sundaram the graduate coordinator for participating in my graduate committee as well I would like thank Dr. Sundaram for his constant guidance through the years.

I would also like to thank Dr. Patrick Shea and Jonathan Garcia at Renesas Electronic Corporation for their technical input and their support for the NSF I/UCRC on Multi-Functional Integrated System Technology (MIST) which was responsible for the partial funding of the research project.

I want thank all of my lab mates: Qutaiba, Jie Lin, Andrew, Shayan, Mahed, and Elliot. As well I would like to thank my classmate and friend Khalil for his support.

Lastly I would like to thank my parents, family, and friends for all of the moral support.
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CHAPTER ONE: INTRODUCTION

With the ever growing demand for smaller and more powerful electronics and computer hardware, and the increase of the number of users and the number of computer devices per person, there has been a push to keep these portable electronic device powered on for longer and more extended periods of time. One of the key aspects that have an effect on keeping these devices powered for longer periods of time is the improvement of the efficiency of the power electronic overhead circuitry. These circuits can be found in the power supplies of these devices, power adapters, and in within mother boards for regulation of power at different stages of computing systems.

In the past power regulation relied heavily on linear power supplies which had very poor power efficiency. They were quite bulky in size and generated much heat. This power limitation held the industry back for quite some time, this continued until the advent of switching power supplies [1]. These switching power supplies served as a very viable solution to the technology cap of these linear power supplies, this due to the fact that they can ideally attain a maximum power conversion efficiency of 100%. This increased efficiency helped cut down on both the size and the cost of these power regulation circuits and enabled the industry to produce more attractive products with higher performance with higher power densities.
Linear Power Regulators

These linear power regulators struggle with their power efficiency ($\eta$), this is mainly due to the fact that it relies heavily on a voltage divider network to achieve its voltage regulation, and an example can be seen in Figure 1.

From Figure 1 it is possible to deduce the voltage gain of the circuit as:

$$M = \frac{V_{out}}{V_{in}} = \frac{R2}{R1 + R2} \quad (1)$$

The voltage divider network achieves its voltage regulation by dissipating input power that is beyond the output power through the resistor $R1$. This energy is then converter to heat which is unwanted and is a waste of the bias supplied to the circuit. This issue is also coupled
with the fact that there is no means of load or line regulation with a simple voltage divider network.

A solution to the lack of load and line regulation of the linear voltage regulator shown in Figure 1 is solved with the low-dropout regulator (LDO) circuit. A simplified LDO regulator circuit can be seen in Figure 2 where a control circuit can be used to regulate the output voltage based on a reference voltage ($V_{ref}$) that is within the control circuit. This helps keep the output voltage at the desired level despite changes in the load and the input bias that is being supplied to the LDO regulator. The LDO employs a PMOS transistor as a variable resistor as it operates in the linear region and its gate is connected to the output of the error amplifier in the control circuit, i.e. the output of the control circuit modulates the PMOS channel width to achieve a varying resistance that will help in regulating the output voltage.

![Figure 2: LDO regulator](image)
As a note despite their low power efficiency LDO regulators are still widely used as a solution for small voltage drops within electrical systems. The reason for this is that regardless of the poor efficiency when the voltage difference between input voltage and the output voltage is small then the power dissipated by the resistors becomes small and tolerable this can be seen in equations 2-3 where:

\[
V_{\text{out}} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{\text{ref}} \tag{2}
\]

\[
P_{\text{loss}} = (V_{\text{in}} - V_{\text{out}}) \cdot I_{\text{out}} + V_{\text{in}} \cdot I_{\text{operating}} \tag{3}
\]

- \(V_{\text{out}}\) = is the regulated output voltage of the LDO regulator
- \(V_{\text{in}}\) = is the input voltage supply to the regulator
- \(P_{\text{loss}}\) = are the power losses that are incurred by the regulator
- \(V_{\text{ref}}\) = is the reference voltage used by the control scheme
- \(I_{\text{out}}\) = is the current flowing through the load
- \(I_{\text{operating}}\) = is the current that is needed by the regulator in order to function

From equation 3 it is important to note that the utility of LDO regulators in small voltage drops can be impaired if the load impedance is too small i.e. the output current is too high. For that reason the use of LDO regulators is limited to digital applications and microprocessors, as opposed to power supplies. For the reasons above linear regulators are not sufficient in power supply voltage regulation and DC-DC power converters that are power hungry and consume much current.
Switching Power Regulators

Switching power regulators or switched mode power supplies have become the standard in the market nowadays. This has been solidified within the consumer market in the 1970’s when Apple’s Apple II computer which was quite popular for its small size and light weight at the time implemented a switching regulator in its power supply [2]. The key advantage of these regulators is due the fact that they have the potential to regulate voltage at ideally 100% efficiency, this is achieved by virtue of the switching on and off of the power signal with a pulse width modulated gate control and the use of a filter on the output to average out the power signal to attain the desired output voltage. Figure 3 gives an example of a switching regulator, the regulator shown is a synchronous buck converter, this converter is a DC to DC converter it takes in a DC input voltage and steps it down to the desired output voltage.
A situation where the buck converter can be used would be to step down a rectified DC output from the AC mains in a power adapter application. Figure 4 gives an example of a system block diagram for a power adapter.

Figure 3: Synchronous buck converter

Figure 4: Power adapter system diagram
The AC mains is the input supply to the system, this AC signal is converted to DC using a full bridge rectifier network. Due to the nature of AC power signals from the line and the potential threat that it may cause to consumers it is important to isolate the signal from the adapter output which come in contact with the user. Lastly the higher voltage DC signal must be stepped down to the operating voltage of the application.

The importance of these efficient switching power supplies with fast transient response and accurate voltage regulation especially at the low voltage (30 V) range has become quite important in the today’s market. This can be mainly attributed to the fast growth and increase in demand for data centers, and the massive increase in the amount of data being transmitted. It is estimated that the amount of annual global data center IP traffic will increase from 4.7 zettabytes in 2015 to 15.3 zettabytes in 2020, where 1 ZB = 1024 exabytes, 1 EB = 1024 petabytes, 1 PB = 1024 terabytes, and 1 TB = 1024 gigabytes [3]. Also consumer cloud storage is predicted to increase from 47% of the internet consumer population in 2015 to 59% in 2020 [3]. With the current system design of data centers there is much utilization of these low voltage devices when it comes to voltage regulation [4]. As a result of this it is quite critical to optimize the design of these power devices such that the most optimal efficiency and performance are achieved when regulating power in data centers.
Figure 5 gives an example of a data center power conversion system from Berkley Lab Data Energy Efficiency Research [5]. The AC line input is connected to an uninterruptible power supply (UPS) which consists of a battery for back up purposes and an inverter to return the power stored in the battery to an AC voltage. The next stage is the power distribution unit (PDU) which is responsible for the distribution of power to different servers within the same rack. Within the server there exists a multi output power supply that is responsible for regulating the voltage for the different components with the server’s computer system or mother board, it outputs the desired voltage for each electronic component, for example the internal drive needs 5 V while on the other hand the external drive requires 12 V and hence the multi output power supply gives each component its desired regulated voltage level.

![Diagram of data center power conversion system]

Figure 5: Example of data center power conversion

The multi output power supplies that are used in these servers have a heavy reliance on low voltage power transistors especially in their output stages. From Figure 5 it can be seen that
the output voltages range from 1.1 V to 12 V which is in the low voltage range. From this it is important to note the impact that the low voltage power transistor has on the efficiency performance and the need for optimization. For a buck converter application there are two major sources of losses that come from the power transistor, they are the conduction losses and the switching losses. Equations 4 and 5 gives the value of conduction and switching losses as a function of circuit parameters and the power device’s parameter [6]. One important aspect to note is that a buck converter has two MOSFET switches a synchronous FET and a control FET or high side and low side FETs, the conduction losses formula assumes that the two transistors are matched and have the same parameters.

\[ P_{CON} = R_{DS(on)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left( I_{O_{OUT}}^2 + \frac{I_{RIPPLE}^2}{12} \right) \]  

\[ P_{SW} = V_{IN} \cdot I_{OUT} \cdot f_{SW} \cdot \frac{Q_{GS} + Q_{GD}}{I_G} \]  

Where:

\( P_{CON} \) = conduction losses.

\( P_{SW} \) = switching losses.

\( V_{OUT} \) = regulator output voltage.

\( V_{IN} \) = regulator input voltage.

\( R_{DS(on)} \) = power transistor on state resistance. This is the resistance of a MOSFET in the linear region.

\( I_{OUT} \) = regulator output current.

\( I_{RIPPLE} \) = current ripple present in the output current.

\( f_{SW} \) = regulator switching frequency.
Q_{GD} = gate to source charge of sync FET.

Q_{DS2} = drain to source charge of control FET.

I_G = gate current.

The parameters R_{DS(on)}, Q_{GD}, and Q_{DS2} are all dependent on the design of the power device in use. This means that for the efficiency of the power converter to be as close to 100% as possible it is critical to have an optimized power transistor that has the lowest possible figure of merit (FOM) on state resistance × gate charge (R_{DS(on)} × Q_G). A low FOM that is driven by a lower R_{DS(on)} and a lower Q_G leading to lower conduction losses and lower switching losses, increasing the efficiency of the power supply. That is the motivation behind the study and research performed and reported in this thesis, to achieve the best possible design and optimization for low voltage power MOSFET device and obtain the lowest possible FOM resulting in voltage regulators with higher efficiency.

**Power MOSFET**

As far as silicon power MOSFETs are considered there are two fundamental designs the vertical double diffused MOSFET or VDMOS and the lateral double diffused MOSFET or LDMOS. Both have their benefits and limitations and find themselves in numerous applications in the industry.
VDMOS

The vertically double-diffused metal oxide semiconductor (VDMOS) field effect transistor is distinguished by its vertical structure shown in Figure 6. The VDMOS device can most commonly be found in power converter applications [7] due to the current carrying capabilities of the vertical structure offering a higher power density [8]. Also the vertical voltage sustaining of the structure allows for a higher cell density, due to a smaller cell pitch. The main limitation of the VDMOS device is the bottom drain placement which comes as an obstacle in process integration.

Figure 6: VDMOS transistor cross section
LDMOS

The laterally double-diffused metal oxide semiconductor (LDMOS) field effect transistor is distinguished by its lateral structure as in Figure 7. Similar to the conventional symmetrical CMOS transistors the flow of the current is in the latter direction close to the surface of the wafer. The asymmetrical structure of the device assists in increasing the breakdown characteristics of the device making more suitable for high voltage and RF applications.

Figure 7: LDMOS transistor cross section
The lateral structure of the LDMOS with the source and drain terminal being on the same surface allows the LDMOS device to offer higher levels of integration for CMOS integrated circuits (ICs) [9]. As a result the LDMOS is viewed as a viable solution for advanced systems on a chip (SoC) which have power integrated within the solution combining both high speed digital logic CMOS and high power LDMOS devices onto the same silicon chip [10]. These SoC are often found in Internet of Things (IoT) applications. LDMOS devices have also found a footing in advanced integrated power electronics modules (IPEMs) and electric vehicles that are now rampant in the market.

Sentaurus TCAD Simulation

The conventional and modified power devices are simulated using two-dimensional (2D) and three-dimensional (3D) Sentaurus Device TCAD in this thesis. For the conventional and most devices considered it was possible to simulate it in a 2D environment, but the same is not true with super-junction (SJ) LDMOS device in particular, which is one of the considered low voltage device schemes. The SJ LDMOS is quite unique in that the SJ N and P pillars do not exist on the front facing 2D cross section, but the pillar array is placed within the width of the device, requiring a 3D simulation [11].

The device simulation uses the following physics models. Old Slotboom model [12] for the effective intrinsic carrier density. Doping dependence [13], high field saturation [14], and Lombardi [15] models are used for the mobility dependence. Schottky Reed Hall [16], Auger [17], and Okuto avalanche models [18] for the recombination
Thesis Organization

This thesis is organized into five chapters, the first chapter in an introduction and gave the context and the purpose for which this study and research was conducted. Chapter two gives details on first technique attempted to improve the FOM for the low voltage LDMOS, i.e. Super-Junction technique. Chapter three gives the second technique used which is using a floating P type region to improve the FOM. Chapter four introduces a new technique developed that combines shallow trench isolation (STI) and floating P region to achieve and even lower FOM. Chapter five closes the thesis with a conclusion on the foundings that were presented in the earlier chapters.
CHAPTER TWO: LOW VOLTAGE SUPER-JUNCTION LDMOS

When it comes to the design of power MOSFETs and their optimization there exists a very critical tradeoff that defines the limit of a specific technology, this tradeoff is breakdown voltage (BV) to on state resistance ($R_{DS(on)}$) tradeoff. Equation 4 gives the relation between BV to $R_{DS(on)}$ generalized over the silicon technology [19].

$$R_{DS(on),\text{conv.}} = \frac{a \cdot \sqrt{B} \cdot BV^2}{\mu_n \cdot \varepsilon \cdot A} \quad (4)$$

Where:

$R_{DS(on),\text{conv.}}$ = on state resistance for a conventional power transistor

$BV$ = breakdown voltage of device

$a$ = constant of value 6.21 for a 30 V device and 1.87 for a 600 V device

$B$ = radiative recombination constant

$\mu_n$ = mobility of electron

$\varepsilon$ = permittivity of silicon

$A$ = area of device

This would imply that at a certain operating voltage the BV to $R_{DS(on)}$ tradeoff would define the performance of the device, this statement is only true for conventional devices that have only the basic constructs of a power device. For that reason it is important to create additional design elements that improve upon the existing conventional design to overcome the hard limit of the technology, i.e. overcoming the silicon limit. Of these modern techniques applied to the LDMOS is techniques such as RESURF, super-junction (SJ), and etc. Such
techniques are used in the industry today, the one investigated for the purposes of this thesis is the SJ technique which has proven its worth in the high voltage range and is tested for the low voltage range in this thesis.

**Super-junction PN junction**

The fundamental basis on which the SJ concept is established is on the employment of P and N pillars in succession where a PN junction forms, i.e. instead of having a planar and flat point of contact in a PN junction the point of contact between the P and the N region wraps around the pillars. This does two things to the PN junction, first it makes it so that the surface of contact between the two regions (the junction) where the electric field peaks to have a much wider surface area, this leads to a better distribution of the electric field leading to a higher breakdown voltage. The second impact is on the resistance of the conducting or drift region, this will increase simply due to the fact that the overall volume for which the carriers can flow is reduced (this is especially apparent in MOS transistors which are unipolar devices that are built with SJ pillar), but this effect can be compensated by the increasing of the doping concentration to reduce the conducting layer’s resistance.

Both the conventional and SJ PN junctions have been simulated to give some insight of the impact of the SJ technique. The cross section of both the conventional and the SJ PN junctions are shown in Figure 8 and Figure 9 respectively. Both PN junctions contain a P+ anode and N+ cathode for the purposes of maintaining good contact. The difference between the two PN junctions is in the N- region as opposed to the conventional device that has a singular N-region, the SJ region contains pillars of N- and P-. Note that a doping concentration of \( N_d = N_a = 1e16 \text{ cm}^{-3} \) was used.
Figure 8: Conventional PN junction

Figure 9: SJ PN junction
This difference in the layout of the structure led to a significant change in the breakdown performance of the PN junction. Figure 10 gives the electric field distribution of both the conventional and SJ PN junctions at their respective reverse breakdown voltages. For the conventional PN junction the electric field is peaking at the junction between the P+ anode and the N- region, as for the SJ PN junction the electric field has a peak point at the edges of the termination pillars with distribution of the electric field on the side walls of the N and P pillars.

Abs(ElectricField-V) [V*cm ^ -1]

![Figure 10: Electric field distribution of (a) conventional PN and (b) SJ PN junction](image)
Figure 11 shows the impact ionization of both PN junctions at a blocking voltage of 55 V. At 55 V it can be seen that the conventional PN junction exhibits heavy impact ionization close to the P+ anode and N- region junction which eventually leads for the device to breakdown soon after as seen by the regions in red. On the other hand the SJ PN junction exhibits less impact ionization at the same voltage leading for it to has a breakdown voltage that is higher than that of conventional device.

**ImpactIonization \([\text{cm}^{-3}\text{s}^{-1}]\)**

![Impact Ionization Image](image)

Figure 11: Impact ionization of (a) conventional and (b) SJ PN junctions @ 55 V
With the physical properties that lead to the modification in performance difference in the SJ, Figure 12 shows that the breakdown voltage of the SJ PN junction is much beyond that of the conventional device with the same device dimension size and breakdown conditions. Note that the breakdown condition used was when the current exceeded $5 \times 10^{-9} \text{ A/µm}$. Also no area factor was used to modify the current density value, this means that a default device width of 1 µm was used to simulate the device.

![Figure 12: Breakdown voltage plot of conventional PN junction and SJ PN junction](image)

Figure 12: Breakdown voltage plot of conventional PN junction and SJ PN junction
Table 1 lists all of critical parameters to compare between the conventional PN junction and the SJ PN junction.

Table 1: SJ PN junction performance comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conventional PN Junction</th>
<th>SJ PN Junction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown voltage</td>
<td>56.7 V</td>
<td>100 V</td>
</tr>
<tr>
<td>Max Impact ionization @ 55 V</td>
<td>2.8e18 cm³s⁻¹</td>
<td>1e17 cm³s⁻¹</td>
</tr>
</tbody>
</table>

Based off of Figure 12 and Table 1 it is clear that the SJ technique is quite impactful to improve the breakdown characteristics of a PN junction. The same SJ technique can be applied to MOS devices which in its design by default contains a PN junction where the drift region of the device and the body or well meet.

Applying SJ technique to the LDMOS

With how the LDMOS device is built the drift region of the device is direct contact with the body or p-well this is that point at which the electric field peaks within the device. This point of contact is basically a PN junction since the drift region is n-type and the body of the device p-type, this means that SJ N and P pillars can be inserted. With the LDMOS device the flow of the majority carriers is in the lateral direction close to the surface of the wafer with that in mind for the SJ N and P pillars to be inserted it would have to be within the width of the device and not within the depth of the device in order to correctly distribute the electric field that causes high impact ionization and breakdown.
Figure 13 gives the cross section of the SJ LDMOS device. The device is modeled in 3 dimensions to incorporate the SJ N and P pillars as shown in the figure.

The example device given in Figure 13 in an NMOS device with a majority carrier of electrons this means that these carriers can only flow in the N type region within the drift region, this implies that the inserted P pillar in the drift region will lead to an increase in the resistance that the electrons exhibit when flowing in the drift region this quite critical when taking the percent contribution that the drift region holds as part of the overall on state resistance of the power device. Table 2 gives the breakdown of each resistance component of a power MOSFET and the contribution of each resistance component to the total on resistance [19, 20].
Table 2: Resistance components contribution

<table>
<thead>
<tr>
<th>Resistance type</th>
<th>30 V device</th>
<th>600 V device</th>
</tr>
</thead>
<tbody>
<tr>
<td>R*</td>
<td>7%</td>
<td>0.5%</td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;n+&lt;/sub&gt;</td>
<td>6%</td>
<td>0.5%</td>
</tr>
<tr>
<td>Source layer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;CH&lt;/sub&gt;</td>
<td>28%</td>
<td>1.5%</td>
</tr>
<tr>
<td>Channel</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;a&lt;/sub&gt;</td>
<td>23%</td>
<td>0.5%</td>
</tr>
<tr>
<td>Accumulation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;e&lt;/sub&gt;</td>
<td>29%</td>
<td>96.5%</td>
</tr>
<tr>
<td>Drift region</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;Sub&lt;/sub&gt; or R&lt;sub&gt;d&lt;/sub&gt;</td>
<td>7%</td>
<td>0.5%</td>
</tr>
<tr>
<td>Substrate for vertical device and drain layer for lateral device</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 14 gives a cross section of a power MOSFET with the location of all the resistance components within the layout of the device.
From Table 2 the contribution of the drift region resistance is 29% which is significant in that any increase in the resistance of this region will immediately reflect on the total on state resistance. This can be mitigated by increasing the doping concentration of the drift region, but an issue arises from equation 4 [21] (which models the breakdown voltage of an abrupt junction as a function of the doping concentration) as it can be seen that the breakdown voltage is inversely proportional to doping concentration, meaning that this will lead to a decrease in breakdown voltage, but it is noted that the SJ technique improves the breakdown characteristics in the first place making the tradeoff a worthy one.
\[ BV = \frac{\varepsilon \cdot E_{\text{crit}}^2}{2 \cdot q \cdot N_B} \]  

(5)

Where:

- \( BV \) = breakdown voltage
- \( \varepsilon \) = permittivity of silicon
- \( E_{\text{crit}} \) = critical electric field for breakdown
- \( q \) = fundamental charge
- \( N_B \) = bulk doping concentration

Table 3 demonstrates improvements in performance with the use of the SJ technique over the conventional LDMOS.

Table 3: SJ LDMOS performance comparison

<table>
<thead>
<tr>
<th>Device</th>
<th>Doping (cm(^{-3}))</th>
<th>BV (V)</th>
<th>( R_{\text{DS(on)}} ) (m(\Omega)-mm(^2))</th>
<th>Vt (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Early conventional</td>
<td>Nepi</td>
<td>30</td>
<td>124</td>
<td>1.6</td>
</tr>
<tr>
<td>SJ</td>
<td>Nepi</td>
<td>37</td>
<td>156.7</td>
<td>1.6</td>
</tr>
<tr>
<td>SJ</td>
<td>2 ( \times ) Nepi</td>
<td>30</td>
<td>116</td>
<td>1.6</td>
</tr>
<tr>
<td>SJ</td>
<td>2.5 ( \times ) Nepi</td>
<td>27.5</td>
<td>108</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Note that Nepi represents the doping concentration in the drift region. Here Nepi = 5\( \times \)10\(^{16}\) cm\(^{-3}\). Another important point to note that the \( R_{\text{DS(on)}} \) considered is the specific on state resistance meaning that it is normalized over an area of 1 mm\(^2\).
Applying the SJ technique to the conventional LMDOS proved it benefits, from Table 3 it can be seen for the same breakdown voltage of 30 V the specific on state resistance has dropped by around 8.9%. Although this is an improvement, it is quite marginal especially when compared to some high voltage (600 V) SJ devices and the benefits the SJ technique can have on these higher breakdown devices. Infineon and their CoolMOS transistor has taken great advantage of this SJ technique, but has limited its use to high voltage devices [22].

Equation 6 gives the relation between $R_{DS(on)}$ and $BV$ for a SJ device [19].

$$R_{DS(on),SJ} = \frac{1}{a \cdot B_{SJ}^6 \cdot BV^6} \cdot q \cdot \mu_n \cdot N_D \cdot A$$

Where:

- $R_{DS(on),SJ}$ = on state resistance for a SJ power transistor
- $BV$ = breakdown voltage of device
- $a$ = constant of value 6.9 for a 30 V device and 2.07 for a 600 V device
- $B_{SJ}$ = radiative recombination constant for a SJ
- $q$ = elemental charge
- $\mu_n$ = mobility of electron
- $N_D$ = drift region doping
- $A$ = area of device
Based off of equation 6 and the previously mentioned equation 4 the trend shown in Figure 15 can be extracted [19].

![Figure 15: \(R_{DS(on)}\) vs BV for conventional and SJ devices](image)

By looking closely at the plot it is possible to discern that at voltages lower than around 200 V the \(R_{DS(on)}\) of the conventional device is actually lower than that of the SJ device, hence diminishing the benefits of the SJ technique for low voltage devices. This is confirmed by the marginal benefit that was achieved with the original SJ device despite all of the optimization efforts that was taken place.

With discrepancy in performance between the low voltage SJ device and high voltage SJ device in mind a there was an apparent need to improve upon the existing low voltage SJ LDMOS. The original SJ LDMOS device taken into consideration (the one shown in Figure 13)
was further investigated to figure out the point of weakness of the device. The investigation started off by looking at the cross section of the device and the electric field distribution. Looking at the electric field distribution helps in the determination of the hot spots on the device or the locations where the electric field peaks leading to breakdown. Figure 16 shows the electric field distribution and the impact ionization of the original SJ LDMOS device.

![Figure 16: (a) electric field distribution and (b) impact ionization of original SJ LDMOS device](image)

From Figure 16 (a) it can be seen that the electric field is peaking at the bottom of the drift region where it makes contact with the P body of the device. This peak in the electric field introduced a heavy amount of impact ionization as shown in Figure 16 (b) around the same region. The reason for this peaking of electric field can be traced down to the level of doping.
concentration, because it had an inverse relation with respect to the breakdown voltage as modeled in equation (5) previously.

As a result of this if the doping concentration were to increase then as a result the breakdown voltage would decrease. To mitigate this the obvious solution would be to reduce the drift region doping concentration to make gains in breakdown voltage, but this is against the principle of using the SJ technique which requires an increase in the drift region doping concentration, particularly near the surface where the carriers flow to reap the benefits of the SJ technique. As such a low doped buffer layer was added under the drift region with this the area of contact with the body would be with the lower doped buffer layer rather than with the drift region.

This can be shown in Figure 17 where the buffer layer is placed with the same majority carrier as the drift region, but with a lower doping concentration.

![Figure 17: SJ LDMOS device with buffer layer](image-url)
With the introduction of this buffer layer the benefits were immediately realized when compared to the original SJ LDMOS device. Figure 18 gives the electric field and impact ionization distributions of this buffer layer SJ LDMOS. Both plots are taken at the device’s breakdown, now the electric field is better spread at the drift and body junction and the value of the peak impact ionization rate has reduced, this allowed a further increase in the doping concentration and further reducing the on state resistance leading to an overall improvement in the device’s FOM.

Figure 18: (a) electric field and (b) impact ionization distribution of buffer layer SJ LDMOS
Table 4 compares the performance results of the buffer layer SJ LDMOS with the conventional and the original SJ LDMOS.

Table 4: Buffer layer SJ LDMOS results comparison

<table>
<thead>
<tr>
<th>Device</th>
<th>Doping (cm(^{-3}))</th>
<th>BV (V)</th>
<th>(R_{DS(on)}) (m(\Omega)-mm(^2))</th>
<th>Vt (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conv.</td>
<td>Nepi</td>
<td>30</td>
<td>124</td>
<td>1.6</td>
</tr>
<tr>
<td>SJ</td>
<td>2 × Nepi</td>
<td>30</td>
<td>116</td>
<td>1.6</td>
</tr>
<tr>
<td>Buffer layer SJ</td>
<td>2 × Nepi</td>
<td>48</td>
<td>110</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td>Nbuffer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Buffer layer SJ</td>
<td>4 × Nepi</td>
<td>30</td>
<td>95</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td>50 × Nbuffer</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note that Nepi represents the doping concentration in the drift region and Nbuffer represents the doping concentration in the buffer region. Here Nepi = 5e16 cm\(^{-3}\) and Nbuffer = 1e15 cm\(^{-3}\).

From Table 4 it is possible to see the performance advantages that the buffer layer has brought upon the low voltage LDMOS structure, but despite all the efforts placed the improvements in the on state resistance are somewhat marginal (a 23% improvement in \(R_{DS(on)}\) from conventional device to buffer layer SJ LDMOS). The main reason why these improvements may not be considered as worthy is due to the many process complexities that come with the SJ technique and that replicating the process may be somewhat difficult.
SJ Process Challenges

There are a few critical parameters that must be considered when designing a device with SJ N and P pillars, amongst them are the ion implantation depth limitation, and the charge imbalance that can occur between the pillars. These limitations greatly impact the performance of any SJ device, this impact on performance can be more prevalent in low voltage SJ devices than it is in high voltage SJ devices. The reason these limitations are more impactful for low voltage devices is mainly due to the fact that the ratio of the pillar width to pillar depth may be smaller and that the pillars may be more tightly packed next to each increasing the room for error within the process.

When designing SJ devices the dimensions, length and width of the N and P pillars are very important parameters. The length and width of the pillars are a determining factor for the device’s operating breakdown voltage limit and on state resistance. A model relating the breakdown voltage and on state resistance to the pillar width are given in equations 7 and 8 [23].

\[
BV = \sqrt{E_{\text{crit}}^2 - E_L^2 \cdot t_{SJ}} \quad (7)
\]

\[
R_{DS(\text{on})} \cdot A = \frac{t_{SJ} \cdot W_n}{\varepsilon \cdot \mu_n \cdot E_L} \quad (8)
\]

Where:

BV = breakdown voltage

\(R_{DS(\text{on})}\) = on state resistance

\(E_{\text{crit}}\) = critical electric field for breakdown for silicon

\(E_L\) = lateral electric field of SJ pillars
A = device’s active area

t_{SJ} = thickness of SJ pillar

W_n = width of SJ pillar

ε = permittivity of silicon

µ_n = electron mobility

Based on the information from equations 7 and 8 that when designing a low voltage
device compared to a high voltage device will require that that the thickness of the pillar t_{SJ} be
reduced, assuming that both are made in silicon meaning that the critical electric field of both
devices will be the same. On the other hand equation 8 states that in order to reduce the on state
resistance which is quite critical for low voltage devices, the width of the pillar must be reduced.
The reduction of R_{DS(on)} is critical for the applications in which these low voltage devices are
used in, e.g. low voltage soft switching applications. These soft switching applications reduce the
switching losses by achieving zero voltage switching or zero current switching which would
normally lead to an increase in the circulating energy causing an increase in the conduction
losses [24], therefore it is important to keep the on state resistance to a minimum to keep the
efficiency up.

With the SJ pillar dimensions in mind it is important to note that most modern SJ
processes use some form of ion implantation as in [25]. A major concern here is the width to
length limitation that is associated with the process of ion implantation. Equation 9 gives the
mathematical model for the distribution of the doping concentration as a function of junction
depth for impact ion implantation [26].

33
$$N(x) = \frac{\phi_i}{\Delta R_p \cdot \sqrt{2\pi}} \cdot \exp\left(-\frac{1}{2} \left(\frac{x - R_p}{\Delta R_p}\right)^2\right)$$  (9)

Where:

- $N(x) = \text{doping distribution as a function of depth}$
- $R_p = \text{projected range, the mean depth of the distribution}$
- $\Delta R_p = \text{projected range lateral straggle, standard deviation of the distribution}$
- $\phi_i = \text{ion implantation dose}$

The stochastic nature of ions being implanted into silicon needs a statistic Gaussian distribution as in equation 9 to be able to model and describe how these ion are distributed within the material. This Gaussian distribution has a lateral straggle $\Delta R_p$ that is approximately $1/2.5$ of the projected range $R_p$ according to the theory of Lindhard et al. for the specific condition that nuclear stopping dominates [26]. This would lead one to believe that as the range decreases so will the lateral straggle, but as the depth or range scales so will the width of the feature and the reduction in width of the feature causes more ion spreading due to the fact that they have a higher probability of colliding with the walls of the mask used. The afore mentioned leads to the lateral straggle to be greater that what is anticipated and may require more advanced ion implantation equipment such as in [27], that uses a different implantation species and a 2-step implantation process. With that it can be seen that the thin (for low $R_{DS(on)}$) and long (for maintaining BV) pillars required for optimal performance of low voltage SJ may be challenging to manufacture.
The other pressing issue with the manufacturing of SJ devices is the need for having the P and N pillars charged balanced with matched donor and acceptor charges, otherwise the performance of the device will degrade [28]. Figure 19 gives a comparison between the electric field distribution between the original balanced SJ PN junction and the charge imbalanced SJ PN junction.

**Figure 19:** Electric field distribution of (a) balanced SJ diode and (b) charge imbalanced SJ diode
The charge imbalanced device has the doping concentration of the P pillars equal to twice that of the N pillars, i.e. $N_a = 2 \times N_d$. The electric field distribution shows that the E-field of the charge imbalanced device is now concentrated on the P termination pillar rather than being evenly distributed between the two termination pillars of the PN junction. This shift in the electric field distribution resulted in a change in the PN junction’s breakdown performance as well. Figure 20 plots the reverse voltage versus the reverse current of charge balanced PN and imbalanced SJ PN junction.

Figure 20: Breakdown voltage plot of charge balanced and imbalanced SJ PN junction
The performance of the SJ PN junction can go down by 45% when the doping of the P pillar is twice that of the N pillar. The degree of degradation of the breakdown voltage depends on level of imbalance between the pillars [28]. The charge imbalance can cause the breakdown voltage of the PN junction to degrade even past that of the of the conventional PN junction as can be seen in Table 5. With how critical it is for the doping of the pillars to be matched and how the features of the SJ pillars need to be smaller of the low voltage application, the manufacturing of devices with the SJ technique become quite sensitive to process variation.

The process difficulties for perfecting the SJ pillars and the lack of great improvement in performance all make the SJ technique less attractive for low voltage (30 V) LDMOS. As such other techniques with better performance and less process complexities are examined to replace SJ at this voltage range.

Table 5: Charge imbalanced SJ PN junction performance comparison

<table>
<thead>
<tr>
<th>Device</th>
<th>Breakdown Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional PN Junction</td>
<td>56.7 V</td>
</tr>
<tr>
<td>Charge Balanced SJ PN Junction</td>
<td>100 V</td>
</tr>
<tr>
<td>Charge Imbalanced SJ PN Junction</td>
<td>55 V</td>
</tr>
</tbody>
</table>
CHAPTER THREE: LDMOS WITH FLOATING P TYPE LAYER

The use of a floating P type layer to exceed the silicon limit for low voltage (30 V) devices came a viable replacement for the SJ technique. It is implemented by taking the conventional device and replacing the shallow trench isolation (STI) layer with a floating P type layer.

Applying floating P type layer to the low voltage LDMOS

When first applying the floating P type region technique initially the STI region was replaced directly by an equivalent P type layer as shown in Figure 21. With this immediate improvement over the SJ LDMOS was observed without any optimization. Table 6 compares this initial floating P LDMOS with the buffer layer SJ LDMOS.

![Initial LDMOS with floating P type region](image)

Figure 21: Initial LDMOS with floating P type region
Table 6: Initial floating P LDMOS performance comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Buffer layer SJ LDMOS</th>
<th>Initial floating P LDMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV (V)</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>$R_{DS(on)}$ (mΩ-mm$^2$)</td>
<td>95</td>
<td>91</td>
</tr>
<tr>
<td>$V_T$ (V)</td>
<td>1.6</td>
<td>1.6</td>
</tr>
</tbody>
</table>

The use of the floating P technique immediately gave a 4.2% improvement in the on state resistance over the SJ LDMOS. The enhancement in performance showed the potential of the device and further optimization was pursued to take advantage of the technique and exploit all of its benefits.

**Optimization of floating P LDMOS**

The electric field and impact ionization for the initial floating P LDMOS were examined to see where the hotspots occur in the device. Figure 22 gives a cross section of the distribution plots, the electric field peakings close to the surface within the floating P layer, and this leads to a high amount of impact ionization within that region. When compared to the E-field and impact ionization of the buffer layer SJ LDMOS in Figure 18 which has its peak electricity field at the drift region interface with the body of the device, it is apparent that the electric field peaking can be pushed down wards towards that interface to further optimize the device.

With the location of the peak E-field in mind modifications were made to the device. The major modification made at this point was to increase the size of the floating P type region Figure 23, this led to an improvement in the breakdown characteristics straightaway. The
improvement in breakdown voltage was followed by increase in drift doping to bring the device to a 30 V breakdown.

Figure 22: (a) Electric field and (b) impact ionization distribution of initial floating P device

Figure 23: Floating P LDMOS optimized P layer size
The optimization of the size of the P layer showed some improvement in the electric field and impact ionization distribution as shown in Figure 24. The peak electric field is moved back down to the drift region and body interface. This is critical to the progression of the device’s optimization, since if the floating P layer was the first point of breakdown then this would imply the technique cannot improve on the existing design by much.

Table 7: Floating P LDMOS with optimized P layer size performance comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Buffer layer SJ LDMOS</th>
<th>Initial floating P LDMOS</th>
<th>Floating P optimized size</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV (V)</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>R_{DS(on)} (mΩ-mm²)</td>
<td>95</td>
<td>91</td>
<td>89</td>
</tr>
<tr>
<td>V_T (V)</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Figure 24: (a) Electric field and (b) impact ionization distribution of floating P optimized layer size
The next optimization step that was taken was to scale the device down to a smaller cell size. The reduction in the cell size would lead to a great improvement in the specific on state resistance properties of the device, this can be attributed to the fact that more of the single device cross section can fit on a given silicon area. Also power device design is now pushing towards a smaller technology node, meaning that it is best to take full advantage of the performance increase that comes with scaling.

The cell size reduction optimization step was taken and the device’s cell pitch (total length) was reduced from 8 µm to 3 µm. When the scaling was first done all the dimension were scaled according to the 3:8 ratio, but this led to a channel length that was too short and caused the device to breakdown much earlier than needed due to punch though. The device’s channel length was reduced to 340 nm. As a result some dimensions were scaled down by different ratios to achieve the best possible device performance. Figure 25 gives a cross section of the cell pitch optimized floating P device.

The reduction of the cell size came with a sizable improvement in the on state resistance at virtually no cost in the breakdown performance of the device. Table 8 compares the performance of the 3 µm cell pitch optimized device with the performance of the original 8 µm cell pitch device. The $R_{DS(on)}$ is reduced from 95 mΩ-mm² to 63 mΩ-mm² for the same breakdown voltage range of 30 V. The on state resistance improvement was accompanied by an improvement in the gate charge which led to the FOM ($Q_G \times R_{DS(on)}$) drop down by a significant amount, the FOM dropped from 45 mΩ-nC down to 9.75 mΩ*nC, that is a 78% reduction is the device’s figure of merit.
Figure 25: Floating P LDMOS optimized cell pitch

Table 8: Performance comparison of optimized cell pitch floating P LDMOS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Original floating P</th>
<th>Optimized cell pitch floating P</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV (V)</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>$R_{DS(on)}$ (mΩ-mm$^2$)</td>
<td>89</td>
<td>63</td>
</tr>
<tr>
<td>$Q_G$ (nC)</td>
<td>0.51</td>
<td>0.155</td>
</tr>
<tr>
<td>$V_T$</td>
<td>1.6</td>
<td>1.6</td>
</tr>
<tr>
<td>$FOM = Q_G \times R_{DS(on)}$ (mΩ-nC)</td>
<td>45</td>
<td>9.75</td>
</tr>
</tbody>
</table>
A major concern with the 8 µm un-optimized cell pitch device was that there was much real-estate as far as the device’s area is concerned that went largely unutilized for depletion and assisting in breakdown. Figure 26 shows the electric field and impact ionization distributions of the 3 µm optimized cell pitch device. In the cross section it is possible to see the depletion line goes deeper into the drift region and that the electric field is spreading across more of that region, this relaxes the electric field from peaking at one point early giving the device more room for breakdown, this explains why the breakdown voltage did not change much despite the drift region length was reduced when scaling.

Figure 26: (a) Electric field and (b) impact ionization distribution of floating P LDMOS with optimized cell pitch
Floating P LDMOS process

The major distinguishing factor between the floating P LDMOS and the SJ LDMOS besides the performance variance is the manufacturing process difference. It was shown in previous sections that the fabrication of the SJ N and P pillars for low voltage 30 V devices can be challenging due to the need for narrow and long pillars and the ion scattering that occurs with smaller features. The fabrication difficulties of SJ at the low voltage application can be averted by switching to the use of the floating P technique which has a commentary MOSFET (CMOS) compatible process that wouldn’t require any added fab equipment. The well-matching of the floating P process can be illustrated from the process simulation that was developed specifically for the device. The process was simulated using Sentaurus Process TCAD.

The device was built on a silicon wafer with <100> lattice orientation. The substrate was P type and had an initial boron doping of $5 \times 10^{16}$ cm$^{-3}$. When building the device 5 masks were used with a combination of positive and negative photoresist to obtain the desired patterns to fabricate the fundamental constructs of the device. Table 9 lists all of the masks used and their function.

<table>
<thead>
<tr>
<th>Mask Name</th>
<th>Photoresist polarity</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>NWELL</td>
<td>Positive</td>
<td>Mask ion implantation of n-well phosphorus dopants</td>
</tr>
<tr>
<td>Mask Name</td>
<td>Photosist polarity</td>
<td>Use</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>Negative</td>
<td>Mask ion implantation of p-well boron dopants</td>
</tr>
<tr>
<td>POLY</td>
<td>Negative</td>
<td>Pattern gate oxide and gate polysilicon.</td>
</tr>
<tr>
<td>FLOATP</td>
<td>Positive</td>
<td>Mask ion implantation of floating P layer boron dopants</td>
</tr>
<tr>
<td>NSOURCE</td>
<td>Positive</td>
<td>Mask ion implantation of source layer phosphorus dopants</td>
</tr>
<tr>
<td>PBODY</td>
<td>Positive</td>
<td>Mask ion implantation of body contact boron dopants</td>
</tr>
</tbody>
</table>

The process developed is self-aligned to the gate, the initial process steps started off with establishing the gate polysilicon. As such the gate oxide layer 50 nm in thickness is grown on the surface of the silicon wafer this is followed by depositing the polysilicon on top of the oxide. This results in a poly – oxide – silicon stack up, the stack up is then patterned with the first mask PLOY and the gate poly are etched down to the silicon. In a cleanroom environment the poly can be etched in a reactive ion etching (RIE) tool with SF$_6$ as the reactive gas, while SiO$_2$ can be etched using CHF$_3$ as the reactive gas. Note the oxide is etched in a later stage in the process to ensure that the dopants don’t diffuse out of the surface of the silicon. Figure 27 gives a cross section of the device upon etching and patterning the gate oxide and poly.
With the gate poly and oxide in place the n-well is then formed using the second mask NWELL and with positive photoresist. Phosphorus ions were used to implant dopants for the n-well, a dose of $3 \times 10^{13} \text{ cm}^{-2}$ with an implantation energy of 150 keV. The same NWELL mask is used in forming the p-well, but negative photoresist is used here. Boron ions were used implant dopants for the p-well, a dose $4 \times 10^{13} \text{ cm}^{-2}$ with an implantation energy of 100 keV. Both the n-well and p-well implants are annealed for activation at a temperature 1100°C, a time of 80 minutes was used to drive the dopants deep into the wafer. The dopant anneal and dive in led to an n-well with a junction depth of 1.35 μm a p-well depth of 1.40 μm. Figure 28 gives the cross section of the device with the implanted n-well and p-well dopants.
Now that the n-well is in place the floating P layer can be deposited on the surface near the gate edge. There was a challenge with depositing the floating P layer that existed due to the process being self-aligned to the, i.e. the gate poly has already been deposited. The p-type layer needs to straddle the gate edge on the surface of the n-well and the gate poly is too thick to have the dopants reliably deposited through polysilicon, as such a solution other than implanting directly was needed. To mitigate this obstacle an angled implant was used as shown in Figure 29, where the dopants were implanted at an angle of 20° with respect to the wafer. Figure 30 shows the cross section of the device with the floating p-type layer implanted.

Figure 28: Floating P LDMOS gate poly and oxide patterned on silicon wafer
Figure 29: Floating P layer angled implantation

Figure 30: Floating P LDMOS p-type layer deposited device cross section
Boron ions were used to dope the floating P layer using the third mask FLOATP. Four incremental dopants were used to dope the p-type layer the total dose was $1.4 \times 10^{13} \text{ cm}^{-2}$ with each dose amounting to $3.5 \times 10^{12} \text{ cm}^{-2}$. Each incremental doping was completed in a specific order with a specific energy level, 20 keV, 40 keV, 80 keV, and 120 keV were used for each dose respectively.

The subsequent step in the process was to prepare the source n-type layer. Phosphorus ions were used as the dopant for this layer using the fourth mask NSOURCE. A dose of $4.5 \times 10^{13} \text{ cm}^{-2}$ was implanted with an energy of 70 keV. After which the dopants are activated using rapid thermal annealing (RTA) for 5 minutes in order to stay within the thermal budget. Figure 31 shows the cross section of the device with source layer implanted.

Figure 31: Floating P LDMOS source n-type layer deposited
In preparing for the N\textsuperscript{+} source and drain contact doping oxide spacers were formed, the N\textsuperscript{+} doping is meaningful such to ensure that schottky contacts are avoided in the LDMOS source and drain side when the device is integrated with other integrated circuit components and interconnects. These spacers are formed by first depositing SiO\textsubscript{2} conformably on the surface if the wafer (chemical vapor deposition (CVD) can be used ensure conformity in a cleanroom environment) and then etching deposited layer using a directional process (dry etching can be used for ensure directionality in a cleanroom environment). With the spacers formed a blanket implant of arsenic ions is used with a dose of $1 \times 10^{15}$ cm\textsuperscript{-2} with an energy of 80 keV, this blanket implant also ensures that the polysilicon ends up with an effective N\textsuperscript{+} doping (note that poly can be deposited doped by including the dopants insitu during the poly deposition), reducing threshold voltage variation.

The final ion implantation step in the process is the implanting of the P\textsuperscript{+} body contact. The body contact is critical for device reliability to avoid device latch up, by reducing the base current as much as possible in the parasitic bipolar junction transistor (BJT) that exist within the construction of the device. Boron ions were used to implant the body contact PBODY is used as the mask. A dose of $1 \times 10^{15}$ with an energy of 60 keV was used during the process step. The body P\textsuperscript{+} contact and source/drain N\textsuperscript{+} contact dopants were both annealed for activation at the same time using RTA for 13 mins to stay within the thermal budget which gets more sensitive as the device approaches completion. Figure 32 shows a cross section of the completed process simulated floating P LDMOS device.

Table 10 gives a performance breakdown of the realistic process simulated device as compared that what was previously simulated.
Figure 32: Floating P LDMOS completed process simulated device

Table 10: Realistic process simulated LDMOS performance comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Original floating P</th>
<th>Optimized cell pitch floating P (ideal)</th>
<th>Optimized cell pitch floating P (realistic)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV (V)</td>
<td>30</td>
<td>30</td>
<td>25.7</td>
</tr>
<tr>
<td>$R_{DS(on)}$ (mΩ-mm$^2$)</td>
<td>89</td>
<td>63</td>
<td>36</td>
</tr>
<tr>
<td>$Q_G$ (nC)</td>
<td>0.51</td>
<td>0.155</td>
<td>0.38</td>
</tr>
<tr>
<td>$V_T$</td>
<td>1.6</td>
<td>1.6</td>
<td>1.9</td>
</tr>
<tr>
<td>FOM = $Q_G \times R_{DS(on)}$ (mΩ-nC)</td>
<td>45</td>
<td>9.75</td>
<td>13.6</td>
</tr>
</tbody>
</table>
The performance of the process simulated floating P device shown in

Table 10 is quite comparable to that of the ideal device. The FOM is greater by a factor of approximately 4 mΩ-nC, this can mainly be attributed to the increase in the gate charge that was a result of the realistic modeling of interface trap charges and lattice damage that may have occurred from the multiple ion implantation steps that were undergone. Interestingly the on state resistance performance is better than that of the ideal device, this can be explained by the lower breakdown voltage at first thought, but it is also due to a higher order reason that the breakdown voltage of graded PN junction is greater than that of an abrupt junction. The abrupt junction has lower doping at the interface this would lead to a higher breakdown voltage compared to the abrupt junction that has higher breakdown voltage at the interface.

Figure 33 gives a summary of the floating P process with cross sections of the device after each process step.

The floating P LDMOS has proven to be a viable solution to replace the SJ LDMOS for low voltage applications as demonstrated by the considerable performance gains that were displayed by the optimized floating P LDMOS. The feasibility and replicability of the floating P LDMOS device when compared to the low voltage SJ LDMOS is also a major factor affirming the significant benefit that can be achieved by using the floating P technique in place of the SJ technique for the 30 V application.
Figure 33: Floating P layer device process flow cross sections (a) gate poly & gate ox patterned on surface of wafer (b) N-well & P-well implanted (c) floating P layer deposited (d) source n-type layer deposited (e) oxide spacers formed (f) N+ contacts and P+ body contact formed.
CHAPTER FOUR: LDMOS WITH SHALLOW TRENCH ISOLATION IN FLOATING P LAYER

The concept of applying the floating p-type layer is built upon by the inclusion of a shallow trench isolation (STI) layer on the surface surrounded by the floating P layer. In Figure 26 (a) it is quite noticeable the electric field is peaking on the surface of the device and is the major cause for impact ionization as in Figure 26 (b) which leads the device to enter breakdown. The addition of STI helps to mitigate this issue and lead the device to higher device performance gains.

Adding STI to Floating P LDMOS

Silicon is known to have a critical electric field of breakdown of $5 \times 10^5$ V/cm, as with most layers in the floating P LDMOS device the floating p-type layer is composed of silicon. Since the device that was simulated and taken into consideration is an n-type MOS device, the majority carriers are electrons, meaning that the holes contained within the floating p-type layer have no contribution to the overall current follow of the device. The contribution of the floating P layer in the LDMOS device is for the purposes of sustaining a higher breakdown voltage, this implies that we can afford to change the material of the p-type layer on the surface of the device where the electric field is peaking.

Silicon oxide ($\text{SiO}_2$) comes as a great substitute for silicon on the surface where the electric field is peaking. $\text{SiO}_2$ has a critical electric field of breakdown that can range between 7-
13.5 MV/cm, which is more than one order of magnitude greater than that of silicon, meaning
that a higher blocking voltage can be sustained. A higher breakdown voltage immediately leads
to a higher on state resistance, since now the design of the device can afford to have an increase
in the drift region doping concentration. Figure 34 gives the cross section of the STI floating P
LDMOS device.

Figure 34: STI Floating P LDMOS
The addition of the STI region immediately led to performance improvements with the breakdown voltage increasing from 30 V to 48 V. The improvement can be seen in the electric field and impact ionization distributions as compared to the device prior to the addition of the STI region as in Figure 35 and Figure 36. Both cross sections are taken at 30 V, the STI floating P device has the same doping profile as that of the original floating P. The peak electric field is now isolated inside of the STI layer. SiO₂ has a higher critical electric field value than Si it immediately leads to the STI floating P device to have a lower total impact ionization rate, this is due to the fact that silicon oxide is an insulator and does not contain free carriers, the lower impact ionization leads to a higher breakdown voltage at the same doping concentration.

Figure 35: Electric field distribution for (a) STI floating P (b) floating P LDMOS
Figure 36: Impact ionization distribution for (a) STI floating P (b) floating P LDMOS

Figure 37 gives a cross section of the current density for the same doping concentration and at 30 V. At 30 V the floating P device is already exhibiting breakdown characteristics, while the STI enhanced floating P device is yet to experience the same levels of off state current. The breakdown improvements in the STI floating P device came at no on state resistance costs, in actuality the exact opposite was true in that $R_{DS(on)}$ did not just remain the same, but it in fact improved with the addition of the STI layer to the surface of the floating p-type layer LDMOS device. But the gate charge ($Q_G$) increases with the addition of the STI layer.
Figure 37: Current density distribution for (a) STI floating P (b) floating P LDMOS

Table 11: STI floating P LDMOS performance comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Optimized cell pitch floating P (ideal)</th>
<th>Optimized cell pitch floating P (realistic)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BV (V)</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>$R_{DS(on)}$ (mΩ-mm²)</td>
<td>63</td>
<td>22.8</td>
</tr>
<tr>
<td>$Q_G$ (nC)</td>
<td>0.155</td>
<td>0.26</td>
</tr>
<tr>
<td>FOM = $Q_G \times R_{DS(on)}$ (mΩ-nC)</td>
<td>9.75</td>
<td>5.93</td>
</tr>
</tbody>
</table>
From Table 11 we can notice that there is a slight increase in the gate charge of the STI plus floating P device which can be attributed to the wider surface area of the oxide in contact with silicon attracting a higher total number of charges. Despite this slight increase in $Q_G$ the on-state resistance was reduced by a significant amount as mentioned previously. The increase in $Q_G$ is due to the larger MOS capacitor plate area at the gate terminal caused by the addition of the STI region. The reduction in $R_{DS(on)}$ stems primarily from the decrease of the depth of the p-type layer, as some of it is occupied by the STI, leading to a thinner space charge region to be formed in the in the N-buffer layer, which is contact with the P layer. Since the buffer layer is lowly doped, any changes in the P layer dimensions would lead sizable variation in the depletion width. The smaller space charge region causes a reduction in the device sheet resistance which leads to the lower on-state resistance.

**Performance Improvement by Staggering STI**

The performance of the device was optimized by adjusting the size and placement of the oxide STI region given in Figure 38. Figure 39 plots the performance of the device when the STI is staggered by shifting it to the left with respect to the center of the P type layer and Figure 40 plots the performance when the STI is centered with respect to the mid-point of the P type layer. A STI width of around 0.25 $\mu$m was the optimal design point giving the desired 30 V breakdown and the lowest $R_{DS(on)}$ (22.8 m$\Omega$-mm$^2$ for staggered STI & 23.1 m$\Omega$-mm$^2$ for centered STI) value. From Figure 39 and Figure 40 we can also see that that the staggered STI achieves an overall better performance as far as the on-state resistance is concerned. Also, the staggered STI achieves a lower $Q_G$ compared to the centered STI, this is due to the smaller surface area of the oxide under the gate field plate.
It is clear from the staggered STI floating P LDMOS in Figure 38 as compared to the centered STI in Figure 34 that the staggered STI device a smaller surface area of the oxide under the gate field plate. The smaller surface area of the MOS capacitor leads the staggered STI device to have a lower $Q_G$ value compared to that of the centered STI. For the staggered STI the oxide was shifted to the left by 0.25 of the width of the p-type layer.
Figure 39: STI staggered with respect to floating P type region

Figure 40: STI centered with respect to floating P type region
The simulation results presented show that the device with the floating P layer has a FOM of 9.75 mΩ-nC while the device with STI plus floating P layer has a FOM of 5.93 mΩ-nC. That is a 39% improvement in the FOM. From our understanding of the current state of art, the implementation of such floating P layer with a STI region is a new design that led towards the given low FOM value observed by device simulation.
CHAPTER FIVE: CONCLUSION

The thesis investigates the super-junction LDMOS figure of merit \( (R_{DS(on)} \times Q_G) \) for the 30 V application. The Sentaurus TCAD device simulation results of this study indicate that the super-junction technique may not be the best choice of direction due to its limited performance improvement in modern power converter applications proven by the specific on-state resistance versus breakdown voltage trend and by device simulation. The process difficulties faced with creating thin and long pillars for small feature sizes and charge balancing the P and N pillars when the super-junction device is fabricated are added unfavorable factors for low voltage super-junction devices.

A replacement for the super-junction technique is suggested in the thesis by removing the super-junction pillars and shallow trench isolation region and adding a floating p-type layer where the isolation was present. This technique shows improvement in the device performance upon optimization. A process simulation for the device was developed; this process demonstrated the feasibility and replicability of using this technique in a standard 180 nm CMOS process. Lastly a new technique of surrounding the shallow trench isolation region with a P type layer is introduced which to our understanding is a new design to achieve a low figure of merit. The figure of merit \( (R_{DS(on)} \times Q_G) \) improved, going from 9.75 m\( \Omega \)-nC down to 5.93 m\( \Omega \)-nC for the floating P device.
LIST OF REFERENCES


[10] P. Heyer, "Meeting the power management needs of portable products," Available: 


