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Excellent Surface Passivation for High Efficiency C_Si Solar Cells

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EXCELLENT SURFACE PASSIVATION FOR HIGH EFFICIENCY C-Si SOLAR CELLS

by

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ABSTRACT

Semiconductor surface clean is sometimes perceived as costly but long recognized as pivotal in determining the final semiconductor device performance and yield. In this contribution, we investigated the effectiveness of crystalline silicon surface cleaning by a simple UV-ozone process in comparison to the industry standard RCA clean for silicon photovoltaic applications. We present a unique method of processing the silicon surface effectively by UV-ozone cleaning. Despite being simple, UV-ozone cleaning results in a superior surface passivation quality that is comparable to high-quality RCA clean. When used as a stack dielectric—UV-ozone oxide overlaid by aluminum oxide—the thickness of UV-ozone oxide plays an important role in determining the passivation quality. Of all treatment times, 15 min of UV-ozone treatment results in an outstanding passivation quality, achieving the effective carrier lifetime of 3 ms and saturation current density of 5 fA/cm². In addition, we present a simple and effective technique to extract values of electron/hole capture cross-section for the purpose of analyzing the interface passivation quality from already measured surface recombination parameters of saturation current density, interfacial trap density and total fixed charge, instead of measuring on the separately prepared metal-insulated-semiconductor (MIS) samples by the techniques: frequency-dependent parallel conductance or deep-level transient spectroscopy.
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CHAPTER 1- INTRODUCTION

1.1 Why Photovoltaics?

At the Climate Summit in Paris on December 2015[1], major industrial countries came to an agreement for taking action on global warming. To success in this goal not only fossil fuels should be replaced by renewable energy but also solar as the most encouraging renewable energy should be cost effective enough to be able to compete with other alternatives. In our world almost %50 percent of the energy need has to be covered fossil fuels. This consumption of fossil fuels is a major cause of global warming due to introducing greenhouse gasses into the atmosphere. More than 1.2 billion people in the world still do not have access to electricity while majority of them leave in developing countries. This developing countries as classified by United Nations and International Monetary Fund, are situated within the region spanning 35 degrees of the equator [2]which is known as the “sunbelt” with highest possible solar irradiance. One of the most encouragement for utilizing solar energy in this area is that despite developed countries lack of high power transmission line can be seen which can be covered by using batteries.

Moreover, solar like other renewable energy sources (wind, geothermal, hydroelectric and ocean thermal) is capable of satisfying peak energy demands. Therefore, solar energy is the superior energy source not only during the peak energy hours of the day, but also for enhancing life quality in less developed countries.

Despite all other clean and environmental friendly energy sources, solar is not limited by low technical potential such as system performance, topographic limitations, environmental, and
land-use constraints. Solar energy is the earth’s major renewable energy resource and the exploitation of the energy from the sun is the potential key to a sustainable energy.

Since beginning of modern photovoltaic devices (PV) in 1973 the cost has been decreased from 500$\$/W to less than 1$\$/W. Hence, PV became $100 billion industry while PV installation increased by %50 from 51.2 GW in 2015 to 76.6 GW in 2016. [3].

![Figure 1 Worldwide Growth of Photovoltaics.](image)

To measure if the price for the electricity provided by solar energy can compete with the cost of available electricity one can use “grid parity” parameter which can be influenced by (1) innovation in photovoltaic technologies, (2) simplification/optimization of the manufacturing processes, (3) increased deployment, and (4) the use of lower-cost materials. Two major breakthrough took place in PV industry which allowed adoption of this technology. First was the introduction of the back-surface field (BSF) where recombination losses have been decreased drastically, and the second one is silicon nitride (SiNx) film deposited by plasma enhanced
chemical vapor deposition which acts as an anti-reflection coating (ARC) and enhances light absorption in bulk Silicon.

**1.2 Needs for Solar Cell**

With global estimated to be 7.3 billion people in 2015 and expected to grow to reach 8 billion by 2030, global energy demand is going to increase[4]. Moreover, as world economies develop, per capita energy consumption is going to increase as well. In such a situation, %0.0025 of world’s energy need can be supplied by solar and there is an ever-increasing need for mankind to increase using this source of clean and renewable energy. An hour of sunlight can satisfy the need for humanity’s energy for a year which is 3000 times the daily output of Palo Verde nuclear station [2]. To compare different technologies regarding cost and practicality levelized-cost of electricity has been introduced. This parameter defined as the lifetime costs of a system divided by energy produced. US investment bank Lazard Capital revealed that as of 2016, utility-scale solar energy is cheaper than coal [1].

Besides being cost effective emits no harm to the environment such as toxic gases except disposal of the PV devices. They do not produce any noise and can be installed basically in every region of the earth. Hence, the challenge would lie on scientist to store this energy using solar cells.

The commercially available solar cells fall into two categories: wafer-based silicon photovoltaics and thin film technologies[5]. Wafer based Si solar cells use crystalline Si wafer and own the highest market share with more than 80% of the total production while thin film alternatives such as CdTe and Cu(In,Ga)Se\textsubscript{2} (CIGS) are well-known for their low-cost manufacturing process. The same advantage can be mention for organic solar cells such as Dye-sensitized solar. The amount of material which will be used for Si based solar cell is almost 100
times more than thin film PV. Although considering terawatt solar energy this is a huge challenge, still conversion efficiency which is another figure of merit that directly influence the cost per Wp is higher for crystalline Si solar cells.

Development of new technologies which are cost effective is the most challenging issue in Si based solar cells industry. This issue can be realized only by fundamental understanding of the mechanisms which are happening in Si PV.
CHAPTER 2- FUNDAMENTALS OF CRYSTALLINE Si SOLAR CELL

A solar cell basically works based on a p-n junction. Silicon which has an indirect band gap of 1.1 eV is an indirect bandgap semiconductor can be doped by Boron (p-type) and Phosphorous (n-type). When light radiates on a solar cell, photon with energy more than band gap can be absorbed and generate electron-hole pair and give their excess energy to the Si lattice. This electron-hole pairs will be separated in depletion region by a built in voltage (Figure 2)

In depletion region all electron from n-type which migrate toward p-type will recombine with holes. At the edge of the junction there is a negative net charge for p-type and positive net charge for n-type which produce a built in voltage. This built in voltage is a driving force for electron and hole to be extracted by an external circuit.

Figure 2. Schematic of depletion region for a p-n junction[6]

Silicon is the most abundant semiconductor on Earth [7] which has been playing an important role in semiconductor industry for decades due to bringing product scalability.
Moreover, in reaction with oxygen in can form a thin native oxide at room temperature after hours of exposure[8] and prevent degradation which is not the case for organic photovoltaics. Band gap of semiconductor is another reason for crucial role of this element. The advantage of Si bandgap is two folds: First is increasing reflection from back surface due to high refractive index difference (Si refractive index (n=3.55 at $\lambda = 1050\,nm$) with the help of a dielectric layer deposited on the back surface. Although Si is not able to efficiently absorb light because of its indirect bandgap, the high refractive index will help in light trapping for certain Si thickness.

Figure 3 depict the dependence of the light absorption in Si needs thickness of 100–200$\mu m$. There is a tradeoff between the optimum thickness for Si wafer and the proper thickness to avoid handling issues. Silicon band gap is almost identical to single-junction band gap energy which is ideal for highest conversion efficiency.

![Absorption depth in Silicon](image)

Figure 3. Absorption depth in silicon at room temperature (300K) [8].
2.1 Loss Mechanism in Solar Cell

Based on principal of detailed-balanced, all the microscopic processes are counter balanced by associated inverse process in thermal equilibrium. Utilizing this principle the theoretical efficiency of solar cell can be achieved without considering the non-radiative recombination which happens in the solar cell and follows the same process that occurs in a light emitting diode (LED) [9], [10] by following equation (1)

\[ EQE_{LED} = \frac{R_{rad}}{R_{rad} + R_{non-rad}} \]  

In this equation, \( EQE_{LED} \), \( R_{rad} \), \( R_{non-rad} \), are external quantum efficiency of an LED, radiative recombination rate, and non-radiative recombination rate, respectively. According to the Schokley limit the highest efficiency of a LED can be defined by the bandgap of semiconductor \( (E_g) \) and temperature. So a solar cell is a simple conversion system which generate electricity by light absorption. Note that the difference between the source temperature \( (T=6000K) \) and room temperature \( (T=300K) \) is the only loss mechanism which decrease the efficiency of solar cell to %95, but here are other deduction sources which limits the efficiency of solar cells.

Under 1 sun illumination the highest achievable efficiency is %29 due to fundamental loss mechanism which are dependent in the bandgap of semiconductor[11-15].

2.1.1 Fundamental Losses

The fundamental losses include the thermalization losses and transmission losses. when a photon with energy more than bandgap \( (h\nu \geq E_g) \) shines on a semiconductor it gives the excess energy to the semiconductor lattice in the form of heat then it can be absorb by the band gap of semiconductor by generation of electron-hole par. Band gap of semiconductor is transparent to
photon with energy less than band gap and this brings us the transmission loss. This heat generation in the lattice along with the photons that can be absorbed by the band gap are responsible for 47.4% of the total losses [16]. The other fundamental loss which decrease the theoretical limit to %29 is radiative and specifically Auger recombination.

![Figure 4](image)

**Figure 4** (a) Fundamental losses in the band gap: (1) Transmission; (2) thermalisation and (3) Auger and radiative recombination. (b) Technological losses in a standard p-type Si cell: Optical losses (a1) Reflection; (a2) Shading; (a3) Parasitic absorption; (b) Electronic recombination in emitter, base and at front and rear surfaces; (c) Resistive losses. Fig. (c) High-efficiency PERL cell (d). High-efficiency back-junction back contacted cell design with n-type Si base [5]

Figure 4(a) and 4(b) illustrate the fundamental loss mechanism that occurs in a solar cell. To decrease technological loss there are different method to modify a given cell while reduction of fundamental losses happens just by taking advantage of novel “next generation” technologies. Hot carrier solar cell has been introduced for reduction of thermalisation loss. [17]. In this type of cell energy selective contacts help to decrease excess photon energy before it changes to phonon in semiconductor lattice. A method to reduce transmission loss is using material with sub band gap energy level which let the phonon with lower energy than band gap gets absorbed by
semiconductor bandgap. They call this method upconversion [18] which mostly uses Er$^{3+}$ ions for this purpose. Tandem cells and photon downshifting are other approached to decrease these losses in a solar cell. Other approaches include use of photon downshifting materials or tandem cells while the feasibility of all these next generation methods is still a challenge due to high processing cost.

2.1.2 Different Recombination Loss Mechanism

There are intrinsic and extrinsic defect in Si which can produce recombination loss in the solar cell.

2.1.2.1 Radiative Recombination

Radiative recombination can be define using equation (2)

$$U^\text{total}_{\text{rad}} = \int \alpha(E) \varphi(E, \Delta\eta) dE$$

This rate shows the ability of the material in light absorption and directly depends on the spontaneous emission. Hence, this value is more important in direct bandgap material such as GaAs in comparison to Si. In equation (2), $\alpha(E)$, $\varphi(E, \Delta\eta)$, represents the absorption coefficient
and the incoming flux respectively. The net recombination rate can be achieved by subtracting the recombination which is due to thermally excited carriers.

\[ U_{rad} = \int \alpha(E) \varphi(E, \Delta \eta) dE - \int \alpha(E) \varphi(E, 0) dE \]  

\[ U_{rad} = B_{rad}(np - n_i^2) \]  

In equation (4), \( B_{rad} \) equals radiative recombination coefficient and is a property of a semiconductor and independent of carrier densities.

2.1.2.2 Auger Recombination

Another unavoidable recombination mechanism occurs due to collision between carrier within the semiconductor. In this process the carrier with excess energy will not emit photon and instead it excites an electron to a higher energy level. This electron relaxation happens by giving the its energy in the form of heat and getting back to the band gap which produce loss.

Figure 6 illustrate the two possible way for this process to happen.

![Auger Recombination Diagram](image)

Figure 6 Auger recombination is shown for both carrier interaction pathways[20]

The total Auger recombination rate, can be define using equation (5) when this interactions happen between electron and two holes.
\[ U_{Aug} = C_n(n^2p - n_o p_o) + C_p(np^2 - n_o p_o) \] (5)

where \( C_n \) (1.7-2.8 \( \times 10^{-31} \) cm\(^6\)/s), \( C_p \) (0.99-1.2 \( \times 10^{-31} \) cm\(^6\)/s) are not a function of carrier concentration and represent Auger coefficients for electrons and holes respectively. Lifetime measurement in low-injection regime as a function of doping concentration is a method to determine Auger recombination in a semiconductor [21]. This type of recombination can limit the performance of high efficiency devices and it is most effective in indirect-band gap semiconductors.

2.1.2.3 Shockley Read Hall Recombination (Recombination via defect states)

Shockley Read Hall (SRH) recombination is due to the defect level in bulk and surface of the semiconductor and is responsible for the most portion of the loss in a devised based on indirect bandgap semiconductor. Impurities inside the semiconductor, crystal lattice imperfections, and dangling bonds on the surface are the possible reasons behind these defect levels.

2.1.2.3.1 Recombination in Bulk

Impurities inside the host material along with any lattice dislocation and defect can disturb the periodic structure of a crystalline semiconductor. An electron or hole can be trapped in this defect levels. This trap levels will be located deeper in a band gap of Si as it is a group IV semiconductor but they will be placed closer to the conduction and valance band when they are due to presence of impurities from group III and VI materials.

The electron and hole recombination due to the SRH process in the semiconductor band gap can reduce effective carrier lifetime significantly in a semiconductor device. The leakage current in results of this recombination have been studied in Shockley and Read well-known paper [22], and the same results have been reported by Hall [23].
Figure above illustrates all type of SRH recombination that can happens in a semiconductor band gap.

(a) The defect level traps an electron
(b) The trapped electron can be excited to the conduction band
(c) A Hole recombine with the rapped electron
(d) The trapped electron can relax to the valance band
(c’) Electron transitioning into an unoccupied space by electron situated in the valence band.
(d’) excitation of an electron into a defect level.

Equation (6) [22] the recombination rate from all electron trapping by the defect states have been calculated.

\[ U_{e-capture} = B_n n D_{it} (1 - f_t) \]  \hspace{1cm} (6)

where \( B_n, n \) define quantum mechanical constant of the transition and electron density. While \( D_{it} \) and \( (1 - f_t) \) represent trap states density and the probability of a unoccupied defect levels. Although the capture and emission rate is different for electrons and holes, in steady state condition the net rate of electrons and holes which are trapped in defect states are equal and
therefore there is no built-up charge in traps. Considering this fact one can derive equation (7) to calculate SRH recombination rate for a single level [24].

\[ U_{SRH} = \frac{np - n_i^2}{\tau_{n,SRH}(p+p_i) + \tau_{p,SRH}(n+n_i)} \]

In the above equation \( \tau_{n,SRH} = \frac{1}{v_n \sigma_n D_{it}} \) and \( v, \sigma \) are the average thermal velocity of an electron and the capture cross section, respectively. In this equation the driving force for the recombination rate is \((np - n_i^2)\) which shows the impact of carrier injection on the recombination rate. Thus, this value can change for different defect level as they act differently to the change in injection level. For example carrier life time \( \tau_{SRH} \) is the same as \( \tau_{n,SRH} \) in a n-type semiconductor while this value equals \( \tau_{p,SRH} \) in a p-type material when the defect levels are deep and under low-injection regime [21]. To conclude the highest recombination rate can be achieved when \( n \approx p \).

### 2.1.2.3.2 Surface Recombination

The highest amount of crystal lattice mismatch in a semiconductor device would happen at the interface of the surface of two crystalline layer. Non-saturated dangling bonds and impurities give rise to continuum defect states within the bandgap of semiconductor. Integral of equation (7) over the bandgap can present the SRH recombination due to the all interface defect levels within the bandgap.

\[ \int_{E_V}^{E_C} D_{it} \frac{p_n s - n_i^2}{v_p \sigma_p (n_s + n_i) + v_n \sigma_n (p_s + p_t)} \]  

while in equation (8) variables with \( s \) subscript define carrier distributions at surfaces. Another parameter which needs to be calculated is the fundamental speed of carrier recombination at the surface. This parameter can be expressed using equation (9).

\[ S_{no} = \int_{E_V}^{E_C} D_{lt} v_n \sigma_n dE. \]
In this equation the impact of charge passivation has not been considered. Therefore, effective surface recombination velocity can be defined by equation (10) [25].

\[ S_{eff} = \frac{u_s}{\Delta n_d} \]  

(10)

Equation (9) and (10) represent that there are two different methods to decrease the surface recombination: saturation of dangling bonds at the interface which happened by introducing oxygen or hydrogen atoms to the dangling bonds (Chemical Passivation) and reduction of one type of carrier concentration significantly from the interface using an electric field (Field effect passivation). Note that this electric field can be provided by creation of a doping profile beneath the surface or utilizing dielectric layers with high amount of built-in charge.

2.1.2.4 Emitter Recombination

Non-uniform doping profile following with the dead layer after diffusion are just two reasons which makes modeling of this highly doped region complex. Different mechanisms should be considered for modeling of doped bulk and doped surfaces. This is due to variation in degeneracy, free carrier absorption and bandgap narrowing for bulk and surface. Hence, to start surface modeling we need to make some assumption which makes the calculation of \( J_0 \) easier. Considering in highly doped surfaces Auger recombination is the dominant process, the recombination lifetime is injection dependent.

\[ J_{recombination} = J_{0-emitter} \frac{np}{n_i^2} \]  

(11)

In equation (11), \( J_{0-emitter} \) is emitter saturation current density (\( mA/cm^2 \)), while \( n \) and \( p \) are electron and hole density at the base space charge region. This let us to consider the emitter a separate layer from the base space charge region and calculate the effective surface velocity using equation (12) [26].
\[ S_{\text{effective}} = I_{0-emitter} \frac{N_A + \Delta n}{q n_i^2} \]  

(12)

Which \( N_A \) in this case is the acceptor doping concentration.

Conventional multicrystalline solar cells typically have the efficiency of 15-17% while this number is 16-18% for monocrystalline cells and these numbers can be improved by implementing new technology for mass production of high efficiency solar cell which are cost effective. To decrease the production cost some researches have been done on decreasing Si wafer thickness, or reducing usage of Silver for contacts.

2.1.2 Technological Loss

Standard Aluminum Back surface field (Al-BSF) solar cell has been studied here to investigate technological losses. Figure 8 present the schematics of Al-BSF and passivated emitter rear contact(PERC)cells. The front side of Al-BSF solar cell is made of a \( p \)-type crystalline Si base and a phosphorous diffused emitter. Next step is metallization using screen printing technique and firing which let the metal punch through Si\( \text{N}_x \) antireflection coating(ACR) layer. Meanwhile Al-BSF will be formed due to Al and Si alloy at the interface of the rear side. In figure 5 the fabrication process of Al-BSF cell has been shown as well. The PERC-cell are taking advantage of passivated back side using a dielectric layer and local contact.

Recombination loss which happens in bulk, emitter, and the surface of Si is the main reason behind technological loss. Glunz \textit{et al.} proved that bulk recombination is responsible for one third of the efficiency gap[27], while another one third can be improved by developing techniques to decrease surface and emitter recombination. Another estimation by Aberle shows that \( \%25 \) of the efficiency loss is due to surface recombination loss[28].Optical loss are associated to reflection from the front surface and the shading by metallization and can be reduced by texturing or using
ARC layers and narrowing down metalized surface area. Figure 8(c) illustrate implementation of selective emitter which is an approach to enhance the surface recombination. In this method low sheet and high sheet resistance areas have been designed below the contacts and for non-contact areas, respectively. Surface passivation is more vital in non-contact area with lower doping concentration.

![Figure 8 schematic](image-url)

Figure 8 schematic (a) of Al-BSF on the left and PERC on the right (b) fabrication process of Al-BSF and PERC[5]

Resistive loss occurs due to contacts and series resistance and can be improved by using plating instead of screen printing of contacts which brings more control on contacts aspect ratio.
and lower sheet resistance[5]. Taking advantage of all these techniques can offer an excellent improvement is solar cell efficiency.

2.2 Solar Cell Efficiency Parameters

To understand the solar cell parameter roles one can model this device by the below structure.

In Figure 9 $I_L$ is photogenerated current and while $I_D$ and $I_{sh}$ are diode and shunt current, respectively. Hence if we define $I$ by equation (13)

$$I = I_L - I_D - I_{sh}$$  \hspace{1cm} (13)

We can calculate $I$ based on equation (14)

$$I = I_L - I_0 \left\{ e^{\frac{q[V+iR_S]}{m k T}} \right\} - \frac{V+iR_S}{R_p}$$  \hspace{1cm} (14)

In equation (14) $I_0$ represent reserve saturation current and $V$ is the output voltage. $R_p$ and $R_s$ are shunt and series resistance while $m$ is the diode ideality factor.

2.2.1 Short Circuit Current

Short circuit current can be calculated while there is zero voltage across the two terminals of the solar cell and it totally depends on carrier generation and extraction towards the external
circuit. Therefore, \( I_{sc} \) is the largest current possible which can be collected from the solar cell. Due to dependence of this value to carrier generation by photon absorption, any techniques which enhance the light absorption such as ARC and texturing would increase \( I_{sc} \). Besides, texturing can decrease the back reflection by increasing the angle of incident at the front surface. Figure 10 shows the mechanism of increasing total internal reflection inside the solar cell using texturing.

\[\text{Figure 10 Schematic illustration of reducing surface reflectance and increased light trapping}\]

**2.2.2 Open Circuit Voltage (\( V_{oc} \))**

At zero current the highest value for voltage for a solar cell is achievable which is known as open circuit voltage. This occurs at zero current. \( V_{oc} \) relies on \( I_L \) and \( I_0 \). Considering \( I_0 \) is a function of recombination within the cell, one way to increase \( V_{oc} \) is reduction of recombination which will increase \( I_0 \).

**2.2.3 Fill Factor**

An IdeaSl solar cell which works with the maximum power (MPP) needs to operate at highest possible voltage (\( V_{oc} \)) and current (\( I_{sc} \)). Based on MPP we can introduce another important parameter in calculation of solar cell efficiency.
\[ FF = \frac{V_{M_i}}{V_{oc,sc}} \]  

(15)

In this equation \( V_M \) and \( I_M \) are voltage and current at maximum power. FF is dependent on the resistance inside the cell due to power loss across \( R_s \) which can be calculated using equation (16)

\[ P_{loss,Rs} = \left(1 - \frac{I_M R_s}{V_M}\right) \]  

(16)

By reducing \( R_s \), FF can be achieved using equation (17)

\[ FF_{loss,Rs} \approx \left(1 - \frac{I_{sc} R_s}{V_{oc}}\right) \]  

(17)

This equation identify that \( R_s \) can reduce the cell power for preparing a new path for dark current through the cell.

### 2.2.4 Conversion Efficiency

This parameter is the ratio of the light energy which irradiate to the solar cell to the electricity which can be generated from the device. The aim for any photovoltaic device is to enhance this efficiency which can be calculated using equation below

\[ \eta = \frac{V_{oc,sc} FF}{P_{in}} \]  

(18)

\( P_{in} \) is the power of the sun under AM 1.5 G sun

Air Mass (AM) shows the impact of light absorption through the atmosphere on the solar spectrum and can be define using equation (19)

\[ AM = \sqrt{1 + \left(\frac{S}{H}\right)^2} \]  

(19)

Where \( \frac{S}{H} \) is the ratio of an object length to its height.
There is always a match between photon emission and absorption rate and that is the reason why under steady state condition electron concentration inside material does not change. The theoretical efficiency of solar cell can be calculated using this principal. Under illumination, the incident flux of photons radiate to the semiconductor can be measured by the following equation,

\[ f(E, \Delta\eta) = \frac{2\pi \frac{e^2}{\hbar^3 c^2 e^{(E-\Delta\eta)/(k_B T)}}}{e^{(E-\Delta\eta)/(k_B T)} - 1} \]  

(20)

In this equation, \( E \) and \( \Delta\eta \) represent energy of a photon and the quasi-fermi levels gap, respectively. While \( \hbar, c, k_B \) are Planck’s constant, speed of light, and Boltzmann constant. Hence using Equation (20) one can calculate the highest limit for efficiency as a function of the bandgap of the semiconductor.

Figure 11 depicts that silicon and gallium arsenide (GaAs) are located very close to the highest theoretical efficiency limit. The theoretical maximum short current density (\( J_{sc} \)) 43.85 \( mA/cm^2 \) and 29.68 \( mA/cm^2 \) for Silicon and GaAs has been calculated. While the actual value of 42.7 \( mA/cm^2 \) for Si and 31.76 \( mA/cm^2 \) for \( J_{sc} \) are not far away from the theoretical limit[29].
The reason behind the difference between theoretical and actual solar cell efficiency is technological loss process.

As it can be seen from equation (18) the maximum efficiency is dependent on $V_{OC}$ which is exponentially a function of excess carrier density. Hence by losing our carrier in recombination $V_{OC}$ drops [9, 31].

Another parameter which plays an important role in solar cell efficiency is $J_{SC}$ which can change by any variation in semiconductor bandgap. Smaller bandgap can absorb broader range of the sun spectrum. Therefore, there is a tradeoff between the optimum bandgap energy for $J_{SC}$ and $V_{OC}$. 

Figure 11 Theoretically possible solar cell efficiency as a function of material bandgap for one-sun illumination [14, 30].
CHAPTER 3- DIAGNOSTIC TECHNIQUES

3.1 Photo Conductance Decay Measurement (PCD)

To characterize recombination parameter of a solar cell or a wafer, the most effective
method is to measure the photoconductivity of the substrate or film. Bulk minority
carrier lifetime (τ) or diffusion length (L = \sqrt{\tau D}) which is directly connected to τ are the most important
recombination parameter. As we mentioned before in chapter 2, parameters such as \(J_0\), and \(S_{eff}\) that
can be calculated by \(\tau_{eff}\) are used to determine the passivation quality and can be obtained using
dynamic method. Recently, steady state photo conductance (SSPC) and quasi-steady state photo
conductance (QSSPC) have been introduced to measure this parameter.

In reality there is always a balance between recombination (R) and generation (G) of
electron-hole pair in a semiconductor (G=R).

Hence, under illumination (\(J_{ph}\)) an excess concentration of electrons and holes (\(\Delta n\))is
established. The relation between \(J_{ph}\) and \(\Delta n\) can be expressed using equation (21)

\[
\frac{J_{ph}}{qd} = \frac{\Delta n}{\tau_{eff}}
\]  
(21)

In this equation d is wafer thickness. By increasing minority and majority carrier the
photoconductivity (\(\sigma_{ph}\)) of the surface increases as it can be seen in equation below

\[
\sigma_{ph} = q(\Delta n\mu_n + \Delta p\mu_p) = q\Delta n(\mu_n + \mu_p)
\]  
(22)

By substituting equation (22) in equation (21), the effective life time can be calculated
using equation (23)

\[
\tau_{eff} = \frac{\sigma_{ph}d}{J_{ph}(\mu_n + \mu_p)}
\]  
(23)
In this equation the only parameter which is needed is the conductivity of the substrate which can easily be measured by a reference photodiode and calibrated instrument.

In Figure 12, after generation of electron–hole pairs by optical excitation, the decay of voltage will be monitored versus time. In a non-contact PCD measurement photoconductivity is measured by microwave reflection or transmission [32, 33]. In this structure a Gunn diode oscillator has used to produce 10 GHz microwaves to be focused on the wafer surface. Microwave power changes the conductivity of the substrate. For the contactless mode, microwave reflection method is used in which the photoconductivity is measured by microwave reflection or transmission [32, 33].

![Diagram](image)

Figure 12 Lifetime measurement techniques with Microwave reflectance photoconductance decay[34]

By using a light pulse which changes very slowly in comparison to the $\tau_{eff}$ of the sample the QSSPC have been utilized [35]. This method can measure photoconductivity of the sample for a wide range of illumination.

As we mentioned in chapter 2 the $J_0$ value which is also a quantity to measure the surface passivation quality can be calculated using $\tau_{eff}$.
\[
\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{Auger}}} - \frac{1}{\tau_{\text{rad}}} = \frac{1}{\tau_{\text{SRH}}} + \left( J_{0,\text{front}} + J_{0,\text{back}} \right) \frac{(N_{\text{dop}}+\Delta n)}{q\mathcal{W}n_i^2}
\] (24)

where \( N_{\text{dop}} \) is the base dopant density and \( n_i \) is the intrinsic carrier density. In this equation \( J_0, \text{front} \) and \( J_0, \text{back} \) represent the saturation current densities for the front and back emitters. \( \tau_{\text{Auger}} \) is proportional to \( \Delta n^3 \) and it can be omitted from this equation. In mid to high injection level regime emitter recombination dominates as the effect of SRH recombination is negligible. As you can see in Figure 13 Kane and Swanson observed that by plotting left side of equation versus carrier density the \( J_0 \) value in low injection regime can be obtained with enough accuracy while the substrate is a high quality, highly doped Fz wafer[36].

Figure 13 Kane’s method to extract \( J_0 \) from the slope of the inverse lifetime [37]
3.2 Corona-Kelvin Probe Measurement

Enhancing passivation quality is the main purpose of this dissertation. To quantify the passivation layers, electrical properties of passivation such as polarity, magnitude of dielectric charge and interface trap densities are as important as optical properties of the dielectric layers.

Conventional method to measure interface quality was capacitance-voltage (CV) measurement on metal-oxide semiconductor (MOS). Wilson et al introduce a non-contact corona charge method to characterize the dielectric layer interface on Si substrate [37]. Using corona charge to characterize the field effect passivation was not novel and it has been used in different studies [38] however measuring $D_{it}$ using this technique has been announced for the first time in 2011. It worth to mention that using new material such as Al$_2$O$_3$ and non-stoichiometric SiN$_x$ brought new challenges and requirement to the field of passivation characterization. The new modified corona charge is able to measure $D_{it}$ value for the high leakage dielectric such as Si rich SiN$_x$.

3.2.1 Non-Contact Corona CV

Figure 14 Vibrating Kelvin probe and corona discharge apparatus[37].
Noncontact CV method despite the traditional one, insert accurate charge dose $\Delta Q_c$ by corona discharge in air to bias the dielectric as it can be seen in Figure 14.

This charge can change the substrate voltage $\Delta V_s$ which can be measured by Kelvin probe in dark and under illumination.[37]. Kelvin probe electrode (2mm) is located close to the surface and vibrates with the frequency of 1100Hz. This vibration can create AC current which is proportional to the potential difference ($V_{CPD}$) between the electrode and semiconductor.

$$V_{CPD} = \phi_{ms} + V_{SB} + V_D$$ (25)

In this equation $\phi_{ms}$ represent metal-semiconductor work function while $V_{SB}$ and $V_D$ are semiconductor surface barrier and dielectric voltage, respectively.

Under illumination with LED, $V_{SB}$ decreases. In lightly doped Si surfaces $V_{SB}$ is a driving force to control the surface recombination. Then the corona charge changes to change $V_{SB}$ and $V_D$. This biasing is applied to the substrate by precise movement of the chuck to locate the desired location under corona discharge and then getting back to the initial location for voltage measurement. This process repeated until $V_{CPD}$ vs $Q_c$ and $V_{SB}$ vs $Q_c$ data is acquired. The electrical properties of the dielectric such as capacitance, flat band voltage, total charge, and $D$ can be extracted by this measurement. Figure below depicts the data which can be plotted after this measurement.
Figure 15 (a) Example VCPD vs QC data for SiO$_2$/Al$_2$O$_3$ stack after firing on n-type Si. (b) Example VSB vs QC data for SiO$_2$/Al$_2$O$_3$ stack after firing on n-type Si[39].
3.2.2 $D_{it}$ Spectra Determination

In general semiconductor-dielectric structure follows charge neutrality principle which can be expressed by equation below

$$Q_{it} + Q_t + Q_m + Q_c + Q_f = -Q_{SC}$$  \hspace{1cm} (26)

Where $Q_{it}$ and $Q_t$ are trapped charge at the interface and in the dielectric, respectively while $Q_f$ and $Q_m$ represent fixed and mobile charges within the dielectric layer. Considering a known value for corona charge ($Q_c$), one can calculate the space charge ($Q_{SC}$) value. Any changes in corona charge will introduce a change in $Q_{SC}$ and $Q_{it}$.

$$\Delta Q_c = -(\Delta Q_{SC} + \Delta Q_{it})$$  \hspace{1cm} (27)

Using this equation $D_{it}$ can be calculated

$$D_{it} = \frac{\Delta Q_{it}}{\Delta V_{SB}}$$  \hspace{1cm} (28)

Considering

$$V_{SB} = V_{Dark} - V_{light}$$  \hspace{1cm} (29)

$\Delta Q_{SC}$ and in result $D_{it}$ can be calculated as it can be seen in Figure 16. Normally the minimum value of $D_{it}$ in this spectra is being reported for comparison between different passivation layers.
Figure 16 Example $D_n$ spectrum for SiO$_2$/Al$_2$O$_3$ stack after firing on $n$-type Si[39].
CHAPTER 4- SURFACE PASSIVATION: TECHNIQUES AND MATERIALS

4.1 Theory and Fundamentals of Surface Passivation

Excellent surface passivation is essential to improve the efficiency of crystalline silicon (c-Si) solar cells. A dielectric passivation layer at the front and rear of the cell brings higher performance due to lower surface recombination velocities [40-44]. Good chemical passivation is achieved by the saturation of dangling bonds resulting in a decrease in interfacial trap densities ($D_{it}$). While field effect passivation decreases the surface concentration of minority carriers by repelling electrons (in p-type surfaces) or holes (in n-type surfaces) with a built in electric field coming from electrostatic charges ($Q_f$) near the silicon surface.

Solar cell devices have a high surface to volume ratio. These make them vulnerable to the effect of interface defect density. Different dielectric and dielectric stacks have been investigated for passivation of front and rear surface of solar cell[45]. Each layer can bring us surface passivation through a specific mechanism based on doping level and surface sheet resistance for diffused surfaces. Furthermore,

the quality of surface passivation is depending on their stability for thermal and UV long time exposure as well as dielectric refractive index and parasitic absorption. Worth to mention that surface treatment and cleaning prior to dielectric material deposition plays an important role in surface passivation, as well.

Silicon nitride (SiNx) is the industry standard for antireflection coatings (ARC) in c-Si solar cells, due to its appropriate refractive index and limited parasitic optical absorption. Additionally, SiNx is a very effective passivation layer [46-48] for n-type surfaces. However, it is not very
effective for p-type silicon due to the large positive $Q_f$ near the Si/SiN$_x$ interface. This positive $Q_f$ introduces an inversion layer underneath of the SiN$_x$, resulting in parasitic shunting\cite{49}. Aluminum oxide (AlO$_x$) is able to solve this problem by inducing large negative $Q_f$ near the Si/AlO$_x$ interface. Aluminum oxide is a great passivation material for p-type surfaces in high-efficiency solar cells \cite{43,50}, coming from the combination of field effect passivation (i.e., large, negative $Q_f$) and good chemical surface passivation (i.e., low $D_{it}$). Several methods of depositing AlO$_x$ have been explored, such as plasma-enhanced chemical vapor deposition (PECVD)\cite{51}, atmospheric pressure chemical vapor deposition (APCVD)\cite{12-13}, reactive sputtering\cite{52}, and atomic layer deposition (ALD)\cite{53}. It has been demonstrated that ALD AlO$_x$ offers a low $D_{it}$ in the range of $10^{11}$ eV$^{-1}$.cm$^{-2}$ at the Si surface and negative $Q_f$ in the $10^{12}-10^{13}$ cm$^{-2}$ range. The AlO$_x$/SiN$_x$ stack also exhibits a negative fixed charge density \cite{54}. This stack offers several advantages in comparison to the single layer of AlO$_x$ or SiN$_x$, such as higher chemical and thermal stability as well as enhanced internal reflectivity\cite{55}.

Here we try to investigate the passivation qualities of AlO$_x$, SiN$_x$ and the stack of AlO$_x$/SiN$_x$, as well as the effect of thermal annealing on effective carrier life time improvement. We also have studied how the growth of a thin SiO$_x$ layer, formed using ozonated deionized water, at the Si surface prior to AlO$_x$ deposition influences the effective carrier lifetime ($\tau_{eff}$) and thermal stability.
4.1.1 Surface Passivation Parameters

Surface passivation is a method to reduce electron-hole recombination at the surface. Equation (21) which is another representation of equation (7) present surface recombination from SRH equation

\[
U_s = \frac{(n_s p_s - n_i^2) v_{th} N_{it}}{\frac{n_s + n_1}{S_p} + \frac{p_s + p_1}{S_n}} = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_p} + \frac{p_s + p_1}{S_n}}
\] (30)

In the above equation \( N_{it} \) refers to interface defect density for a single defect in midgap while \( n_1 \) and \( p_1 \) are some statistical factors. \( n_i \) is the intrinsic carrier concentration and \( S_{n/p} = \sigma_{n/p} v_{th} N_{it} \). In real life defect levels have been distributed within the band gap. Thus with an integral over the band gap we can replace \( N_{it} \) with \( D_{it} \) (eVcm-2)[56]. Based on equation (7) \((n_s p_s - n_i^2)\) which shows the deviation from thermal equilibrium under illumination is the most important term in determining \( U_s \). Decreasing \( D_{it} \) for the purpose of decreasing \( U_s \) called chemical passivation. Another method is reduction of one type of carrier at the interface significantly using an electric field which is called field effect passivation[45, 57].

The effect of an electric field has been simulated by inserting total charge value of \( 2 \times 10^{12} \) cm\(^{-2} \) and its impact on the band bending of \( n\)-type and \( p\)-type Si wafer is illustrated in Figure 17.
12. Positive charge with increasing the majority carrier close to the surface of p-type wafer will take it to the accumulation while for the n-type Si wafer it would go to inversion. For both cases reduction of \( n_s \) will decrease the recombination rate at the surface but while the device is in inversion, the electron and holes density will be the same in the bulk of Si which can increase the recombination.

As we mentioned before one parameter that can be used to measure the surface passivation quality surface recombination velocity which can be achieved by equation (10). Another method to calculate this parameter is using minority carrier lifetime and using equation below

\[
\frac{1}{\tau_{\text{eff}}} = \left[ \frac{1}{\tau_{\text{SRH}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{rad}}} \right] + \frac{1}{\tau_{\text{surf}}} \tag{31}
\]

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{surf}}} \tag{32}
\]

Effective life time \((\tau_{\text{eff}})\) is depend on both bulk and surface recombination. While bulk life time is accumulation of intrinsic (Auger and radiative recombination) and extrinsic recombination (SRH). SRH in multicrystalline Si is the result of lattice fault due to some impurities such as Fe [58] or boron-oxygen in Czochralski monocrystalline Si. While in float zone Si wafer Auger and radiative recombination are more dominant in limiting the bulk life time in high injection level regime[59-61].

Using equation (22) and (23) one can deduce \( S_{\text{eff}} \) by equation (24).

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2S_{\text{eff}}}{W} \tag{33}
\]

Where \( W \) is the wafer thickness and this equation is valid for good passivation with fairly low \( S \) and in the case of higher value of \( S \) one might consider the minority carrier diffusion to the interface for more accurate calculation. Still bulk life time is an un-known value for \( S_{\text{eff}} \) calculation.
Kerr et al that has reported approximate values for this parameter [62] and Benick et al reported that $\tau_{eff}$ higher than Auger limit [63] for Kerr’s values and suggest that in real world intrinsic lifetime is higher. Hence $S_{eff}$ can be deduced from equation (25)

$$S_{eff, max} = S_{eff} = \frac{W}{2\tau_{eff}}$$  \hspace{1cm} (34)

The driving force for effective life time in very good surface passivation is intrinsic recombination and define limit for lowest possible value for $S_{eff}$ which can be attained experimentally.

Studies shows that $S_{eff}$ is a linear function of Nit (impact of chemical passivation). More over increasing $Q_f$ can decrease $S_{eff}$ by factor of two (impact of field effect passivation)[5]. Another parameter which plays an important role in determination of $S_{eff}$ is capture cross section ratio $\sigma_n/\sigma_p$. By variation of this parameter from 1 to 100 in this parameter significant change in $S_{eff}$ observed. It's been proved that for $\sigma_n/\sigma_p$ equal to 100 the highest value for $S_{eff}$ can be achieved and higher value of $Q_f$ can activate the field effect passivation.

Note that a high quality surface passivation is limited by bulk life time and hence in this case $S_{eff, max}$ does not define the real $S_{eff}$ anymore. In other word, in high level surface passivation notable variation in $Q_f$ cannot imply significant change $S_{eff, max}$.

4.2. Surface Passivation Materials

4.2.1 Silicon Oxide

The most effective passivation using thermally grown oxide has been achieve using alneal process which has been introduced by Kerr and Cuevas[62] and stayed the best passivation layer in 2000s. They achieved life time of 5.25 and 1.65 ms in 1.5Ωcm n-type and 1Ωcm p-type which resulted SRVs of 1.72 and 7 cms$^{-1}$, respectively. During alneal process a SiO2 film will be
deposited prior to deposition of 0.1 ~ 1 μm aluminum using thermal evaporation. This stack will go through annealing at 400-450 °C in a tube furnace with forming gas ambient[64, 65]. Although the advantage of this process has been proved by Kerr and Cuevas using PCD measurement for the first time, Balk had observed the effectiveness of this method for passivation earlier[66]. In this process water which is pre-exist on the surface will react to aluminum and form aluminum oxide. The result of this reaction (hydrogen) will be pushed to the interface of Si/SiO₂ and passivate the dangling bonds. With introducing charge to this layer during deposition it would be beneficial for field effect passivation as well [67]. Considering high temperature annealing and long timescale anneal process is not practical for manufacturing however the best passivated emitter rear locally diffused (PERL) cell has been fabricated using this method in UNSW laboratory [68]. Due to really low interface defect density at Si/SiO₂ interface, this dielectric has been utilized prior to other dielectric for the purpose of tunneling oxide [69] decreasing pinhole density [70], and carrier selective contact [71] applications.

4.2.2 Silicon Nitride

Plasma enhanced chemical vapor (PECVD) SiNₓ is one of the most applicable dielectric layer in PV industry. Based on the optical properties of SiNₓ it is a good candidate for ARC. Figure below shows how material composition can vary the refractive index of the film.
This figure illustrates that to take advantage of ARC properties of SiN\textsubscript{x} film on the front side of a solar cell, the refractive index of almost 2 is needed which is achievable in films with higher nitrogen content. Considering high amount of hydrogen content, SiN\textsubscript{x} can provide high bulk passivation in multicrystalline Si wafers and enhance surface passivation for monocrystalline as well [72]. While the film with higher amount of Si are more successful for surface passivation nitrogen rich film bring more thermal and chemical stability.

Nitrogen content of the film defines the dominant passivation mechanism of SiN\textsubscript{x} film. In low amount of nitrogen, the driving force is the chemical passivation as this film act as an amorphous Si. In contrast high nitrogen content owns positive fixed charge in the order of $10^{12}$ cm\textsuperscript{-2} and will produce field effect passivation[73, 74]. The positive charge due to the SiN\textsubscript{x} layer can take a $p$-type Si surface to the inversion regime. Hence by applying this film on the rear side of a $p$-type cell, the efficiency of solar cell drops due to the inversion layer shunting effect[74]. TO solve this problem SiO\textsubscript{2}/ SiN\textsubscript{x} stack has been introduced [75].
4.2.3 Al₂O₃

Recently, introduction of Aluminum oxide (Al₂O₃) to PV industry made a huge advancement in this field[53, 76, 77]. Properties of this dielectric is fundamentally different with the other conventional material which being used for surface passivation. Al₂O₃ layer contain high density of built-in negative charge [77], in contrast to silicon nitride (SiNₓ) or silicon dioxide (SiO₂) provide positive charge to the interface. This is the major difference and results using less injection level dependence on p-type surfaces[53] and avoids shunting at the rear side of PERL solar cells[42]. This dielectric delivers also the best passivation for boron-diffused p⁺-emitters as well as screen-printed Al⁺p⁺ emitters for n-type silicon solar cells [78, 79] due to reducing the interface defect density.

The refractive index of Al₂O₃ which is close to 1.65 and this dielectric wont absorb the visible part of the spectrum, so it can increase the optical properties of the front and rear surfaces. Hoex showed that this dielectric is applicable for passivation of both n-type and p-type silicon[53].

4.2.3.1 PECVD

Miayajima et al were the first group to report using PECVD Al₂O₃ for the passivation purpose[80]. They used Al(CH₃)₃, H₂, and CO₂ as precursor gases at 200°C temperature with the excitation frequency of 60MHz in a capacitively-coupled plasma system. This process then developed for an industrial inline reactor while they changed the carrier gas to Argon and the precursors to Al(CH₃)₃ and N₂O. In this system plasma produced using linear antenna by 2.45 GHz microwave pulse[81].
4.2.3.2 ALD

The reason behind ALD is to use the self-limiting surface reaction to control the deposition at the atomic level. For this purpose, alternate exposure of precursors to the substrate has been designed[82-84]

The precursors in the form of gas react to the functional group at the surface. It is called self-limiting as the reaction stops automatically when all of these surface groups react.

ALD process normally contain two precursors in gas phase which will be introduced to the surface alternatively. After reaction of the first precursor with the functional groups at the surface the excess material along with the reaction products will be pumped away. Then the second one will be introduced to the chamber. This element reacts with the newly formed groups at the surface and after the reaction the original functional group will be created. This makes the repetition of this process possible and finishes one cycle of a ALD process. Every cycle can grow one or less than one atomic of the film. This process will continue to achieve the desired film thickness that can be calculated by measuring the grow rate per cycle GRC which is normally 0.5-2 Å/cycle.

By varying each step of ALD process, sub-saturated growth, true ALD growth, or ALD growth with an additional chemical vapor deposition(CVD) observed. Increasing precursor and oxidant exposure time will not affect GPC in a true ALD process while the purging time is long enough. In this case a conformal and uniform deposition will be achieved.

Unlike some other deposition method, the GRC is not a function of precursors flux and as long as the precursor is sufficient enough to react with all the active surface groups the same amount of material will be deposited on the surface. The most famous material for Al₂O₃
deposition is trimethylaluminum (TMA) while the precursor for the oxidant can be O₂, H₂O, or O₃. Figure below shows the ALD process using water for oxidant material.

![ALD cycle schematic](image)

**Figure 19 Schematic of ALD cycle comprising two precursor dosing steps and two purge steps[5]**

Based on the different application for Al₂O₃, layer, various oxidant precursor might be applied. In general, O₂ which produced using plasma is more reactive than H₂O. Enhancement in oxidant reactivity can increase the quality of the deposited film by reduction of impurities and lowering the temperature[85]. Industrial deposition Al₂O₃ is generally possible using O₃ which bring the reactivity without need to plasma creation[86].

4.2.3.2.1 ALD Deposition Parameters

The impact of process parameter on GPC has been illustrated in Figure 20. It can be seen that in both thermal and plasma ALD the precursor pulse time will not affect the grow rate and in fact after a certain value GPC will saturate. In contrast, the purge time after introduction of each precursor affect the deposition rate. Having low purge time will give rise to GPC while decrease the film refractive index and mass density. Low purge time can also result parasitic deposition of
CVD film due to presence both precursor at the same time in the chamber which imply the non-uniformity to the film.

By decreasing the dosing time of oxidant in case of thermal ALD, a subsaturated ALD process along with an increase in refractive index has been observed. In plasma ALD process the oxidant dose time (plasma time) is more effective in changing GPC. In short plasma time subsaturated growth can be seen in Figure 20. This is due to insufficient oxygen radical to restore the initial surface functional groups (OH). In this case impurities also will be present in the film and results low refractive index. Moreover, it will destroy the film uniformity. This film also depicts that although the purging time after the oxidant does not influence the GPC in plasma ALD, it plays an important role in resulting the parasitic CVD along with the film deposition in

Figure 20 Growth per cycle (GPC) as a function of the length ALD process for (a) thermal ALD and (b) plasma ALD. The films were[50]
the cases with short purging time. In general plasma ALD provide more uniform film in comparison to thermal ALD as it can be seen in Figure 21.

![Thickness uniformity for Al₂O₃ films deposited by (a) plasma ALD and (b) thermal ALD](image)

**4.2.3.2.2 Process Temperature**

Substrate temperature plays the most important role in properties and grow rate of Al₂O₃ film using ALD. This parameter also works differently in two different type of ALD. As it can be seen in Figure 22, both the growth rate and the number of Al atom will decrease in plasma ALD in higher temperature. This happens due less surface coverage with OH groups will be resulted at higher temperature. This behavior is slightly different in thermal ALD and increasing the substrate temperature until 250°C will increase the GPC and after this temperature it will drop. This non-similarity arises from the different response of reactivity of plasma and H₂O to the temperature. Considering the significant increment in purge time after H₂O which is needed in low temperature of thermal ALD, plasma is more beneficial for deposition of Al₂O₃.
4.2.3.2 Influence of Process Parameters on the Passivation Quality

Process parameters have significant effect on the quality of passivation as it can be seen in Figure 23. Note that designing a true ALD mode for deposition process is not necessary to have a high performance passivation layer. In fact, reducing TMA purging time will increase GPC drastically without reduction in passivation quality[5].
4.3 Annealing to Activate the Passivation

The annealing effect on passivation mechanism varies based on different types of ALD. Annealing will increase $Q_f$ for the case of thermal ALD and reduce $D_i$ when the layer has been deposited by plasma ALD. Both ALD processes will result low $D_i$ along with high $Q_f$ after annealing.

Figure 24 illustrates that thermal ALD in general shows lower value of $Q_f$ in comparison to plasma ALD. Although after $T>300$ °C the $Q_f$ has increased, this value is independent of temperature for values higher than 400 °C. 

Figure 23 Influence of ALD Al$_2$O$_3$ process parameters on refractive index $n$, growth per cycle GPC and maximum surface recombination velocity $S_{eff,max}$. The passivation properties were evaluated on both p- and n-type c-Si wafers, for thermal and plasma ALD processes, before and after annealing [5]
As it can be seen in Figure 25 symmetrical lifetime samples were fabricated using 5Ω·cm
-type Cz Si wafers with a 200 µm thickness. All wafers received an RCA clean, followed by a dip
in hydrofluoric (HF) acid, and then the growth of a ≈1-2 nm SiO$_x$ layer using ozonated deionized

4.4 Experiment Details

Figure 24 Negative fixed charge density $Q_f$ vs annealing temperature. for plasma and thermal ALD Al$_2$O$_3$ films. $Q_f$ was determined from C–V measurements.

<table>
<thead>
<tr>
<th>Surface preparation and cleaning (DiO$_3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dilute HF Dip</td>
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<tr>
<td>Oxide Growth using ozonated deionized water</td>
</tr>
<tr>
<td>Deposition of two different passivation layer (ALD deposition of AlOx or PECVD deposition of SiNx)</td>
</tr>
<tr>
<td>Activating Passivation by Annealing at 450°C in N2</td>
</tr>
</tbody>
</table>

Figure 25 process flow for cleaning and surface passivation
water. Passivation layers were then deposited directly onto a group of the SiO\textsubscript{x} coated wafers. Other wafers went through an additional HF dip and ozonated deionized water rinse just before the deposition of the passivation layer(s).

For the passivation layers, three different experimental groups were used: (1) SiN\textsubscript{x} only; (2) AlO\textsubscript{x}; and (3) AlO\textsubscript{x}/SiN\textsubscript{x} stack. For the SiN\textsubscript{x} group, an 80 nm layer of SiN\textsubscript{x} was deposited using PECVD at a temperature of 300\textdegree C with a SiH\textsubscript{4}/NH\textsubscript{3}/N\textsubscript{2} ratio of 250/5/25. For the AlO\textsubscript{x} group, ALD (Cambridge Savanah 100) was used to deposit 15 nm Al\textsubscript{2}O\textsubscript{3} at a temperature of 200\textdegree C. This process is split up into two self-limiting reactions consisting of trimethylaluminium (TMA) exposure until it is saturated. The deposition rate is only 0.09 nm/cycle and a very thin layer of AlO\textsubscript{x} can be achieved using this technique. The AlO\textsubscript{x}/SiN\textsubscript{x} stack was fabricated using the same processes described above sequentially.

The samples were annealed at various temperatures (300-450\textdegree C) in a tube furnace with N\textsubscript{2} ambient for 30 minutes. The injection-level dependent $\tau_{\text{eff}}$ was measured at each step using a Sinton Instruments WCT-120. The highest $\tau_{\text{eff}}$ and lowest saturation current density ($J_0$) were achieved with either the 425\textdegree C or 450\textdegree C anneal for different samples.

The electrical properties and surface passivation of the samples were measured by means of corona-voltage measurements (SemilabSDI PV-2000). Corona charging is a contactless method which induces an electric charge on the silicon surface to change the electric field in the dielectric film and the semiconductor itself. The surface band bending on silicon wafer will be varied and thus the flat-band voltage ($V_{fb}$) can be attained when there is no band bending observed[37, 88].

4.4.1 Results and Discussion

It can be observed in Figure 21 that passivation quality is enhanced upon annealing, leading to a higher $\tau_{\text{eff}}$. Thermal annealing under certain condition is critical for full activation of field-
effect passivation. This can be attributed to local reconstruction of the AlO$_x$ which increases the negative built-in potential and hydrogen diffusion from SiN$_x$ or AlO$_x$ bulk to the interface and provides chemical passivation.

Table 1 Effective carrier life time and current density for 6 various

<table>
<thead>
<tr>
<th></th>
<th>$\tau_{\text{eff}}$ ($\mu$Sec)</th>
<th>$J_0$ ($10^{-15}$A/cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiN$_x$</td>
<td>490</td>
<td>38.5</td>
</tr>
<tr>
<td>SiO$_x$/SiN$_x$</td>
<td>1391</td>
<td>15.5</td>
</tr>
<tr>
<td>AlO$_x$</td>
<td>516</td>
<td>5.5</td>
</tr>
<tr>
<td>SiO$_x$/AlO$_x$</td>
<td>1818</td>
<td>7.5</td>
</tr>
<tr>
<td>AlO$_x$/SiN$_x$</td>
<td>1033</td>
<td>9.5</td>
</tr>
<tr>
<td>SiO$_x$/AlO$_x$/SiN$_x$</td>
<td>2991</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 1 shows the best value that has been achieved for $J_0$ and $\tau_{\text{eff}}$ of each samples after annealing.
The result shows that all samples that have the ozonated SiO$_x$ provide a $\tau_{eff}$ that is more than two times higher than the same wafers where the oxide has been removed. Hence, the stack of SiO$_x$/AlO$_x$/SiN$_x$ with ~3 ms of $\tau_{eff}$ and $16.3 \times 10^{15}$ A/cm$^2$ of $J_0$ depicts the best results in this contribution. The effective life time versus the injection level for this sample can be seen in Figure 27. It depicted the effective life time is high and almost independent of the injection level.
Figure 27 Carrier effective lifetime versus injection level

Figure 28 is a comparison of $Q_c$ and $D_d$ for between all samples while figure illustrates the interface state defect density ($D_d$) versus voltage, and charge ($Q_c$) versus voltage for each sample. As we expected, AlO$_x$ provided the highest amount of negative charge density equal to $4.7 \times 10^{12}$ q/cm$^2$, while the stack of SiO$_x$/ AlO$_x$/SiN$_x$ has a negative charge density of $3.8 \times 10^{12}$ q/cm$^2$. It is due to the compensation of the negative charge of the AlO$_x$ layer with the positive charge that the SiN$_x$ layer provides. Obviously, this stack brings the lowest interface defect density among these samples which is $4.49 \times 10^{11}$ q/cm$^2$ eV and confirms the effective carrier lifetime results.
The average value for $Q_f$ and $D_{it}$ for each samples has been shown in figure below.

Figure 28 Interfacial state density versus substrate voltage (a), and charge versus substrate voltage (b) for 6 different samples.
In this section we have studied three different passivation techniques, SiN$_x$, AlO$_x$, and the stack of AlO$_x$/SiN$_x$. SiN$_x$ deposition was achieved by using PECVD, for the deposition of the AlO$_x$, an ALD system has been utilized. For all three groups, the effect of the presence of the ozonated oxide has been examined. Effective carrier Lifetime and corona-voltage measurement have been performed to investigate the passivation quality and electrical properties of these layers.

Figure 29  
(a) Interfacial state density  
(b) total charge for all 6 samples

In this section we have studied three different passivation techniques, SiN$_x$, AlO$_x$, and the stack of AlO$_x$/SiN$_x$. SiN$_x$ deposition was achieved by using PECVD, for the deposition of the AlO$_x$, an ALD system has been utilized. For all three groups, the effect of the presence of the ozonated oxide has been examined. Effective carrier Lifetime and corona-voltage measurement have been performed to investigate the passivation quality and electrical properties of these layers.
The highest $\tau_{\text{eff}}$ of $\sim$3mSec belongs to the stack of AlO$_x$/SiN$_x$ in presence of ozonated oxide underneath of the stack. The lowest $D_{it}$ among these 6 samples is $4.49 \times 10^{11}$ q/cm$^2$ eV, which belongs to the same sample and is compatible with the lifetime results.
CHAPTER 5- A NOVEL SURFACE CLEANING APPROACH

Semiconductor surface clean is sometimes perceived as costly but long recognized as pivotal in determining the final semiconductor device performance and yield. In this contribution, we investigated the effectiveness of crystalline silicon surface cleaning by a simple UV-ozone process in comparison to the industry standard RCA clean for silicon photovoltaic applications. We present a unique method of processing the silicon surface effectively by UV-ozone cleaning. Despite being simple, UV-ozone cleaning results in a superior surface passivation quality that is comparable to high-quality RCA clean. When used as a stack dielectric—UV-ozone oxide overlaid by aluminum oxide—the thickness of UV-ozone oxide plays an important role in determining the passivation quality. Of all treatment times, 15 min of UV-ozone treatment results in an outstanding passivation quality, achieving the effective carrier lifetime of 3 ms and saturation current density of 5 fA/cm\(^2\). In addition, we present a simple and effective technique to extract values of electron/hole capture cross-section for the purpose of analyzing the interface passivation quality from already measured surface recombination parameters of saturation current density, interfacial trap density and total fixed charge, instead of measuring on the separately prepared metal-insulated-semiconductor (MIS) samples by the techniques: frequency-dependent parallel conductance or deep-level transient spectroscopy.

5.1 Background

Semiconductor surface clean is sometimes seen as a costly process as it consumes a significant amount of chemical resources and waste disposal. In addition, it is perceived as not playing much part in building device structures, film deposition and contact formation. However, it is accepted that an effective surface cleaning leads to improved device performance. Over the years, various types of crystalline silicon (c-Si) wafer cleaning sequences have been applied, based
on the mixture of NH₄OH+H₂O₂, HCl+H₂O₂ and HF [89]; plasma etch [90], plasma treatment for small-geometry devices [91], chlorine cleaning [92] and hydrogen peroxide as an oxidant in the chlorine cleaning [93] to remove photoresist, contaminants, particles, organic/inorganic impurities and native oxide on the silicon wafer surface. Wafer cleaning chemistry, based on hot alkaline and acidic hydrogen peroxide solution—called RCA (Radio Corporation of America) standard clean—has been the primary method of cleaning in the microelectronic industry [94]. RCA standard clean includes the mixture of NH₄OH/H₂O₂/H₂O, referred as SC-1, and HCl/H₂O₂/H₂O, referred as SC-2. SC-1 removes the organic contaminants, while inorganic contaminants are removed by SC-2. Ultraclean deionized water is used for intermediate and final rinses after SC-1 and SC-2, respectively [89]. However, the SC-1 was found to cause the surface damage, due to micro-roughness formed by NH₄OH [95]. A new candidate, named “IMEC-Clean” to potentially replace the RCA clean was later introduced, enabling near-perfect removal of metallic particles [96]. The IMEC-Clean includes a mixture of H₂SO₄/H₂O₂, followed by a 1% diluted HF. The use of H₂SO₄/H₂O₂ mixture was also demonstrated in the development of Nanowire Solar Cells to increase the conversion efficiency [97]. Development of interdigitated back contact (IBC) silicon solar cells was also enabled by a cost-effective cleaning mixture of H₂O/NH₃/H₂O₂ with various chemical concentrations and different cleaning temperature. Recently, the application of ozone in wet and dry semiconductor surface cleaning processes has gained significant attention. Ozone has been extensively used in waste and swimming pool water treatment, water purification, medical sterilization, odor control and many other industries, due to its strong oxidizing ability. A reliable ozone generation based on the dielectric barrier discharge was first developed by Werner Siemens in 1857 [98-100]. Since then it has become the standard ozone generation technique in many industries including water treatment and semiconductor processing. Chen discussed benefits and
applications of ozonated deionized water (DI-O_3) for wafer surface preparation in detail [101]. DI-O_3 research has already been reported by a number of groups [102-104]. Bakhshi et al. also demonstrated the use of DI-O_3 in surface preparation prior to the application of single or stacked dielectric layers such as SiN_x, AlO_x, and AlO_x/SiN_x. This has resulted in the outstanding surface passivation achieving the saturation current density _J_0 of 8 fA/cm^2 (per side) [105]. In addition to wet ozone cleaning, dry ozone cleaning based on the exposure of ultraviolet radiation is less complicated to operate and is effective in removing a wide variety of contaminants from surfaces. The ability of UV ozone in removing the organic layer such as photoresist polymer was reported as early as 1972 [106]. In 1974 Sowell et al. presented the UV cleaning of adsorbed hydrocarbons from glass and gold surfaces, in air and vacuum environment [107]. Also, in 1974 John Vig and his team also described through a series of experiments that UV-ozone cleaning is capable of producing clean surfaces in less than a minute [108]. Chemically cleaned silicon surfaces (such as after HF process) are at risk of particle contaminations and absorption of hydrocarbon from the ambient air, organic resists, etc.; therefore passivating c-Si surface with a protective coating such as UV-ozone oxide significantly reduces contaminations and hydrocarbon absorptions [109]. Studies have shown that UV-ozone oxide treatment leads to a significant reduction of carbon content in the subsequently grown dielectric films [110, 111]. Moldovan et al. also presented the use of UV-ozone to remove fingerprints and glue on the c-Si wafer surface, and that conditioning 70 Ω/□ boron diffused layer with UV-ozone and passivating it with AlO_x/SiN_x stack achieved an emitter saturation current density of 49 fA/cm^2 [112]. The benefits of UV ozone have also been realized in organic photovoltaics. The use of UV-ozone to treat the ultrathin aluminum to form an alumina interlayer—between the active layer and indium tin oxide (ITO)—has been presented to improve electron extraction [113]. Treating the (zinc oxide–poly vinyl pyrrolidone (ZnO-PVP)
nanocomposite film used as an electron tunneling layer with UV ozone also improves the charge collections in dithienogermole–thienopyrroloiodine-based polymer solar cells [114]. Besides the electron tunneling layers, treating the hole collection layer such as molybdenum trioxide (MoO₃) with UV ozone improves the surface morphology, transmittance and film quality [115]. Also, UV-ozone was demonstrated to change the highest occupied molecular orbital (HOMO) level of Phenyl-C61-butyric acid methyl ester (PC₆₁BM) [116]. In this paper, we present a novel method of cleaning the silicon surface by the UV-ozone technique in comparison to the industry standard RCA clean for application in silicon photovoltaics. We also employ a thin UV-ozone oxide (UVo) as an interface dielectric layer prior to the passivation of aluminum oxide (AlOₓ) on c-Si samples. A deposition time of UVo interface dielectric was varied to optimize the passivation quality. We demonstrate that UVo technique is capable of providing both effective surface cleaning and outstanding passivation quality on c-Si silicon samples. In addition, we present a simple method to extract capture cross section values from already measured parameters of saturation current density J₀, interfacial trap density Dᵢ and total fixed charge Qₜₒₜ.

5.2 Material and Methods

Planar 1-5 Ω.cm n-type 250 μm Cz wafers were used in this contribution. Saw damage silicon etch was processed in Tetramethylammonium hydroxide (TMAH) at 90 °C, removing approximately 1 μm of silicon per minute. Effective carrier lifetime τₑffective and J₀ (per side) were measured using the transient photoconductance (PCD) decay technique at the excess carrier densities of 1×10¹⁵ and 5×10¹⁵ cm⁻³, respectively. The measurement of J₀ at regions where the excess carrier densities greater than the substrate doping maximizes the range of carrier lifetime’s linear dependence on the carrier density, thereby distinguishing the surface from the bulk effects for the improved accuracy of J₀ analysis. J₀ is determined by the relation of J₀ =
\[
\frac{q W n_i^2 (\Delta n + N_d)}{2} \left( \frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk}}} \right),
\]
where \( q \) is the electronic charge, \( W \) is the thickness of the silicon sample, \( n_i \) is the intrinsic carrier concentration, \( N_d \) is the bulk dopant concentration of the silicon sample, \( \tau_{\text{eff}} \) is the effective minority carrier concentration and \( \tau_{\text{bulk}} \) is the intrinsic bulk lifetime of crystalline silicon parameterized by Richter et al [117]. Carrier lifetime represents bulk and surface recombination. Symmetrically passivated samples were used for measurement of \( \tau_{\text{eff}} \) and \( J_0 \). RCA cleaning used a mixture of NH\(_3\):H\(_2\)O\(_2\):H\(_2\)O 1:1:5 and HCl:H\(_2\)O\(_2\):H\(_2\)O 1:1:5 for the first and second cleaning step, respectively. UV\(_o\) growth took place in JetLight 30 UV-ozone generator. In the ozone generator contaminant molecules and ozone absorb the short wavelength UV of 253.7 nm, and excite and simultaneously dissociate molecular oxygen at the wavelength of 189.9 nm. The photosensitized oxidation process happens when contaminant molecules react with atomic oxygen and so desorb from the surface. Recent technologies have made ozone cleaning process an extremely economical approach in both laboratories and industry. Using this technique, we have formed a thin layer of SiO\(_x\) on our samples. Dielectric layers (SiO\(_x\), AlO\(_x\), and RCA oxides) were removed in dilute (10\%) HF prior to re-passivation. The thickness of UV\(_o\) (or thin SiO\(_x\)) and AlO\(_x\) were measured by spectral ellipsometry (M-2000 J.A. Woollam) in a range of wavelength between 250 nm and 1200 nm. The measured signals are fitted using the Cauchy model. Based on the model, UV\(_o\) oxides with the thickness of 1.5 nm, 1.7 nm, and 1.8 nm were achieved for 10 min, 15 min, and 20 min of process time, respectively. Deposition of AlO\(_x\) was by thermal atomic layer deposition (Cambridge NanoTech Savannah 100 ALD) with the deposition rate of 0.088 nm/Cycle at 200°C. Annealing of UV\(_o\)/AlO\(_x\) passivated samples was processed in the nitrogen ambient at 450°C for 30 min. A contactless capacitance-voltage (C-V) measurement technique using PV2000 Semilab SDI instrument was used to characterize \( D_{lt} \) and \( Q_{tot} \). PV2000 tool dispenses charges on
dielectric surface and measures surface voltage with vibrating Kelvin probe. Unless otherwise stated, $D_n$ and capture cross section $\sigma_n$ (or $\sigma_p$) reported in this contribution represent the values near the midgap. $D_n$ and $Q_{tot}$—based on the contactless CV measurement—have the measurement uncertainty of 2% and 1%, respectively; while $\tau_{eff}$ and $J_0$ have the reported uncertainty of 3% [118, 119]. Finally, nano-scale interface characterization was carried out with the help of transmission electron microscopy (TEM). For this purpose, cross-sectional TEM specimens were prepared by focused ion beam (FIB) milling technique using a FEI 200 TEM FIB. High-resolution TEM (HRTEM) images were obtained with the help of FEI Tecnai F30 TEM system at an operating voltage of 300 KV with a point-to-point resolution of 0.2 nm.

5.3 Results and Discussions

First, n-type Cz $\langle 100 \rangle$ 1-5 $\Omega$-cm samples were processed in TMAH to remove saw damage, followed by cleaning them in RCA solutions to make the surface hydrophobic. Post-TMAH processed samples have resulted with $\sim 180$ $\mu$m in thickness. Half of the samples were deposited with AlO$_x$ having the thickness of 10-15 nm, while the rest were deposited with a very thin UVo (10 min of deposition) overlaid by the AlO$_x$ of 10-15 nm. All samples were then annealed in N$_2$ ambient, followed by the PCD measurement. As shown in Figure 30, the sample deposited by the UVo/AlO$_x$ stack has notably improved $\tau_{eff}$ (i.e., 1554 $\mu$s compared to 1019 $\mu$s) and $J_0$ (7 fA/cm$^2$ compared to 11 fA/cm$^2$) than that by AlO$_x$ alone. The passivation quality in terms of an effective surface recombination velocity, $S_{eff}$ of the sample passivated by AlO$_x$ only in this experiment is 8 cm/s, somewhat comparable the published result of 5 cm/s [120]. $S_{eff}$, in this contribution and published literature [120], is determined by the ratio of the wafer thickness to two times the $\tau_{eff}$, assuming an infinite bulk lifetime time, and thus represents the upper limit. Typically, AlO$_x$ effectively passivates the $c$-Si surface by the combination of chemical passivation and field
effect passivation, reducing the interface defect density and concentration of minority carriers near the surface, respectively [120]. While field effect passivation of AlOₓ is driven by high negative built-in charge, the chemical passivation is owing to the interfacial SiOₓ layer, grown intrinsically during the AlOₓ deposition and annealing [121].

Figure 30 Comparison of τₑff and J₀ (inset figure) between samples passivated by AlOₓ and UV₀/AlOₓ stack.

The results in Figure 30 shows that high-quality interfacial layer such as UV₀ provides a superior passivation than the SiOₓ, which was grown intrinsically during the deposition and anneal of AlOₓ.

Figure 31 shows HRTEM images of samples deposited by AlOₓ only and UV₀/AlOₓ stack. As in Figure 31a, the SiOₓ grown intrinsically during the AlOₓ deposition has the thickness of 1-2
nm, which is in accordance with the published results [120, 122]. However, SiO$_x$, having a relatively higher thickness of $\approx 4$ nm is observed in case of the sample subjected to UVo followed by deposition of AlO$_x$ by ALD. (see Figure 31b). This can be attributed to oxygen diffusion into Si during UV ozone treatment resulting in the formation of SiO$_x$ interlayer, which further grows during the deposition of AlO$_x$ by ALD. The relatively higher thickness of SiO$_x$ in case of UVo deposited sample leads to improved surface passivation performance of the UVo/AlO$_x$ stack, as compared to the AlO$_x$ only.

To investigate whether UVo technique can be used as an effective surface cleaning technique, in comparison to the industry standard of RCA clean, an experiment was carried out by subjecting the saw-damage etched $n$-type low-resistivity sample to the 15 min of UVo growth on both sides of the sample. This sample was named as 1st UVo sample. Another saw-damage etched $n$-type sample was subjected to cleaning in RCA1 and RCA2 solutions, with dipping in dilute HF before and after RCA2, and then growing 15 min of UVo on both sides of the sample. To determine

![HRTEM images of samples deposited with AlOx only (left figure) and with UVo/AlOx (right figure).](image)

(a) (b)

Figure 31 HRTEM images of samples deposited with AlOx only (left figure) and with UVo/AlOx (right figure).
the effectiveness of surface cleaning, both RCA-and the 1st UVo-cleaned samples were then deposited with AlO$_x$ (10-15 nm). Following the AlO$_x$ deposition, samples were subjected to N$_2$ anneal and $J_0$ was extracted from the PCD measurement. $J_0$ of RCA cleaned sample was found to be lower than the 1st UVo sample (i.e., 5 fA/cm$^2$ versus 10 fA/cm$^2$ in the Figure 32). Assuming the infinite bulk lifetime, RCA cleaned samples have achieved the $S_{eff}$ of 3 cm/s—an equivalent to the published result [120]. The 1st UVo sample was then dipped in dilute HF to make the surface hydrophobic, followed with the process of growing and removing UVo (15 min) on the same sample and repeating these for another two times. These samples were named as 2nd UVo and 3rd UVo samples. Deposition of AlO$_x$ and N$_2$ anneal was included after each UVo growth to assess the effectiveness of surface cleaning by the UVo. As shown in Figure 32, subsequent deposition and removal of UVo have reduced $J_0$ further to 7 fA/cm$^2$ and 5 fA/cm$^2$, respectively, which have become comparable to that of the RCA cleaned sample. This improvement in $J_0$ is likely due to an effective oxidation of c-Si surface by the UVo technique and removal of UVo to make the c-Si surface free from contaminants. AlO$_x$ deposition and N$_2$ anneal included after each UVo clean were just to assess the incremental improvement of post-UVo surface clean. A separate experiment for the sample processed with the UVo clean (i.e., deposit UVo and strip in HF) for three times, without AlO$_x$ and N$_2$ anneal showed the same reduction in $J_0$. This experiment demonstrates that UVo clean aided by HF dip to remove the contaminants in the grown oxides can be used as an effective cleaning technique—an attractive alternative to the standard RCA cleaning, as it uses less chemicals for the surface clean and also alleviates the negative effects of contaminants that could exist in the SiO$_x$-AlO$_x$ interface.
Results in the aforementioned section demonstrate that in addition to providing the effective cleaning, UVo can be used in conjunction with passivation dielectric (e.g., AlO\textsubscript{x}) to provide superior surface passivation. A further investigation was carried out when a thicker UVo was used. Saw damage etched n-type low-resistivity samples were grown with UVo for 10 min, 15 min, and 20 min, respectively; followed by deposition of 10-15 nm of AlO\textsubscript{x} and N\textsubscript{2} annealing. The PCD measurement was undertaken to extract \( J_0 \) and \( \tau_{\text{eff}} \). As seen in Figure 33, an increased thickness of UVo (i.e., from 10 min to 15 min) have reduced the \( J_0 \) from 7 fA/cm\textsuperscript{2} to 5 fA/cm\textsuperscript{2}. However, an additional increase of UVo deposition time longer than 15 min has resulted in a significantly increased \( J_0 \) of 21 fA/cm\textsuperscript{2}. Possible reasons for this could have been due to (1) the increased thickness of UVo has diminished the field passivation effect of shielding the minority

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Figure 32 Auger-corrected inverse \( \tau_{\text{eff}} \) (\( \Delta n \)) of samples following RCA clean (1 & 2) and UVo clean (1\textsuperscript{st}, 2\textsuperscript{nd}, and 3\textsuperscript{rd}). Inset of Figure 3 indicates the cleaning sequence of samples that went through RCA and UVo clean.
carriers from the interface between c-Si surface and UVo, and/or (2) degradation of film passivation quality owing to prolonged UV exposure. \( \tau_{\text{eff}} \) of samples (see inset of Figure 33) deposited with different UVo deposition times follow the same trend as the \( J_0 \).

A nondestructive corona/Kelvin probe measurement (contactless C-V) was then used to further characterize the interface passivation quality of the UVo/AlO\(_x\) stack [123, 124]. The contactless C-V technique is used to determine interface defect density near midgap (\( D_{it} \)), which indicates how well the dangling bonds are passivated, and total fixed negative charge (\( Q_{\text{tot}} \)), which establishes the electric field that in turn minimizes the minority carrier concentration near the surface, thereby reducing the recombination [125]. Figure 5 shows the dependence of \( J_0 \) on the interface parameters of \( D_{it} \) and \( Q_{\text{tot}} \) of samples grown with UVo of different thicknesses (1.5, 1.7...
and 1.8 nm). As shown in Figure 5, of all deposition times the sample with UVo of 1.5 nm have resulted in the lowest $D_{it}$. Increasing the thickness of UVo from 1.5 nm to 1.7 nm has sharply increased the $D_{it}$ by about two-fold, but the $D_{it}$ increase was saturated with further increasing the thickness of UVo to 1.8 nm. The increase of $D_{it}$ as a result of increasing the deposition time of UVo (i.e., from 1.5 nm to 1.7 nm) is likely due to the degradation of the film quality at the expense of prolonged UV exposure. However, further investigations are required to determine why the $D_{it}$ increase is saturated beyond 1.7 nm of UVo thickness. $Q_{tot}$, on the other hand, has barely changed (i.e., $-3.0 \times 10^{12}$ and $-3.4 \times 10^{12}$) between the UVo thickness of 1.5 to 1.7 nm, but notably when the UVo thickness was increased beyond 1.7 nm. $J_0$ was also observed to notably follow the trend of $Q_{tot}$ with respect to changes in the UVo thickness. C-V results in Figure 34 indicate that $Q_{tot}$, rather than $D_{it}$, apparently determines the passivation quality of UVo/AlO$_x$ stack. The following section further quantifies if the surface passivation of the n-type c-Si by the UVo/AlO$_x$ is dominated by $Q_{tot}$ or $D_{it}$. 
An effective surface recombination can be determined by two parameters: effective surface recombination velocity $S_{\text{eff}}$ and surface saturation current density $J_0$. A detailed discussion has been presented by McIntosh et al. [126] that $J_0$ is a superior metric, compared to $S_{\text{eff}}$, to quantify the surface passivation for undiffused silicon, since for the c-Si at 300 K in low-injection $J_0$ is independent of surface dopant concentration $N_s$ when the surface charge $Q^{1.85}/N_s$ is greater than $1.5 \times 10^6$ cm for the inversion. This boundary condition is analogous to the experimental conditions in this contribution. The relationship of $J_0$ to the $D_{it}$ and $Q_{\text{tot}}$ derived from [126] is given as:

$$J_0 = qS_{\text{no}}^2 kT \varepsilon_{Si} n_{ie}^2/\epsilon^2$$

(35)

where $q$ is the electron charge, $T$ is the temperature at Kelvin, $S_{\text{no}}$ is the surface recombination parameter of electrons, $n_{ie}$ is the effective intrinsic carrier concentration, $\varepsilon_{Si}$ is the

Figure 34 Dependence of $J_0$, $D_{it}$, and $Q_{\text{tot}}$ of samples grown with UVo of 1.5, 1.7 and 1.8 nm, respectively. $D_{it}$ and $Q_{\text{tot}}$ have the measurement uncertainty of 2% and 1%, respectively, based on non-contact CV measurement; while $J_0$ has the uncertainty of 3%.
permittivity of silicon, and $Q \, (q/cm^2)$ is the charge within the semiconductor that is invoked to balance the sum of the charge in the insulator and at the insulator–semiconductor interface. $S_{n0}$ can be presented as:

$$S_{n0} = v_{th,n}D_{it}\sigma_n$$  \hspace{1cm} (36)

where $v_{th,n}$ is the thermal velocity of electrons, $\sigma_n$ is the capture cross section of electrons, and $D_{it}$ is the defect density at midgap. $\sigma_n$ and $D_{it}$ in the equation are assumed as independent of energy. Parameterization of $J_0$ and $S_{n0}$ can be found elsewhere [126]. Equations (35) and (36) can be used to determine the dependence of $J_0$ on $S_{n0}$ and $Q_{tot}$, but $\sigma_n$ is unknown and needs to be determined first. Generally, metal-insulator-semiconductor (MIS) structures can be measured either by the frequency-dependent parallel conductance [127] or time-domain capacitance transients using deep-level transient spectroscopy (DLTS) [128] to determine $\sigma_n$ (or $\sigma_p$).

Preparation of MIS structures requires quite a number of process steps such as growing the insulation oxide (~10 nm of SiO$_2$ or thicker) on low resistivity (~1 Ω-cm or less) silicon substrate, single-sided removal of SiO$_2$, deposition of aluminum (~500 nm or thickness) on the SiO$_2$ and applying indium gallium (InGa) eutectic paste on the silicon to form contacts. Here, we present the alternate method of determining $\sigma_n$ (or $\sigma_p$) values from already measured surface recombination parameters of $J_0$, $D_{it}$, and $Q_{tot}$, without the need to prepare MIS structures separately. Reorganizing the equations (35) and (36), $\sigma_n$ (or $\sigma_p$) can be written as:

$$\sigma_n = J_0 \frac{Q^2}{2kTq} v_{th,n}D_{it} \varepsilon_{Si} n_{ie}^2.$$  \hspace{1cm} (37)
An analogous equation can be derived for $\sigma_p$. In equation (37) $J_0$, $D_{it}$ and $Q_{tot}$ are values extracted from photoconductance and contactless $C-V$ measurements, respectively, while the rest ($k$, $T$, $q$, $v_{th,n}$, $E_{Si}$ and $n_{ie}$) are known constant values; therefore $\sigma_n$ can be determined. Figure 6 shows the comparison between $\sigma_n$ (see B-1, B-2 and B-3) extracted by the equation (37) and reported in the literature (A [129], C [130], D [131] and E [132]). As in Figure 6, both $\sigma_n$ extracted and reported in the literature are found to be comparable, only with some variations; which is not uncommon, based on the fact that measurement uncertainties (an order of magnitude [121, 129]) exist with extracting $\sigma_n$ (or $\sigma_p$) on typical MIS structures, and extracted $\sigma_p$ (or $\sigma_p$) values depend on the normalized surface potential $\nu_s$ at which the measurement is made, thereby resulting in the significant error in $\sigma_p$ (or $\sigma_p$) as a result of the error in determining $\nu_s$ [129]. By employing the
extracted $\sigma_p$ (or $\sigma_p$) in the equations (35) and (36), the relationship of $J_0$ to $D_{it}$ and $Q_{tot}$ can be determined that $Q_{tot}$ has a significant influence than $D_{it}$ to $J_0$, due to its inverse of square $Q_{tot}$ relationship to $J_0$. Additionally, as measured $D_{it}$ values are low or moderate, $J_0$ is strongly related to the concentration of charge $Q_{tot}$ in the dielectric layer [133].

Using the equation (37), $\sigma_n$ of AlO$_x$ deposited n-type sample—discussed in Figure 1—was further determined following the measurement of $D_{it}$ ($7.5 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$) and $Q_{tot}$ ($-4.8 \times 10^{12}$ cm$^{-2}$) by the contactless CV measurement technique. In comparison to $\sigma_n$ of UVo/AlO$_x$ stack, $\sigma_n$ (2.7\times10^{-15}$ cm$^2$) of AlO$_x$ deposited sample is at least 1.5 times higher, which additionally explains the improved passivation quality attained by the UVo/AlO$_x$ stack.

5.4 Conclusion

We presented a novel method of employing the UVo technique to effectively clean the c-Si surface. Not only is the UVo technique relatively simple and inexpensive, it provides an effective cleaning efficiency, comparable to the industry standard RCA clean technique, despite consuming less chemicals. In addition to the effective surface cleaning, UVo provides the outstanding chemical passivation to reduce $D_{it}$. Passivation quality was found to vary with UVo thickness. When capped with AlO$_x$, 15 min of UVo processing time was found to be optimum, resulting in the $\tau_{eff}$ of 3 ms, $J_0$ of 5 fA/cm$^2$, $D_{it}$ of 6.2\times10^{11}$ eV$^{-1}$cm$^{-2}$, and $Q_{tot}$ of 3.3\times10^{12}$ cm$^{-2}$. We also identified that the relationship of $J_0$ to $Q_{tot}$ is the inverse of square $Q_{tot}$, while that to $D_{it}$ is linear; as a result, the passivation quality of UVo/AlO$_x$ stack on the c-Si is largely dependent upon $Q_{tot}$ rather than $D_{it}$. In addition, the technique we presented to extract comparable $\sigma_n$ (or $\sigma_p$) from already measured surface recombination parameters of $J_0$, $D_{it}$ and $Q_{tot}$ offers a simple and less-time consuming mean to the existing techniques of extracting $\sigma_n$ (or $\sigma_p$) from the separately prepared MIS structures, for the purpose of analyzing the interface passivation quality.
Implementation of unique surface clean techniques and passivation capabilities of UVo demonstrated in the contribution could lead to further improvement in surface cleaning and passivation quality, and they have emerged as potential low-cost alternatives to standard RCA clean in the photovoltaics industry.
CHAPTER 6-RECOMBINATION PARAMETERS FOR TEXTURE AND DIFFUSED SURFACES

6.1 Texture Surfaces

To increase light capturing and trapping Si surface texturing has been added to the manufacturing process. Between all various techniques which have been known for surface texturing, using KOH as a buffered alkaline etchant to form the upright random pyramids has been considered to be used in industry for monocrystalline silicon [134].

Formation of these pyramids will increase the silicon surface about 37% of the original surface [32, 134] which increase the recombination, although this is not the only reason behind larger recombination rate after texturing. The number of dangling bond in <111> surfaces is higher than <100> and the interface defect density increases by having pyramids due to mechanical stress at the dielectric-silicon interface [134]. Baker and McIntosh proved that the impact of this reason in recombination can be taken into account by multiplying $j_0$ by a scaling factor [135-137].

In this chapter of the dissertation the dielectric passivation layer that has been characterize in chapter 4 and 5 applied on the texture surfaces as well. These substrates are 180 nm thick Cz $<100>$ $n$-type wafers. They have been textured and 5, 10, and 15 min UVo oxide have been grown on these samples. At the end they have been capped with 15 nm of AlO$_x$ to passivate the surface. PCD measurement has been done and $J_0$ value of 4, 9, 9.5 fA/cm$^2$ have been achieved, respectively. Figure 36(a) depicts how saturation current changes according to thickness of the oxide while Figure 36 (b-d) illustrate $\tau_{eff}$ for these samples using PL imaging.
As it can be observed in this figure having 5 nm UVo underneath of our passivation layer for textured surfaces bring more uniformity regarding to $\tau_{eff}$.

6.2 Diffused Surface Passivation

The main goal of diffusion layer formation is separating charge. Considering a p-type Si wafer, the front surface needs to be a n+ region which happens by phosphorous diffusion (Figure 37 (a)). This layer can transport electron and acts as an electron selective contact. In this layer the
concentration of electrons is higher than holes and results a huge asymmetry between electron and hole conductivities as it can be seen in Figure 37(c).

![Figure 37 n+pp+ silicon solar cell band diagram(a) in equilibrium and (b) at the maximum power point (c) The electron and hole conductivities at the maximum power point [138]](image)

although increasing the phosphorous concentration to the highest possible amount \((10^{20} \text{ cm}^{-3})\) is desirable, it can impact electronic properties of the device by narrowing the band gap and increasing three particle Augur recombination[139, 140]. This phenomenon can decrease the selectivity of this region due to the induction of holes to the n+ region while it reduces the blue response of the device[141].

The other reason behind this diffused region is reduction of contact resistance between metal and the absorber region of the semiconductor. There is always a potential barrier between the metal work function and the semiconductor. to cope with this potential trough tunneling effect high concentration of phosphorous is needed [142]. By implementing a high concentration of phosphorous very close to the surface (junction depth of 0.2-0.3 mm), the contact resistivity decreases along with reduction in the absorption of ultraviolet and blue light and reasonable blue response is maintained [143]. Note that high concentration of diffused layer is vulnerable to increase the recombination within the semiconductor which can be limited by taking advantage of surface passivation layers.
Metal contact on the front surface is another parameter which needs to be considered in determination of phosphorous concentration. Normally Metal contact can cover only 5% of the front surface due to their shading effect. Hence, the diffused layer should provide lateral transport of the collected carriers towards the contacts on the front surface. For this purpose, high concentration of phosphorous is desirable.

Considering the negative impact of high concentration of diffused layer in carrier separation, bulk and surface recombination while it is vital for having the lateral electron transport, makes the determination of the concentration for this n+ region complicated [138].

The phenomenon where the metal impurities such as iron, nickel, chromium, etc, diffuse from bulk to the diffused region called gettering. These impurities do not affect the device performance while they are in this region and so gettering is another benefit of having a diffused layer on the surface[144, 145].

Preparation of a phosphorous diffused layer usually occurs in a quartz tube in presence of phosphorus oxychloride (POCl\(_3\)) gas in the N\(_2\) ambient. A small amount of O\(_2\) helps with the formation of phosphorus–silica glass on the wafer surface. This glass layer helps the diffusion process of dopant in to the wafer at high temperature (760-850°C). After removing the glass layer in HF the sheet resistance of 50-100 Ω/□ can be achieved by etching the surface in TMAH.

6.2.1 Experimental Detail

Planar High resistivity 100 Ω.cm n-type 290 µm Cz wafers were used in this contribution. Phosphorus and Boron diffusion have taken place for these wafer in a tube furnace and the sheet resistance of 20 Ω/□ and 22 Ω/□ have been achieved for phosphorous and boron diffused samples.
respectively. To tune the sheet resistance of these samples to a desired one they have been treated in TMAH at different temperature and for various time. Table 2 shows the sheet resistance of different treatment parameter.

Table 2 sheet resistance for Phosphorous samples after etching them in TMAH at 50 °C, and Boron samples that have been etched at 65 °C and 70 °C

<table>
<thead>
<tr>
<th>@ 50°C</th>
<th>Phosphorous</th>
<th>Time</th>
<th>SR(Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3 min</td>
<td>71</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>4 min</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>3:30 min</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>3:45 min</td>
<td>120</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T=65°C</th>
<th>Boron</th>
<th>Time</th>
<th>SR (Ω/□)</th>
<th>Time</th>
<th>SR (Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>9 min</td>
<td>30</td>
<td>3 min</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td>8 min</td>
<td>112</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>10 min</td>
<td>high</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>8:30 min</td>
<td>146</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Saw damage silicon etch was processed in Tetramethylammonium hydroxide (TMAH) at 90 °C, removing approximately 1 μm of silicon per minute. Effective carrier lifetime $\tau_{eff}$ and $J_0$ (per side) were measured using the transient photoconductance (PCD) decay technique at the excess carrier densities of $1 \times 10^{15}$ and $5 \times 10^{15}$ cm$^{-3}$, respectively. The measurement of $J_0$ at regions where the excess carrier densities greater than the substrate doping maximizes the range of carrier lifetime’s linear dependence on the carrier density, thereby distinguishing the surface from the bulk effects for the improved accuracy of $J_0$ analysis. $J_0$ is determined by the relation of $J_0 = \frac{qWn_i^2(\Delta n+N_d)}{2} \left( \frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}} \right)$, where $q$ is the electronic charge, $W$ is the thickness of the silicon sample, $n_i$ is the intrinsic carrier concentration, $N_d$ is the bulk dopant concentration of the silicon sample, $\tau_{eff}$ is the effective minority carrier concentration and $\tau_{bulk}$ is the intrinsic bulk lifetime of
crystalline silicon parameterized by Richter \textit{et al} [117]. Carrier lifetime represents bulk and surface recombination. Symmetrically passivated samples were used for measurement of $\tau_{\text{eff}}$ and $J_0$.

For surface cleaning we have followed the cleaning process that has been explained in chapter four which contains three times of UVo cleaning and HF dip. UVo growth took place in JetLight 30 UV-ozone generator. Using this technique, we have formed a thin layer of SiO$_x$ on our samples. Dielectric layers (SiO$_x$, AlO$_x$, and RCA oxides) were removed in dilute (10\%) HF prior to re-passivation. As before 15 min of UVo has been deposited on these samples followed by deposition of AlO$_x$ by thermal ALD (Cambridge NanoTech Savannah 100 ALD), PECVD deposition of SiN$_x$ and stack of AlO$_x$/SiN$_x$. Annealing of UVo/AlO$_x$ passivated samples was processed in the nitrogen ambient at 450°C for 30 min.

6.2.2 Results and Discussion

Figure below depicts the $J_0$ value for three different diffusion concentration having different sheet resistance. As it can be seen in Figure 38 increasing sheet resistance results reduction in $J_0$ value which is due to less boron atoms which acts as recombination centers. Although higher sheet resistance is favorable in regards to leakage current, it will increase contact resistivity in presence of metal contacts.
We have discussed that there is always a tradeoff between the low contact resistivity and low $J_0$. Hence, we always try to keep the resistivity between 50-150 $\Omega$/sq. In this figure sample with sheet resistance of 112 $\Omega$/sq does not follow the trends and it shows higher value of $J_0$ (38 fA/cm$^2$) in comparison to 146 $\Omega$/sq (31 fA/cm$^2$). To investigate the reason behind this data we have done photo luminescence imaging for these samples. This characterization method defines the spatial distribution of recombination centers both in surface and bulk and it helps us to understand the uniformity of our passivation by giving us the lifetime value on the whole area of the sample.

According to the results in Figure 39 the PL image of this outlier data also shows less uniformity along with less effective lifetime value. This approach is beneficial to investigate why the $J_0$ does not follow the same trends as other samples.

Figure 38 $J_0$ of three Boron diffused samples with various sheet resistance

![Graph showing $J_0$ vs Excess Carrier Density](image-url)

We have discussed that there is always a tradeoff between the low contact resistivity and low $J_0$. Hence, we always try to keep the resistivity between 50-150 $\Omega$/sq. In this figure sample with sheet resistance of 112 $\Omega$/sq does not follow the trends and it shows higher value of $J_0$ (38 fA/cm$^2$) in comparison to 146 $\Omega$/sq (31 fA/cm$^2$). To investigate the reason behind this data we have done photo luminescence imaging for these samples. This characterization method defines the spatial distribution of recombination centers both in surface and bulk and it helps us to understand the uniformity of our passivation by giving us the lifetime value on the whole area of the sample.

According to the results in Figure 39 the PL image of this outlier data also shows less uniformity along with less effective lifetime value. This approach is beneficial to investigate why the $J_0$ does not follow the same trends as other samples.
The same experiment has been conducted for phosphorous diffused samples and the $J_0$ value of different samples has been reported in the figure below. For these samples, a decrease in sheet resistance leads to a higher $J_0$ value. It is important to note that in this experiment, the sample with a sheet resistance of 160 $\Omega/\square$ does not follow the trend, and the PL images of these samples show how bulk non-uniformity of this sample increases the leakage current for this specific samples.

Figure 39: Boron diffused PL image capped with AlO$_x$ layer after SiO$_x$ growth
The \( \tau_{eff} \) effective life time of these four samples measured by PCD techniques shows values of 1.7, 2.8, 2.9, 1.6 ms for samples with contact resistivity of 71, 90, 120, 160 \( \Omega/\text{Sq} \) respectively. Although we expected to observe the largest \( J_0 \) value for the sample with sheet resistance of 71 \( \Omega/\text{Sq} \) it can be seen that according to the low bulk life time for 160 \( \Omega/\text{Sq} \) sample, the highest \( J_0 \) belongs to this sample. PL images of this samples can been seen in Figure 40.
In the next step, both PCD and PL imaging for boron and phosphorous diffused samples have been performed while these samples have been passivated by the stack of SiN$_x$/AlO$_x$ and SiN$_x$. Note that for all deposited passivation layer a thin layer of UVo-Oxide has been grown prior to passivation. The results for PL images of boron and phosphorous sample passivated by the stack of SiN$_x$/AlO$_x$ have been illustrated in Figure 42 and Figure 43 respectively. The $J_0$ extracted from PCD measurement has been shown in Table 3.

Figure 41 Phosphorous diffused PL image capped with AlO$_x$ layer after SiO$_x$ growth

71 $\Omega$/Sq  

160 $\Omega$/Sq

90 $\Omega$/Sq  

120 $\Omega$/Sq

$4.196E+4$  

$2.256E+4$

$3.5E+4$  

$1.8E+4$

$3E+4$  

$1.6E+4$

$2.5E+4$  

$1.4E+4$

$2E+4$  

$1.2E+4$

$1.5E+4$  

$1E+4$

$5000$  

$6000$

$537.5$  

$8000$

$5$  

$10$

$4E+4$  

$1E+4$

$5E+4$  

$2E+4$

$779.2$  

$1E+4$

$6.315E+4$  

$6.234E+4$

$5.375$  

$578.6$

$2.2679$  

$7537.9$

$35173$  

$23523$
Figure 42 Boron diffused PL image capped with AlOₓ/SiNₓ layer after SiOₓ growth

Figure 43 Phosphorous diffused PL image capped with AlOₓ/SiNₓ layer after SiOₓ growth
In table below we have shown the results of the PCD measurement for stack of SiN$_x$/AlO$_x$ and SiN$_x$ for all diffused samples.

Table 3 Saturation current density and effective lifetime for Phosphorous and Boron diffused samples capped with SiN$_x$ and AlO$_x$/SiN$_x$

<table>
<thead>
<tr>
<th>Sheet Resistance Ω/□</th>
<th>Boron</th>
<th>Phosphorous</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>80</td>
<td>112</td>
</tr>
<tr>
<td>$J_0$ (fA/cm$^2$) SiN$_x$</td>
<td>450</td>
<td>500</td>
</tr>
<tr>
<td>AlO$_x$/SiN$_x$</td>
<td>32</td>
<td>38</td>
</tr>
<tr>
<td>$\tau_{eff}$ (ms) SiN$_x$</td>
<td>0.3</td>
<td>0.2</td>
</tr>
<tr>
<td>AlO$_x$/SiN$_x$</td>
<td>2.6</td>
<td>1.6</td>
</tr>
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</table>
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