Digital Control Of Half-Bridge Dc-Dc Converters With Current Doubler Rectification

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DIGITAL CONTROL OF HALF-BRIDGE DC-DC CONVERTERS WITH CURRENT DOUBLER RECTIFICATION

by

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B.S. Zhejiang University, 2003

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in the Department of Electrical & Computer Engineering in the College of Electrical and Computer Science at the University of Central Florida Orlando, Florida

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ABSTRACT

DC-DC power converters play an important role in powering telecom and computing systems. Complex systems, including power electronics systems, are increasingly using digital controllers because of the major advancements in digital controllers and DSP as well as their ability to perform sophisticated and enhanced control schemes. In this thesis, the digital controller is investigated for DC-DC converters in high current low voltage applications.

For an optimal design of a regulated DC-DC converter, it is necessary to derive a valid model. The current doubler rectified half bridge (CDRHB) DC-DC converter is suitable for high current low voltage applications. In this thesis, the topology operations are analyzed and then the unified state space model, analog small signal model and digital small signal model are derived. Then the digital compensator design is discussed as well as the analog-digital converter (ADC) and the digital pulse-width-modulator (DPWM) design rules. In addition, voltage driving optimization is proposed for the benefit of the digital controller. Finally, experimental results based on the CDRHB are presented and analyzed.
This document is dedicated to God, my parents.
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# TABLE OF CONTENT

CHAPTER ONE: INTRODUCTION ........................................................................................................... 1  
1.1 DC-DC Converter ......................................................................................................................... 1  
1.2 Controller for DC-DC Converter ................................................................................................. 7  
    1.2.1 Analog Controller for DC-DC Converter ............................................................................... 8  
    1.2.2 Digital Controller for DC-DC Converter ............................................................................... 9  
1.3 Thesis Chapter Synopses ........................................................................................................... 13  

CHAPTER TWO: HALF BRIDGE DC-DC CONVERTER WITH CURRENT DOUBLER RECTIFIER ........................................................................................................... 14  
2.1 Topology and Operation .............................................................................................................. 15  
2.2 Unified State Space Model for HB Converter with Current Doubler Rectifier .. 17  
2.3 Unified Analog Small Signal Model for HB Current Doubler Converter .................. 20  
2.4 Unified Digital Small Signal Model for HB Current Doubler Converter .............. 21  

CHAPTER THREE: DIGITAL CONTROLLER FOR SWITCHING POWER CONVERTER ..................................................................................................................... 27  
3.1 Digital Compensator Design .................................................................................................... 29  
    3.1.1 Digital Redesign Approach ................................................................................................. 29  
    3.1.2 Digital Direct Design ......................................................................................................... 38  
3.2 A/D Converter ........................................................................................................................... 40  
    3.2.1 A/D Converter Requirement ............................................................................................ 42  
    3.2.2 A/D Converter Architectures .......................................................................................... 42  
3.3 Digital Pulse Width Modulator .................................................................................................. 45  
    3.3.1 DPWM Requirements ....................................................................................................... 45
3.3.2 DPWM Generation Schemes ................................................................. 46

CHAPTER FOUR: DIGITAL VOLTAGE DRIVING OPTIMIZATION................... 51

4.1 Introduction ......................................................................................... 51
4.2 DVO Implementation ........................................................................ 55
4.3 Initial Experimental Results .............................................................. 57

CHAPTER FIVE: EXPERIMENTAL RESULTS AND ANALYSIS .................. 64

5.1 Experimental Results ........................................................................ 64
5.2 Consideration and Analysis ............................................................... 70
5.2.1 Noise Issue .................................................................................... 70
5.2.2 Frequency Limitations ................................................................. 71
5.2.3 Synchronization ........................................................................... 71

CHAPTER SIX: CONCLUSION ................................................................. 73

6.1 Summary ......................................................................................... 73
6.2 Future Work .................................................................................... 74

LIST OF REFERENCES ............................................................................. 75
LIST OF FIGURES

Figure 1.1 Typical block diagram of a linear regulator power supply ......................... 2
Figure 1.2 Block diagram of a switch mode power supply with multiple outputs ........ 3
Figure 1.3 Non-isolated DC-DC topologies ................................................................. 4
Figure 1.4 Block Diagram of conventional PWM isolated DC-DC converters .......... 5
Figure 1.5 Various types of rectifier topologies .............................................................. 6
Figure 1.6 Examples of isolated DC-DC topologies ......................................................... 7
Figure 1.7 Typical switching power converter architecture with analog controller .... 8
Figure 1.8 Typical switching power converter architecture with digital controller .... 10
Figure 2.1 Half bridge DC-DC converters with current doubler rectifier ............... 16
Figure 2.2 Operation modes ................................................................................... 17
Figure 2.3 Bode diagrams of three converter models ............................................... 25
Figure 2.4 Close loop gain of theoretical design .......................................................... 26
Figure 2.5 Close loop gain of experimental result ....................................................... 26
Figure 3.1: Typical switching power converter architecture with digital controller ... 28
Figure 3.2 Digital compensator design flow chart ......................................................... 29
Figure 3.3 Block diagram for analog PID compensator design .................................... 31
Figure 3.4: Frequency warping effects of bilinear and LDI discretization methods ... 33
Figure 3.5: Frequency warping effects comparison ...................................................... 34
Figure 3.6: Bode plots comparison .............................................................................. 37
Figure 3.7: MatLab simulation results of the designed closed-Loop converter using both analog and digital discretized controllers ......................................................... 38
Figure 3.8 Close loop gain of theoretical design ............................................................ 40
Figure 3.9 Close loop gain of experimental result................................................................. 40
Figure 3.10 A/D converter model ............................................................................................ 41
Figure 3.11 Bode diagram of zero order hold......................................................................... 41
Figure 3.12 The ADC resolution effect on output .................................................................... 42
Figure 3.13 A/D converter flash architecture........................................................................... 43
Figure 3.14 ADC successive approximation registers architecture ........................................ 44
Figure 3.15 ADC pipelined with multiple flashes architecture................................................. 44
Figure 3.16 Limit Cycle Phenomenon........................................................................................ 46
Figure 3.17 Fast clocked DPWM ............................................................................................ 47
Figure 3.18 Tapped delay line DPWM ..................................................................................... 48
Figure 3.19 Hybrid delay line/counter DPWM ....................................................................... 49
Figure 3.20 Ring oscillator MUX DPWM ............................................................................... 49
Figure 3.21 DSP based DPWM ............................................................................................... 50
Figure 4.1 Typical MOSFET datasheet characteristics curves ............................................. 53
Figure 4.2 DVO close loop algorithm flowchart ..................................................................... 56
Figure 4.3 Efficiency vs. Driving Voltage Curve Showing VDO’s Operation Process.... 57
Figure 4.4 Digital controller block diagram ........................................................................... 58
Figure 4.5 Variable driving voltage supply schematic for initial experiment....................... 58
Figure 4.6 Output voltages of variable driving voltage supply and DSP input signals .... 61
Figure 4.7 DVO initial open loop experiment ......................................................................... 63
Figure 5.1: The primary and secondary gate signals with 100ns dead time in a symmetrical case.................................................................................................................. 65
Figure 5.2: The gate signals with 100ns dead time in an asymmetrical case, the signals are
complementary signals with controlled dead time............................................................... 66

Figure 5.3: The primary signals with 100ns dead time in a DCS case ....................... 67

Figure 5.4: The output voltage with significant noise .................................................. 68

Figure 5.5: Close loop diagram with power stage and DSP controller ....................... 68

Figure 5.6: The output voltage 1.5 volt and gate signal with 0.26 duty cycle at steady state with a DSP controller (digital PI compensator) in symmetrical case ....................... 69

Figure 5.7: The transform primary current ................................................................. 69

Figure 5.8: The transform primary current, gate and drain-source signals of the low-side switch .................................................................................................................. 70
LIST OF TABLES

TABLE 2-1 Transfer Functions for Analog Controlled Half Bridge Current doubler Converters with Different Control Schemes................................................................. 20

TABLE 2-2 Transfer Functions for Digital Controlled Half Bridge Current doubler Converters with Different Control Schemes................................................................. 24

Table 3-1 Discretization Methods........................................................................................................... 31

Table 3-2 Simulation Results Comparison ............................................................................................. 38
CHAPTER ONE: INTRODUCTION

Power control schemes have been revolutionized over the past few decades. Compared with analog controllers, the digital controller is gaining more attention because of its stable performance, flexibility, and ability to handle more complicated control techniques.

The advent of programmable digital signal processors (DSP) is creating thriving opportunities in the field of power electronics. The special architecture and high performance of DSP make it possible to implement a wide variety of control and measurement algorithms at a high sampling rate and reasonable cost. Power electronics systems are typically a complex combination of linear, nonlinear and switching elements. High-frequency converters add another dimension of complexity because of their fast dynamics.

Modern power electronics systems, therefore, demand the use of high-speed data-acquisition and real-time control. High performance DSP could meet these processing requirements imposed by such systems.

1.1 DC-DC Converter

DC-DC converters are used in power electronics systems that convert system voltages from one DC level to another DC level.

Today DC-DC switching power converters are very popular and prevailing in power supply systems market. Prior to 1970s, a majority of commercially available power supplies were of linear regulator type. Figure 1.1 shows a typical block diagram of
a linear regulator power supply [1]. The front end of the linear regulator is a 60 Hz transformer, \( T_1 \), used to provide input electrical isolation and to step up or step down the line voltage, and this is followed by a full-wave bridge rectifier to convert the AC input to a DC input.

![Typical block diagram of a linear regulator power supply](image)

**Figure 1.1** Typical block diagram of a linear regulator power supply [1]

by adding a large filtering capacitor at the input of the linear regulator. The input to the linear regulator, \( V_{in} \), is unregulated DC and cannot be used to drive the load directly. Using a linear circuit that provides a stable DC output regulates the DC voltage at the output, \( V_o \). The linear regulator are simple to use and provide tight control, good output voltage ripples and a low components count, but their main disadvantage for practical use is high power loss, hence, low power efficiency.

In the early 1970s, DC-DC switch mode converters entered the market. Because
of high power efficiencies compared with linear regulators, they gradually replaced traditional linear regulator power supplies for medium and high power applications. Unlike linear regulators, switching converters use power semiconductor devices to operate in either the on-state (saturation or conduction) or the off-state (cutoff or no conduction). Since either state will lead to low switching voltage or low switching current, it is possible to convert DC to DC with higher efficiency using a switching regulator. Figure 1.2 shows a simplified block diagram for a switched mode AC-to-DC power converter with multi-output application. Compared with the block diagram of Fig. 1.1, a switching network and high frequency output electrical isolation transformer $T_2$ are added.

![Figure 1.2 Block diagram of a switch mode power supply with multiple outputs](image)

The DC-DC switching converters can be classified as either non-isolated or
isolated converter, depending on whether high frequency transformers are added between the power stage and output. The non-isolated converters have three basic topologies: buck, boost and buck-boost. There are also some other high order non-isolated topologies: CUK, SEPIC and ZETA. All non-isolated topologies are shown in Figure 1.3.

The output voltage of non-isolated DC-DC topologies is determined by the duty ratio $D$. For the application with high input voltage level and low output level, the converters must operate with very small duty cycles and asymmetrical transient responses.
As a result, transformers are added in DC-DC switching converters and therefore becoming isolated DC-DC topologies.

The conventional isolated PWM DC-DC converter structure is shown in Figure 1.4, which consists of three parts: PWM converter, isolated transformer and rectifier. The PWM converter behaves as an inverter to generate AC voltage or current which is applied to the transformer primary winding. The transformer delivers AC voltage or current from the primary side to the secondary side and provides electrical isolation. With a transformer turns ratio, the converter may work at a desirable duty cycle and achieve good efficiency. AC voltages or currents are delivered to the transformer’s secondary side, and through the rectifier, a DC voltage can be obtained from the output. Hence, the procedure in energy processing in a DC-DC converter is: dc→ac→transformer→ac→dc.

![Figure 1.4 Block Diagram of conventional PWM isolated DC-DC converters](image)

PWM converters, like the one shown in Figure 1.4, can be realized in a variety of state-of-the-art topologies, such as forward, flyback, two-switch forward, push pull, half
bridge, and full bridge. The rectifier topologies can be forward rectifier, center tapped, full bridge and current doubler rectifier as shown in Figure 1.5. Figure 1.6 shows the isolated DC-DC topologies.

Figure 1.5 Various types of rectifier topologies

(a) Forward rectifier                         (b) Center-tapped rectifier

(c) Full-bridge rectifier                   (d) Current-doubler rectifier

Figure 1.5 Various types of rectifier topologies

(a) Forward converter                (b) Flyback converter
The objective of DC-DC converters is to deliver a stable and regulated DC output voltage from an unregulated DC input voltage. The pulse width modulation (PWM) regulation method is used in switching converters, which controls the on time of the power switch devices to regulate the DC output voltage.

Based on the implementation of the PWM control method and compensator, the controller can be classified as either an analog controller or a digital controller.
1.2.1 Analog Controller for DC-DC Converter

A typical switching power converter is shown above in Fig. 1.7 [2]. An analog control system provides output voltage regulation by comparing a scaled representation of the output voltage to a reference voltage and amplifying the difference. The “error voltage”, applied to an analog Pulse Width Modulator, results in a variable width driving pulse that has an average value equal to the desired output voltage. After power amplification by the power stage, driving pulses are averaged by the filter to yield a DC output voltage.

As a closed loop system, this circuit requires a control mechanism to insure that the gain around the loop (from output sensing back to the filter) does not exceed unity at any frequency where phase shift around the loop reaches 360 degrees. In addition to the built-in 180 degrees phase shift necessary for regulation, the phase shift around the control loop is also caused by delays introduced by reactive elements (capacitors or inductors) and to a smaller degree by operational delays in amplifiers, modulators, and
switching devices.

Adjustments, or compensations, for gain variation and phase shift over a range of frequencies is usually incorporated into error amplifier circuitry to assure that the circuit will be stable when operating under anticipated conditions.

Isolation between input and output may be included in the design, but even with isolation, conceptually; most power converters operate as shown in Figure 1.7.

It is possible to incorporate digital devices, such as “micro-controllers”, into an analog control system like that of Fig. 1.7. A microprocessor control unit (MCU) can be set up to adjust and manage operation of an analog PWM (change switching frequency, for example) but that sort of control is still classified as an analog controlled DC-DC switching converter. Digital controlled switching converters are classified as a control system in which the feedback process is managed entirely by digital techniques. Specifically, the PWM functions, error signals, and compensator functions are performed in digital mode.

1.2.2 Digital Controller for DC-DC Converter

A digital control system, equivalent to that in Fig. 1.7, is depicted in Fig. 1.8 [2]. Notice that voltage sensing, compensator and pulse width modulator functions are still present but appear under different names. Power switching, scaling, and filtering functions are exactly the same as in the analog design shown in Fig. 1.7.

Working back from the power switching stage, the Digital Pulse Width Modulator (DPWM) performs the same drive signal generation function as its analog counterpart. However, it does so by “calculating” and then “timing” the desired duration of ON and
OFF periods of its output signal. In contrast, the analog PWM usually operates by triggering ON at a clock transition and triggering OFF when a fixed voltage “ramp” reaches a pre-set trip voltage. The distinction is important because it leads to many of the advantages and challenges associated with digital control.

Located before the DPWM, is a “control law” processor. Typically a PI or PID style subsystem is used to perform the task of translating a digital representation of output voltage into pulse duration (duty-cycle) information used by the DPWM. It is the job of the PID control element to center the output voltage on a pre-set value and adjust the pulse width, in real-time, to provide voltage regulation. It must do so by compensating for gain and phase-shift factors around the control loop, as seen in the analog version. In digital systems, there are additional phase shift factors arising from time delays in processing the control data stream. The major gain and phase-shift factors present in an analog system (mostly from the output filter), are also present in digital mode, with calculation and A/D conversion delay factors added.

Figure 1.8 Typical switching power converter architecture with digital controller [2]

Moving farther upstream, an Analog-to-Digital (A/D) converter produces digital
data that represents output voltage. Each binary “word”, containing upwards of 8 bits of data, is sent at a high clock rate to the PID control law processor. Word length and A/D reference voltages set the precision to which the output voltage can be maintained. In digital systems, analog quantities such as voltage, must be represented as a range of discrete values. Spacing between values, or the size of each “bucket”, is set by the number of data bits divided into the total range of voltage over which the A/D conversion stage operates.

The digital controlled switching power converters have the following advantages over traditional analog controlled converters [2-11]:

- Generate flexible power switch drive waveforms with programmable relationships to one another
- Implement sophisticated control laws
- Potential space saving and less component counts
- Offer Precision that can counter the effects of component tolerance, parametric drift, aging, etc.
- Adapt to changing environmental conditions
- Store data for operational purposes and/or record keeping
- Communicate with the external digital world.

However, the digital controllers have their own disadvantages: high resolution is a must to satisfy the converter tight regulation requirements and high speed is also a must in order to satisfy the converter dynamic requirements [7-8] [11]. These two requirements results in cost increase.

Generally, there are several implementation approaches for digital controllers today, which include Microprocessor/DSP’s (Digital Signal Processors), FPGA (Field Programmed Gates Array) and Custom IC. The features of these approaches are
compared as follows:

**DSP:**

• DSP chips can be reprogrammed;

• The speed is generally slower than ICs;

• Implementation is exceedingly complex for the intended application;

• DSP is costly over custom IC design;

• High frequency power converters have to use high performance DSP;

**FPGA:**

• FPGA can be programmed on site;

• The processing is faster than a general purpose DSP;

• For FPGA design there is no physical manufacturing step, which results in very short design time;

• FPGA’s typical price is higher than DSP;

**Custom IC Design:**

• Due to physical design consideration, Custom IC’s typically have better performance than FPGA;

• However it results in much longer design time than FPGA since there is a layout step;

• Custom IC design has lower price than FPGA and DSP.
1.3 Thesis Chapter Synopses

Chapter Two analyzes the topology and operation of the half-bridge DC-DC converter with current doublers. The unified state space model, analog small signal model, and digital small signal model are developed respectively.

Chapter Three discusses digital control, which includes the theory, methodology and digital compensator design. In addition, digital controller design examples are given for different digital compensator design approaches. Also the introduction about the ADC, DPWM, and design requirements are covered in this chapter.

Chapter Four introduces the voltage driving optimization (VDO)’s background, implementation, and initial experimental results.

Chapter Five provides and analyzes the experimental results of the closed-loop DSP controlled half-bridge DC-DC converter. It also includes practical issues for DSP-based controller design on the platform discussed. Finally, the conclusion of future work will be presented in chapter six.
CHAPTER TWO: HALF BRIDGE DC-DC CONVERTER WITH CURRENT DOUBLER RECTIFIER

To further increase the processing speed and decrease the power consumption in VLSI (Very Large Scale Integration) circuits, the operating voltages of ICs keep decreasing with operation current increasing. So the study on isolated DC-DC topology, suitable for low voltage high current applications is a must.

Among four rectification topologies shown in Figure 1.5, current doubler rectifier (CDR) can minimize secondary winding \( \text{rms} \) current and have a good utilization of the transformer. Since around half of the load current flows through each output inductor, it has better thermal management for the output inductors. Moreover, the current doubler rectifier can step down more voltage than full bridge and center tapped rectifiers. In addition, CDR minimizes the numbers of high current interconnections that simplify secondary side layout and further reduces layout-related losses. Therefore, current doubler rectification is very suitable for low voltage high current applications [12-13].

For the half bridge (HB) topology, the voltage rating of switching devices is half that required by push-pull and forward converters. In addition, HB has efficient use of transformer core and copper, and the leakage inductance energy can be recycled to the input capacitors. Due to the input bridge capacitors, HB has an additional 1/2 voltage step-down ratio as compared with forward, flyback, push-pull and full bridge, from the line voltage to the transformer primary side. For the primary
topology of isolated DC-DC converters, Half Bridge is good a candidate for low voltage applications. Since current doubler rectifier can be used with half bridge topology, the half bridge DC-DC converter with current doubler rectifier is a suitable isolated DC-DC switching converter topology for high current low voltage applications [14].

For an optimal design of a regulated current doubler rectified half bridge (CDRHB) DC-DC converter, it is necessary to derive a valid small signal model.

In this chapter, the operation and control schemes of half bridge topology with current doubler rectifier is analyzed. Based on this analysis, the topology’s unified state-space model, unified small signal analog model, and unified small signal digital model are developed respectively.

### 2.1 Topology and Operation

Figure 2.1 shows the half bridge DC-DC converter topology with current doubler rectifier. There are two conventional control schemes for the HB DC-DC converters, which are symmetric control and asymmetric (complimentary) control [33-35]. Each of these two control schemes has its own advantages and disadvantages. When the conventional symmetric control is used for the half-bridge converter, its two switches operate at hard-switching with symmetric components stresses, while when the asymmetric (complimentary) control is used, the two half-bridge switches operate at soft-switching, but unfortunately, causing asymmetric stresses on the converter components which is not desirable especially for wide input voltage range. Moreover,
the DC gain is not linear which degrades the converter performance. A recently proposed half-bridge control scheme, the DCS (Duty-Cycle-Shifted) control [16], results in achieving soft-switching for one of the two half-bridge switches while maintaining symmetric duty cycle and hence symmetric components stresses.

![Figure 2.1 Half bridge DC-DC converters with current doubler rectifier](image)

However, no matter which control scheme is applied, there are three typical operation modes shown in Figure 2.2, supposing the converter operates in CCM mode and neglecting transformer leakage energy and transient commutation [15]. In Figure 2.2, \( R_s \) is the equivalent resistance of the reflected switches on-resistance and DCR of the transformer windings, \( R_{L1} \) and \( R_{L2} \) are equivalent DCR’s of inductor \( L_1 \) and \( L_2 \), respectively, and \( R_c \) is the ESR (Equivalent Series Resistance) of the output capacitor.

![Figure 2.2 Operation modes](image)

(a) Mode 1: \( S_1 \) is on, \( S_2 \) is off
Mode 2: S₂ is on, S₁ is off

Mode 3: Both S₁ and S₂ are off

Figure 2.2 Operation modes

2.2 Unified State Space Model for HB Converter with Current Doubler Rectifier

State space equations can be derived according to three different operation modes in terms of \( x = A_m \cdot x + B_m \cdot u \) and \( y = C_m \cdot x \), where \( m \) denotes the corresponding operation mode. The state variable \( x \) is chosen as
\[
\begin{bmatrix}
v_{c1} \\
v_c \\
i_1 \\
i_2 \\
i_M
\end{bmatrix}
\] input \( u = V_m \), and output is the voltage across the
During the on time of switch $S_1$, $A_1$ and $B_1$ are as shown in Equation (2-1):

$$A_1 = \begin{bmatrix}
0 & \frac{1}{n \cdot (C_1 + C_2)} & \frac{1}{L_1} & 0 & 0 & \frac{1}{C_1 + C_2} \\
\frac{1}{n \cdot L_1} & \frac{R_v + R_{s1} + R_{s2}}{R + R_c} & \frac{R_{s1}}{R + R_c} & \frac{R}{L_1} & 0 & 0 \\
0 & \frac{R_{s2}}{R + R_c} & \frac{R}{L_2} & \frac{L_2}{R} & 0 & 0 \\
0 & \frac{L_2}{R} & \frac{R}{C \cdot (R + R_c)} & 0 & 0 & 0 \\
\frac{1}{L_m} & 0 & 0 & 0 & 0 & 0
\end{bmatrix},$$

$$B_1 = \begin{bmatrix}
0 \\
0 \\
0 \\
0 \\
0
\end{bmatrix}$$

$$C_1 = \begin{bmatrix}
0 & \frac{R_v \cdot R}{R + R_c} & \frac{R_{s1} \cdot R}{R + R_c} & \frac{R}{R + R_c} & 0
\end{bmatrix}$$

(2-1)

During the on time of switch $S_2$, $A_2$ and $B_2$ are as shown in Equation (2-2):

$$A_2 = \begin{bmatrix}
0 & 0 & \frac{1}{n \cdot (C_1 + C_2)} & \frac{1}{L_1} & 0 & \frac{1}{C_1 + C_2} \\
\frac{1}{n \cdot L_1} & \frac{R_v + R_{s1} + R_{s2}}{R + R_c} & \frac{R_{s1}}{R + R_c} & \frac{R}{L_1} & 0 & 0 \\
0 & \frac{R_{s2}}{R + R_c} & \frac{R}{L_2} & \frac{L_2}{R} & 0 & 0 \\
0 & \frac{L_2}{R} & \frac{R}{C \cdot (R + R_c)} & 0 & 0 & 0 \\
\frac{1}{L_m} & 0 & 0 & 0 & 0 & 0
\end{bmatrix},$$

$$B_2 = \begin{bmatrix}
0 \\
0 \\
0 \\
0 \\
\frac{1}{n \cdot L_2} \\
\frac{1}{L_m}
\end{bmatrix},$$

$$C_2 = \begin{bmatrix}
0 & \frac{R_v \cdot R}{R + R_c} & \frac{R_{s1} \cdot R}{R + R_c} & \frac{R}{R + R_c} & 0
\end{bmatrix}$$

(2-2)
During the off time of both $S_1$ and $S_2$, Equation (2-3) shows the corresponding $A_3$ and $B_3$:

$$A_3 = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & -\frac{R_{n_1} + R_{m} + \frac{R \cdot R}{R + R_c}}{L_1} & -\frac{R \cdot R_c}{L_2 \cdot (R + R_c)} & -\frac{R}{L_2} & -\frac{n \cdot R_{d_1}}{L_2} \\
0 & -\frac{R \cdot R_c}{L_2 \cdot (R + R_c)} & -\frac{R}{L_2} & -\frac{n \cdot R_{d_1}}{L_2} \\
0 & -\frac{C \cdot (R + R_c)}{R} & -\frac{1}{C \cdot (R + R_c)} \\
0 & -\frac{n \cdot R_{d_1}}{L_M} & 0 & -\frac{n^2 \cdot (R_c + R_{d_1} + R_{d_2})}{L_M}
\end{bmatrix}$$

$$B_3 = \begin{bmatrix}
0 \\
0 \\
0 \\
0 \\
0
\end{bmatrix}$$

$$C_3 = \begin{bmatrix}
0 & \frac{R \cdot R}{R + R_c} & \frac{R_c \cdot R}{R + R_c} & \frac{R}{R + R_c} & 0
\end{bmatrix}$$

(2-3)

In order to obtain a unified state space averaged model [33], let the switching cycle be $T$, the on time of switch $S_1$ and $S_2$ are $d_1 \cdot T$ and $d_2 \cdot T$, respectively. Then the unified state space averaged model for half bridge current doubler converter can be derived as follows:

$$\dot{x} = A \cdot x + B \cdot u = f(x, u, d_1, d_2)$$

$$y = C \cdot x$$

(2-4)

where,

$$A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3$$

(2-5)

$$B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3$$

(2-6)

and

$$C = \begin{bmatrix}
0 & \frac{R \cdot R}{R + R_c} & \frac{R_c \cdot R}{R + R_c} & \frac{R}{R + R_c} & 0
\end{bmatrix}$$

(2-7)
2.3 Unified Analog Small Signal Model for HB Current Doubler Converter

Based on the unified state space averaged model derived in the previous section, we can further analyze the analog small signal model. In general, let

\[ x = X_{ss} + \hat{x}, \quad y = Y_{ss} + \hat{y}, \quad u = V_{in} + \hat{v}_{in}, \quad d_1 = D_1 + \hat{d}_1, \]

and \( d_2 = D_2 + \hat{d}_2 \), where \( X_{ss}, Y_{ss}, V_{in}, D_1 \) and \( D_2 \) are the steady state values of \( x, y, v_{in}, d_1 \) and \( d_2 \) respectively, and \( \hat{x}, \hat{y}, \hat{v}_{in}, \hat{d}_1 \) and \( \hat{d}_2 \) represent the small signal disturbances. Since in the steady state, \( x = A \cdot X_{ss} + B \cdot V_{in} = 0 \), then the following can be determined:

\[ X_{ss} = -A_{ss}^{-1} \cdot B_{ss} \cdot V_{in} \]  
(2-8)

From Equation (2-4), Equation (2-9) can be derived as follows:

\[ \frac{\partial \hat{x}}{\partial t} \approx \frac{\partial f}{\partial x} \cdot \hat{x} + \frac{\partial f}{\partial v_{in}} \cdot \hat{v}_{in} + \frac{\partial f}{\partial d_1} \cdot \hat{d}_1 + \frac{\partial f}{\partial d_2} \cdot \hat{d}_2 \]  
(2-9)

Based on Equations (2-4) and (2-8) ~ (2-9), we can conduct unified small signal analysis for CDRHB converters.

<table>
<thead>
<tr>
<th>Control Scheme</th>
<th>Duty Cycle</th>
<th>( G_{v_g} (s) )</th>
<th>( G_{vd} (s) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symmetric</td>
<td>( D_1 = D_2 = D )</td>
<td>( C(s \cdot I - A_{ss})^{-1} \cdot B_{ss} )</td>
<td>( C \cdot (s \cdot I - A_{ss})^{-1} \left[ (A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in} \right] )</td>
</tr>
<tr>
<td>Asymmetric</td>
<td>( D_1 = 1 - D_2 = D )</td>
<td>( C(s \cdot I - A_{ss})^{-1} \cdot B_{ss} )</td>
<td>( C \cdot (s \cdot I - A_{ss})^{-1} \left[ (A_1 - A_2) \cdot X_{ss} + (B_1 - B_2) \cdot V_{in} \right] )</td>
</tr>
<tr>
<td>Duty Cycle Shift</td>
<td>( D_1 = D_2 = D )</td>
<td>( C(s \cdot I - A_{ss})^{-1} \cdot B_{ss} )</td>
<td>( C \cdot (s \cdot I - A_{ss})^{-1} \left[ (A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in} \right] )</td>
</tr>
</tbody>
</table>
2.4 Unified Digital Small Signal Model for HB Current Doubler Converter

For developing the linear time invariant (LTI) digital model of the half bridge DC-DC converter with current doubler rectification in Figure 2.1, the following assumptions should be considered:

- The converter operates in continuous conduction mode (CCM);
- $V_{in}$ is constant within each switching cycle;
- There is no ripple in the inductors currents and output capacitor voltage.

For simplicity, the digital model of the symmetric half bridge converter with current doubler rectifier will be derived first.

Assuming that the derivation starts from the $k^{th}$ switching cycle, using the Forward Euler approximation method as follows:

$$x(t_0 + \varepsilon) \approx x(t) + \varepsilon \frac{dx(t_0)}{dt}$$ \hspace{1cm} (2-10)

When $kT < t \leq kT + d_1T$, converter operates in mode 1 (switch $S_1$ is on), according to Forward Euler approximation, we can get

$$x(kT + d_1T) \approx x(kT) + d_1T \cdot (A_1 \cdot x(kT) + B_1 \cdot V_{in}[k])$$ \hspace{1cm} (2-11)

After reformatting Eqn. (2-11),

$$x(kT + d_1T) \approx [I + d_1T \cdot A_1]x(kT) + d_1T \cdot B_1 \cdot V_{in}[k]$$ \hspace{1cm} (2-12)

When $kT + d_1T < t \leq kT + d_1T + \frac{1 - d_1 - d_2}{2}T$, the converter operates in mode 3 (both $S_1$ and $S_2$ is off), so after Forward Euler approximation:

$$x(kT + d_1T + \frac{1 - d_1 - d_2}{2}T) \approx x(kT + d_1T) + \frac{1 - d_1 - d_2}{2}T \cdot (A_3 \cdot x(kT + d_1T) + B_3 \cdot V_{in}[k])$$ \hspace{1cm} (2-13)
After reformatting (2-13), the following is obtained:

\[
x(kT + d_1 T + \frac{1-d_1-d_2}{2} T) \approx [I + \frac{1-d_1-d_2}{2} T \cdot A_3] x(kT + d_1 T) + \frac{1-d_1-d_2}{2} T \cdot B_3 \cdot V_{in}[k]
\]  

(2-14)

When \( kT + d_1 T + \frac{1-d_1-d_2}{2} T < t \leq kT + d_1 T + \frac{1-d_1-d_2}{2} T + d_2 T \), converter operates in mode 2 (S_2 is on),

\[
x(kT + (d_1 + d_2) T + \frac{1-d_1-d_2}{2} T) \approx x(kT + d_1 T + \frac{1-d_1-d_2}{2} T) + d_2 T \cdot (A_2 \cdot x(kT + d_1 T + \frac{1-d_1-d_2}{2} T) + B_2 \cdot V_{in}[k])
\]  

(2-15)

After reformatting (2-15),

\[
x(kT + (d_1 + d_2) T + \frac{1-d_1-d_2}{2} T) \approx [I + (d_2 T \cdot A_2) x(kT + d_1 T + \frac{1-d_1-d_2}{2} T) + \frac{1-d_1-d_2}{2} T \cdot B_2 \cdot V_{in}[k]
\]  

(2-16)

When \( kT + d_1 T + \frac{1-d_1-d_2}{2} T + d_2 T < t \leq kT + T \), converter operates in mode 3 (both S_1 and S_2 is off), so:

\[
x(kT + T) \approx x(kT + (d_1 + d_2) T + \frac{1-d_1-d_2}{2} T) + \frac{1-d_1-d_2}{2} T \cdot (A_3 \cdot x(kT + (d_1 + d_2) T + \frac{1-d_1-d_2}{2} T) + B_3 \cdot V_{in}[k])
\]  

(2-17)

After reformatting, Eqn. (2-18) can be written as follows:

\[
x(kT + T) \approx [I + \frac{1-d_1-d_2}{2} T \cdot A_3] x(kT + (d_1 + d_2) T + \frac{1-d_1-d_2}{2} T) + \frac{1-d_1-d_2}{2} T \cdot B_3 \cdot V_{in}[k]
\]  

(2-18)

Then substitute Equation (2-12), (2-14) and (2-16) to (2-18) and neglect the terms including \( T^N (N \geq 2) \), a state space digital model is developed as follows:
\[ x[k+1] = [I + A \cdot T]x[k] + B \cdot T \cdot V_{in}[k] = \phi(x[k], v_{in}[k], d_1, d_2) \] (2-19)

In order to derive the LTI digital model, linearization of the digital model (2-19) at the steady state operation point is taken to obtain:

\[ \hat{x}[k+1] \approx \frac{\partial \phi}{\partial x} \hat{x}[k] + \frac{\partial \phi}{\partial v_{in}} \hat{v}_{in}[k] + \frac{\partial \phi}{\partial d_1} \hat{d}_1 + \frac{\partial \phi}{\partial d_2} \hat{d}_2 \]

\[ y[k] = C \cdot x[k] \] (2-20)

And in steady state, \( x[k+1] = x[k] = X_{ss} \), from (2-19), it can be derived as follows:

\[ X_{ss} = -A_{ss}^{-1} \cdot B_{ss} \cdot V_{in} \] (2-21)

The deviations in Equation (2-22) can also be derived from (2-19) to obtain the LTI digital model:

\[ \hat{x}[k+1] \approx (I + A_{ss} \cdot T) \hat{x}[k] + B_{ss} \cdot T \cdot \hat{v}_{in}[k] \]
\[ + [(A_1 - A_3) X_{ss} + (B_1 - B_3) V_{in}] \cdot T \cdot \hat{d}_1 \]
\[ + [(A_2 - A_3) X_{ss} + (B_2 - B_3) V_{in}] \cdot T \cdot \hat{d}_2 \]

\[ y[k] = C \cdot x[k] \] (2-22)

Although the above derivations are based on the symmetric controlled half
bridge current doubler DC-DC converter, the linearized digital model (2-20) is unified, and only different in derivatives in Equation (2-20) according to the different control schemes.

Different transfer functions can also be derived based on different control schemes from the LTI digital model in Equation (2-22), and they are listed in table 2-2.

### TABLE 2-2
Transfer Functions for Digital Controlled Half Bridge Current doubler Converters with Different Control Schemes

<table>
<thead>
<tr>
<th>Control Scheme</th>
<th>Duty Cycle</th>
<th>( G_{vg} (z) = \frac{V_o}{V_{in}} )</th>
<th>( G_{vd} (z) = \frac{V_o}{d} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symmetric</td>
<td>( D_1 = D_2 = D )</td>
<td>( C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss} )</td>
<td>( C \cdot (z \cdot I - A_{ss} \cdot T)^{-1} \cdot T \cdot [(A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}] )</td>
</tr>
<tr>
<td>Asymmetric</td>
<td>( D_1 = 1 - D_2 = D )</td>
<td>( C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss} )</td>
<td>( C \cdot (z \cdot I - A_{ss} \cdot T)^{-1} \cdot T \cdot [(A_1 - A_2) \cdot X_{ss} + (B_1 - B_2) \cdot V_{in}] )</td>
</tr>
<tr>
<td>Duty Cycle Shift</td>
<td>( D_1 = D_2 = D )</td>
<td>( C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss} )</td>
<td>( C \cdot (z \cdot I - A_{ss} \cdot T)^{-1} \cdot T \cdot [(A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}] )</td>
</tr>
</tbody>
</table>

For comparison, bode plots of the derived digital model are depicted in Figure 2.3 together with bode plots of analog models and discretized analog models. The converter’s specification is \( V_{in} = 48V \), \( n=6 \), \( V_o=1V \), \( I_o= 50A \), \( C_o=1000 \mu F \), \( L_o= 90 \text{nH} \), and switching frequency of 400 KHz. It can be found that differences exist among these three models at high frequencies. Because digital systems will have additional phase shift compared to analog systems, a difference between the analog model and the digital model can be noticed at the high frequencies. Furthermore, it can be noticed that the discretized analog model starts to alias as approaching half of the
sampling frequency. Therefore, it can be concluded that the derived digital model is more valid than the other two models for digital control design of the digitally controlled half bridge DC-DC converter.

Figure 2.3 Bode diagrams of three converter models

(Dot trace: analog model, dash trace: discretized analog model, solid trace: digital model)

A digital compensator based on the digital model of the converter is designed and the bode plot of its loop gain is shown in Figure 2.4. A prototype with the same design specification is built and the close loop bode plot is shown in Figure 2.5. The experimental results match theoretical design and therefore verify the derived digital model.
Figure 2.4 Close loop gain of theoretical design

Figure 2.5 Close loop gain of experimental result
CHAPTER THREE: DIGITAL CONTROLLER FOR SWITCHING POWER CONVERTER

With the advances made in Digital Signal Processors (DSP) and ICs, digital control has been an increasingly important topic in the switch mode power converter area. Digital controllers are increasingly being used especially in complex systems, including power electronics systems. Compared with analog controllers, digital controllers have many advantages, including ease of integration and interface with other digital systems, elimination of component tolerances and ageing, ability to perform sophisticated and advanced control schemes, and they can easily be used to realize other control functions besides the regulation and compensation. Also, important for switching power converters, it can generate flexible power switch drive waveforms with programmable relationships to one another [2-11].

However, there are still some disadvantages/challenges in using digital controllers for analog systems such as DC-DC converters in power electronics including the required high resolution from the digital controller to satisfy the converter tight regulation requirements and the required high speed to satisfy the converter dynamic requirements, which results in cost increase. Fortunately, the digital controllers industry is rapidly developing, allowing the availability for faster and higher resolution digital controllers at a lower cost. Therefore, in the future the digital controller will have more functionality, which makes power systems more
intelligent, as well as lower price. More digital controlled power converters can be expected to be commercially available and maybe at a comparable price with analog controlled counterpart but with more intelligent functions in some applications.

The digital controller for switch mode power converters can be defined that the digital controller can perform power conversions PWM function, error signal, and compensator functions in digital mode. It can also perform protection, prevention, and monitoring functions such as fan control for over temperature prevention, overvoltage/overcurrent protection, as well as monitoring current sharing and temperature and so on. Typical digital controlled power converter architecture is shown in Figure 3.1.

![Figure 3.1: Typical switching power converter architecture with digital controller](image)

From the definition and Figure 3.1, digital controller has three indispensable parts: A/D converter, digital compensator, and digital pulse width modulator (DPWM)

In this chapter, we will discuss two digital compensator design approaches; the
redesign approach and the direct design approach. Then the A/D converter and DPWM design requirements for digital controller will be covered. In addition, popular A/D converter architectures and DPWM architectures are introduced.

3.1 Digital Compensator Design

Generally speaking, there are two approaches for digital compensator design: one is the digital redesign based on analog controller, and the other is the direct digital design approach [3-5]. Figure 3.2 shows the digital compensator design flow chart.

![Digital compensator design flow chart](image)

Figure 3.2 Digital compensator design flow chart

3.1.1 Digital Redesign Approach

With the digital redesign approach, as shown in Figure 3.2, the analog
controller is first designed based on the analog model of the converter and then transformed to the Z-domain using different discretization methods. Then the discretized digital controller is optimized and approximated for practical realization.

The benefit of the redesign approach is to make use of the analog design approach. For analog design, the large and small-signal averaged models of all system blocks are readily available and well understood; design oriented analysis is based on intuitive relationships between frequency response and system specifications; extensive design experience. The proven design procedure for the analog controller is shown as follows:

- Develop an average small signal model of the switching converter at the quiescent operation point
- Solve for the uncompensated loop gain taking into account the combined delay in the digital system (over design to correct for delay)
- Design the compensator to shape loop gain in the frequency domain to achieve the desired stability margin, voltage regulation, and line, load, noise rejection.

30
One key step in digital redesign approach is the discretization step. The objective of discretization is to match frequency characteristics of discrete equivalent compensator with that of the designed analog controller.

A. Traditional discretization methods

There are several s-z transformation methods discussed in literature, such as the step invariant transformation method, the bilinear transformation method, the pole/zero match transformation method, LDI (Lossless digital integrator) transformation method, and the backward Euler and forward Euler transformation methods [3-5] [35-37]. Table 3-1 shows some popular discretization methods.
Due to the frequency warping effect in these transformations, the frequency response of the discretized controllers does not correspond with that of the designed analog controller. Moreover, the frequency warping effects of different transformations differs. For example, the bilinear, LDI, and Backward Euler transformations are as follows:

\[
s = \frac{2}{T_s} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \quad \text{(Bilinear Transformation)} \quad (3-1)
\]

\[
s = \frac{1}{T_s} \cdot \frac{1 - z^{-1}}{z^{-1/2}} \quad \text{(LDI Transformation)} \quad (3-2)
\]

\[
s = \frac{1}{T_s} \cdot \frac{z^{-1}}{1} \quad \text{(Backward Euler Transformation)} \quad (3-3)
\]

The frequency warping effects of Bilinear and LDI transformations compared to the ideal case are as shown in the Figure 3-4. In Figure 3-4, the dotted line represents the ideal transformation which preserves all the frequency characteristics of the analog signal or controller without the warping effect, resulting in a digitized controller that is very close to the original analog controller transfer function.
However, the upper dashed line and the lower dashed-dotted line of the bilinear and LDI transformations have warping effects that will result in a digital controller with different characteristics of the analog controller to a certain extent.

![Figure 3.4: Frequency warping effects of bilinear and LDI discretization methods](image)

Figure 3.4: Frequency warping effects of bilinear and LDI discretization methods

**B. Hybrid discretization Method**

Less warping effect can be achieved by combining different discretization methods, namely, the hybrid discretization. The hybrid discretization result in discretized controller with much smaller warping effect compared to those discretized by a single transformation method, if properly used. Because the warping effects can be cancelled to some extent, the frequency range where the discrete time transfer function agrees well with its continuous counterpart can be extended. Hence, a better and more accurate transformation can be achieved.
C. Methods of implementing hybrid discretization

Three ways of implementing hybrid discretization are discussed here. Considering the following general transfer function:

\[
H(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_2 s^2 + a_1 s + a_0}{b_m s^m + b_{m-1} s^{m-1} + \cdots + b_2 s^2 + b_1 s + b_0}
\]  
(3-4)

The first way is to discretize different \( s \) terms using different discretization methods in each \( s^n \) term. For example, the following can be rewritten (3-4):

\[
H_1(s) = \frac{a_n s_1^p \cdot s_2^Q + a_{n-1} s_1^p \cdot s_2^Q + \cdots + a_2 s_1 \cdot s_2 + a_1 s_1 + a_0}{b_m s_1^I \cdot s_2^J + b_{m-1} s_1^I \cdot s_2^J + \cdots + b_2 s_1 \cdot s_2 + b_1 s_1 + b_0}
\]  
(3-5)

Where, \( p + Q = n, I + J = m \). Then \( s_1 \) is discretized with one discretization method and \( s_2 \) with another discretization method.

The second way is to discretize odd power terms with one discretization method and even power terms using another discretization method in a polynomial [38]. For example, given that \( n \) is even and \( m \) is odd, Equation (3-4) can be rewritten as:
Then $s_1$ is discretized by one discretization method and $s_2$ with another discretization method.

The third way is to combine different discretization methods into each $s$ transformation from continuous domain to discrete time domain, similar to [39]. For example, combining $s_1$ and $s_2$ in each $s$ with a ratio $K$ as $s = K \cdot s_1 + (1 - K) \cdot s_2$, where $0 < K < 1$, then $s_1$ is discretized by one discretization method and $s_2$ by another discretization method, and substitute $s$ in Equation (3-4) in order to get a discrete-time transfer function.

In order to illustrate the hybrid discretization method application in power converters digital controller design, a design example is given.

A voltage-mode-controlled symmetric isolated half-bridge converter system with the following parameters is considered in the design: $V_{in} = 48V$, $n=6$, $V_o=1V$, $I_o=50A$, $C_o=1000 \ \mu F$, $L_o=90 \ \text{nH}$, and switching frequency of 400 KHz. An analog controller based on the continuous model of the converter can be designed as in Equation (3-4) with bandwidth of 79.2 KHz and the phase margin of 56 degrees.

$$H_a = \frac{4.947 \times 10^{-6}s^2 + 1.374 s + 49680}{2.843 \times 10^{-13}s^3 + 1.069 \times 10^{-6}s^2 + s} \quad (3-7)$$

The analog controller of Equation (3-4) is discretized, at 400 kHz sampling frequency, using several discretization methods including the hybrid one shown in Equations (3-8), (3-9), and (3-10):

$$H_{z4} = \frac{2.648z^3 - 1.177z^2 - 2.526z + 1.299}{z^3 - 0.1967z^2 - 0.6427z - 0.1606} \quad \text{(Using Bilinear Transformation)} \quad (3-8)$$
Hz5 = \frac{2.361 z^3 - 3.62 z^2 + 1.344 z}{z^2 - 1.352 z^2 + 0.3828 z - 0.03088} \quad \text{(Using Backward Euler Transformation)} \quad (3-9)

Hz6 = \frac{2.804 z^3 - 4.004 z^2 + 1.328 z}{z^3 - 1.019 z^2 + 0.06562 z - 0.04675} \quad \text{(Using Bilinear- Backward Euler Hybrid Transformation)} \quad (3-10)

Figure 3.6 shows the bode-plots of the three discretized functions for comparison. It can be noticed that the bilinear-backward Euler hybrid transformed transfer function gain and phase plots are closer to the analog transfer function gain and phase plots compared to using single transformation methods of bilinear and Backward Euler.
Figure 3.6: Bode plots comparison: (a) full view, and (b) zoomed view (Dot-dashed trace: analog, dot trace: Bilinear digital, dashed trace: Backward Euler digital, solid trace: Bilinear-Backward Euler hybrid)

The controller was simulated in the MatLab. Figure 3.7 shows the output voltage simulation results comparison using analog and discretized digital controllers during steady-state and load transients. Table 3-2 shows a comparison between the simulation results of Figure 3.7. It can be noticed that closer results to the analog compensator is achieved with hybrid discretization.
Figure 3.7: MatLab simulation results of the designed closed-Loop converter using both analog and digital discretized controllers: (a) output voltage during steady-state, load step-down, and load step-up (Middle trace: analog, lower trace: Bilinear digital, and upper trace: Bilinear- LDI Hybrid), (b) zoomed output voltage during load step down, and (c) zoomed output voltage during load step-up.

Table 3-2: Simulation Results Comparison

<table>
<thead>
<tr>
<th>Compensator/Controller</th>
<th>Steady-State Error (%)</th>
<th>Transient Deviation (%)</th>
<th>Settling Time (sec.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog</td>
<td>0</td>
<td>13</td>
<td>50u</td>
</tr>
<tr>
<td>Bilinear</td>
<td>1.2</td>
<td>14</td>
<td>78u</td>
</tr>
<tr>
<td>Bilinear- LDI Hybrid</td>
<td>0.8</td>
<td>13</td>
<td>45u</td>
</tr>
</tbody>
</table>

3.1.2 Digital Direct Design

The digital direct design approach, as shown in Figure 3.2, is to design the digital compensators directly in the Z-domain based on the discrete model of the switching power converters, then optimize and approximate the designed digital controller for practical realization.

The discrete model for digital direct design can be derived through the following two ways: one is to discretize the analog model of converter with different
discretization methods shown in Table 3-1 or hybrid discretization method mention above. The other way is to develop digital model of converter directly as Section 2.4.

To illustrate the digital direct design approach, a digital compensator design example for a voltage mode controlled symmetric half bridge is given. The converter’s specification are $V_{in}=48V$, $n=6$, $V_o=1V$, $I_o=50A$, $C_o=1000\ \mu F$, $L_o=90\ \text{nH}$, and switching frequency of 400 KHz.

In section 2.4, it has been verified by experiment and proven that it is better than the analog model and the digitized analog model for digital compensator design. Here, we use the direct digital model for compensator design. The digital model can be derived based on section 2.4.

A digital compensator based on the digital model of the converter is designed and bode plot of the loop gain is shown in Figure 3.8. A prototype with the same design specification is built and the close loop bode plot is shown in Figure 3.9. The experimental results match theoretical design.
3.2 A/D Converter

The A/D converter can be modeled as shown in Figure 3.10 [37]. The zero order hold’s frequency response can be studied by the body diagram shown in Figure 3.11. From Figure 3.11, it can be found that the A/D converter introduces the phase lag into the system. If the bandwidth of the system is equal to the sampling frequency and the phase delay goes to 180 Degree. Generally, in order to make the phase delay of the zero-order hold as small as possible, the sampling frequency should be at least 10 times the bandwidth, which means the phase delay is 18 degree.
According to the Shannon sampling theorem, when the input signal is reconstructed, any frequencies \( \omega > \frac{\omega_s}{2} \) will reflect into the frequency range \( 0 < \omega < \frac{\omega_s}{2} \). This effect is called frequency aliasing. The frequency aliasing can be prevented either by increasing \( \omega_s \) or by placing an analog antialiasing filter in front of the sampler. The antialiasing filter is a low pass filter that removes any frequency components in \( e(t) \) that are greater than \( \frac{\omega_s}{2} \), since the low pass filters introduce phase lag. However, the cutoff frequency of the antialiasing filter cannot be made so low as to destabilize the control system.
3.2.1 A/D Converter Requirement

To satisfy specifications for output voltage regulation, resolution of the A/D converter has to enable error lower than the allowed variation of the output voltage $\Delta V_o$ \cite{5} \cite{11}:

$$
\Delta V_o \leq K \geq \frac{V_{ADCMax}}{2^n_{ADC}} \quad (3-11)
$$

Where $K$ is the output voltage sensor gain, $\Delta V_o$ is the output voltage tolerance and $n_{ADC}$ is the number of bits of the A/D converter. The resolution effect on the output is shown in Figure 3.12.

Although theoretically speaking, it’s okay if the sampling frequency is at least twice bandwidth. But for practical application, as discussed above, in order to make the phase delay of the zero-order hold as small as possible, the sampling frequency should be at least 10 times the bandwidth, which means the phase delay is 18 degree.

![Figure 3.12 The ADC resolution effect on output \cite{40}](image)

(a) Insufficient resolution  (b) Sufficient resolution

3.2.2 A/D Converter Architectures
Generally speaking, there are three ADC architectures: flash, successive approximation register, and pipelined with multiple flashes.

The flash architecture is shown in Figure 3.13. It needs $2^n - 1$ comparators for an $n$ bit A/D converter. For a high resolution ADC, it will need a large number of comparators, for example, for 10 bit ADC, it will need 1023 comparators. But it is very fast since it only needs one cycle to convert.

![Figure 3.13 A/D converter flash architecture [40]](image)

Figure 3.14 shows the successive approximation register (SAR) architecture. It only needs one comparator to realize high resolution ADC, so its advantage is simple structure and low gate count. But it is very slow since it needs $N$ comparisons for an $N$ bit resolution. As a result, it has $N$ times delay time by one comparator.
The ADC pipelined with multiple flashes architecture, shown in Figure 3.15, is a combined structure for flash and successive approximation registers architectures. As a result, it is a trade-off of the advantages between these two architectures. For a n-bit A/D converter, it requires \( p \) SAR stages and \( k = n/p \) flash A/Ds. It has \( k \) times delay time caused by one comparator, so it is slower than flash but faster than SAR A/D. In addition, it needs \( k \left( 2^p - 1 \right) \) comparators, which is more than SAR but less than flash structure.
3.3 Digital Pulse Width Modulator

The digital pulse width modulator (DPWM) is acting as D/A converter, and performs the same drive signal generation function as analog PWM, but it does so by “calculating” and then “timing” the desired duration of ON and OFF periods of its output signal [2].

3.3.1 DPWM Requirements

The resolution of DPWM should be at least one bit higher than A/D converter in order that one LSB change of the A/D converter can be represented by DPWM and results in at least one LSB equivalent change in output voltage by DPWM. Otherwise, periodic oscillations of $V_o$ at frequencies lower than the PWM switching frequency will happen as shown in Figure 3.16. This phenomenon is called “limit-cycle”.

$$n_{DPWM} \geq n_{ADC} + 1$$  \hspace{1cm} (3-12)

Where $n_{DPWM}$ is the number of bit of DPWM and $n_{ADC}$ is the number of bit of A/D converter [5] [7-8] [11] [41].

Limit cycle can possibly produce undesirable output noise and electro-magnetic interference (EMI). Because the steady-state limit cycling is undesirable, its amplitude & frequency are difficult to predict, and therefore difficult to analysis the resulting noise and EMI
3.3.2 DPWM Generation Schemes

There are state-of-the-art DPWM generation schemes, fast clocked scheme, tapped delay line scheme, hybrid delay line/counter scheme, ring oscillator MUX scheme, and DSP based scheme [7-8] [42-44].

A. Fast clocked scheme

As shown in Figure 3.17, this scheme uses an external fast clock to generate the PWM waveform. The A/D converter outputs a N-bit binary number which represents the duty cycle. This binary number is loaded into a register and compared with the output from a counter clocked at $f_{clk}$ using a digital comparator. The RS flip-flop is set at the beginning of the switch cycle and reset when the counter reach zero.
The structure is simple and has a low gate count. But the external clock has to be very fast, at least \(2^n\) times higher than the switching frequency (\(n\) is the DPWM’s resolution). In addition, power consumption has been reported to be on the order of mWs. Also it is not suitable for multiphase VRM applications since each counter has to be implemented for each phase independently. As a result, an increase in the die area and power consumption is a must for multiphase applications.

**B. Tapped delay line scheme**

This scheme is shown in Figure 3.18. A pulse from a reference clock initiates the cycle and sets the PWM signal to logic high level. This reference pulse is then propagated along a sequence of delay lines and when it reaches the output selected by the multiplexer, it sets the PWM signal to logic low level. The total delay of the delay line is adjusted to be equal to that of the reference clock period. Additionally feedback is used to provide a delay locked loop (DLL) which locks to the period of the input
clock. This technique reduces power consumption significantly. The frequency of the ring oscillator is equal to the switching frequency which is much better than the fast clocked DPWM scheme. But it suffers from large silicon area due to many delay lines and MUX’s. It can be utilized to generate multiple PWM signals by adding multiplexers to a single delay line, but result in larger silicon area and therefore not suitable for multiphase applications.

![Tapped delay line DPWM](image)

Figure 3.18 Tapped delay line DPWM

C. Hybrid delay line/counter scheme

The hybrid delay line/counter scheme combines the fast clocked scheme and tapped delay line scheme. It is illustrated in Figure 3.19. The rising edge of the PWM signal is set by the reference clock and is reset when the pulse, after propagating along the delay line, is sensed by the multiplexer. Actually, this scheme is a trade off between die area and power consumption. At the same time, it reduces maximum clock speed by combining the delay line oscillator with the counter.
**D. Ring Oscillator MUX scheme**

This scheme operation principal is similar to the tapped delay line approach, as shown in Figure 3.20. As a result, it has similar power consumption and die area as the delay line scheme. What makes this scheme attractive is that it has a symmetrical structure and therefore suitable for multiphase applications.
E. DSP based DPWM scheme

This scheme is illustrated in Figure 3.21. The DPWM generation is based on the calculation. Its advantages include its ability to be reprogrammed as well as its wide use in low frequency applications like motor control and PFC’s. But it is costly and too complex for this intended application as well as delays degrading the performance.

![Figure 3.21 DSP based DPWM](image-url)
CHAPTER FOUR: DIGITAL VOLTAGE DRIVING

OPTIMIZATION

4.1 Introduction

For isolated low-output-voltage topologies, the secondary side losses are dominant. The main losses in the secondary side are conduction loss, driving loss, and switching loss.

The conduction loss can be calculated as:

\[ P_{\text{Conduction}} = I^2 \cdot \frac{R_{\text{dson}}}{N} \]  

(4-1)

The driving loss can be estimated as:

\[ P_{\text{Driving}} = N \cdot Q_g \cdot U_{\text{Driving}} \cdot f_s \]  

(4-2)

The switching loss can be estimated as:

\[ P_{\text{switching}} = \frac{1}{3} \cdot (t_r + t_f) \cdot f_s \cdot \frac{I}{N} \cdot U \]  

(4-3)

In equation (4-1) through (4-3), N is the number of MOSFETS used, I is the current flowing through MOSFET and U is the voltage across MOSFET, \( Q_g \) is the gate charge of the MOSFET and \( R_{\text{dson}} \) represents the on state resistance of the MOSFET; \( f_s \) is the switching frequency of the converter, \( U_{\text{Driving}} \) is the driving voltage of the MOSFET. \( t_r \) and \( t_f \) are the rising time and falling time for the driving voltage of MOSFET’s, respectively.

From the equations (4-1) through (4-3), it can found that one optimal efficiency point can be reached when applying different driving voltages according to
different operation conditions. Because, $R_{\text{ds(on)}}$ will be lowered as the increase of driving voltage, which results in conduction loss decrease, given the same current. In the meanwhile, the driving loss is increasing, resulting from the increase of the gate charge of each MOSFET due to the driving voltage’s increase. All of these characteristics can be found from the MOSFET’s datasheet on the typical characteristics curves as shown in Figure 4.1.

(a) On resistance vs. gate-to-source voltage

(b) Gate charge vs. gate-to-source voltage
Figure 4.1 Typical MOSFET datasheet characteristics curves

The conduction loss will decrease with the driving voltage increase, leading to reduction of the overall losses. As a result, an optimal efficiency point can be reached for a given operation point. This is the motivation of driving voltage optimization.
(DVO). The driving voltage optimization’s significance on efficiency is more obvious for high current low voltage with high frequency applications. Currently most MOSFET are figure-of-merit (FOM) optimized. From Figure 4.1, it can be found that $R_{\text{ds(on)}}$ changes a little with the driving voltage variation. As a result, the conduction loss maybe reduced so little to be negligible for low current applications. But for high current high frequency applications, the conduction loss variation can be significant while the driving loss can be comparable to the conduction loss due to its high frequency operation. For this case, the voltage driving optimization will have a significant effect on efficiency optimization.

For the analog controller, the implementation of voltage driving optimization seems difficult or at least costly, since DVO applications need online programmability. Fortunately, in recent years, as advances in digital controller IC and digital signal processors (DSP’s), digital controllers are going to be an alternative candidate for power switching converters besides analog controllers. Digital controller can provide online real time control features, which is one of the advantages of digital controllers over their analog counterparts. So DVO implementation becomes possible with application of digital controller in switching converters. Furthermore, DVO make digital controllers more cost effective due to there better utilization of single digital controller chips. It can be expected that DVO can be a great feature of digital controlled switch mode power converters as the continuous increase of output currents for converters and further cost reduction with development of digital controller.
4.2 DVO Implementation

Digital driving voltage optimization adjusts the driving voltage for MOSFETS according to the line voltage and load current variation. The DVO close loop algorithm flowchart is shown in Figure 4.2.

N samples of $I_{in}$ by an ADC are stored and then averaged and filtered by a LP digital filter difference equation to eliminate noise and generate $I_{in}(n)$. The current difference $\Delta I_{in}(n)$ between new current value $I_{in}(n)$ and the previous value $I_{in}(n-1)$ is calculated. At the same time, the driving voltage difference $\Delta V_D(n)$ between new current value $V_D(n)$ and the previous value $V_D(n-1)$ is calculated.

\[
\Delta I_{in} = I_{in}(n - 1) - I_{in}(n) \tag{4-4}
\]

\[
\Delta V_D = V_D(n) - V_D(n - 1) \tag{4-5}
\]

A check will be performed to see if $\Delta I_{in}(n)$ has sufficient value ($I_e$) to update $V_D$ or not. If this value is sufficient, the program will proceed to the next step, otherwise, it will start from the beginning by sampling $I_{in}$ again. If the signs (positive or negative) of Equations (4-4) and (4-5) are same, this means that the current efficiency-driving voltage point is located on the left side of $V_{DO}$, as shown in Figure 4.3 and $V_D$ should be increased by an increment $V_{step}$ to move toward the maximum efficiency point. Otherwise, If the signs of Equations (4-4) and (4-5) are not same, this means that the current efficiency-driving voltage point is located on the right side of $V_{DO}$ as shown in Figure 4.3 and $V_D$ should be decreased by a decrement $V_{step}$ to move toward the maximum efficiency point. After storing the current values of $I_{in}$ and
N samples of $I_w$ by ADC

Apply averaging and LP Filter difference equation to $I_w$ to find $I_w(n)$

Calculate

$$\Delta I_w = I_w(n-1) - I_w(n)$$
$$\Delta V_D = V_D(n) - V_D(n-1)$$

$[\Delta I_w] < I_e$

Yes

No

$I_w(n-1) = I_w(n)$
$V_D(n-1) = V_D(n)$

$\text{Sign}(\Delta I_w) = \text{Sign}(\Delta V_D)$

Yes

No

$V_D(n) = V_D(n) + V_{\text{step}}$

$V_D(n) = V_D(n) - V_{\text{step}}$

Start

Wait M switching Cycles

Figure 4.2 DVO close loop algorithm flowchart
V_D, the program will decrease or increase V_D and update it. Then, after several (M) switching cycles, I_in is sampled again and the driving voltage optimization process will be repeated.

4.3 Initial Experimental Results

A half bridge current doubler DC-DC converter prototype is used for the power stage to experiment and implement the digital voltage optimization. The half bridge prototype is 1 V/40 A output and used for 36-75 input range. The synchronous rectifiers are used for the current doubler and the switching frequency is 400 kHz. The digital controller is implemented with TMS320F2812 DSP chip, for initial experiment verification, the DVO technique is only applied for the secondary side synchronous rectifiers.

The digital controller with DVO block diagram is shown in Figure 4.4. The
digital controller determines duty cycle and outputs the driving signals for the switching. At the same time, as mentioned in section 4.2, it also detects and samples the input current and read by the DVO subroutine. Then the driving voltage optimization subroutine adjusts the driving voltage according to operation condition to achieve optimal efficiency as shown in Figure 4.2.

![Figure 4.4 Digital controller block diagram](image)

In order to adjust the driving voltage online, variable driving voltage supply is needed. To verify the DVO concept, we use linear regulators to build a prototype for the initial experiment. The schematic is shown in Figure 4.5. The linear regulator part number is LM 317.

![Figure 4.5 Variable driving voltage supply schematic for initial experiment](image)
Figure 4.6 shows the different output voltages of the variable driving voltage supply from different input signal from the DSP. The DSP generates different duty cycle signals according to different input current by the DVO subroutine.

(a)

(b)
(c) Vdd=5.8V, Ddsp=0.5

(d) Vdd=7.1V, Ddsp=0.8

(e) Vdd=7.6V, Ddsp=0.9
The initial DVO open loop experimental results are shown in Figure 4.7. For the initial experiment, the line voltage is 48 V and the output voltage is 1 V. The frequency is 400 kHz. DVO open loop experimental results are tested under the load current from 5 A through 20 A.

From Figure 4.7, it can be found that optimal driving voltage is different for different load currents. For Io=5A case, the optimal driving voltage is 3.5 V; 4 V is the driving voltage when the optimal efficiency achieved for Io=10 A case; When load change to 15 A, the optimal driving voltage rises to 5.5 V; 6V is required to achieve maximum frequency for the load current Io=20 A case. Compared with the constant driving voltage converter, let’s say driving voltage is 5 volts. The maximum efficiency improved can be 1% by VDO technique for Io=5 A, light load case. The results can be expected to be more significant after VDO technique is further developed and the digital controller and power stage are optimized the experimental set up is improved.

Since this is only an initial open loop experiment for DVO technique, further
close loop experiments are needed. What’s more, for better efficiency, the variable voltage supply for DVO implementation may use switching converters to get better results.

(a) \( I_o = 5A \)

(b) \( I_o = 10A \)
Figure 4.7 DVO initial open loop experiment

(c) Io= 15A

(d) Io= 20A
CHAPTER FIVE: EXPERIMENTAL RESULTS AND ANALYSIS

5.1 Experimental Results

The specifications of the DSP-controlled half-bridge DC-DC converter prototype with a current doubler are as follows:

\[ V_{in} = 48V, n = 6, V_o = 1V, I_o = 50A, f_{sw} = 400kHz, C_o = 500 uF, L_o = 270 nH \]

The digital compensator is implemented by TMS320F2812 DSP chip with DSP program with C language. A 12 bit ADC with 80 ns conversion time is setup for the digital controller in TMS320F2812 DSP chip. The DPWM can support 16 bit maximum resolution [24-27]. From the sections 3.2 and 3.3, this DSP satisfy the digital controller design requirements.

Based on the small signal model of HB DC-DC converter and digital controller design theory, the digital controller is designed in chapter four as follows:

\[
H_c(z) = \frac{0.6113z^3 - 0.2847z^2 - 0.5968z + 0.2992}{z^3 - 1.418z^2 + 0.4619z - 0.04364} \quad (5-1)
\]

The corresponding difference equation is

\[
D[n] = 1.418D[n-1] - 0.4619D[n-2] + 0.0436D[n-3] + 0.6113e[n] - 0.2847e[n-1] - 0.5968e[n-2] + 0.2992e[n-3]. \quad (5-2)
\]

The DPWM generator in the chip can generate symmetrical, asymmetrical and DCS PWM signals for the power stage.
Figure 5.1 shows the primary and secondary gate signals with 100ns dead time in a symmetrical case, which is generated by the DSP chip, TMS320F2812. The two primary signals have the same duty cycle with a 180-degree phase shift, and the secondary signals are the complementary signals of the primary signals with a controlled dead time. In Figure 5.2, the asymmetrical primary-side gate signals are shown with 100ns dead time. Actually, the dead time mentioned above is adjustable with the program.

Figure 5.1: The primary and secondary gate signals with 100ns dead time in a symmetrical case
Figure 5.2: The gate signals with 100ns dead time in an asymmetrical case, the signals are complementary signals with controlled dead time.

Figure 5.3 shows the primary signals with 100ns dead time in a DCS (Duty Cycle Shift) case. DCS control technology is used to reduce primary ringing of the signals [3]. In a DCS case, the two primary signals have the same duty cycle but with a fixed dead time, which is independent of the duty cycle and SR dead time. Figure 5.4 shows the output voltage with significant noise and in this case the output is hard to regulate.
ZVS Dead time is Independent of SR Dead times and Duty cycle

Figure 5.3: The primary signals with 100ns dead time in a DCS case

In the actual experiments, the close loop system was set up with the DSP-controlled HB power train as shown in Figure 5.5. The low-pass filter was used before the DSP board to filter the switching noise. This filter also behaves as an anti-liaising filter for the sampling of the ADC. The protection circuit is used to give a voltage limit from 0 volts to 3 volts for the input signal of the DSP since that is the range the DSP can accept.
Figure 5.4: The output voltage with significant noise

Figure 5.5: Close loop diagram with power stage and DSP controller

Figure 5.6 shows the output voltage and the gate signal for the closed-loop DSP controller. In this case, the input voltage is 48 volts. It can be seen that the output voltage is regulated to the reference voltage of 1.5 volts, which is actually set up in the DSP program. The duty cycle is regulated at $D=0.26$, which is the calculation
result of a digital PI compensator based on the error difference compared with the reference voltage. Figure 5.7 and 5.8 are showing the transformer current at steady state.

Figure 5.6: The output voltage 1.5 volt and gate signal with 0.26 duty cycle at steady state with a DSP controller (digital PI compensator) in symmetrical case

Figure 5.7: The transform primary current
5.2 Consideration and Analysis

5.2.1 Noise Issue

Due to the switching noise and connection noise in the experiment, the low-pass filter is necessary for stability of the system. However, the bandwidth of the low-pass filter obviously will affect the entire bandwidth of the system. This means that if the bandwidth of the low-pass filter is too low, the dynamic performance of the system is going to be affected. Therefore, the tradeoff should be considered before choosing the bandwidth of the low-pass filter when a system has considerable noise.

One of the approaches to reduce the switching noise is to make the sampling happen after the switching noise, which is supposed to appear at the beginning of each switching cycle. This approach needs to synchronize the sampling cycle and the
PWM cycle with fixed phase shift inside the DSP, which will be discussed in the synchronization section of this chapter.

### 5.2.2 Frequency Limitations

The sampling frequency of the ADC of the TMS320F2812 can reach 12.5MHz theoretically. However, the maximum switching frequency at which the converter can be operated is dependent upon the time required by the processor to complete all instructions as well as the performance requirement. Let $\tau$ be the time required to complete one instruction, $N$ be the number of instructions to be computed, $\eta$ be the time required for ADC conversions and other delays and $f$ be the sampling frequency. Then, we must have: $\tau \cdot N + \eta < \frac{1}{f}$.

In the interrupt routine of the ADC, dealing with the data and calculation of the compensator will consume considerable instructions, which makes it impossible to reach the maximum sampling frequency of 12.5MHz for the ADC. In the experiment, the interrupt routine consumes about 100 instructions, which is around 700ns, so the sampling frequency is around 1.4MHz. Therefore, optimizing and reducing the number of the instructions for the compensator calculation and digital filtering is an important issue.

### 5.2.3 Synchronization

Synchronization is an important requirement in any digital controller. Signals
must be sampled at the same relative position in each period, and failing to do so will cause the calculated duty cycle to be meaningless — especially when the ripple amplitudes are significant. For simplicity and ease of implementation, the processor will take control of all signals that determine the start of a period, the sampling time for the input signals and the time needed to issue the duty cycle signal. Furthermore, to minimize the effect of noise, sampling of the input signals is scheduled to take place at the instant before the power MOSFET is switched off.

In short, the period starts when a triggering signal is sent out to sample all the necessary inputs. Immediately after this, the power MOSFET is turned off, and the processor commences to calculate the required value of the duty cycle.

In the experiment, this synchronization has not been achieved yet, so the low-pass filter is used to deal with the switching noise.
CHAPTER SIX: CONCLUSION

6.1 Summary

As the developments made in Digital Signal Processors (DSP) and ICs, digital controls have been an increasingly hot topic in switch mode power converter area. Digital controllers have been used increasingly, especially in complex systems, including power electronics systems. It can be expected that digital controllers will play a more important role in switching power converter as the further advances and cost decrease of the digital controller in the near future.

This thesis presents the unified state space model, analog small signal model and, digital small signal model of the half-bridge converters with current doubler for symmetrical, asymmetrical, and DCS cases. Based on the derived small signal models of HB CDR converters, a digital compensator is designed to stabilize and optimize the system. The digital controller with ADC and DPWM generators is implemented by TI TMS320F2812 DSP chip, which is a high performance DSP chip especially for digital control applications.

Based on the small-signal models, the digital compensator design methods are discussed as well as the ADC and DPWM design rules. Experimental work shows that a digital compensator that is implemented in a DSP program can regulate the output voltage by adjusting the duty cycle for the desired performance.

Moreover, digital voltage driving optimization is proposed and discussed in order to improve the efficiency and achieve better utilization of the digital controller.
The initial experimental results show the efficiency can be optimized by 1% with DVO for the experimental case.

### 6.2 Future Work

In the near future, more attention may be directed towards how to optimize the digital controller, which includes: reducing the number of the instructions to increase the achievable sampling frequency, implementing the synchronization of the sampling and switching cycle, tuning up the coefficients of the compensator, and increasing the bandwidth of the low-pass filter to improve the transient response of the system.

Digital voltage optimization will be finalized with close loop control. The switching converter will be used as variable voltage supply instead of a linear regulator for better efficiency and the technique will be improved as well as the experimental platform in order to obtain better results.

Sophisticated nonlinear algorithms will be one of the potential future research directions in the digital controller to improve system performance, which is one of the advantages of digital controllers over analog controllers.

To take advantage of the digital controller and achieve better utilization of it, more ideas will be investigated based on the digital control implementation.
LIST OF REFERENCES


[40] Zaki Moussaoui, “Digital Vs. Analog Power Control for Microprocessor Core Regulation”, Seminar, APEC 2004

