A High Speed Pulse Code Laser Diode Modulator

1974

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A HIGH SPEED PULSE CODE LASER DIODE MODULATOR

BY

JOHN LAWRENCE McDONOUGH, JR.
B.S., University of Southwestern Louisiana, 1969

RESEARCH REPORT

Submitted in partial fulfillment of the requirements for the degree of Master of Science in the Graduate Studies Program of Florida Technological University

Orlando, Florida
1974
ABSTRACT

A HIGH SPEED PULSE CODE LASER DIODE MODULATOR

BY

JOHN LAWRENCE McDONOUGH, JR.

This research report reviews the basics of pulse code modulation (PCM) techniques and includes a special encoder design for a system which uses a laser diode output for the transmitted pulse. The text discusses PCM and its features, PCM formats, synchronization, and various accepted PCM codes. The encoder circuit design is complete with a description of the circuit, circuit components, and operation. Included are the necessary diagrams, figures, specifications, and parts list. The transmitted output of the design circuit has a repetition rate of one megabit per second.

Approved

Director of Research Report
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INTRODUCTION

This research report reviews the basics of pulse code modulation (PCM) techniques and includes a special encoder design for a system which uses a laser diode output for the transmitted pulse. The text discusses PCM and its features, PCM formats, synchronization, and various accepted PCM codes. The encoder circuit design is complete with a description of the circuit, circuit components, and operation. Included are the necessary diagrams, figures, specifications, and parts list. The transmitted output of the design circuit has a repetition rate of one megabit per second.
A pulse code modulated system provides the distinct advantage of data transmission with excellent noise immunity. Transmission can be via radio frequency signals, hardwire cables, or with light or laser beams. The overall operation of such a system involves:

- Energy conversion to voltage
- Signal conditioning of the data source
- Time sampling
- Conversion of the analog sample to a binary code
- Synchronization
- PCM code selection
- Transmission
- Reception
- Noise removal and clock generation
- Synchronization recognition and data correlation
- Conversion to useable form

The PCM technique is usually used with many data sources of relatively low frequency. Signal conditioning may or may not be necessary. Figure 1 illustrates a typical PCM system. It consists of a commutator to time-division multiplex each sampled information channel, an encoder to convert the sampled input into a discrete
Fig. 1.—A typical PCM system
pattern of pulses representing the binary code including synchronization, a transmitter, and a receiver to detect the information being transmitted over the communication link. A decoder accepts the received pulses from the receiver, separates clock and synchronization from the data, and regenerates the input sample. The decommutator reverses the function of the commutator so that coherent information is presented at the output.

Commutators used in time division multiplexing can be mechanical, electromechanical, or electronic. The mechanical and electromechanical devices are usually motor-driven rotating switches and are limited in operational speeds to a few hundred revolutions per second. These speeds are sufficient for channels in which the signal variations change very slowly. For more rapid signal variations, electronic commutators must be used because only they are capable of the higher rates. Electronic commutators usually consist of a number of gate generators which are interconnected in a manner such that the output gates are enabled one at a time in a definite sequence. A pulse generator (clock) controls these devices.

The encoder changes the sampled input intelligence into a group of pulses which represents the measured variable. Each pulse corresponds to a small portion of the original signal. The device which performs this conversion is known as an analog-to-digital (A/D) converter and the output may be any one of several pulse code modulation waveforms. Synchronization may be inserted into the pulse train by special inputs from the commutator or may be added along with parity and other special information data in the encoder. The encoder output is used to modulate the transmitter.
The transmitter is where the serial information is inserted onto the carrier. Generally the transmitter generates either a frequency modulated (FM) carrier or a phase modulated (PM) carrier. The transmission requirements are bandwidth (determined by the bit rate) and threshold power. Ideally, two samples per cycle of the input information is required, the actual number affecting bandwidth as does the number of binary bits per word. Bandwidth here is the product of the number of samples per cycle and the number of bits per data word. The more bits representing the sample, the greater the resolution, but the basic frequency of the output signal increases resulting in a greater bandwidth for the transmitted signal. Threshold power is the level necessary at the receiver to detect the presence of a pulse. If the pulse power is too low compared to the noise, even the best possible receiver will make mistakes. Generally, the threshold power necessary for acceptable operation requires a signal to noise ratio greater than 20 db.

The receiver serves to detect the information being transmitted. The type of receiver is determined by the transmitted pulse. The receiver circuits should be designed so that maximum gain with minimum noise is provided.

The decoder converts the digital data back to analog form. Synchronization and other extraneous information is processed as intended by the design but does not influence the magnitude of the original analog pulse. The output of the decoder is a series of quantized analog samples.
PCM Formats

PCM data is written in a format constructed of a series of pulses called bits which when grouped form words, frames, and subframes. In PCM we generally have only two symbols to choose from: The logic one (1) bit and the logic zero (0) bit. Complete information transfer is accomplished with these two symbols. The input signal is quantized into discrete voltage levels corresponding to the desired binary code. Table 1 shows the result of quantizing a signal into sixteen levels. Each level is represented by a series of one and zero bits. Other bits may be added to represent additional information; i.e., parity, synchronization, etc. These bit series or syllables represent a PCM word. Every time the input signal is sampled a word is generated.

For a PCM system designed to sample several input variables a definite sequence must be established. A complete cycle of the commutator generates a frame. The frame is composed of words and must include additional synchronization to allow meaningful communication. Figure 2 gives a typical PCM format including bit representation, syllables, words, and frames.

The generation of a format consisting of multiple frames is known as subcommutation and sampling of a particular variable more frequently than once within a frame is called super-commutation.

Synchronization

Synchronization must be acquired and maintained if data is to be successfully processed by the receiving equipment. To insure this
### TABLE 1

**SIGNAL QUANTIZATION**

<table>
<thead>
<tr>
<th>Level</th>
<th>Code</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>1111</td>
<td>9.375 &lt; 10.000</td>
</tr>
<tr>
<td>14</td>
<td>1110</td>
<td>8.750 &lt; 9.375</td>
</tr>
<tr>
<td>13</td>
<td>1101</td>
<td>8.125 &lt; 8.750</td>
</tr>
<tr>
<td>12</td>
<td>1100</td>
<td>7.500 &lt; 8.125</td>
</tr>
<tr>
<td>11</td>
<td>1011</td>
<td>6.875 &lt; 7.500</td>
</tr>
<tr>
<td>10</td>
<td>1010</td>
<td>6.125 &lt; 6.875</td>
</tr>
<tr>
<td>9</td>
<td>1001</td>
<td>5.625 &lt; 6.125</td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td>5.000 &lt; 5.625</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>4.375 &lt; 5.000</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>3.750 &lt; 4.375</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>3.125 &lt; 3.750</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>2.500 &lt; 3.125</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>1.875 &lt; 2.500</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>1.125 &lt; 1.875</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>0.625 &lt; 1.125</td>
</tr>
<tr>
<td>0</td>
<td>0000</td>
<td>0 &lt; 0.625</td>
</tr>
</tbody>
</table>

*Resolution is within 0.625 volts or 6.25 percent of full scale*
Fig. 2.—A typical PCM format
synchronization the transmitted pulses must include information to allow the receiver to generate timing information and provide correlation of the desired data. There are several synchronization methods and combinations of which may be used. These involve bit, word, frame, and subframe synchronization. The data format determines which combinations of these methods may be used.

Since the most rapid signal level changes are at the bit rate, to keep errors to a minimum and generate timing, bit synchronization is often used. This allows signal lock with the incoming pulse train and clock generation within the receiver. Bit synchronization is readily achievable when using certain PCM codes, namely split-phase and return to zero (RZ), if sufficient signal transitions are available.

A PCM word is usually made up of a number of bits. It is also possible to reserve one (or more) of these bits for synchronization purposes. For words up to ten bits long, one-bit word synchronization is generally used, and for words up to twenty-seven bits, a maximum of three bits are reserved for word synchronization. Word synchronization usually represents about ten percent of the word length.

Frame synchronization usually involves at least one word of the frame length. The code for this word should be unique so that it can be distinguished from the data. Frame synchronization is necessary for coherent data display of the commutated signal inputs. At the end of each frame, the synchronization word or words cause the decoder to reset and thus prepare to count the words in the next frame. Synchronization patterns which require no bit errors work
well when signal-to-noise ratios are sufficient to provide easy detection by the receiving circuitry. Majority logic recognition however, allows the use of pseudo-random patterns and bit errors within the sync patterns. The pattern recognizer used with the majority logic patterns operates by outputting a discrete level for each bit agreement and the accept criteria is determined by the number of bit errors allowed.

Subframe synchronization and synchronization modes (search and lock) are but additional extensions of these concepts.

**PCM Codes**

Once we have the binary data in serial form it can be converted to whatever PCM code is appropriate for the transmission and receiving equipment. The Inter-range Instrument Group (IRIG) has standardized several transmission codes. These are return-to-zero (RZ), non-return-to-zero and Bi-phase. These seven standard codes are illustrated in figure 3. Included are three distinct variations of the NRZ, and Bi-phase, specifically the level, mark, and space forms.

The RZ pulse code modulation is a method in which a binary One is represented by a PCM One for the first half of a bit period and a PCM Zero for the last half of a bit period. A binary Zero is a PCM Zero for the entire bit period. This code requires dc response in all processing equipment. Clock information is not provided when all zeros are sent. The RZ code results in a maximum frequency equal to the bit rate when transmitting all one's.

The three NRZ codes all have the same advantages and disadvantages.
RZ
"One" is represented by a half-bit wide pulse
"Zero" is represented by no pulse condition

NRZ-Level
"One" is represented by one level
"Zero" is represented by the other level

NRZ-Mark
"One" is represented by a change in level
"Zero" is represented by no change in level

NRZ-Space
"One" is represented by no change in level
"Zero" is represented by a change in level

Bi-Phase-Level
"One" is represented by a 10
"Zero" is represented by a 01

Bi-Phase-Mark
A transition occurs at the beginning of every bit period
"One" is represented by a second transition ½ bit period later
"Zero" is represented by no second transition

Bi-Phase-Space
A transition occurs at the beginning of every bit period
"One" is represented by no second transition
"Zero" is represented by a second transition ½ bit period later

Fig. 3.--PCM transmission codes
They require dc coupling and pre-modulation filters may cause problems. The advantage of the NRZ type is that they generate a maximum frequency equal to one-half the bit rate. This eases bandwidth requirements. The mark and space codes also provide immunity to ambiguity of data.

The NRZ-L code provides a one-to-one correspondence between the binary ones and zeros and the PCM ones and zeros. NRZ-M is a method of modulation with a change of PCM bit state for each binary One. There is no change of PCM bit state for a binary Zero. NRZ-S represents a One by no change in level and Zero by a change in level.

The split phase codes offer the advantage of using an alternating current (ac) coupled system. The bandwidth however is the same as the bit rate.

Bi-\(\phi\)-L uses one cycle of the coherent carrier per bit period and a 180 degree phase reversal to distinguish between the Ones and Zeros. Bi-\(\phi\)-M is a combination of the split phase and NRZ-M codes which has a 180 degree phase reversal of the coherent carrier for each binary One and no change of phase for a binary Zero. Bi-\(\phi\)-S provides a transition at the beginning of every bit period later.
CHAPTER II

PCM ENCODER DESIGN

Design Circuit

This section considers the design of the encoder and transmitter portion of a PCM system using a laser as the communication link. It involves time sampling of the input signal, conversion of the analog sample to binary form, synchronization, PCM code selection, and transmission of the resulting serial data. The encoder design is specifically for pulsing the laser at high repetition rates.

A block diagram of the encoder circuit is shown in figure 4. The input is a single time varying analog signal with a cyclic rate (frequency) to 50 thousand Hertz. The output is a binary serial pulse train capable of pulsing the laser diode driver at a rate of one megabit per second. The encoder provides eight bit resolution of the analog input, a parity bit, and a unique two bit synchronization pattern.

The PCM code selected for pulsing the laser diode is a modified return-to-zero (RZ) signal, selected in this case for its simplicity, ease of synchronization, and application to laser diode characteristics. It specifically considers the low duty cycle requirement of laser diode devices.

The laser diode and drive circuit are included in the block diagram of the encoder even though they are not part of this function.
Fig. 4.--Encoder block diagram
Fig. 5.—Timing diagram
Fig. 6.—Encoder wiring diagram
Fig. 7.—Laser drive circuit
# TABLE 2

## PARTS LIST FOR PCM LASER DIODE MODULATOR

<table>
<thead>
<tr>
<th>Description</th>
<th>Part Number</th>
<th>Symbol</th>
<th>Manufacturer</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample-Hold</td>
<td>SHA-2A</td>
<td>U1</td>
<td>Analog Devices</td>
<td>1</td>
</tr>
<tr>
<td>Analog-to-Digital Converter</td>
<td>ADC -QU</td>
<td>U2</td>
<td>Analog Devices</td>
<td>1</td>
</tr>
<tr>
<td>Shift-Register</td>
<td>5496</td>
<td>U3,4</td>
<td>Fairchild Semiconductor</td>
<td>2</td>
</tr>
<tr>
<td>Monostable Multivibrator</td>
<td>SN54121</td>
<td>U5</td>
<td>Texas Instruments</td>
<td>1</td>
</tr>
<tr>
<td>Monostable Multivibrator</td>
<td>SN54123</td>
<td>U6</td>
<td>Texas Instruments</td>
<td>1</td>
</tr>
<tr>
<td>Parity Generator</td>
<td>SN54S280</td>
<td>U7</td>
<td>Texas Instruments</td>
<td>1</td>
</tr>
<tr>
<td>OR Gate</td>
<td>SN5432</td>
<td>U8</td>
<td>Texas Instruments</td>
<td>1</td>
</tr>
<tr>
<td>AND Gate</td>
<td>SN54LS08</td>
<td>U9</td>
<td>Texas Instruments</td>
<td>1</td>
</tr>
<tr>
<td>Decade Counter</td>
<td>9310</td>
<td>U10</td>
<td>Fairchild Semiconductor</td>
<td>1</td>
</tr>
<tr>
<td><strong>Misc. Components</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistors,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Variable(10KΩ)</td>
<td>-</td>
<td>R1,2</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>Resistor(2MΩ)</td>
<td>-</td>
<td>R3</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Resistor(30KΩ)</td>
<td>-</td>
<td>R4</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Resistor(10KΩ)</td>
<td>-</td>
<td>R5</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Capacitor(10 pf)</td>
<td>-</td>
<td>C1</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td><strong>Driver Circuit:</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor</td>
<td>RCA</td>
<td>Q1</td>
<td>2N5918</td>
<td>1</td>
</tr>
<tr>
<td>Transistor</td>
<td>RCA</td>
<td>Q2, Q3</td>
<td>2N6105</td>
<td>2</td>
</tr>
<tr>
<td>Capacitor(0.01pf)</td>
<td>-</td>
<td>C3</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Capacitor(0.47pf)</td>
<td>-</td>
<td>C1</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Capacitor(0.33pf)</td>
<td>-</td>
<td>C2</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Resistor(3.9Ω)</td>
<td>-</td>
<td>R2</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Resistor(100Ω)</td>
<td>-</td>
<td>R1</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Resistor(3.3Ω)</td>
<td>-</td>
<td>R3</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Diode</td>
<td>-</td>
<td>CR1</td>
<td>1N4007</td>
<td>1</td>
</tr>
<tr>
<td>Laser Diode</td>
<td>C30025</td>
<td>CR2</td>
<td>RCA</td>
<td>1</td>
</tr>
</tbody>
</table>
The drive circuit supplies the high current necessary to cause the laser diode to generate light by lasing. The current requirement is five to eight amperes with a pulse width of less than 50 nanoseconds. This corresponds to the laser diode duty cycle at the cryogenic temperature and a one megabit repetition rate. Smaller pulse currents down to the lasing threshold allow operation at higher temperatures provided the reduced power output of the laser is acceptable to the receiving equipment.

A timing diagram for the encoder is given in figure 5. It indicates the necessary timing and pulse widths associated with the design. The timing pulses involved are a clock pulse, decade counter, parallel load/synchronization, convert command, status, and the series data. The dashed lines in the diagram indicate the signal prior to the one-shot devices which further shape the pulses.

The wiring diagram for the PCM encoder is given in figure 6 and in figure 7 is the drive circuit and laser diode. These diagrams include all the components and their electrical interconnections.

The required parts list for the design is given in table 2. This table gives the device type, part number, recommended manufacturer, and the quantity necessary for circuit assembly.

All appropriate component specification sheets are readily available from the appropriate vendor.

**Component Description**

The components of the PCM encoder, laser, and drive circuit
involve: 1) Sample hold; 2) A/D converter; 3) Shift register(s); 4) Parity generator; 5) Multivibrator(s); 6) Positive and/or logic; 7) A laser diode driver; and 8) the laser diode. A description of these devices is given below.

Sample-Hold Device

This device is a typical sample-and-hold module in that it consists of an input isolator, a fast switch, the storage element, and an output buffer. It is compatible with converters which convert within one micro-second. Data may be acquired from fast slewing signal sources. The slewing rate is 100 volts per micro-second with settling time to within 0.01 percent in less than 500 nano-seconds. The aperture time is less than ten nano-seconds, with a jitter of 0.25 nano-seconds. The maximum droop rate is 100 micro volts per second.

A/D Converter

This unit provides eight bit resolution with a plus or minus one-half least significant bit (LSB) accuracy. It uses the techniques of successive approximation to convert analog input voltages to equivalent binary output numbers. The total conversion time is less than 6.4 micro-seconds. The analog input span is zero volts to ten volts with the data outputs being parallel. The device provides its own internal clocking and gives a status output for synchronization with other components.

A convert command initiates each program with the leading edge of
the pulse resetting previous data and the trailing edge starting the conversion. This pulse must be greater than 100 nano-seconds. Special adjustment of the zero offset and gain is necessary for proper operation.

**Shift Register**

Two five bit parallel-to-series shift registers are required to accept the eight bits of parallel data from the A/D converter, a parity bit from the parity generator, and one bit of the word synchronization pattern. Operation speed of these shift registers is to ten mega-Hertz. The parallel loading is accomplished by putting a high (Logic One) on the parallel load input. It is independent of the clock input. The transfer of information to the output pins occurs when the clock input goes from low to high; hence, information to be transferred must be available prior to the rising edge of the external clock input waveform.

**Parity Generator**

An odd/even parity bit is provided by the nine-bit parity generator. Output delay time is less than 18 nano-seconds.

**Multivibrators**

The circuitry uses three multivibrators for pulse shaping; one single output and a dual output type. Both are monostable devices. The dual output multivibrator features direct current (dc) triggering from gated low level and high level inputs. They provide a propagation delay of 23 and 28 nano-seconds, respectfully.
Output pulse widths as small as 65 nano-seconds can be obtained. The devices are used for the convert and parallel load/sync signal pulse width control. Duty cycles to 90 percent are achievable.

The single output multivibrator has schmitt trigger inputs which allow jitter free triggering and provides excellent noise immunity. It is used to shape the input pulse of the laser diode drive circuit; the maximum output pulse width being less than 50 nano-seconds. Once fired the output pulse is independent of further transition and is a function only of the timing components. Input pulses may be of any duration relative the output pulse. The pulse width is virtually independent of the supply voltage and temperature, with a duty cycle as high as 90 percent achievable.

Positive and/or Logic

These devices are quadruple two input gates having totem pole outputs. They are used in the modulator circuit to provide the appropriate signal output combinations and for timing delays. Two "and" gates and one "or" gate are required in the modulator circuit. The propagation delay for the and/or gates is a maximum of 24 and 15 nano-seconds, respectively.

Decade Counter

This device is a high speed synchronous decade counter. The device provides a terminal count (TC) output on the leading edge of every tenth clock pulse waveform and is reset with the leading edge of the following clock pulse. The turn on/turn off delay to the TC is less than 35 nano-seconds.
Laser Diode Drive Circuit

This circuit provides the high current for the laser diode. An output from five to eight amperes is required of the device at small pulse widths consistent with the duty cycle of the diode. Pulse widths at these currents have been recorded down to ten nano-seconds. The input should be less than forty volts. All transistors are radio frequency (RF) power devices.

Laser Diode

This diode type represents the latest step in the semiconcductor technology. It is a Gallium-Arsenide large-optical-cavity (LOC) device and requires lower threshold current densities, and lower drive currents. High repetition rates to one megahertz have been recorded for these devices. The diode draws between five and eight amperes, a value which is denoted specifically for each item. The operating current density is 15,000 amperes per square centimeter. The duty factor is one percent at room temperature and four percent at the cryogenic temperature of 77 degrees Kelvin. The output wavelength is in the vicinity of 900 nano-meters.

Circuit Operation

The laser diode pulse code modulator design converts a zero to ten volt analog input signal into a series of binary data bits with pulse widths of less than 50 nano-seconds. Sampling is accomplished with a sample-hold device which inputs an eight bit A/D converter. The eight bit parallel output of the A/D converter is transferred into the two five bit shift registers along with a
parity bit and one bit of the word synchronization pattern. The data is clocked serially through the and/or logic to the laser driver one-shot and pulses the laser diode drive circuit creating lasing action from the laser diode. The decade counter provides a pulse for every ten external clock cycles and is used to generate the A/D convert command, parallel load signal, and word synchronization pulse. These pulses are shaped by the two multivibrator circuits to the desired waveforms. These pulses are 100 nano-seconds in duration. The rising edge of the convert command sets all outputs of the A/D converter to zero and conversion begins with the trailing edge of the pulse. All data processing in the shift register occurs with a rising waveform. A status command is given by the analog-to-digital converter which goes high when the conversion is complete. This allows the sample-hold device to sample. This pulse occurs within 6.4 microseconds after the trailing edge of the convert command. The parallel load/word synchronization pulse shifts the parallel output of the A/D converter after processing the ten bits of information in the shift registers. The signal occurs prior to the generation of the convert command. The parallel load/word synchronization pulse is generated by the decade counter terminal count and the not clock pulse signal ($\bar{C}_p$). In addition to inputting the shift register this pulse also forms the remaining part of the synchronization pattern. A timing diagram is shown in figure 5.

The data word pattern for the PCM modulator is given below:

<table>
<thead>
<tr>
<th>2</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
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| PARITY | DATA | SYNC |
There are eight data bits, a parity bit, and an always high bit which is part of the synchronization pattern. The other part of synchronization is the parallel load/word synchronization pulse generated between two of the normal pulse times. It is to synchronize the receiver to the data word, while the always high bit is used to generate clocking. Timing is such that the clocking pulse follows immediately the unique off-frequency word synchronization pulse. The eight data bits are then received beginning with the most significant bit and ending on the LSB. The final bit of the data word provides a parity check, being high if the number of high data pulses is odd. A total of eleven pulses make up the data word.

Propagation delays are indicated in the timing diagram, though no significant problems are obvious as the result of these circuit imperfections. The delay of the data from the shift register is less than 200 nano-seconds. The overall delay from the input is ten micro-seconds.

Design Specifications

The input requirements and operation characteristics of the laser diode modulator design are given below:

Input Power

Four external voltage inputs are necessary to operate the PCM circuit. These are plus and minus 15 volts dc, plus 5 volts dc, and plus 40 volts dc. The tolerances and current requirements are given below:

+ 15 volts ± 2 percent at 125 milli-amperes
- 15 volts ± 2 percent at 150 milli-amperes
+ 5 volts ± 5 percent at 750 milli-amperes
+ 40 volts ± 5 percent at 10 amperes

It is recommended that separate analog and digital grounds be provided in the circuitry.

External Clock

A clock signal must be available as an input to the circuit. It must have at least a one mega-hertz frequency capability with a fifty percent minimum duty cycle. The clock output should be transistor-transistor logic (TTL) compatible and provide a 500 nano-second output pulse. Stability should be no less than 0.15 percent.

Input Signal

The PCM circuit is designed for one analog input signal; the voltage range being zero to ten volts (single ended). The input impedance is $10^{11}$ ohms and 7 pico-farads (pf). The input bias current is 100 pico-ampere maximum.

The sampling rate of the input signal is 100 kilo-hertz.

Output Signals

The PCM output signal prior to the laser diode drive circuit is a series of pulses representing an eleven bit modified RZ PCM code. The PCM word includes eight data bits, a parity bit, and a unique two bit synchronization signal. The pulses have the following characteristics:

- A bit rate of one mega-bit per second plus or minus 0.15 percent
• Voltage amplitude:
  1) A logic Zero is zero to plus 0.4 volts dc
  2) A logic One is 2.4 to 3.5 volts dc

• The pulse duration is nominally 30 nano-seconds and 50 nano-seconds maximum

• The propagation delay is 6.6 micro-seconds maximum

Laser Diode Output

The laser diode is pulsed with a repetition rate up to one mega-hertz and emits a total peak radiant flux (\(\Phi_M\)) of 0.5 watts minimum at the maximum forward current (\(I_{FM}\)). The output wavelength is in the vicinity of 900 nano-meters. The pulse duration is typically 30 nano-seconds and is always less than 50 nano-seconds. The minimum threshold current is 1.5 amperes with the forward current maximum being between five and eight amperes. The duty factor for the device is one percent at 27 degrees centigrade, increasing to about four percent at the cryogenic temperature of 77 degrees Kelvin. Cooling of the diode is required for the high repetition rate in the design if the maximum output power is required.
This research report provides a pulse code modulator circuit design for a high speed laser diode. The design is complete with a description of the circuit (timing, block, and wiring diagrams), parts list, and specifications. It represents present state-of-the-art capabilities using existing commercially available components.

The circuit involves an encoder, laser diode drive circuit, and a high speed laser diode. The encoder converts a fifty kilohertz time varying analog input into an eight bit binary signal, provides synchronization and parity information, and pulses the laser diode drive circuit. Pulse widths are less than 50 nanoseconds at currents between five and eight amperes. The transmitted output has a repetition rate of up to one megabit per second.

The synchronization of the binary word generated by the encoder is unique in that one of the two pulses utilized for this function occurs between normal bit times. This pattern allows improved detection of the synchronizing signal without increased word length. The other synchronization pulse can be used to provide clock generation in the receiving equipment.

External inputs required by the design involve four power supplies (± 15, + 5, and + 40 volts) and clock signal generation.
BIBLIOGRAPHY


