Digital Communication Systems Technical Control

1975

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DIGITAL COMMUNICATION SYSTEMS

TECHNICAL CONTROL

BY

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B.S.E.E. UNIVERSITY OF ILLINOIS, 1958

THESIS

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ABSTRACT

This is a study of the methods of control of an advanced military communication system. The Tactical Communication Control System has been conceived to meet the demands of military users which are currently both analog and digital but steadily evolving to all-digital. It is a study of the design and application of multiplexers, modems, processors, switches, and other nodal equipment to accommodate communications among telephone and data users in a tactical environment. The main points of interest are the communication node and the control techniques used to carry out system objectives.
The purpose of this thesis is to probe into the many facets of control of a modern digital communication system. The subject of the study is the military Tri-Services Tactical Communication Control System (TCCF). The system is in the conceptual stages and, while a great deal of work has been done in these areas, a system of this scope and complexity has not yet been designed or developed. An in-depth study of the system is therefore appropriate because it represents a significant advancement in the state-of-the-art of technical communication control.

Communication systems are rapidly changing from analog to digital. Not only is a greater proportion of traffic now originating from digital sources (such as teletype, computer, facsimile, etc.) but also the main traffic load from the voice telephone is phasing into the digital realm. The impact from the advent of digital voice has been great enough so that by the mid 1980's, the basic texture of the communication system will have gone from hybrid mixes of analog and digital to all-digital users. The TCCF has been conceived with the transition period in mind (e.g., to accommodate both analog and digital users in its first implementation and eventually to evolve exclusively to digital).

Much of the work for this thesis was done by the author as a preparation for the design and development of the TCCF system. Background material has evolved from various sources that, although not appropriate for reference citation, are nevertheless basic to the formulation of the system design and concepts. Such things as military specifications, concept papers, equipment designs, and a variety of discussions
on the subject have contributed immeasurably to the formulation of the
data base that went into preparation of the thesis.
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INTRODUCTION

Technical control is the management of communication resources to accomplish the objectives of the communication mission. This is a study of the methods of control of an advanced digital communication system - the Tri-Services (TRI-TAC) digital communication system. Communication resources in this case include all equipment at the communication node, the multiplexers, modems, processors, switches, radios, and operating personnel. The objectives of the communication mission, broadly stated, are to accommodate communication among all telephone and data users in a tactical, highly flexible deployment of land or sea forces.

Operation is centered around a communication node containing an automatic switch with multi-link access via cable and radio, and a technical communication control facility (TCCF) that coordinates operations at the node. It is the Communication Nodal Control Element (CNCE) of the TCCF that is the focal point of this study. The communication and study techniques used are critiqued and areas of particular interest are analyzed. Areas of concentration are traffic processing (i.e., multiplexing and switching, transmission, processor control, nodal timing and synchronization, quality monitoring and communications supervisory control).
CHAPTER ONE

THE TECHNICAL COMMUNICATION CONTROL FACILITY

INTRODUCTION

Present tactical communication systems in the field are generally analog, manual-switched systems with a high dependence on dedicated circuits for handling critical command traffic. These systems, in general, also provide parallel alternate routes for critical circuits. This concept is inefficient in terms of transmission facilities. Furthermore, the systems are slow to react in dynamic tactical situations. The planned TRI-TAC program will provide automatic message and circuit switching capabilities for tactical systems as well as base for evolution toward totally secure digital networks. These new tactical communication capabilities combined with the changing demands placed on deployed networks resulting from changing traffic patterns, network outages and equipment degradation require a Technical Communication Control Facility (TCCF) capability not presently available in commercial, tactical, or strategic communications systems. Other systems do not place such a demand on the network controller. Of great importance is the ability of the controller to select, display, and assess pertinent information on the current status of the system configuration. After appropriate evaluation and assessment of the data, execution of various options can be effected that will optimize the performance of the available network resources in near real-time.

The Technical Communication Control Facility is composed of two major elements: a Communication System Control Element (CSCE), and a Communication Nodal Control Element (CNCE). The CSCE is the higher
element in the control hierarchy, providing direction and authority to several nodes as shown in Figure 1. Other communication elements that are involved are a Communications System Planning Element (CSPE) which provides overall planning, and the Communication Equipment Support Elements (CESE) which are subordinate to the CNCE and generally provide specific equipment functions such as switching, radio transmission, power, and others that interface with the CNCE.

Figure 2 is representative of the conceivable nodal configurations that could exist in a network during the present time frame. As may be noted, it is possible to have 4-kHz analog telephones, frequency-division multiplex (FDM) analog trunks, asynchronous digital signals, pulse-code modulation (PCM) voice, time-division multiplex (TDM) digital groups, continuously variable slope delta (CVSD) digital voice, and both secure and nonsecure circuits in the same network. The present plan is that networks will evolve to a TDM all-digital system with CVSD voice circuits and end-to-end, all-secure circuits.

OVERVIEW OF THE CSCE

The CSCE provides the major system control capability for a portion of the tactical communication network, offering real-time management of the network during continually changing connectivity patterns and traffic loads. The configuration comprises two shelters such as those shown in Figures 3 and 4 illustrating the CNCE, and a facilities pallet. One shelter is identified as the Management Shelter and contains consoles for three network controllers. Visual display units and hard copy printers are the interface between the controllers and a data processor. The processing capability provides a variety of aids to the
Figure 1. TCCF Control Hierarchy
Figure 2. Possible Nodal Configurations in Tactical Communications Network
controller that quickly and accurately report the network statistics and near real-time information. A controller can rapidly display, review, and direct changes to maintain maximum system operability through the use of the computational resources and data files of the subsystem.

The second shelter is designated as the Technical Shelter and contains such major elements as a communications subsystem providing inter- and intra-shelter voice and data transmission; a control subsystem that directs various control and message handling operations; and a set of processors and peripherals that make up the processing capability. An operator's console is provided in this shelter that allows monitoring and control of the CSCE equipment, patching of communication lines, equipment fault detection and isolation, and similar housekeeping functions.

The facilities pallet contains an environmental control unit (ECU) for each shelter and a common power unit. The power unit provides standard power voltage and frequency to the shelters regardless of the primary source characteristics. It also contains sufficient battery power to sustain temporary operation if primary power is lost.

OVERVIEW OF THE CNCE

The CNCE provides control for the communication nodes within the tactical network, serving as the interface between users and the transmission facilities of the node, providing real-time management and monitoring of the communication resources at the node during continually changing traffic loads connectivity patterns, with interoperability of both analog and digital inventory of equipment.

The configuration comprises two shelters shown in Figures 3 and 4.
Figure 3. Type II Management Shelter
Figure 4 Type I CNCE Technical Shelter
together with one environmental control/power pallet for the CNCE system. One shelter is identified as the Management Shelter and contains a visual display unit to provide the interface between the controller and the data processing unit, quality monitoring equipment, COMSEC, and other digital signal processing equipment. The processing capability provides a variety of aids to the controller that report equipment status, channel and group interconnect information, network status, and real-time equipment diagnostics information and network link quality status. A controller can display, review, and direct channel/group data changes and equipment changes to maintain maximum system operability.

The second shelter is designated as the Technical Shelter and contains patching facilities, orderwire circuits/select panel, timing module, and an operator's console and visual display unit. This console allows monitoring and control of the equipment within the technical shelter and status interface with the management shelter.

The facilities pallet contains an environmental control unit for each shelter and a common power unit. The power unit provides standard power voltage and frequency to the shelters regardless of the primary source characteristics. It also contains sufficient battery power to sustain temporary operation if primary power is lost.

SYNOPSIS OF STUDY ITEMS

The unique position of the CNCE being the focal point of nodal activities in the tactical communication system affords an ideal opportunity to examine the wide variety of communication techniques used in the most advanced of all practical voice and data communication systems. Therefore, the emphasis of this study will be on the CNCE and
will only include the CSCE or other CESE as they directly support CNCE operations. The following is a summary of the system techniques to be examined.

System Operation

A description of the communication system, how it is used, and what some of the problems are. This discussion provides a framework for understanding how the system elements work together. It also provides the scope of the study. The subsystems are described in their functional usages. The supervisory function associated with technical control (such as orderwires, traffic control, and processor control) is also discussed.

Traffic Processing

A study of the methods of processing the digital links at the communication node; these are mainly multiplexing and switching operations. The methods of time-division multiplexing is discussed with frame synchronization, multiplexer hierarchies, asynchronous and synchronous combining, bit stuffing, and related techniques analyzed. A method of time-division switching is also discussed as an alternate to space-division switching.

Transmission

The transmission system is analyzed with methods of coding for cable transmission such as bipolar and dipulse and diphase coding examined. Optimum detection methods are also included. A system of supervisory channels imposed in-band and out-of-band on the transmission system is studied.

Processor Control
The function of a processor in the communication node as a means of automatic control and analysis is studied with the role of the processor in traffic load balancing analysis of quality of the links and status display analyzed.

**Timing, Link Synchronization**

The effects of timing differences between master timing systems (atomic clocks) of separate nodes is studied. Elastic buffering techniques and techniques to maintain and restore bit-count integrity (BCI) are also studied.

**Quality Monitoring**

Methods for determining the quality of the transmission links and equipment and nodal equipment are studied. A method of predicting bit-error rates (BER) by observing radio baseband eye patterns is also analyzed.

**Communications Supervisory Control**

The methods for communication between controller by orderwire and supervisory channels (both in-band and out-of-band) in the system of multiplexed links are studied. Methods of combining and interfacing low data rate PCM systems for this use are also studied.

**Frame Synchronization**

Frame synchronization is studied as it applies to the requirements of the transmission links with special emphasis on the effects of bit errors caused by radio fades. A comparison is made of three candidate systems, one of which has been designed and recommended by the author.

**Further Study**

Two specialized studies are suggested as a result of these inves-
tigations for making more optimum equipment designs. They are the further study of the telemetry combining techniques at remote sites and a determination of the feasibility of integrating multiplexers and cable modems into one design.
CHAPTER TWO
SYSTEM DESIGN

NATURE OF THE COMMUNICATION LINKS

Communication links that enter and leave the CNCE (i.e., those that are under the auspices of the nodal controller) can be divided into the three general categories of traffic links, control links, and test signals (Figure 5). Traffic links are those that are used by a subscriber; they originate in a field telephone, teletype machine, or computer. Control links are those that are used by communication facility supervisors, maintenance personnel, administrative personnel, or others to control the communication resources of the network. Test signals are those that are passed between elements for the purpose of maintaining the equipment; they include equipment status, test messages, test commands, etc.

An understanding of the flow of signals within the CNCE is helpful in determining the functions of the CNCE subsystems and their interactions with external devices. Refer to Figure 6 for a summary signal flow.

Traffic Signals

Subscribers may use either analog or digital telephones for voice communications; these are referred to as loops. Analog loops are normally 4-kHz signals. Digital loops may originate in digital telephones, which include 32-kb/s CVSD converters in the instrument. Analog signals may be carried throughout the system as loops or multiplexed into digital groups by multiplexers that perform analog-to-digital (A/D) conversion and time-division multiplexing. The basic group multiplexer,
Figure 5. Classes of Signal Flow Through CNCE
Figure 6. CNCE System Signal Flow Block Diagram
the TD-660, accepts twelve analog loops, quantizes each into 6-bit PCM, and transmits a 48-kb/s loop complete with framing pattern. One basic group is therefore a 48-kb/s PCM group. There are higher order groups formed from this basic rate that take a multiplexer up to a 4.9152-Mb/s supergroup rate. A table of these rates and trunking hierarchies is shown below.

<table>
<thead>
<tr>
<th>Channel (No.)</th>
<th>Rate (kb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>48</td>
</tr>
<tr>
<td>12</td>
<td>576</td>
</tr>
<tr>
<td>24</td>
<td>1,152</td>
</tr>
<tr>
<td>48</td>
<td>2,304</td>
</tr>
<tr>
<td>96</td>
<td>4,608</td>
</tr>
<tr>
<td>96</td>
<td>4,915.2, asynchronous</td>
</tr>
</tbody>
</table>

Loops originating in digital telephones at the 32 kb rate can be combined into groups, trunks, or supergroups in multiplex of 32 kb up to the supergroup rate of 4.9152 mb. Rates in these hierarchies are shown in Table I-2.

<table>
<thead>
<tr>
<th>Channel (No.)</th>
<th>Rate (kb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td>4</td>
<td>128</td>
</tr>
<tr>
<td>4.5</td>
<td>144</td>
</tr>
<tr>
<td>7</td>
<td>256</td>
</tr>
<tr>
<td>9</td>
<td>288</td>
</tr>
<tr>
<td>16</td>
<td>512</td>
</tr>
<tr>
<td>18</td>
<td>576</td>
</tr>
</tbody>
</table>
Teletype traffic may be passed in single loops of 45 baud to 150 baud, depending upon the operating speed of the originating machine. These loops may be combined by teletype combiners into trunks of 300 to 1200 baud.

Control Signals

These signals which are used by the network controllers, form a special network of orderwires, dedicated links, and supervisory channels overlaid on the traffic network. The traffic controllers use the same types of instruments as used by subscribers, analog and digital telephones, and teletype machines. In addition, computer-to-computer links at 2.4, 16, and 32 kb/s are used. Telemetry signals used to report status of remote equipment are passed to the controller by 150-b/s, 2-kb/s, and 4-kb/s links that are combined into trunks of 2, 4, 2.4, 16, or 32 kb/s, depending upon the complexity of the remote transmission path and the multiplexer hierarchial combining required en route to the CNCE.

Test Signals
Test signals are those used throughout the network to determine link status or to isolate faults. They include pseudorandom sequences as test multiplexes, tones, and DC signals.

**SYSTEM OPERATION, MANAGEMENT, AND CONTROL**

The Communications Nodal Control Element (CNCE) is designed to accommodate both existing analog and digital inventory equipment, but emphasizes the evolution to an all-digital system. This includes manual analog and DC patching; automated channel reassignment through time-division switching; processor control for re-routing and system control; real-time test and quality monitoring subsystem; advanced techniques for Bit-Count Integrity (BCI) restoral and prevention of synchronization loss.

As its prime missions, the CNCE provides the interface between transmission facilities and users, and the management of communication resources at its node. To accomplish its mission, the CNCE is provided with a group of functional subsystems and capabilities. These are the Patch and Test Subsystem, Control Communications Subsystem, Control Subsystem, Processor Subsystem, timing and synchronization capability, COMSEC capability, and Facilities Subsystem.

The functions provided by these subsystems are classified as management and technical direction; implementation and execution; line conditioning and interfacing; technical coordination; monitoring and fault isolation; re-route and restoral; reporting; and record keeping. The resources provided at the CNCE are therefore used by the operating personnel to accomplish these functions and fulfill its mission.
The system considerations included in the baseline design are:

- Management and technical direction of the node and its subordinate elements.
- Implementation and execution of directives from other TCCF elements.
- Line conditioning and interface for the various users.
- Technical coordination activities with the CSCE, other CNCE's, and other subordinate elements.
- Performance assessment of all lines and communication resources related to its node.
- Fault isolation for degraded/failed equipment and circuits.
- Re-routing and restoring various types of network circuits, as required.
- Reporting and record keeping for monitoring nodal resources status and performance.

THE ROLE OF THE PROCESSOR SUBSYSTEM

The fact that a processor is used as a primary element of nodal control is a significant advance in the state of technical control. In the past, such functions as traffic routes, status of equipment, quality of the transmission medium, control directives, message routing, alternate routing, and traffic profiles were kept by manual means and records stored in conventional files. With the complexities involved in present day communication, it is natural for these efforts to be taken over by a processor.

The processor acts as a central point of access and control for
any data generated on the links, providing the current status of the communications plant. The processor receives 150-b/s telemetered data from every unit of equipment to which it is connected and displays alarm conditions when there is a malfunction. A data base is maintained that stores the network connectivity so that upon request, alternate routing of trunks may be displayed to the operator. An I/O-to-I/O link is maintained between all network processors so memory and load sharing can take place between them. One processor may substitute operation for another in case of emergency. All appropriate records and directives are maintained in disc or magnetic tape files to be recalled upon request.

The processor stores operating criteria for equipment or link quality and sets alarms if the BER or signal-to-noise margins are exceeded anywhere. The circuit monitoring data amassed in this manner is subjected to predictive trend analysis within the processor and possible problem circuits brought to the attention of the controller through use of the visual display unit. Link quality can be assessed over a period of time so degradation trends can be established. After receiving a bad trend alert through the display, the controller can call up other data base information to help him in his decision of how best to repair, alternate route, or restore the troubled circuit. Finally, after the decision is made, the controller can direct a patch to be made on an analog circuit at the patch panels in the equipment shelter or, in the case of the digital circuits, he can re-route it through the computer or directly from the control panel on the console in the management shelter. Re-routing of digital circuits is performed using the
channel/group reassignment function previously described. The processor has a complete set of peripheral equipment (i.e., teletype, keyboard, hard copy printer, visual display unit, disc and magnetic tape storage, keypunch, card file, and other operating equipment).

Operational/Aplications Software

The TCCF operational/application software consists of those modules that are required to perform the overall network controlling functions. These groups of modules establish and maintain the logical interface between network nodes as well as between subsystems within a node. They are responsible for network integrity and provide dynamic control of the network by constantly monitoring the status and adapting to changes in the environment. To accomplish this task efficiently, a multiple processing scheme of the operating system is employed.

CSCE System Fault Detection and Diagnostics

For the CSCE to fulfill its mission, not only must the processing function have full back-up capability, but also must use the Control and Communication Subsystem to provide for signal control and monitoring of the element. Inherent diagnostics, self-test, and redundancy features are available to assure extremely high CSCE mission availability. Diagnostics in the CSCE may be categorized in the following manner:

1. **ON-LINE SYSTEM** diagnostics.
2. **ON-LINE EQUIPMENT** diagnostics.
3. **OFF-LINE PROCESSOR** diagnostics.

CNCE Computer, With Display and Software, Aids In Rapid Circuit Analysis and Restoral
A minicomputer, with an associated display and a modular software approach, is used in the CNCE because of the ability of this combination to provide the most cost-effective solution to the problem of aiding the controller in his functions of Quality Assurance. As mentioned above, provision of automatic digital and analog test equipment and circuit access allows quality assurance to be carried out by the processor.

**Systems Software**

A general-purpose and comprehensive systems software package is used to support and control the TCCF software. The software modules are configured easily to support the wide variety of equipment to be installed in the CSCE and CNCE. At the heart of the systems software package is a real-time, communications-oriented operating system. Under control, and an integral part of the system, is a host of support software programs handling such features as:

- Multi-programming or multi-tasking support.
- Automatic task scheduling and rescheduling.
- Priority task execution.
- Dynamic memory management.
- Input/output processing.
- Data base management.
- Background assembly and compiling.
- Full-scale man/machine interface via the real-time executive.

**COMMUNICATION SECURITY**

One of the most fundamental reasons for the conversion from analog to digital transmission is for security. A digital bit stream can be
encrypted in a much simpler operation because of its discrete nature. A simple message scrambler, for instance, can be made by modulo 2 addition of a known pseudorandom sequence to a bit stream at the transmission site, then performing the same operation in reverse at the receiver to recover the data.

In the TCCF system, all message trunks are encrypted in key generators prior to leaving the shelter and are decrypted upon entering by similar devices that act in duplex pairs. Analog loops are encrypted in analog devices wherever analog voice is used, including all order-wires. Furthermore, strict adherence to RED-BLACK (red = nonsecure; black = secure) isolation policies is retained. That is, wherever a possibility of an unencrypted voice and its encrypted counterpart being detected together exists, the two signals are strictly isolated by a classified isolation device. The need to isolate between RED and BLACK circuits is apparent in such places as input and output ports in a multiplexer that is being driven by a key generator.

Frame sync must be maintained in a multiplexer, even though its framing pattern encrypted poses a synchronization problem for both multiplexer and key generator. The problem is solved by a method of cooperative resynchronization whereby both the key generator and framing device are interdependent.

Suppose, for instance, that a multiplexer with a 1,0 frame pattern is transmitting through a key generator that scrambles the framing pattern along with other data; how can the multiplexer on the other end of the link recover frame synchronization? During normal operation, the framing pattern is decrypted at its destination and is thus
clear to the receiving multiplexer. However, if the multiplexer loses frame, was it due to bit errors, bit slippage, or due to the key generator losing sync? Furthermore, if the key generator loses sync, how does it resync if its sequence contains data from the transmitting multiplexer? To resync the key generator requires a number of bits without data or "pure key". To accommodate this situation, a cooperative resync procedure is used. When sync is lost in the receiving multiplexer, it searches for sync for a given period of time (milliseconds); failure to find sync causes its transmitting key generator to send pure key to the distant demultiplexer. Since the link is duplex, the distant demultiplexer recognizes a pure key condition and sends pure key back. This condition allows both key generators to resync since no data interferes from either direction. Once accomplished, key generator sync initiates the flow of data in both directions and allows proper detection of the framing pattern by both demultiplexers. This procedure is referred to as cooperative resync and is one reason to minimize frame resync times in the frame synchronizer of the multiplexers.

This treatment of communication security subjects is superficial because of their classified nature.

THE FAMILY OF DIGITAL GROUP MULTIPLEXERS

DGM Function in the Tactical Communications Network

The purpose of the Family of Digital Group Multiplexers (DGM) is to provide digital combining and cable transmission functions for the fielded terminal users or subscribers that are served by the node. This equipment may be located any place in the field where clusters of
users create the need for trunks and can be mounted in trucks, tents, buildings, or other communication facilities where necessary.

The DGM equipment is designed only for the data rates described earlier, which are part of the TRI-TAC all-digital, synchronous system. However, since a fielded group of units could use equipment from earlier systems such as the asynchronous Army ATACS equipment or even analog telephones, the DGM equipment must operate in situations that either require direct interfaces or use of common facilities. The new DGM equipment is shown in a variety of interface situations in Figure 8. The family of DGM equipment consists of the following items:

1 Loop Group Multiplexers (LGM) - An LGM will multiplex up to 17 32-kb/s CVSD loops from digital telephone into trunks with rate from 144 to 576 kb/s.

2 Trunk Group Multiplexers (TGM) - A TGM multiplexes inputs from several LGM's into trunk rates that range from 576 to 2304 kb/s.

3 Master Group Multiplexers (MGM) - An MGM is an asynchronous device that provides an interface in the trunk network with the older asynchronous equipment, accepting TGM or LGM rates and outputting 18.72-Mb/s diphase.

Since LGM, TGM, and MGM equipment operate in situations that require a great degree of interconnecting flexibility to form hierarchies of trunks, they operate in the NRZ mode. All require modems to provide the proper cable coding and drive. A family of modems, consisting of the following, is required for this function:

1 Low-speed cable driver modem (LSCDM).
2 High-speed cable driver modem (HSCDM).

3 Group modem (GM).

In some applications, where hierarchial combining is limited, there are remote counterparts to the LGM and TGM that incorporate a cable drive in the multiplexer function; these are:

1 Remote Loop-Group Modem (RLGM) - The RLGM accepts 32-kb/s CVSD diphase inputs from digital telephones and outputs 144-kb/s diphase.

2 Remote Multiplexer Combiner (RMC) - The RMC accepts either 32-kb/s inputs from digital telephones or a 144-kb/s input from an RLGM and outputs 288 or 576 kb/s.

The system diagram of Figure 8 shows the usage of DGM equipment along with other transmission equipment as they access the CNCE.

Digital subscribers from telephone terminals and individual users are grouped for trunking at multiplexer facilities by LGM's, TGM's, and MGM's and in remote facilities by RMC's and RLGM's. Parts (A) through (E) of Figure 8, depict various assemblages of DGM multiplexers that could be used in TRI-TAC in different deployments. Multiplexer shelters shown are versions of the AN/TCC-73 and AN/TCC-72 existing today. Analog and digital subscribers can use the same trunking facility in a configuration depicted in part (A). Here, the TD-660, an analog-to-digital multiplexer with asynchronous output, interfaces with the TGM through a special interface card of the Group Modem. The use of RMC-RLGM-DSVT combinations is shown in part (C), where isolated groups of users are shown. Part (D) shows the introduction of present day Army (ATACS) analog equipment into the synchronous system at the group
modem by 576-kb/s diphase transmission. Also depicted is the use of a manual teletype in ATACS to report equipment quality instead of the automated telemetry system of TRI-TAC. An all-TRI-TAC application is shown in part (E) where digital telephones, DSVT's, access a small, unit-level, switch, the output of which is further combined with other loops and trunked into the CNCE. Here, orderwires are all-digital and telemetry outputs from the DGM equipment are externally combined in a CNCE-type telemetry combiner.

Cable transmission and radio interface functions are provided by Group Modems, Cable Driver Modems, and Pulse Restorers. The functions of this equipment is to provide the interface between multiplexing and radio modulation functions, which are typically NRZ, and codes conditioned suitably for transmission such as diphase, bipolar, and dipulse. The introduction of the DGM group modem that can accept diphase and bipolar codes, which are used by ATACS, provides the versatility of interfacing hybrid systems at any suitable point in the cable or radio system. The radios are shown in parts (G) through (I). The short-range, wide-band radio (SRWBR) at the top-of-the-hill, part (M), transmits supergroups to the CNCE technical shelter via a colocated SRWBR. The MGM in the SRWBR at radio park collects trunks and orderwire from both synchronous and asynchronous systems, from TRI-TAC and ATACS deployments, and from other nodes.

The system of orderwires in the network provides the necessary communication link between network operators and the facilities controller at the CNCE or elsewhere. The DGM equipment provides 16/32 kb/s, 2-kb/s, and 4-kHz orderwire capability, both in-band and out-of-
band channels, and automated BITE in the form of 150-b/s telemetry outputs from DGM equipment. Compatibility must be maintained between ATACS orderwire, which are mostly 4-kHz, and provide only limited BITE capability. Some methods of transmitting orderwire and telemetry are depicted in Figure 8. The interoperation of the orderwire system is discussed in later paragraphs.

The DGM equipment in facilities, extended throughout the network, ultimately interfaces with complementary equipment in the CNCE. The modems in the CNCE are identical to those in the DGM. The asynchronous combining function in the CNCE is identical to the DGM MGM and the channel multiplexing function, which is part of the channel reassignment function, is identical to the multiplexing functions of the DGM. The DGM orderwire and telemetry functions are compatible with the CNCE orderwire functions such as the telemetry combiner data channel multiplexer and orderwire end instruments. Generally, the DGM equipment does not interface with the circuit switch. However, it is possible to access the switch at any of the DGM rates and formats. The switch accesses the DGM through the CNCE via digital trunks. Where analog loops are involved, it is possible to access the switch through the CNCE in the analog domain. In this mode, it is necessary to demultiplex digital ATACS groups in an AN/TCC-73 or equivalent and provide loop access from the TD-660's through the CNCE patch panels. This configuration is shown in part (N) of Figure 8.

There is normally no access of DGM equipment to the CSCE since it is exclusively accessed by a CNCE, CSPE, or other CSCE. However, it is possible to access the CSCE from a DGM loop or orderwire equipment; in
which case, the 32-kb/s diphase, 150-b/s telemetry, and 4-kHz voice orderwire are compatible with CSCE orderwire and DSVT equipment.

Interoperability of DGM Orderwires

The orderwire and telemetry functions in the DGM equipment interoperate effectively with the facilities control in the TCCF and with existing ATACS orderwires. They are part of the network of system orderwires that are used by system controllers and network operators to coordinate supervisory and maintenance activities of a deployed tactical system. The DGM equipment interfaces, for the most part, with facilities control equipment in the TCCF (CNCE) and with fielded units of the ATACS system that are part of the hybrid analog-digital system deployed during the transitional periods from hybrid to all-digital phases.

The characteristics of orderwire systems are summarized in the table below. By designing the DGM with orderwire functions as specified, compatibility at the system interface is assured (e.g., the 4-kHz analog orderwire used in ATACS is compatible with the DGM and TCCF equipment at both bipolar and dipulse modems, where the system interface occurs). The system interface between DGM equipment and the CNCE occurs generally at diphase modems or at an MGM, in which cases, 32- and 2.0-kb/s diphase orderwires are compatible.

The capability of the DGM multiplexers and modems to carry 150-b/s ASCII telemetry in the TDM band is compatible with the capability of the TCCF multiplexing functions to demultiplex and use this data. The telemetry combiner, which accepts 150-b/s ASCII outputting 2.0 kb/s, and data channel multiplexers and data converter, which accept 2.0 kb/s outputting 32 kb/s are compatible with rates and formats generated in the
Examples of the use of orderwires and telemetry are shown in a representative network configuration (Figure 8) in which there are at least three types of system interface.

**Orderwire Interoperability**

**Orderwire and Telemetry Characteristics**

<table>
<thead>
<tr>
<th>Tactical System</th>
<th>Terminal Equipment Instrument</th>
<th>Transmission</th>
<th>Combining Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td>DGM</td>
<td>Multiplexers, Modems</td>
<td>2, in-band</td>
<td>TDM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32, in-band</td>
<td>TDM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2, diphas</td>
<td>Radio, cable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32, diphas</td>
<td>Radio, cable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 kHz, ana-</td>
<td>Radio, cable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>log</td>
<td>Radio, cable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>150 b/s, ASCII</td>
<td>TDM</td>
</tr>
<tr>
<td>TCCF</td>
<td>Multiplexers</td>
<td>2, in-band</td>
<td>Telemetry combiners</td>
</tr>
<tr>
<td></td>
<td>Modems</td>
<td>2.4, in-band</td>
<td>data channel mux</td>
</tr>
<tr>
<td></td>
<td>Analog Phones</td>
<td>32, in-band</td>
<td>data converters</td>
</tr>
<tr>
<td></td>
<td>Digital Phones</td>
<td>75-150 b/s,</td>
<td>VFCT (voice-frequency</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ASCII</td>
<td>carrier telegraph)</td>
</tr>
<tr>
<td></td>
<td>Teletype</td>
<td>4 kHz, analog</td>
<td>TMRC (teletype modula-</td>
</tr>
<tr>
<td></td>
<td>Computer I/O</td>
<td>32, diphas</td>
<td>tion-rate converter)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DSVT data adapter</td>
</tr>
<tr>
<td>ATACS</td>
<td>Analog Phones</td>
<td>4 kHz, analog</td>
<td>Radio, cable</td>
</tr>
<tr>
<td></td>
<td>Digital Phones</td>
<td>75-150 b/s,</td>
<td>wire</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ASCII</td>
<td>TD-660</td>
</tr>
<tr>
<td></td>
<td>Teletype</td>
<td>32, diphas</td>
<td>TD-1069</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TD-1065</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Others</td>
</tr>
</tbody>
</table>
CHAPTER THREE

EQUIPMENT DESIGN

DIGITAL SIGNAL MONITORING AND PROCESSING FACILITY

Digital Channel Multiplexing

The channel multiplex function is designed to generate digital groups from digital channels or loops. These loops enter the CNCE as 32-kb/s diphase signals from digital telephones. They contain no framing information and all signaling to the switch or other device is done in-band. The coding of the loops is changed from diphase to NRZ in loop modems because NRZ, being a "full-Baud" signal, is better suited to multiplexing than diphase, a "half-Baud" signal (refer to the overall signal flow diagram of Figure 6). The NRZ loops are then directed to the channel multiplex function for formation of groups.

These groups are again processed by the channel reassignment function, if required, or transmitted directly over cable to other destinations. Each group consists of an S-channel or supervisory channel that contains framing and N additional data channels. The formats used to assemble the digital groups are shown in Figures 9 and 10. Figure 11 lists the group data rates. The S-channel or supervisory channel consists of a framing bit followed by bits that can be used for various supervisory functions such as orderwire or in-band signaling. In a few cases, some supervisory bits are used for transmitting the status of synchronization of link encryption devices or of submultiplexers in higher multiplexing hierarchies. The framing pattern itself, designated SF, is an alternating 1-0 pattern. It can be seen from Figure 9 that SF is a distributed pattern rather
NOTE:
CHANNEL RATE = 32 KB/S (16 KB/S)
GROUP RATE = 144 KB/S (72 KB/S)

Figure 9. Digital Channel MUX Function Format
N = 7, 8, 15, 17, 31 or 35

31.25 MICROSECONDS

![Diagram of Digital Channel MUX Function Data Format]

**Figure 10. Digital Channel MUX Function Data Format**

<table>
<thead>
<tr>
<th>NUMBER OF CHANNELS (N)</th>
<th>CHANNEL RATE = 32 Kb/S</th>
<th>GROUP RATE (Kb/S)</th>
<th>CHANNEL RATE = 16 Kb/S</th>
<th>GROUP RATE (Kb/S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>144</td>
<td></td>
<td>72</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>256</td>
<td></td>
<td>128</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>288</td>
<td></td>
<td>144</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>512</td>
<td></td>
<td>256</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>576</td>
<td></td>
<td>288</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>1024</td>
<td></td>
<td>512</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>1152</td>
<td></td>
<td>576</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 11. Data Rates for Channel MUX Function**
than occurring in contiguous bits. In the case of $N = 4$, a bit of SF, say the first 1, is followed by eight bits from the four data (digitized voice telephone) loops; these are followed by $S_1$, the first of the supervisory channel bits, eight more data bits, and $S_2$, etc., until 36 bits after the second bit of SF, a 0 is transmitted. For $N = 4$ or 4 data channels, the information rate is the group rate or 144-kb/s. From this, it can be seen that the frame rate is $1/36$th of the information rate or 4-kb/s. The supervisory channel as a whole is $1/9$th of the information rate (or 16 kb/s) and each channel of data is transmitted at $2/9$th of the information rate (or 32 kb/s).

A block diagram of the channel multiplexer is shown in Figure 12. The output of the multiplexer is data formatted according to the previous paragraph. The S-channel is formed by multiplexing the framing subchannel with the supervisory subchannels; SF is generated by dividing the channel data rate $R_C$ by eight and using this signal to clock a divide-by-two flip-flop to produce the alternating 1-0 pattern.

The multiplexing technique in the channel multiplexing function uses a Random-Access Memory (RAM) to perform a buffering and timing recovery function that is necessary to accommodate small timing offsets, which may occur in each channel. This buffering is required because the incoming loops are not completely synchronous even though their timing originates in the same atomic clock. The problem of small timing variation arises from the fact that, while the atomic clock in the node drives all user devices and assures long-term rate synchronism, phase delays due to transmission over several hundred yards to users' telephones and subsequent variations in stabilities
Figure 12. Digital Channel MUX Block Diagram
of timing recovery circuits (i.e., phase-locked loops) in the telephones cause short-term variations that must be accounted for. One approach (the one used here), is to sample the incoming data at a high rate, in this case 5(N+1); then, by using a RAM as a high-rate circulating comparison device, determine when a bit is not aligned with the multiplexer clock and correct this alignment by an elastic buffer. This method can correct for static offsets of 4/5 of a bit period or for dynamic offsets within the range of about 1/6 of the bit rate. It should be noted that these variations are entirely within the definitions of the term "synchronous" and are not in any way connected with the "asynchronous" combining function covered later or with the requirement for buffering node-to-node transmissions from separate atomic clocks.

Each bit of channel data is sampled by using an (N+1) multiplexer and is stored in an (N+1) word shift-register file. The shift-register file is implemented by using an (N+1) word by 6-bit RAM in which the output data is fed back, right shifted by one position, and restored in the same memory location for each read/write operation of the memory. The first bit position vacated by the right shift is loaded with the new data bit from the multiplexer. This 6-bit word is also examined by a 111000 detector, used to identify a ZERO-to-ONE transition for each channel data bit and to notify the timing recovery file of which count the modulo 5 phase counter had when the transition occurred. The phase counter is loaded into the timing recovery file every time the 111000 pattern is detected, which continually updates the phase for the ZERO-to-ONE transition of the
channel data. To avoid a possible timing problem, the comparator circuit that compares the timing recovery file with the modulo 5 phase counter is inhibited during the time that the 111000 pattern is present, causing the comparison to be delayed for one complete scan of the input channels. When a comparison is made, a data bit is written into the elastic store file. The bit sense of the channel data bit is located in the first bit of the \((N+1)\) shift-register file.

The elastic store file is also implemented by using \((N+1)\) word RAM's. This file is similar to the shift-register file except it is only four bits in length. To provide the elastic storage capability for this file, it is necessary to select which one of the 4 bits contains the current output data bit. Changes of the selected output bit occurs when the timing recovery file and the phase counter comparator encounter a bit slip due to minor rate variations of the selected channel data input. To keep track of this bit selection, a 4:1 multiplexer is addressed by the address control file. This file is used to provide accounting for each bit of data entered into elastic storage and each bit removed. For each bit entered, a +1 is added to the address control file while for each bit removed, a -1 is added. If both operations occur simultaneously, no action is performed.

The register file address sequence must allow for an output sequence that contains an S-bit followed by channel data bits in sequential order. To provide this sequence, it is necessary to supply a unique sequence for addressing each RAM file. The unique properties of the sequencer are that the number of states for one
complete sequence is \((N+1)\) and starting at any state in the sequence, the next sequential channel will be found 5 counts later. An example of this for the sequence used for the 7-channel multiplexer is:

\[ S, 5, 2, 7, 4, 1, 6, 3 \]

Since the addressing is performed at 5 times the output rate, dividing this sequence by 5 results in the desired output sequence of:

\[ S, 1, 2, 3, 4, 5, 6, 7 \]

**Digital Channel Demultiplexing**

The digital channel demultiplex function synchronously decombines digital group data streams comprised of \(N\) channels for values of \(N\) up to \(N = 35\). The hardware design for this function is shown in block diagram form in Figure 13. The design incorporates a 01 frame synchronizer technique and also provides for the decombining of the 7-channel into its appropriate subchannels. Operator-controlled switch selection configures the hardware for processing the received digital group data rate.

In operation, the received digital group data stream is clocked via the selected data rate station timing into a 36-bit parallel output shift register. The register outputs are tapped in accordance with the family of group rates and the appropriate tap is fed to a second shift register whose length has been selected to provide the additional digital delay required to effect a full frame plus one bit delay. The incoming data and the frame delayed data are simultaneously fed to the frame synchronizer.

The output of the frame synchronizer hardware is a frame sync signal that indicates frame sync acquisition or loss and a frame sync
Figure 13. Channel Demultiplexer Block Diagram

NOTE:
TSB = TRI-STATE BUFFER
"N" CHANNELS 16-KHZ DEMUX DATA OUT

32-KHZ (16-KHZ WHEN N = 4)
pulse that identifies the position of the $S_f$ bit in the group data stream. The divide-by-$(N+1)$, or divide-by-9 when $N = 4$, hardware converts the selected data rate station clock into a 32-kHz clock (16 kHz when $N = 4$), synchronized to the frame sync pulse. The 32-kHz clock strobes the 36-bit latch, thus performing the decombining of the group digital data into the respective 32-kb/s digital channels. When $N = 4$, the 16-kHz clock strobes the latch and during each half cycle of the 16-kHz clock, alternately enables one of the two quad tri-state buffers (TSB). This action results in the appropriate decombining of the four digital channels at 32 kb/s. Decombining the $S$-channel into the required subchannels is accomplished by clocking the $S$-channel into an 8-bit shift register and strobing the associated latch with the 4-kHz frame-synchronized clock.

**Asynchronous Combining Function**

The asynchronous combining function provides for independent multiplexing and demultiplexing facilities for combining/decombining a wide range of asynchronous data rates up to twelve independent adaptable channels. The communication node in which the CNCE operates is primarily a synchronous node. That is, most of its incoming links are derived from timing that originated in its own atomic clock or in other atomic clocks in adjacent nodes. Timing derived in this manner is subject to bit phasing offsets, short-term rate variations due to such phenomena as fading in the RF transmission paths and timing jitter in phase-locked loops that are used at various points in the process to recover timing. All variations are accounted for in the synchronous multiplexing functions and can be tolerated only
because the basic rates in the synchronous system are derived from atomic clocks that are stable to approximately 1 part in $10^{11}$. However, other systems are connected to the node that, out of necessity, are derived from timing sources with long-term average instabilities on the order of 50 parts per million ($50$ parts in $10^6$). These systems are termed asynchronous (asynchronous, as used here, is not to be confused with the asynchronous word format used in teletype transmission that employs start-stop word synchronism and is asynchronous in the sense of bit timing). The problem in multiplexing asynchronous bit streams is in the continually drifting clocks of each input source.

Methods of asynchronous combining have been studied and developed in the past few years with the most popular being bit stuffing. In bit stuffing, each input is entered into an elastic buffer that reads in with the data clock and out into the multiplexer with multiplexer timing. This establishes all outputs on a common timing base. Variations in input rates are accounted for by stuffing dummy bits into channels to make their average rates the same as that of the output and by identifying the positions of the dummy bit through a coded word that is inserted as part of the overhead in the output multiplex. At the receiving end of the link, decoding of the stuff command allows deletion of the dummy bits from the demultiplexed output and restoration of each original bit stream, intact at the rate at which it was generated.

The asynchronous combiner (shown in Figure 14) consists of the following major subsections:
Figure 14. Asynchronous Combiner (MUX Section)
1 **Channel Cards** - Input channel cards are rate comparison buffers used as elastic buffers while output channel cards are smoothing devices.

2 **Timing Generator** - Used in both combiner and decombiner to develop and distribute major frames, frames, subframes, byte intervals, bit times, rate comparison strobes, timing, and data gating for multiplexing and demultiplexing; conversion from the 18.720-Mb/s operation to the 9.360-Mb/s operation is accomplished in this section by clock division and selective distribution.

3 **Priority Enabling and Encoding** - Used in combining and decombiner sections for sequencing channel data and controls for multiplexing and demultiplexing.

4 **Diagnostic and Alarms** - Used to detect and isolate faults to a subassembly and provide the system status and alarms to the distribution frame.

5 **Overhead Code Enabling and Generation** - Used in the combining function to determine the channel to be serviced, type of service, and generation of corresponding code to designate type of service granted; forms the overhead bytes, including formatting of the orderwire and telemetry data and +STF sense bit.

6 **Multiplexer** - Converts the serial channel data to bytes and multiplexes the bytes according to the encoded channel address, inserts overhead, the converts multiplexed data to the serial supergroup rate (18.720/9.360 Mb/s) for output.
7 **Frame Sync** - Used to acquire decombiner synchronization, decode STF decisions, and perform synchronization maintenance.

8 **Demultiplexer** - Used to convert the serial supergroup data into channel bytes and distribute serialized data to the channel smoothing buffers (Figure 15).

**CONTROL COMMUNICATIONS FACILITY**

The Control Communication Subsystem (CCS) provides the necessary equipment for the CNCE operator to coordinate control of the node with other elements of the TCCF over voice and data orderwires. It is essentially the focal point for all control actions except those requiring access to the processor, which are done in the (processor) Control Subsystem described in the next section.

The four types of orderwires used in the system all terminate in patch panels and may require some sort of conditioning before being terminated by the operator in a headset or teletype machine, or passed onto another destination such as the CSCE, switch, or other CNCE. Figure 16 is a block diagram showing how the four types of orderwires can be terminated. It may be clearer to refer to the control communication subsystems in the overall signal flow diagram of Figure 7, which shows interconnections from other subsystems. The terminating equipment shown in Figure 17 are all part of the subsystem.

The voice orderwires ultimately terminate in the operator's headset or a speaker via a selection panel shown in Figure 16. The data orderwires, at 2.4 or 16/32 kb/s, may be patched to the processor,
Figure 15. Asynchronous Combiner (DEMUX Section)
Figure 16. Orderwire/Intercommunications Selection Panel Equipment
Figure 17. Control Communication Subsystem Block Diagram
while 75/150-Baud teletype may go to the teletype machine or processor. Either group of digital signals may require combining in data channel multiplexers or telemetry combiners for transmission to the CSCE. Some teletype or telemetry signals may also require conversion to 32 kb/s and use a data part of the digital telephone (DSVT) for transmission. The data converter is used for this application.

The following description may clarify some of the functions performed by the system controller and provide insight into the degree of versatility designed into this subsystem.

The control communication facility is designed so the operator of the CNCE technical shelter has access to orderwire control functions. The patch panels are located so that they may be readily observed and changed by the operator. The voice circuits terminate in the voice/intercom patch panel where conditioning and monitoring equipment may be connected by the operator to end instruments in the operator console. Analog circuits may interconnect with signaling units or signaling converters, depending upon the type of signaling used. A 2- to 4-wire hybrid unit is interconnected to convert 2-wire intercom circuits to 4-wire circuits. A 6-way conference bridge allows analog voice conferencing. Digital voice circuits use circuit actuation units for signaling except for DSVT's that signal in-band from the terminating set. The 16/32-kb/s stuffers are used to resolve any difference between mixes of 16-kb/s digitized voice. The digital conferencing unit, with its associated parity selection call unit, is used for conferencing digital calls by the operator. The interconnection and use of these elements by the operator depends on
the situation or deployment at hand. The orderwire/intercom selection panel on the operator's console terminates the analog signaling and control equipment from the voice/intercom patch panel. The Communication Security devices (i.e., Parkhill (analog), Vinson and DSVT (digital) are also connected via distribution frames prior to use in the operations console.

An analog telephone (TA-341) and a speaker/amplifier/microphone are connected to the voice orderwire patch panel to monitor circuits when the operator is away from the console. The voice/intercom patch panel and the data orderwire patch panel are located in a rack adjacent to the operator's console in the technical shelter.

**Orderwire/Intercom Patching**

The voice and data orderwire patching facility provides a means for accessing, extending, and routing control circuits from the network to CNCE operator positions. The orderwire/intercom patch facility consists of two patch panels, one for voice and one for data. The orderwire patch panels consist of 4-wire jackfields. Each circuit has a line and equipment jack with monitors for both duplex directions. This is a total of eight jacks per circuit. The jacks are connected in a normal through configuration; that is, the circuits through them are connected normally until disconnected and changed by patching (refer to Figure 18). There are 36 circuits in the voice/intercom patch panel; 12 for secure analog voice; 12 for nonsecure intercom; and 12 for 16/32-kb/s digitized voice.

There are 72 such circuits in the digital orderwire patch panel. They provide the capability to transmit 150-b/s or 2.4-b/s data and
Figure 18A. Voice Orderwire/Intercommunications Patch Panel Layout

Figure 18B. Data Orderwire Patch Panel Layout
75 and 150 Baud teletype between test elements. The jacks are designed to permit interconnection of the following circuits;

- 24 MUX circuits at 2.4 kb/s, unbalanced.
- 20 data link from the processor I/O circuits, unbalanced.
- 12 telemetry-data-collection circuits at 2.4 kb/s, unbalanced.
- 75 and 150 Baud teletype.

Manual teletype from operator console.

**Data Channel Multiplexer**

The Data Channel Multiplexer synchronously combines and decomposes 6 or 12 channels of 2.0- or 2.4-kb/s data from the telemetry combiner or from the processor I/O. If more than one such link goes to a certain destination, it is efficient to use the data channel multiplexer for transmission. Data from up to 12 channels is processed through the timing recovery and elastic storage buffer functions for each channel. Channel data extracted from the buffers is then interleaved with the channel data by using a 13:1 multiplexer as shown in Figure 19. The 12 gated clocks used to sample data from the buffers are sequenced by the timing and control generator detailed in Figure 20. The block diagram indicates how four required sequences are generated by operator control using the front panel switches. Formats for each configuration are given in Figure 21. In addition to the gated clocks outputs, a 4-bit binary address is provided to sequentially select one of the 12 data channels or the S-channel to be gated through the 13:1 addressable multiplexer.

The design of the demultiplexer is shown in Figure 22. The received digital data stream and its derived timing is fed to the
Figure 19. Data Channel Multiplexer Block Diagram
Figure 20. Timing and Control Generator for Data Channel MUX/DEMUX
12 CHANNELS,
2.4-KB/S CHANNEL RATE,
32-KB/S GROUP RATE

\[ SC_1 \ldots C_{12} C_1 \ldots C_{12} C_1 \ldots C_{12} \varnothing \varnothing \varnothing \]

6 CHANNELS,
2.4 KB/S CHANNEL RATE,
16-KB/S GROUP RATE

\[ SC_1 \ldots C_6 C_1 \ldots C_6 C_1 \ldots C_6 \varnothing_1 \]

12 CHANNELS,
2.0-KB/S CHANNEL RATE,
32-KB/S GROUP RATE

\[ SC_1 \ldots C_{12} \varnothing_1 \varnothing_2 \varnothing_3 \]

6 CHANNELS,
2.0-KB/S CHANNEL RATE,
16-KB/S GROUP RATE

\[ SC_1 \ldots C_6 \varnothing_1 \]

NOTES:
S = ALTERNATING 1,0 PATTERN (I.E., 1,0,1,0----)
\varnothing_1, \varnothing_2, OR \varnothing_3 ALL LOGIC 0

Figure 21. Data Channel MUX Formats
Figure 22. Data Channel De-multiplexer Block Diagram
buffer that retimes the data stream to the station clock while maintaining bit integrity for at least 48 hours. The data stream is then clocked through a frame length shift register (the SR length is tap-selected to conform to the received multiplexed format). The SR input and output are simultaneously fed to the 01 frame synchronizer. The frame synchronizer acquires and maintains frame sync and outputs a sync status signal and frame sync pulse signal. The frame sync pulse signal strobes the latch, allowing intermediate storage of one frame of data. As shown in the diagram, the latch outputs are connected in groups of six to tristate buffers. These buffers are enabled in an ordered sequence as determined by the timing decode logic and are selected to conform to the appropriate multiplexing format. The timing and control generator hardware is designed to convert either the 16- or 32-kHz station clock into the frame synchronized 2- or 2.4-kHz data channel demultiplexing clock.

**Telemetry Combiner**

The Telemetry Combiner multiplexes and demultiplexes 13 balanced NRZ telemetry channels with data rates of 150 b/s into one 2.0-kb/s or 2.4-kb/s channel. The telemetry combiner function is designed to process asynchronous 150-b/s teletype or telemetry data for transmission to another CNCE. Due to the asynchronous nature of the channel inputs, it is necessary to construct a data format that includes overhead (OH) data as well as framing and channel data. The format selected (Figure 23) is also structured such that the output rate of 2.0 or 2.4 kb/s can be selected with little change in format or performance. To change the format from a 2.0-kb/s rate to
NOTES:
1. **SEARCH MODE**
   1ST 10 BITS
   OF PATTERN
   WITH NO ERRORS

2. **STUFF COMMAND**
   17-BIT PATTERN
   (X1 - X8 = SPARE BITS FOR 2.4 KB/S)
   A = NO ACTION
   B = + STUFF (+STF)
   C = - STUFF (-STF)

3. **BITS 18-21 = FRAME NUMBER**

4. **BIT 22 = STUFF SENSE BIT**

---

**Figure 23. Telemetry Combiner Format**
2.4. OH bits X1 through X8 are inserted as fill bits to increase the length of a subframe from 40 to 48 bits. A frame is defined as 22 subframes and a major frame as 13 frames (one for each channel). These frames are defined so that + stuff (+STF) commands can be transmitted in the overhead to allow each channel one chance in each major frame to correct any discrepancy in clock rate by bit stuffing. The 22-bit frame length was chosen to provide 17 bits for the command code (no action, + stuff, - stuff) with sufficient redundancy to allow decoding of the transmitted code in an error environment. The next four bits (18-21) identify the frame number while bit 22 contains the bit sense of an inserted OH bit if a + stuff (+STF) code is transmitted.

Bit stuffing (or deletion) is required in asynchronous combining because the input data rate may be slightly higher (or lower) than the clock rate of the local equipment. This is especially necessary where the input is from a teletype machine where the input band rate is mechanically timed and not so necessary, if at all, from 150-b/s sources derived from stable or atomic clocks. The corrective action of bit stuffing (or deletion) is performed in the following manner. Since the elastic buffer at the input reads input data and writes to the multiplexer port, it knows when the input rate is overtaking (or, being overtaken by) the multiplexing rate by the degree of depletion of excess storage capacity. When either depletion or overrun is about to occur, a bit is deliberately delayed entry into the store in the case of overrun, or a dummy bit is inserted in the case of depletion. The depletion condition causes a stuff, + stuff
(+STF), command to be generated whereas overrun causes a -stuff (-STF) command. The command is inserted into the overhead frame as a 17-bit word. Upon receipt of this word by the demultiplexer, a corresponding action can be taken to ignore the extra or dummy bits in that particular channel. The method works effectively to put all rates on a common timing base for the multiplexing and demultiplexing functions.

The multiplexer implementation is shown by Figure 24 with emphasis on the +STF controls for individual channels and combining of the OH code with the 13 channel data bits. Balanced NRZ data is connected to the channel cards, which contains a line receiver to convert the logic signals to TTL-compatible levels. This data is then used to extract channel input timing, using the station clock as a reference and adjusting the derived sample clock such that data transitions and clock have the proper phase relationship. Since the channel data and derived timing are not necessarily synchronized with the station timing, the elastic buffer with +STF controls is used to correct for any rate variations between these two signals. If the incoming data is received at a rate faster than the gated clock sampling rate, a +STF control signal is provided to the gated clocks and stuff control logic, indicating the need for an additional clock at the OH data time slot. This additional clock is the method used to prevent the elastic storage buffer from overflowing. The opposite condition exists when the input data rate is slower than the gated clock sampling rate. For this condition, a gated clock is inhibited on the selected channel to effectively slow down the sampling rate.
Figure 24. Telemetry Combiner Multiplexer Block Diagram
The OH data is generated in accordance with the format given in Figure 25. A modulo-13 major frame counter is used to determine which one of 13 channels is provided with OH service. This channel is then interrogated by using the +STF controls to determine which command code is to be transmitted during the current major frame. Three command codes are stored in a Read Only Memory (ROM) and selectively gated to the OH channel. Following the 17-bit command code, the contents of the major frame counter are serially gated to the OH channel. The sense bit, although a part of the OH word, is not gated to the OH channel, but through the normal data channel during the time slot for OH bit 22. This operation is made possible by exchanging the multiplexer address from 0000, which is the OH address, to an address equal to the major frame number. Multiplexer data is serially transmitted to other CNCE's by using a line driver.

Demultiplexing of telemetry channels involves many of the same circuits as the multiplexer but, in addition, requires frame synchronization first be detected and a sync preset pulse provided to preset the modulo-40/48 subframe counter and the modulo-22 frame counter (Figure 25). Major frame sync is controlled by an up/down confidence counter that indicates loss of major frame sync when the counter is counted down to 0. The up/down control decision is made by comparing the contents of the major frame counter with the received major frame number. For each agreement, the confidence counter is counted up to a maximum value of 15. A disagreement forces the counter to count down. If the confidence counter continues to count down and count 0 is reached, this causes a new number to be loaded
Figure 25. Telemetry Combiner Demultiplexer Block Diagram
into the major frame counter.

When synchronization has been achieved, the time slot for sampling OH, data is used to store each OH data bit. This bit is then compared serially with the three command codes generated by a ROM. Three error counters are provided to accumulate the total number of disagreements between the received OH bit and commands. The error counter with the fewest errors after each frame determines which OH code was actually transmitted by an associated multiplexer.

The gated clocks and stuff control logic performs the same function as the multiplexer. The DEMUX elastic buffers receive a gated clock pulse, which is identical to the associated multiplexer gated clock, to sample the common serial data line into the buffers. To extract data from the buffer, it is necessary to derive a smooth, homogenous, clock from the gated clocks. This is done by using a digital PLL that smooths the gated clocks, which are characterized by added or deleted clock pulses. Output data from the buffer is then connected to line drivers.

**Miscellaneous Terminations**

Equipment performing minor control functions are also terminated on the orderwire patch panels. A speaker/amplifier microphone system provides hand-free use to the operator. The system is wall-mounted in the technical shelters.

The analog conference bridge terminates six 4-wire, 600-ohm circuits. The circuit activation units give an indication of an incoming call on the 16/32-kb/s digital lines by recognizing KY-58 circuit transition (phasing) and is used to activate a call light on the
operator's console. The 2/4-wire hybrid transformers and termination sets are standard type audio transformers that may be used for either 2-wire or 4-wire terminations by port strapping.

The digital conference device enables up to 6 voice orderwire signals from CONSEC units to be combined in a party line or conference type arrangement. The 16/32-kb/s bit stuffer provides interface with an encrypted 16-kb/s circuit to a dedicated 32-kb/s transmission channel.

CONTROL SUBSYSTEM

The control subsystem provides the operator with access to the control functions of the system. The control subsystem provides access to the processor communication control subsystem and the environmental control system. Using extended orderwire circuits from the control subsystem and visual display from the processor, the operator can assert system, link, and channel quality control, monitor performance of the CNCE and associated CESE's, analyze status information, perform tests, isolate faults, and direct implementation of corrective action. The operator can supervise, monitor, and direct personnel at the node and schedule, supervise, and coordinate testing between adjacent nodes. The operator has control of such functions as activation, deactivation, and routing as well as monitoring traffic flow conditions and adapting to traffic flow needs.

Voice orderwires are extended from the communication control subsystem to the operator console and controlled at an orderwire/intercom selection panel that is identical to the one used by the communication control subsystem (refer to Figure 26, which shows the
Figure 26. Control Subsystem Block Diagram
control function and its integration into the orderwire system in the OW/IC selection panel). Access to the processor through the console keyboard, processor control panel, and readout is via the visual display unit mounted on the console, using a cursor positioning device and hard copy printer. The operator can access the processor or other CNCE with a teletype mounted at the console. The following table lists the control subsystem equipment, much of which is common to the communication control subsystem.

**Control Subsystem Equipment**

1. Operator Console
2. Orderwire/Intercom Selection Panel
3. Operator Headset and Adapter
4. Circuit Call ID Units
5. Call Selection Unit
6. Digital (VINSON) Buffer
7. 4-wire Digital Hybrid
8. VINSON (TSEC/KY-58)
9. PARKHILL (TSEC/KY-75)
11. Processor Switchover Control
12. Processor Control Panel
13. Channel Reassignment Control Panel

**Operator Console**

The operator console provides the CNCE controller with a central facility from which to direct, monitor, control, and analyze conditions and status of the CNCE equipment under his direction. The
functions of the control subsystem are performed from the operator's console position. Figure 27 illustrates in block form the activities of the console operator. The impact of each category of inputs, outputs, diagnostics, and controls are shown.

**Processor Control Panel**

The processor control panel provides the controller with monitors and controls to manage processors and peripherals of the CNCE, Figure 28. The processor controls and monitors provide the CNCE controller capability to manually select the necessary peripheral equipment. When malfunctions occur, the controller may override any automatic selection feature of the CNCE peripheral interfaces and direct by positive switch control the connection of peripherals to the processor that are necessary to maintain CNCE service.

In addition to the computer controls logic, the panel contains processor critical parameter status indicators that will allow the controller to visually assess the condition of the CNCE processor subsystem. Figure 28 shows a layout of the panel. Computer parameters to be monitored will be main power on, memory faults, parity errors, and over-temperature. Each will interface with the processor control panel to provide on-line status indicators for presentation to the controller.

**Monitor and Control Panel**

The CNCE controller has the capability of rapidly accessing emergency conditions at the control console and taking corrective action. The control subsystem will provide manual switching to enable rapid control of power and other critical circuits of the
Figure 27. CNCE Control Console Activities
Figure 28. Processor Control Panel
CNCE power supply subsystem equipment at the console. The console will provide main power override switches for emergency shutdown of any major equipment subsystem in the CNCE. Malfunction of any power circuit will result in automatic protection devices being utilized to prevent damage to equipment. The CNCE controller will maintain final responsibility for operation of the CNCE equipment with the control subsystem.

PROCESSOR SUBSYSTEMS

The processor subsystem of the CNCE is basically a subset of its counterpart in the CSCE. The CSCE contains three separate processor subsystems that perform the functions of communication control, batch processing, and display processing. All are minicomputers, modified from the Univac AN/UYK-20 family. The I/O unit of the processors operate on a data bus control concept that utilizes microprocessors as I/O units extended throughout the system and connected to the main processor by a data bus. The three processors in the CSCE have separate functions but share the same data bus; thus, any processor that is overloaded or faulty can have its load diverted in total or in part to one of the other two processors. The processor subsystem is a subject of study, in itself; therefore, a comprehensive analysis, even at the system level, is beyond the scope of this thesis study.

CHANNEL REASSIGNMENT FUNCTION

The channel reassignment function is used to establish the routing of trunks or channels in the network. It is distinguished from the loop routing function of the circuit switch (in the CESE)
by the fact that reconfiguration is not done on a call-for-call basis but responds to less frequent reconfigurations from the network controller because of longer term effects such as equipment outages or user deployment changes. The most important systems feature of an automated channel reassignment function is the ability to respond to the network changes brought about in a rapidly changing positions, a manual patching method for changing the trunking network could become very difficult to manage. The channel reassignment function is, therefore, automatically control-by the processor and responds to inputs from the network controller when a change is necessary. Alternate network configurations are stored in memory and recalled for examination on the CRT display. If a change is necessary, a cursor positioning device operated on the face of the display may be used to eliminate faulty trunks and create new configurations. The channel reassignment function then responds to the new configuration automatically.

Channel reassignment is done on a time-division matrix, employing a method of time slot interchange. The time-division matrix is essentially a demultiplexer with outputs that are programmable as inputs to a multiplexer. The demultiplexer works back-to-back with a multiplexer through a programmable matrix to perform the time slot interchange.
CHAPTER FOUR
SYSTEM ANALYSIS

TIMING SUBSYSTEM

The Synchronously Timed Node

In a multi-node system such as this where a communication complex (node) can originate digital data that is to be processed at another node located miles away and possibly relayed through other nodes en-route, some means of maintaining a uniform timing system must be established. This problem is not encountered in analog systems because timing is not required in the processing functions. The nearest thing to a requirement for timing integrity between analog nodes would be that of maintaining coherence in the transmission media if coherent detection processes were used in modulation and demodulation, but without a requirement for end-to-end coherence through several nodes. The requirement for a uniform timing system is therefore unique to a synchronous digital system and presents a problem that has not yet been solved in operational because heretofore there has been no deployment of a multi-node synchronous digital system.

The first solution to the problem of maintaining timing integrity throughout a multi-nodal system was solved by the asynchronous method of data processing. In this method, two interconnected nodes are timed by clocks that are nominally at the same rates but not necessarily kept accurately on frequency and certainly not in phase. Clock accuracies were on the order of ±50 ppm off a nominal reference. The differences between rates were resolved by pulse stuffing techniques. This enabled each node to operate multiplexers and modems at the same nominal rates.
between interconnecting links but to be completely isolated in frequency from each other. Each node therefore operates as an independent timing entity within the ±50 PPM constraint. Asynchronous nodal systems have the advantage of rate isolation but suffer the disadvantage of equipment complexity in the stuffing process. Since the stuff codes, which are necessary, require additional overhead in the multiplex, they are inefficient. Furthermore, reconstruction of the rate from data that has been stuffed requires a smoothing phase-locked loop or its equivalent, which introduces an unwanted jitter in the resulting bit stream. There is a limit to the number of times this stuffing/smoothing process can take place in a tandem chain and maintain jitter within tolerable bounds. This is a fundamental limitation on the use of asynchronous communication systems.

A second method of maintaining system timing integrity by simultaneous timing sources in each node was developed as an improved method in the multi-node system. In this method, each node employs a highly accurate, stable atomic clock as a reference with the processing at interconnecting links done with open-looped frequency control systems. That is, no attempt is made to keep the two or more clocks running at the same frequency once they are set. The system depends upon the fact that the clocks at each node can be set to the same frequency and remain there for long periods of time. The objective for the ultimate system is to maintain a time tolerance within ±2 microseconds between any two transmission nodes. Maintenance of this time tolerance throughout the network provides the capability to synchronize all equipment in the network, including user terminals. To the extent that the clocks
at two nodes differ in frequency, buffers are necessary to account for this difference. Buffers are also required to account for propagation delay variations. A frequency tolerance of $1 \times 10^{11}$ per day is practical for the independent clocks, along with buffer sizes that will limit buffers to, at most, one reset per day when frequency standards at adjacent nodes are at the extremes of their tolerance value in opposite directions. The timing reference at each node can be supplied by a timing subsystem that consists of a primary timing standard, an atomic clock, a secondary timing standard, which is a crystal oscillator acting as a back-up, and a timing distribution system, which provides the various system clock rates from the reference.

**Primary Timing Function**

The fact that atomic clocks are commercially available that can be set to accuracies on the order of one part in $10^{12}$ and maintained over long periods of to 6 parts in $10^{12}$ with short-term variations held to one part in $10^7$ has made the synchronous communication system possible. The problem with less accurate clocks that have made the synchronous system impractical is that heretofore data rate buffering of relatively inaccurate clocks from two sources required either excessively large amounts of bit storage or too frequent resetting intervals to be of practical value.

The primary timing function provides a cesium-beam frequency standard. The system is shown in Figure 29. The cesium-beam tube utilizes a cavity tuned to $f_c = 9.1926317700$ GHz. This is the frequency corresponding to the energy difference between the energy state of the cesium atoms that are allowed to enter the cavity and proceed through
Figure 29. Functional Diagram of Cesium Frequency Standard
the loop via selective magnet B, and the next lower cesium energy state
\((E_2 - E_1 = \hbar f_c)\). An electromagnetic wave of frequency \(f_i\) close to \(f_c\) is injected into the cavity from which energy is stored in greater or lesser amounts depending upon how close \(f_i\) is to \(f_c\). By energy conservation, as \(f_i\) approaches \(f_c\), more energy is supplied to the cavity from the EM wave, less is supplied by the cesium beam atoms, and more atoms remain in the higher energy state. These atoms are allowed to be coherently detected, integrated and dumped, then used to control the crystal oscillator. When \(f_i\) is equal to \(f_c\), the loop is in a DC condition but as the crystal drifts away from \(f_c\), the modulation and coherent detection process result in an error voltage that is applied to the crystal. In this manner, the long-term frequency stability inherent in the cesium atom due to quantum effects, combined with the short-term stability of the quartz crystal oscillator, provides ultra-accurate and stable frequencies. The quartz crystal oscillator in the standard is not to be confused with the dual external oscillators that are phase locked to the frequency standard. In case of failure of the cesium mechanism, the crystal oscillator within the standard can be used without the cesium beam.

**Frequency Synthesizer**

A frequency synthesizer provides the deviation of the proper timing rates for local units from the frequency standard. Figure 30 is a block diagram of the timing distribution subsystem. The reference for the node is taken from the 1.0-MHz output of the cesium clock. A selection can be made to use one of two timing sources from another node. In any case, the selected reference is divided to 8 kHz to start the distribu-
Figure 30. Timing Distribution Configuration
tion timing chain. This reference is used to provide 8-kHz and 18.72-MHz phase-locked signals in extremely stable VCXO-controlled phase-locked loops. Two parallel redundant loops are provided for system reliability, as shown in Figure 31. The 18.72-Mb/s output is used for supergroup multiplexing while the 8-kHz output is used for a distribution reference in the master synthesizer. Since there are two shelters at a node, a slaved frequency synthesizer, identical to the master, is also required.

The 8-kHz reference is multiplied by 576 and 512 to provide the highest reference for two separate countdown chains (refer to Figure 32). One is based on clock rates requiring binary multiples of $2^n$ and the other on multiples of 48 kb/s.

**Secondary Timing and Control**

This method of centralized timing has one important disadvantage - the vulnerability of the entire node to a failure of the timing reference. To offset this, an elaborate scheme has been devised to switch over to one of a number of alternate secondary sources in the event of failure of the primary clock.

The first backup is the crystal oscillator within the cesium clock itself which will provide an accurate output for a period of time after failure of the cesium mechanism. This failure, on any of the modes that follow, is reported to the processor as an alarm condition demanding attention by the operator.

The three sources of primary reference are the local atomic clock and two data streams from interconnected nodes. Provided no clock failure has occurred in distant nodes, these links provide atomic standards
Figure 31. Phase-Locked VCXO Simplified Block Diagram
Figure 32. Functional Synthesizer Distribution Diagram
that can be used locally. The switchover is accomplished when the local clock signals a failure. If a distant clock has had a failure and is itself operating on back-up timing, its failure mode if signaled to the local node and the other back-up link is used. If both back-up inputs are operating themselves on back-up timing, a random selection of one of them is made. The redundancy of the VCXO phase-locked loops that initiate timing distribution from the 8-kHz reference add a further degree of system redundancy.

**FRAME SYNC MODULE AND BUFFER DEVICE**

Each of the digital groups, received and processed by the CNCE after being buffered by a buffer device to allow for timing variations, is monitored by a frame synchronizer to establish framing bit position in the data stream. The buffer device receives the group data and timing from its associated input unit and outputs group data that is timed to the station clock. Design of the buffer device provides the bit capacity required for maintaining bit integrity for at least 48 hours under the specified conditions. The buffer also provides an alarm signal when an overflow or underflow condition occurs.

The group buffer device accepts incoming synchronous data at rates whose long-term average can differ from the station timing by one part in $10^{10}$ and with short-term variations, zero mean, less than or equal to two microseconds. First-in/First-out (FIFO) memories with a storage capacity of 256 bits perform the buffer device function. The FIFO is an asynchronous memory that accepts data under control of the timing input clock and ripples this data through the device to the output. Normal operation requires that the FIFO be loaded to half capacity before
any data is read from the memory. This operation is performed at power on and when the buffer overflow condition is detected. The data bits then line up at the output end in the order in which they were written. An output timing clock causes the next to the last word of data to move to the output and all data shifts one place down in the stack. Reading and writing operations are completely independent.

Although the normal FIFO has controls that indicate when the buffer is empty or full, it is necessary to maintain a bit accounting system by using input and output binary counters so that information, such as capacity reduced to 10 percent and differences in input/output rates exceeding selected thresholds, can be detected and transmitted to the processor for performance monitoring. The scheme used to implement these alarm conditions is shown in Figure 33. The area of interest in this figure is how the relative difference between two counters, asynchronous to each other, can be monitored. This is done by using the terminal count of the output counter to set a latch that in turn sets an edge-triggered flip-flop clocked by the input timing clock, with the flip-flop output strobing the contents of the input counter into a storage latch. The number now loaded in the latch is the difference between the terminal count of the output counter and the input counter. All measurements of storage capacity are made by magnitude comparisons of the latched number with switch-selectable thresholds. To determine if the input/output rate differential is in excess of a predetermined threshold, a second latch is used to store a previous input counter number. The difference between the two latches is proportional to the rate difference.
Figure 33. Buffer Device Block Diagram
FRAME-SYNC ACQUISITION AND MAINTENANCE

A key function in digital combiners and multiplexers is frame-sync acquisition and maintenance. Each of the digital groups received by the CNCE is buffered to allow for timing variation and processed by a frame synchronizer to establish frame sync. It is important to determine the best framing methods that are consistent with the synchronization philosophy of the network. The links are subjected to RF fades and other degradation. Frame synchronization must be compatible with crypto synchronization because they are interdependent. Framing reacquisition times must be consistent with crypto resync times to implement cooperative resync. In addition, the framing pattern itself must be compatible with as many fielded models of multiplexers as possible. The framing analysis that follows is constrained to these bounds. Three methods of frame synchronization are examined:

1. The Bookkeeper Synchronizer, analysis of which is based upon a Monte Carlo simulation model of a Markov first order process.

2. A basic 2-mode synchronizer, which lends itself to an easier understanding of the processes involved.

3. A method that uses a Sequential Probability Ratio Test (SPRT) to determine the most optimum sync position.

Requirements

Frame sync must be maintained in fading environments experienced by both troposcatter (tropo) and line-of-sight (LOS) systems. In tropo systems, fades are characteristically fast and relatively shallow compared to the slow deep fades experienced in LOS. Consequently, the
synchronizer must be able to recover quickly from a fast tropo fade in which sync may have been lost and a bit slippage occurred as well as to coast through relatively long LOS fades where bit slippage is unlikely but the bit error rate (BER) is bad for a relatively long period of time. These requirements have prompted specification of the synchronization process as follows: the synchronizer must perform in a worst case environment of a nominal 0.1% BER condition with 20% BER bursts interspersed with a duty cycle of 5% occurring at a rate of 1 to 20 Hz. Under these conditions, the frame synchronizer must acquire sync within 50 milliseconds with a 0.9 probability and must be able to coast through a 5-second condition of BER worse than 20% without losing bit count integrity (ie, without the bit synchronizer slipping a bit).

The framing pattern used in this system is required to be an alternating 1-0 pattern spaced n bits apart. This pattern is compatible with many multiplexers now in use. The framing format has been discussed previously. A framing bit is followed by n bits of data where n is between 8 and 143. Therefore, the frame densities are from 1/9 to 1/144.

Basic 2-Mode System

Of the three synchronizers to be discussed, the basic 2-mode synchronizer is the simplest to analyze and implement. The fact that it is uncomplicated gives insight to the two more sophisticated methods that follow. The two modes of operation are "search" and "maintenance". That is, the system searches all bit positions for a sync pattern until one is found upon which it initiates a maintenance mode and checks only that position one frame away from then on until the
pattern ceases to occur; at which time, search for a new pattern is reinstated. The system description that follows is for sync patterns N continuous bits long separated by B data bits in the frame. For later comparison, N will be required to be 1-bit long and complemented every frame to produce the alternating 1-0 frame pattern. In addition, when there are more than one bit in the pattern, it may be better to allow e errors in pattern recognition and still accept it as good.

The logic of the basic two-mode system is shown in Figure 34. The serial data is shifted through an N-bit shift register, where N is at least as long as the known sync pattern. The pattern recognizer is programmed to provide two outputs. Whenever the expected sync pattern appears, during a bit interval, in the shift register with some preset number of errors e, or fewer, there is one output, and whenever there are e' or fewer errors, there is another output.

A single bistable mode register keeps track of whether the system is in the search or maintenance mode. The words search and scan are used interchangeably in this discussion, as are the words maintenance and lock. When in the search mode, the mode register controls the AND date to transmit a reset pulse to the counter, which counts out the bits between sync patterns whenever a pattern is found while scanning. The cycle length of the counter will always be the number of bits per sync frame. This same pulse also sets the mode register to define the maintenance mode, which then closes the AND gate so that no new resets can reach the counter while in the maintenance mode. During the maintenance mode, a gating of the counter defines when the next periodic sync pattern should again arrive if the last reset was caused by a true sync
Figure 34. Basic Two-Mode Sync Circuit
pattern. At that bit time, a clock pulse is inhibited from passing through gate A and setting the mode register to the search mode if the pattern recognizer does find another pattern of bits that resembles the expected sync pattern to the point of having e' or fewer errors.

The idea in the basic two-mode system is that, short of adding additional hardware to simultaneously test multiple scan decisions, the minimum time to acquire true sync can be obtained by taking each scan decision and making rapid tests to verify or reject that relative position in the data that appears to contain a sync pattern.

The selection of any combination of e or fewer errors while scanning for a possible sync pattern allows optimum balance between the probability of detecting a false sync pattern among the "random" data between sync patterns while increasing the probability of detection of the true sync pattern when it is reached but which may have some bits in error due to noise on the received signal. It is extremely desirable to be able to acquire sync rapidly and maintain it with a high degree of reliability in the presence of noise that is still slightly greater than that which would produce "barely usable data".

**Bookkeeper System**

The bookkeeper system uses one frame length of digital delay to compare bits one frame apart for correlation to the alternating pattern. Correlations are stored throughout each subsequent frame in a shift register that keeps track of all patterns of both false and true sync position. Alternating 1-0 patterns in false positions are sustained for relatively short periods of time compared to the true position. When all false positions are rejected, the true position remains without
initiating additional searches and the synchronizer begins maintenance mode, which accumulates only true sync positions in a confidence counter.

The logic of the frame synchronizer is shown in Figure 35. The incoming digital group data stream is clocked by the data rate clock through frame-length shift register A (also referred to as the DATA SR). During each bit time, the data bit at the input of DATA SR is compared against the output of DATA SR by exclusive-OR gate 1. The output of the exclusive-OR (a ONE when the comparison bits differ) is then AND'ed with the output complement of the B frame-length shift register (also referred to as the BOOKKEEPER SR) and the complement of the result fed back to the input of the BOOKKEEPER SR. Assuming the BOOKKEEPER SR to have been initially cleared, the continuous bit comparison and gating operations will result, after an interval of time, in all but one of the bits cycling through the bookkeeper register being set to ONE (due to the random states of all but the framing bits). The single ZERO bit, cycling through the BOOKKEEPER SR, then identifies the position of the framing pattern bits in the digital group data stream.

The modulo-N counter allows the frame synchronizer to operate in an error environment. Each time a ZERO is clocked from the BOOKKEEPER SR, the modulo-N counter is reset; thus, the counter cannot output a terminal count signal until only one ZERO bit cycles through the BOOKKEEPER SR. During the first terminal count output from the modulo-N counter, the output of the exclusive-OR gate is examined and if it is a ONE, the confidence counter is incremented, indicating the probable detection of the framing pattern. The confidence counter is then incremented or de-
Figure 35. Zero-One Frame Synchronizer Design Philosophy
cremented during each modulo-N terminal count output in accordance with the exclusive-OR gate output. Additionally, as long as the confidence counter is not at zero count, a ZERO will be clocked into the BOOK-KEEPER SR during the modulo-N terminal count output, irrespective of the output state of the exclusive-OR gate.

If, during the terminal count output of the modulo-N counter, the confidence counter is at zero count and the output of the exclusive-OR gate is zero, the BOOKKEEPER SR is reset to all ZERO's, initiating a new frame pattern search.

**SPRT Synchronizer System**

The SPRT (Sequential Probability Ratio Test) Synchronizer\(^1\) is based upon the premise that when testing a serial data stream for the occurrence of a known framing pattern, if a correlation decision is made a bit at a time and correlations vs noncorrelations stored, the true pattern will accumulate the highest confidence in the shortest time of any other method. A significant difference between the SPRT method and both 2-mode and bookkeeper methods is that it inherently adapts its confidence count to the error rate. That is, in low error rates, fewer correlations of pattern bits are required to establish a given degree of sync confidence than in a high error rate. In the other two methods, an attempt is made to optimize the threshold of confidence for the worst expected error rate and lesser error rates must use that value. This should be made clearer as the description continues.

Wald\(^1\) has shown that a SPRT of strength \((\alpha, \beta)\) for testing hypothesis \(H_1\) against alternate hypothesis \(H_0\) is defined by the inequality:

\[
\frac{\beta}{1-\alpha} < \frac{P_{in}}{P_{on}} < \frac{1-\beta}{\alpha}
\]  

(1)

where \(P_{in}\) and \(P_{on}\) are probabilities that \(H_1\) and \(H_0\) are true after \(n\) samples and \(\alpha\) and \(\beta\) are decision error probabilities in determining if \(H_1\) or \(H_0\) are true.

This inequality has been related to frame synchronization by noting the following correlation to the sync process:

- \(\beta\) = cost of rejecting good pattern.
- \(\alpha\) = cost of accepting bad pattern.
- \(P_{in}\) = probability density function of recognizing true sync.
- \(P_{on}\) = probability of accepting false sync.
- \(\Sigma J\) = number of bits that do not correlate with pattern after \(n\) samples.
- \(\Sigma I\) = number of bits that do correlate after \(n\) samples

\[\Sigma = n - \Sigma J\].

The inequality can now be interpreted. If each bit in the bit stream containing the framing pattern and random data is sequentially tested and correlation to pattern bits counted as \(P_{in}\) and noncorrelations counted as \(P_{on}\), the ratio \(P_{in}/P_{on}\) will eventually reach a limit determined by \(\alpha\) and \(\beta\) to either accept the preceding bits as framing bits or to reject them as random data (Figure 36). This, in effect, places limits \(L_1\) on the confidence counter determined by the bit error

Figure 36 SPRT Flow Chart

rate $E$ and the cost terms $\alpha$ and $\beta$. The cost terms are arbitrarily chosen to be the degree of correctness required by the sync decision and are found to be the exponent of the degree of correctness required. For example, if a decision is required to be correct to $1/1000$, $\alpha$ and $\beta$ are selected as minus 3.

With every agreement, the confidence counter counts up, and with every disagreement, it counts down, but not necessarily up-one, down-one. By manipulating the inequality, it can be shown that if the up count is by one, the down count is $K$, where $K$ is a function of the error rate $E$. The resulting synchronizer implementation is a system that compares each incoming bit to the expected frame sync pattern (Figure 37). Agreements increment a confidence counter by one; disagreements decrement by $K$ until either the upper limit of the counter is reached and frame sync is declared or the lower and absence of sync is declared. Upon declaration of the sync decision, the synchronizer enters a maintenance mode and thereafter checks only the selected frame position in each frame. If the pattern deteriorates later, due to a slip of bits or other causes, the confidence counter will be decremented to the lower limit and search mode will again be reinstated.

**Synchronization Program and Simulation**

Computer programs have been prepared for each method and provide a means of analyzing and predicting their performance. The 2-mode and SFRT synchronizers have been programmed by using probabilistic calculations based upon binomial probability. An additional consideration in the 2-mode program has been to model a confidence count with it, since it does not normally accumulate confidence counts. The search and
Figure 37. SPRT Block Diagram

1Ibid.
maintenance operations are more clearly seen and the confidence opera-
tion makes the 2-mode system more powerful (hence, practical and com-
parable to the other two methods). Both probabilistic programs assume 
that the error rate is constant during a particular sync process. The 
bookkeeper synchronizer was modeled by a Monte Carlo process whereby 
the synchronizer was simulated by the computer, a random data stream 
generated, and actual times to acquire sync tabulated. In the Monte 
Carlo simulation, the error rate can be easily modeled after the tropo 
or LOS fading characteristics; however, in this case, the error rate 
was constant as in the other two programs.

**Programs Based on Probabilistic Calculation**

(a) **Basic 2-mode system**

The computer program for calculating performance of the 
basic 2-mode is one that determines the probability of the occurrence 
of both true sync and false sync for every bit position in the frame 
one bit at a time, continuing through enough frames to assure that the 
accumulated probability of finding true sync is arbitrarily high. As 
the process proceeds through the frame, the probability of achieving 
either true or false sync depends upon the probability that neither was 
found in preceding bit positions. The program is an implementation of 
the expressions for the probability of achieving true sync expressed as 
the average number of bits to acquire true sync with the bit error rate, 
sync pattern length, and frame length as independent variables. For 
example, a set of calculations was made with a 6-bit sync pattern in a 
1024-bit frame at an error rate of 1 in 1000, (0.001). The result is 
expressed as the mean time to acquire sync. Then, one of the para-
meters, such as error rate, is changed to say 0.01, and the calculations repeated. A family of curves such as that in Figure 38 results, showing any of the independent variables of interest as a function of time to acquire true sync.

The basic expression is derived from the probabilistic occurrences in the system, of the probability of true sync, false sync, and bit errors. A definition of the terms involved is

\[ P_c \] is the probability of the occurrence of a pattern of \( n \) bits long in an error rate of \( e \)

\[ P_c = (1 - e)^n \], when no errors are tolerated in the correlation.

Some advantage can be obtained by allowing errors \( e \) in the pattern and still accept it as sync. In this case:

\[ P_c = \sum_{e=0}^{n} \binom{n}{e} P_c^e q^{n-e} \]  \hspace{1cm} (3)

where: \( P_c = 1 - e \)

\( q = e \)

which is recognized as the binomial probability theorem.

Similarly, \( P_i \) is the probability of detecting \( n \) bits of random data as an \( n \)-bit pattern:

\[ P_i = \sum_{e=0}^{n} \binom{n}{e} P_i^e q^{n-e} \]  \hspace{1cm} (4)

(THIS EQUATION IS CONTINUED ON NEXT PAGE)
Figure 38: Average Bits to Reacquire Sync Versus Sync Pattern Length
where \( P_i = 1 - 0.5 \)

\[ q = 0.5 \]

where 0.5 is the probability of a 1 or a 0 occurring in random data.

The quantities \( P_c \) and \( P_i \) are single-look probabilities. In analyzing the scan process, the accumulated probability of sync is desired. If the probability of finding false sync in one sample of random data is \( P_i \), the probability of not finding one is \( (1 - P_i) \). Then, \( P_i (1 - P_i) \) is the probability of finding a false sync pattern in the second sample of random data and the sum \( P_i + P_c (1 - P_i) \) is the probability of finding a false sync pattern in one of the first two samples. The probability of reaching a third sample without a false detection is \( (1 - P_i)^2 \). Proceeding with this line of reasoning, if \( P_t \) can be called the probability of finding a false sync pattern in \( b \) bits, then \( P_t = 1 - (1-P_c)^b \). The probability of reaching a sync position without a false sync and that of detecting true sync is \( P_c (1-P_t) \) and the probability that true sync is not detected in the first frame is \( (1 - P_c)(1 - P_t) \).

Without deriving the process any further, it can be shown that the mean time to the first sync decision and the probability that it is a correct one can be found by solving for \( P_c \), then \( P_t \) by:

\[ P_c = \frac{T}{M-1 + T}, \quad P_t = \frac{1 - T}{M} \]

where \( M \) is the average number of groups of data for the scan mode to come to a decision or:

\[ M = \frac{1}{P_t + P_c (1 - P_t)} \]
and $T$ is the probability that the decision is a correct one.

(b) **SPRT System**

A computer program\(^1\) for analysis of the SPRT system was developed in a manner similar to the 2-mode system, but is based on the implementation of the basic SPRT inequality:

$$\frac{\beta}{1 - \alpha} < \frac{P_{\text{in}}}{P_{\text{on}}} < \frac{1 - \beta}{\alpha} \quad (7)$$

where $\alpha$ and $\beta$ are decision error probabilities and $P_{\text{in}}$ and $P_{\text{on}}$ are the probability density functions of sync and random data, respectively, after $n$ bits; $P_{\text{in}}$ is the probability that the hypothesis $H_i$, thru sync, is true and $P_{\text{on}}$ is the probability that the alternate hypothesis, random data, is true.

Using these assumptions, after $n$ samples of serial pattern correlation $\Sigma j$ of errors occur and $\Sigma i = n - \Sigma j$ bits correlate, then the inequality becomes

$$\frac{\beta}{1 - \alpha} < \frac{\varepsilon_o \Sigma j (1 - \alpha) \Sigma i}{0.5 \Sigma j (1 - 0.5) \Sigma i} < \frac{1 - \beta}{\alpha} \quad (8)$$

making $\alpha = \beta$ and assigning $-L \Sigma i = K \Sigma j + L$, where

$$L = \frac{\ln \frac{\beta}{1 - \alpha}}{\ln 2 (1 - \varepsilon_o)}$$

$$K = \frac{\ln \varepsilon_o}{\ln 2 (1 - \varepsilon_o)}$$

The decision process of the SPRT is thus defined as follows. Each

\(^1\)Peter E. Mallory, *METHODS OF FRAME SYNC ANALYSIS.*
Figure 39. Mean Time To Reach Frame Sync

\footnote{Peter E. Mallory, Methods of Frame Sync Analysis, technical paper presented at National Telemetering Conference, Washington, D.C., July 1970.}
bit correlation increments an accumulator by one and each bit error decrements an accumulator by K. The resultant total is compared to the limits \( \pm L \). If \(+L\) is exceeded, an accept \( H \) (true sync) decision is made and if the total is less than \(-L\), a return to search or reject decision (accept \( H_0 \)) is made. Curves of mean time to acquire sync, based on the implementation of this inequality, are shown in Figure 39.

**Comparison of Synchronizers**

Each synchronizer discussed for this application has advantages and disadvantages. A summary of the relative merits of each for use in CNCE equipment is given in the following paragraphs.

The basic 2-mode synchronizer is not a contender for an operational system because it is too easily put into the search mode from a good sync condition. That is, because there is no confidence count in the maintenance mode, the detection of one bad pattern due to errors causes a rejection of the maintenance mode and re-initiation of search. The value of this system is its usefulness in understanding and analyzing the sync process and its simplicity of implementation. Even so, if the number of errors tolerated in the pattern is carefully selected from an understanding of the worst error rate expected, the mean time between losses of sync is long enough to make the system usable in applications where the error rate is favorable (say, no worse than \( P_e = 10^{-3} \)).

The bookkeeper synchronizer adds two important dimensions to the sync process, a confidence counter and a powerful method for rejecting false sync during search. Its immunity to false sync during search makes the bookkeeper synchronizer especially attractive to systems such as those used in TCCF with one-bit patterns, alternating 1 and 0, be-
cause even in random data every bit position in the frame looks like the start or end of a 1 - 0 pattern. By other scan means, such as the 2-mode system, many false starts would be attempted before the true sync position were found. It will be recalled that the bookkeeper register stores the results of all comparisons of each incoming data bit to the corresponding bit one frame away to see if it alternates 1 - 0. For as many frames as a given position continues to carry alternating 1 - 0, it is regarded as a contender for true sync. All positions thus noted are carried until it fails to alternate, whereupon it is dropped from consideration. Since the true position has by far the highest likelihood of continuing to alternate 1 - 0, all but one will eventually be dropped from contention and sync declared. It is this simultaneous "keeping book" on all sync positions in a frame, both true and false, that makes this synchronizer unique and powerful. The confidence counter adds another dimension by ensuring that once true sync has been observed for a number of times in its position, it cannot easily be rejected by errors in the pattern since it takes a number of bad patterns in a row to return to search. This powerful rejection of false sync makes the bookkeeper synchronizer ideal for a 1 - 0 distributed pattern where the probability of a false sync in random data is so high. However, the bookkeeper has three deficiencies that make it less than optimum:

1. In the search mode, the system will not declare true sync or go into the maintenance mode until two rather stringent conditions are met:

(a) There can be no false patterns remaining in the frame
(i.e., they must have all been dropped from contention by failing at least once to continue alternating 1 - 0).

(b) The true position or the one remaining after all others have dropped must not have had any errors from the start of the search mode (otherwise it too would have been dropped).

2 The confidence count is a fixed number.

3 Storage for a complete frame of data is required.

By requiring, in effect, one perfect frame in the search mode before going to maintenance, the average time to acquire sync is made longer than optimum. That can be seen as follows since the condition for the occurrence of $n$ pattern bits without errors is:

$$ P_C = (1-E)^n $$

(9)

The condition for the absence of false sync for $n$ frames with $b$ bits in a frame is:

$$ P_i = (1-0.5)^n (1-0.5)^b $$

(10)

Therefore, the condition for the occurrence of both events is:

$$ P_C P_i = (1 - 0.5)^{nb} (1 - E)^n $$

(11)

Since there are many bits per frame $b$, the likelihood of both events is less than the occurrence of the simpler event $P_C$ with errors $e$, which has been shown to be:

$$ P_C = \sum_{e=0}^{n} \binom{n}{e} P^e q^{n-e} $$

(12)

where $P = E$, $q = 1 - E$, summed to the $e$th power of $P$. 
The average time to acquire sync can then be made smaller than that attained by the bookkeeper method if a way is found to implement the recognition of sync with errors and still reject false sync equally well. Such a way has been designed by the author and presented in the next section.

The trouble with a fixed confidence count is that to be optimum, a higher count would be needed in high error rates and a lower count for lower rates. The average time to acquire is not affected since the system is in sync at the first detection of sync but once at the top count and having lost the true sync position due to a bit slip or other cause, the confidence counter must decrement once per frame to zero before returning to the search mode. During this time, it is still indicating true sync but is, in fact, in a false position. A synchronizer with a high confidence count limit set for high error rates will require more time than necessary to decrement when the error rate becomes low. That is, high error rates may require a top confidence count of say 20 frames to assure adequate confidence in the sync position while a low error rate may require only 3. If sync is lost in a low error rate, it is effectively penalized by the time required for 17 frames before initiating search and reacquisition in the new position. The full 20 counts would be necessary only when sync were lost under the worst conditions. Sync is in fact lost many times in good error rates due to bad error rates occurring at other links in a tandem connection of multiplexers.

The fact that one frame of data is stored in the synchronizer is not usually a troublesome factor. There are, however, some cases when delay for a full frame time before sync information reaches its destina-
tion is important. When the synchronizer is in a cooperative resync condition with a crypto unit, for example, the framing processors are interdependent and the addition of a multiplexer framing period to the crypto acquisition time is a significant amount. It would therefore be an advantage to eliminate as much delay as possible, not to mention the additional hardware required to effect a full frame storage of up to 1152 bits.

The SPRT synchronizer combines the best acquisition qualities of the 2-mode systems with the confidence count of the bookkeeper. An additional feature is the confidence count limit that is effectively adaptive to the BER. The SPRT system does not require a frame of storage but has the disadvantage of being more susceptible to false sync in the search mode than the bookkeeper. Another feature that makes the SPRT less than optimum is that in the search mode when a true pattern is being tested and fails to meet the true criteria due to errors, it is rejected and search is started in a new position. To be completely optimum, the fact that some correlation or some degree of confidence in the true sync position was initially attained is relevant information and should be stored and accumulated to be used as a starting point for the confidence count one frame later. The SPRT system is therefore a powerful method because of its adaptive, optimum confidence count, but suffers a loss of average acquisition time when used in a system like TCCF in which the pattern has a high probability of a false sync in random data.

Because the bookkeeping synchronizer is so well adapted for a 1-0 framing pattern, it is the best choice of the three for use in the TCCF
system. The suboptimum features of the bookkeeper do not cause it to perform in any way less than the specification requirements; therefore, it is the one selected for application in TCCF.

An Optimum Synchronizer

It is desirable to have a synchronizer with all the advantages of both the bookkeeper and the SPRT but with none of the disadvantages of either. Such a synchronizer would:

1. "keep book" on all candidate sync positions in search and accept true sync only after a decisive difference was seen between one position, true, and all others; thereby effecting a powerful false sync rejection.

2. Run a SPRT on all candidate sync positions, thereby effecting the acceptance of the best pattern, even when errors occur.

3. Accumulate confidence, or lack of confidence, in all candidate systems from the start of search until declaration of sync. The partial correlation of a pattern would be retained and accumulated from frame to frame until it is accepted. The fact that a true pattern is partially correlated is not lost just because it failed the minimum criteria on one scan.

4. Operate with no storage or delay of the data stream.

An optimum synchronizer that has all three desirable features has been designed by the author and is shown in Figure 40. The synchronizer consists of five major parts:

1. A pattern correlation matrix that provides the means to
Figure 40 Bookkeeper-SPRT Frame Synchronizer
correlate the incoming data with the sync pattern in n successive starting positions.

2 A correlation gate generator that supplies control to the correlation matrix so n successive data bits can be entered into each set of correlation.

3 An operating circuit to assign the proper weights to the correlation process, depending upon the strength of the SPRT process.

4 An SPRT result storage matrix that keeps running track or "book" on each test decision.

5 A sync-search decision circuit to interpret the test limit condition and matrix start of the test results.

The serial data stream is entered into the correlation matrix. The framing pattern is assumed to have n successive pattern bits in a frame of b bits. The first n pattern bits are entered into the first row of the pattern correlator by the modulo-n counter (1). There are n 3-input AND gates that are denoted the t₁ pattern correlator. One bit of the pattern is entered into one leg of each gate. A sequential test is performed on the n bits. Correlations are given weights +1 and non-correlations are given weights -K. Weight 1 is one clock pulse toward +L in the SPRT result storage matrix, whereas weight K is K clock pulses toward -L. When the second data bit arrives, it is entered into the t₂ pattern correlator as are the next n bits. The same weight storage process as with the t₁ correlation then repeats in the second up-1/down-K circuit and is stored in the t₂ section of the storage matrix. Note that while the first n bits are in the t₁ pattern cor-
relator column, the next n, starting one bit later with \( t_2 \), are in the \( t_2 \) column and that the second bit through bit \( n-1 \) are in both. The n-bit reference pattern is of course the same in all \( n \) columns of the matrix. The correlation matrix is organized in this way so \( n \) pattern bits may be serially scanned starting with each bit in the data stream. This makes it certain that by the time one frame of data is scanned, each starting position for an n-bit pattern has been tested.

Figure 41 shows how a serial data stream with six pattern bits is correlated and stored. At an arbitrary time \( t_1 \), data bit \( d_3 \) is entered into the first gate of the correlator; subsequently, \( d_2, d_1 \) and the first three bits of the true sync patterns are entered into \( t_1 \) pattern correlator. An accumulated weight results, moving a 1 storage condition toward either +L or -L in the storage matrix. This is designated as \( C_1 \) - starting-with-\( d_3 \). Starting with \( d_2 \) at \( t_2 \), correlation of \( d_2 \) through the next 4 bits of the pattern are done in the \( t_2 \) pattern correlator and the result designated a \( C_2 \) - starting-with-\( d_2 \) is stored. After \( t_6 \) is similarly tested, the next six starting positions are done the same way, again starting back at \( t_1 \). After one complete frame, the process has been repeated \( b/n \) times. When starting position \( d_3 \) is again under test, its accumulated confidence count is added to the results of the last test a frame away, thereby continuing a running confidence of each position. This feature is an improvement over any other method because, conventionally, a test is made of in bits and if errors cause rejections, the fact that some bits were correlated is not used. Of course, in the first run to \( t_4 \), there would have been correlation in this example, +L would have been enabled in the storage matrix, the
Serial Bit Stream With Pattern in Data

<table>
<thead>
<tr>
<th>Pattern</th>
<th>SPRT Test Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>t₁</td>
<td>d₁ d₂ d₃ d₄ d₅ 0 1 0 1 1 d₁ d₂ d₃ d₄ d₅</td>
</tr>
<tr>
<td></td>
<td>C C C C C C C</td>
</tr>
<tr>
<td>Is start position here?</td>
<td></td>
</tr>
<tr>
<td>t₂</td>
<td>d₁ d₂ d₃ d₄ d₅ 0 1 0 1 1 d₁ d₂ d₃ d₄ d₅</td>
</tr>
<tr>
<td></td>
<td>C C C C C C C</td>
</tr>
<tr>
<td>Accumulated Confidence Count, C</td>
<td></td>
</tr>
<tr>
<td>t₃</td>
<td>d₁ d₂ d₃ d₄ d₅ 0 1 0 1 1 d₁ d₂ d₃ d₄ d₅</td>
</tr>
<tr>
<td></td>
<td>C C C C C C C</td>
</tr>
<tr>
<td>Count C, C, C</td>
<td></td>
</tr>
<tr>
<td>t₄</td>
<td>d₁ d₂ d₃ d₄ d₅ 0 1 0 1 1 d₁ d₂ d₃ d₄ d₅</td>
</tr>
<tr>
<td></td>
<td>C C C C C C C</td>
</tr>
<tr>
<td>(Correct Position for Correlation)</td>
<td></td>
</tr>
<tr>
<td>t₅</td>
<td>d₁ d₂ d₃ d₄ d₅ 0 1 0 1 1 d₁ d₂ d₃ d₄ d₅</td>
</tr>
<tr>
<td></td>
<td>C C C C C C C</td>
</tr>
<tr>
<td>t₆</td>
<td>d₁ d₂ d₃ d₄ d₅ 0 1 0 1 1 d₁ d₂ d₃ d₄ d₅</td>
</tr>
<tr>
<td></td>
<td>C C C C C C C</td>
</tr>
</tbody>
</table>

Figure 41 Bookkeeper-SPRT Search Algorithm for 6 Bit Pattern
decision made to go into sync. This action would then have inhibited the limit decision of all other positions in the matrix except $t_1$. The reset of the bits-per-frame counter at time $t_4$ would then change the modulo-N counter indexing to start the true sync position at $t_1$ and the system would be in sync. If, at any time, errors in the pattern would cause $-L$ to be activated, the system would revert to the search mode.

It can be seen that prior to detecting a sync pattern, all positions are tested and a running "book" kept of each position. Since false sync positions build confidence more slowly than true and all false sync positions are tested along with true, the advantage of the bookkeeper synchronizer is retained without requiring the suboptimum condition of no errors in search and no false sync pattern in one frame. Errors are allowed in the sync pattern. The confidence count is based upon SPRT results from the assignment of weights; and there is no storage of the data stream required for synchronization. Therefore, the synchronizer incorporates all advantages of the bookkeeper and SPRT synchronizers with none of their disadvantages.

**CNCE Applications**

The framing formats in CNCE equipment are in the two general types of those with distributed pattern and those with contiguous pattern bits. Synchronous equipment such as the digital channel multiplexers and data channel multiplexers generally use the distributed 1 - 0 pattern because interface is made with the synchronous traffic network, which uses distributed patterns in other equipment. Asynchronous multiplexers use contiguous pattern bits probably because there is more freedom of choice
Figure 42. Sync Acquisition
Figure 43. Data Channel MUX Acquisition Performance for Worst Case Format
Figure 44. Telemetry Combiner Sync Acquisition
in the design and contiguous pattern bits give better performance.

The formats for the synchronous equipment are shown in the section on the digital and data channel multiplexer description made earlier. From the Monte Carlo simulation model of the 0-1 synchronizer referred to earlier, the performance curves are shown in Figure 42. The bookkeeper synchronizer confidence counter counts up-1/down-1 with a top count of 36 to allow coasting through a 50-ms period of 0-2 BER in the specified fading environment. The curves are for \( L = 1152 \) (a worst case condition); the accumulated probability of bottom count over 1 second including 50 ms of 0.2 BER and 950 ms of 0.001 BER for 36-level counter is \( 9.272 \times 10^{-10} \). Accumulating this probability as a binomial event over 86,400 seconds, the probability of no loss of sync is 0.9999202. From a count of 36, it detects loss of sync in random data on the average in 35.4 ms and with 99.9% probability in 60 ms. This far exceeds the requirements. The longest frame of the data channel multiplexer is 40 bits for twelve 2.0 or 2.4-kb/s inputs and outputs 32 kb/s. Figure 43 shows this performance.

The telemetry combiner sync acquisition results are shown in Figure 44. The telemetry combiner has up to thirteen 150-b/s inputs and outputs data at 2.0 or 2.4 kb/s. The curves show results for BER of 0.1 to 0.001 in the lowest sync density (that of 13 inputs). Approximately two frames (2277 bits, on the average) are required to achieve sync.

**DIPHASE CABLE AND ORDERWIRE ANALYSIS**

All data links access the node at the CNCE through interconnecting cables. Microwave links are terminated at the radio site in cable mo-
dems and transmitted 1/2-mile or more to the CNCE. Long-haul cable systems terminate directly at CNCE modems. Transmission data rates, discussed earlier, range from 32 kb/s to 18.72 Mb/s. Cable transmission is handled by different families of modems that are grouped by data rate and code type. One family handles bit rates of 32-kb/s to 288-kb/s diphase and uses a twisted pair cable (WF-16 field wire) for transmission. Another family handles rates from 512-kb/s to 4608 kb/s diphase, dipulse, or bipolar coding, depending upon the originating system. These rates use CX-11230 trin axial cable, which is a shielded twisted coax. For long-haul transmission of up to 40 miles of cable, regenerative repeaters are spaced every 1-1/2, 1, or 1/2 mile, depending upon the transmission rate. For transmission of data at 4.9152 Mb/s and 18.72 Mb/s, a high-speed family of modems is used with repeaters required at 1/4-mile intervals.

Dipulse and bipolar modems have been in use in existing systems. The asynchronous AN/TSQ-85 system uses the TD-976 multiplexer with a bipolar cable driver and TD-982 cable repeater. The TD-754 multiplexer used in the 1152/2304-kb/s 40-mile cable system is a dipulse coded system. These transmission systems have been previously designed and therefore will not be addressed here. Since the new TRI-TAC system uses diphase transmission, exclusively, a complete analysis of this type system is necessary. In addition, there is a change in the orderwire system attendant with the change to diphase. In both previous systems, an analog orderwire was placed on the cable below the dipulse or bipolar signal. The orderwire was an analog voice signal that was band-limited to approximately 1700 Hz. Since the data rates in both systems were
1152 kb/s or greater, there was a sufficient separation between the data and orderwire spectrum to give satisfactory isolation. The spectrums of both dipulse and bipolar signals go to zero at zero frequency and have little energy below 1700 Hz.

A different orderwire system exists on the diphase cable system. There is a 2.4-kb/s data orderwire and a 32-kb/s digital voice orderwire to be placed on all systems where the rate is 144 kb/s or greater. All signals are diphase. An arbitrary decision has been made to place both orderwires below the data for data rates greater than 1024 kb/s and to place the 32-kb/s orderwire above the data for data rates below 516 kb/s. In both cases, the group data will require band limiting at both ends of its spectrum to prevent overlap of the three spectrums. The spectrum of the three signals is shown in Figure 45. Band limiting of the group data required for the orderwires places a significant restraint on the optimization of the transmission system.

Equalization is the common term applied to the process of signal shaping pre-emphasis, compensation, or filtering that is done to optimize the output signal energy to compensate for losses or degradation in the transmission medium. Optimum equalization design involves the appropriate choice of transmitting and receiving filters so that the intersymbol interference is minimized to allow for signal regeneration with low probability of error in the presence of noise and degradation.

Equalization is accomplished by applying the pulse stream received from the cable through a preamplifier and fixed adaptive equalization amplifier sections (Figure 46). The purpose of the fixed section is to provide gross compensation of the cable characteristics. The adaptive
Figure 45. Diphasic Group Modem Spectrum
section compensates for cable temperature variations and for variations in cable length by inserting a shaped loss corresponding to an addition or subtraction of appropriate cable length, which keeps the overall characteristics constant over the range of variation.

Optimizing the System

An approach to optimizing the system, which includes equalization and signal detection, is to design the transmission system for minimum intersymbol interference and design the signal detection system for maximum signal-to-noise in the decision process. Since an increase in bandwidth tends to reduce intersymbol interference but decrease S/N, these goals are mutually contradictory and a design that is somewhat between the two extremes with a given signaling speed will be optimum. The transmission system is designed to produce a raised cosine impulse response to the input signal; the resulting signal is detected in a matched-filter integrate-and-dump decision process.

Signal Transmission

The signal P(t), a diphase-coded pulse train, is applied to the transmission medium comprising the filter at signal driver, \( H_t(f) \), the cable, \( H_c(f) \), and the receiving filter, \( H_r(f) \). These can be lumped into one transfer function, \( H_t(f) \). The output X(f) is then the result of applying P(t) to \( H_t(f) \) Figure 46B). In order for \( H(f) \) to respond to \( p(f) \) and produce no intersymbol interference, it is necessary that the output signal, expressed as a function of time, \( x(t) \), have a zero-crossing on the time axis at points where sampling of the pulse will take place (ie, at \( T, 2T, 3T, \) etc., as shown in Figure 47).

That is, \( x(t) \) should have periodic zero values spaced by \( T = \frac{1}{Y} \)
Figure 46. Cable System Equalization and Transfer Functions
where $\gamma$ is the signaling speed. This is known as Nyquist's first criteria and when it is satisfied, allows signaling at a rate of $2T$ without inter-symbol interference. The most practical function that satisfies this criteria is that of a raised cosine shown in Figure 48\(^1\).

The raised cosine is expressed in frequency and time as\(^2\):

$$X_\beta(f) = \frac{1}{2W} \cos \frac{\pi f}{4W} \Pi(f/2W) \quad X_\beta(f) = \frac{\pi f}{4\beta} \cos \frac{\pi f}{2} \quad \Pi \frac{f}{2\beta} \quad 0 < \beta \leq \frac{T}{2} \quad (13)$$

where $\Pi$ denotes a rectangular pulse of width $\gamma/2$.

$$x(t) = \text{sync} \frac{4Wt}{1 - (4Wt)^2} \quad x(t) = \frac{\sin 2\gamma t}{1 - (2\gamma t)^2} \quad \beta = \frac{\gamma}{2} \quad (14)$$

The problem of determining the best filter is then to solve:

$$H_t(f) = \frac{X(f)}{P(f)} \quad (15)$$

where $X(f)$ is the desired raised cosine response and $P(f)$ is the spectral density of the diphase input signal.

Since the characteristics of the cable are known, the above expression can be written as:

$$H_t(f) H_r(f) = X(f)/H_c(f) \quad P(f) \quad (16)$$

where any realizable combination of $H_t(f)$ and $H_r(f)$ that satisfies the expression is satisfactory.

The term $P(f)$ is the spectral density of the input signal. The time expression for the diphase signal is shown in Figure 49. The spectrum of $x(t)$ can be obtained either by autocorrelation in the time

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\(^2\)A. B. Carlson, ibid.
Figure 47 Nyquist Pulse

Figure 48 Raised Cosine Pulse Spectra

Figure 49 Diphasic Waveform

Diphasic: A one is represented by a change in phase of the symbol and a zero by no change.
domain and transformation to frequency by the Fourier transform:

$$P(f) = F[R(\tau)] = \int_{-\infty}^{\infty} R(\tau)e^{-j\omega \tau} d\tau$$

(17)

where $$R(\tau) = \frac{1}{T_o} \int_{-T_o}^{T_o} x(t) x(t+\tau) dt$$.

or by taking the Fourier transform of the basic signaling shapes, multiplying, and determine the spectrum from a consideration of the source probabilities of each symbol. The latter method is most straightforward and will be used.

It has been determined that the following expression is approximate for determining the spectral density of a diphase signal:

$$P(f) = \frac{1}{T^2} \sum_{n=-\infty}^{\infty} \left| P_1 \left( \frac{n}{T} \right) + (1-p) P_2 \left( \frac{n}{T} \right) \right|^2 \delta(f - \frac{n}{T})$$

(18)

$$+ \frac{1}{T} P(1-p) \left| P_1(f) - P_2(f) \right|^2$$

where $T =$ the period of the transmitted signal or Baud rate.

$p =$ the source probability of 1 or 0 being transmitted.

$P_1 =$ the spectral density of the full-rate pulse.

$P_2 =$ the spectral density of the half-rate pulse.

This applies because, in diphase, the transitional probabilities between any two symbols are the same and the stationary probabilities of both sets of signals are the same. The two signal sets are rectangular pulses at the signaling pulse period and at half the signaling pulse period.

For a source probability $p$ of 1/2, $P(f)$ becomes:

$$P(f) = A^2 T \frac{\sin^4 (\pi ft/2)}{(\pi ft/2)^2}$$

(19)
The expression for the transfer function then becomes:

$$H_t(f) H_r(f) = \left[ \frac{1}{H_c(f)} \right] \left[ \frac{2W \cos^2 \frac{\pi f/2W}{A_T \sin^2 \frac{\pi f T/2}{(\pi f T/2)}}}{(\pi f T/2)} \right] \Pi \left( \frac{f}{2W} \right) e^{j\omega t} \tag{20}$$

The cable transfer function, $H_c(f)$, is determined from the CX-11230 cable. The characteristics of the cable have been determined from its specifications and measured data to closely conform to the empirical relationship:

$$\text{Loss/mile} = 50 \log_{10} \left[ 1.37 + 1.25 \times 10^{-6} f \right] + (0.625 \times 10^{-6} f)^2 \text{db} \tag{21}$$

Figure 50 shows the cable characteristics and an amplifier gain curve that has been matched to compensate for cable losses.

**Signal Detection**

Matched filter signal detection is a method that allows a bit decision to be made at a time when the signal-to-noise ratio at the filter output is maximum. The signal-to-noise ratio, expressed as a function of $H(f)$, $X(f)$, and $G(f)$, is shown to have the solution:

$$H(A) = K \frac{X^*(A)}{G_n(f)} e^{j\omega t_0} \tag{22}$$

where $G_n(f)$ is the power spectral density of white noise.

If the output of this filter is sampled at $t_0$, the optimum bit decision can be made. In diphasic, $t_0$ occurs at the end of the bit period.

In previous paragraphs of this thesis, it was shown that the best

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Figure 50. Cable Attenuation Characteristics, CX11233 Cable
results could be obtained by a raised cosine response to the transmission system transfer function. If $X(f)$ is therefore a raised cosine, it can be applied as $X(f)$ in the above expression; the result is a filter matched to the optimum response.

There are practical difficulties, however, in a matched filter. One is that matched filters are difficult to build in practice and must be approximated. Furthermore, because the integration results in spreading energy from one bit over two-bit periods in a triangular shape, that is not consistent with Nyquist criteria, they lead to increased intersymbol interference. The intersymbol difficulty can be avoided by dumping or discharging the energy in the filter immediately after the decision has been made at $t_0$. The energy that would have remained after the bit decision to contribute to intersymbol interference is eliminated. The matched-filter integrate-and-dump technique therefore retains the desirable feature of minimizing intersymbol interference and, at the same time, maximizing the signal-to-noise ratio in the system. The optimization goals stated at the outset are therefore approximately realized.

Several practical matters make an approximation to the optimum necessary. No realizable filter can cut off to absolute zero like the raised-cosine. A sharp cutoff filter requires multiple poles in the transfer function and may be difficult to realize. Filter designs, based on a Bessel pole pattern, for maximum flat envelope delay or a Butterworth filter, are approximations. The Butterworth-Thomson filters provide another compromise but may still require additional equalization. These tradeoffs, as well as the complexity of the filters,
must enter final design considerations.

A computerized optimization strategy can be used to adjust equalizer parameters until the error probability based on the computed equalized response is minimized. Considerations in the program can be included for:

1. Unequalized pulse shapes at various cable lengths and temperature.
2. Noise and crosstalk.
3. Amplitude degradation of the regenerator.
4. Sampling offsets and timing jitter.

The strategy used to optimize $H(f)$ in the above expression can be illustrated by writing a computer program in which the only variable is the transmission bandwidth. It is possible to optimize the eye opening of a digital signal simulated responding to $H(f)$ by observing the effect on the eye opening of varying filter bandwidth. Of particular interest is the effect of eliminating response at the low end of the spectrum, since a section of the low end must be isolated for the transmission of orderwires in the regions from 4 to 32 kb/s. Figure 51 shows the degradation of the eye pattern from such effects obtained by computer analysis.

DESIGN DECISION STUDIES

During the course of this investigation, two specific areas have been noted that require additional study before design decisions can be made. They are:

1. A study to produce the best method for combining telemetry data from sources external to the CNCE.
<table>
<thead>
<tr>
<th>LOW-FREQUENCY CUTOFF, NORMALIZED TO DATA RATE, D</th>
<th>HIGH-FREQUENCY CUTOFF, NORMALIZED TO DATA RATE, D</th>
<th>EYE PATTERNS</th>
</tr>
</thead>
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<td></td>
</tr>
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<tr>
<td>0.5D</td>
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</tbody>
</table>

Figure 51. Eye Pattern Degradation From Non-Optimum Bandwidth
A study to determine to what extent modems and multiplexers should be combined.

Both apply to field application of the DGM equipment and not to the CNCE.

Combining Received and Local Telemetry in DGM Applications

A system study should be made to produce the best method for combining telemetry data. This would stem from a study of the requirements for the flow of telemetry information in the system to determine the best method for combining telemetry in a received group with locally generated telemetry for further transmission to the CNCE.

The DGM family provides a system of 2.0-kb/s supervisory channels in-band that carries telemetry information in the format of each multiplexer. Furthermore, there are 32-kb/s out-of-band channels in some modems for orderwires that can carry telemetry, if necessary. This is in addition to 4-kHz analog channels in the diphase and bipolar modems that are included for compatibility with the analog system. Telemetry signals are generated in each DGM equipment at 150 b/s for transmission to a remote facility over one of these channels. In some situations, only one of these 2.0-kb/s supervisory channels is used for each 150-b/s telemetry signals. For equipment simplicity, an over-sampling rather than a time-division multiplexing technique is required at each multiplexer. While this method adds versatility to the DGM multiplexers and may be adequate in simple deployments, it is not adequate where large numbers of modems or other telemetry generating equipment are in the same location. In addition, there are hybrid situations in which ATACS analog or asynchronous equipment is used with the all
digital DGM system (refer to Figure 8). In these situations, it may be advantageous to use common transmission channels and combining equipment wherever possible. Telemetry combining and data channel multiplexing equipment under development for use in the CNCE, if appropriately modified for field usage, could meet all-digital requirements but would not be entirely satisfactory for hybrid situations. It is necessary, therefore, to determine from this study the proper mix of inventory equipment, equipment now under development, and possibly new equipment designs to meet the telemetry system requirements.

A telemetry system study should be performed that takes these considerations into account and has the specific objective of determining the best methods of combining telemetry information in a received group with locally generated telemetry for further transmission. The study should consist of the following phases (Figure 52):

(a) **Requirement Definition** - The objectives of the study would be related to system requirements. The telemetry function in tactical situations would be studied with the combining and transmission requirements defined.

(b) **Selection of Alternatives** - Alternative methods of meeting the requirement should be selected. Candidates may be:

1. Telemetry combining in each DGM multiplexer.
2. Telemetry combining by new design.
3. Use of TCCF telemetry combiner and data channel multiplexer equipment (Figure 50B). The use of the TCCF telemetry combiner and data channel multiplexer provides an additional level of flexibility in the
a), b) Telemetry Equipment

c) Study Phase

Figure 52. Combining Received and Local Telemetry
2.0-kb/s interface.

4 Use of ATACS inventory equipment such as TD-1069 (Figure 50A). The TD-1069 data combiner, which is presently used with the TD-1065 and TD-660 to insert data at a rate of 75 to 9600 b/s into the ATACS 576-kb/s groups, if modified to operate in a slaved-clock mode, could combine any 150-b/s telemetry outputs from DGM or other equipment and output at 32-kb/s diphase into a DGM telemetry channel.

Whatever combining equipment is ultimately used will require format compatibility within the DGM family, with the CNCE, and with the CSCE (since in some situations telemetry may be routed directly to the CSCE bypassing the CNCE).

(c) System Analysis - An analysis should be made of each of the alternate systems defining all the pertinent performance characteristics.

(d) Comparison and Recommendations - A comparative analysis should be made of all candidate systems, using system criteria appropriately selected in accordance with system and study objectives. The best method combining received and local telemetry should be recommended from this comparison.

Integrated Multiplexers and Modems

A tradeoff study should be performed to determine the feasibility of integrating modems with multiplexers to reduce equipment in situations in which both may be used together. The LGM, TGM, and MGM equipment are used in DGM applications in which the main function is
combining and decombining of loops, groups, trunks, and supergroups in contrast to RMC and RLGM equipment that have dual functions of combining and cable driving. In the latter case, integration of multiplexer and modem functions is justified since this equipment serves small groups of users in remote areas. This minimizes the combining function with respect to that of cable drivers. In the former case, the reverse is true. Hence, the separation of the multiplexing functions of the LGM, TGM, and MGM from that of the cable modems for larger scale applications (Figure 51). But in overall system usage, there is expected to be a large number of applications in which these multiplexers are required to drive cables compared to those in which the multiplexers are used strictly for hierarchial combining. This fact introduces the likelihood that a considerable simplification of equipment and cost savings could be made if integration of the diphase modem function into the LGM, TGM, and MGM could be justified. Whether or not this is feasible depends upon the ratio of multiplexers that drive modems to those that simply combine in all deployments that can be anticipated. The objective of this study would be to determine if it is practical from operational and cost-effective considerations to provide integrated equipment.

The technical problem stems from the fact that the operational mode for the combining function is NRZ because it is a full baud binary signal, and diphase is desirable for transmission because of its spectral characteristics and its predictable occurrences of bit transitions which make timing recovery easier. Cable equalization and drive requirements as well as orderwire channels are also considerations.
Another factor to consider is the interface with security devices. This is an NRZ interface and must occur between the multiplexer and modem (Figure 53). Therefore, any integrated configuration would necessarily require access to the security device before the cable driver function. This has both advantages and disadvantages. The BCI restoral is aided because information of sync outages on the link is available to the multiplexer at the same time as the security device, making the restoral decision process simpler, but the fact that secure and nonsecure signals then appear in the same equipment is undesirable.

Several alternatives to the present approach are available. One is to simply provide two types of multiplexers, one for the NRZ combining function and a second that has a diphase cable modem. Another approach is to provide a modular modem that can be plugged into a multiplexer chassis, and derive power and timing. Other alternatives may also be desirable.

The approach to the tradeoff study would be (Figure 52) to:

1. Determine as closely as possible what future deployments will be so the ratio of multiplexers outputting directly to cables to those that do not can be determined.

2. Select alternate methods of integrating modems with multiplexers.

3. Analyze each of the alternates, considering the input on interfacing equipment, such as security devices, as well as internal equipment functions.

4. Provide a tradeoff of the alternate approaches, making a companion of the operational features, logistic impact.
Figure 53. Integrated Multiplexers and Modems
and life-cycle costs of each.

5 Recommend the most desirable alternative for possible incorporation in the program.
SELECTED BIBLIOGRAPHY


