Development of a UHF Digital Frequency Synthesizer for Distance Measuring Equipment

1975

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DEVELOPMENT OF A UHF DIGITAL FREQUENCY SYNTHESIZER
FOR DISTANCE MEASURING EQUIPMENT

BY

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RESEARCH REPORT
Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Engineering
in the Graduate Studies Program of
Florida Technological University

Orlando, Florida
1975
ABSTRACT

This report summarizes the design of a digital frequency synthesizer for airborne distance measuring equipment.

It is the purpose of the frequency synthesizer to provide a stable frequency source for the local oscillator of the airborne receiver and for the power amplifiers in the transmitter chain.

The synthesizer is required to furnish a frequency ranging from 260.250 mHz to 287.50 mHz in channel steps of 250 kHz at a power level of +7.0 dBm. The stability of the frequency must be greater than .005% over the temperature range of from minus 45 degrees centigrade to plus 55 degrees centigrade, requiring a crystal controlled source. Digital techniques are employed using two crystal controlled oscillators to synthesize all required channel frequencies.

Linear circuits using standard configurations are employed for the oscillators, buffers, and mixers. Primary attention is paid to optimizing the transient characteristics of the synthesizer which employs programmable digital counters to change the division ratio in a phase locked loop. Decoding is provided to interface the modulus of the counters with the aircraft cockpit controls.
# TABLE OF CONTENTS

ABSTRACT .................................................................................. iii

LIST OF TABLES ............................................................................ v

LIST OF ILLUSTRATIONS .............................................................. vi

1.1 INTRODUCTION ....................................................................... 1

1.2 PREDESIGN CONSIDERATIONS ............................................... 3

1.3 INITIAL DESIGN ..................................................................... 7

2.1 VOLTAGE CONTROLLED OSCILLATOR ................................. 15

2.2 VARIABLE MODULUS DIVIDER ................................................ 20

2.3 PHASE DETECTOR .................................................................... 31

2.4 LOOP CHARACTERISTICS ....................................................... 41

2.5 SPURIOUS OUTPUTS ............................................................... 53

2.6 PERIPHERAL CIRCUITRY ......................................................... 60

3.1 SUMMARY AND CONCLUSIONS ............................................. 64

APPENDIX .................................................................................... 65

BIBLIOGRAPHY ............................................................................. 74
LIST OF TABLES

1. Computer Survey of VCO Components ....................... 18
2. Worst Case Analysis of Direct Loading .................... 25
3. Worst Case Analysis with Frequency Extension .......... 28
4. Unstable States of Phase Detector ....................... 36
5. Loop Error Response for Step Inputs ..................... 43
6. Frequency Relationship for Single Channel Change ...... 47
7. Frequency Relationship for Band Edge Channel Change ... 48
8. Calculated Loop Parameters ............................... 50
9. Summary of Loop Parameters ............................... 51
LIST OF ILLUSTRATIONS

1. Block Diagram of Total System Approach ........................................ 1
2. Block Diagram of General System Concept ....................................... 2
3. Phase Lock Loop with Divider Network ............................................ 7
4. Frequency Scheme Using E C L Approach ......................................... 10
5. General Block Diagram of Frequency Synthesizer .............................. 13
6. Block Diagram for Final Synthesizer System .................................... 14
7. VCO Circuit Configuration .......................................................... 15
8. Programmable Divider Chip Operations .......................................... 21
9. Cascade Configuration for Division by Fixed Integer .......................... 22
10. Worst Case Analysis of Direct Loading ........................................... 24
11. Frequency Extender Technique for Programmable Divider .................. 26
12. Timing Diagram of Frequency Extender Operation ............................ 27
13. Final Version of Programmable Divider ......................................... 29
14. Idealized Frequency-Phase Comparator Response ............................. 31
15. Pulse Rate Comparison ................................................................... 32
16. Frequency/Phase Comparison Circuit .............................................. 34
17. Action Map for Freq/Phase Comparator .......................................... 34
18. State Transition Diagram for Figure 16 .......................................... 37
19. Low Pass Filter Pumping Operation ............................................... 38
20. Closed Loop System with Defining Equations ................................... 41
21. Error Due to Phase Step .................................................................. 44
22. Error Due to Frequency Step .......................................................... 45
23. Error Response of High Gain Loop ................................................. 46
24. Open Loop Equivalent Circuit ....................................................... 49
<table>
<thead>
<tr>
<th>Illustration</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>Loop Model for Spurious Analysis</td>
<td>55</td>
</tr>
<tr>
<td>26</td>
<td>Finite Pulse from Phase Comparator</td>
<td>56</td>
</tr>
<tr>
<td>27</td>
<td>Offset Currents in Low Pass Filter</td>
<td>58</td>
</tr>
<tr>
<td>28</td>
<td>Lowpass Network in Loop Filter</td>
<td>59</td>
</tr>
<tr>
<td>29</td>
<td>Total System Schematic</td>
<td>63</td>
</tr>
<tr>
<td>30</td>
<td>Finite Pulse for Fourier Analysis</td>
<td>68</td>
</tr>
<tr>
<td>31</td>
<td>General Phase Locked Loop</td>
<td>70</td>
</tr>
<tr>
<td>32</td>
<td>Digital Phase Locked Loop</td>
<td>71</td>
</tr>
<tr>
<td>33</td>
<td>Lowpass Filter</td>
<td>72</td>
</tr>
</tbody>
</table>
DEVELOPMENT OF A DIGITAL FREQUENCY SYNTHESIZER
FOR DISTANCE MEASURING EQUIPMENT

1.1 INTRODUCTION

A stable frequency source which ranges from 1041 to 1150 MHz in 1.0 MHz steps is to be developed. Economic and technical considerations show that it is practical to synthesize a frequency ranging from 260.25 MHz to 287.50 MHz in steps of 250 kHz to be multiplied by four in a later stage. The multiplied output which ranges from 1041 to 1150 MHz is then used to provide both drive for the transmitter and a local oscillator signal for the receiver. A block diagram of this general approach is shown in Figure 1.

Using this approach, the drive level into the multiplier must be at least +7.0 dBm across the synthesizer band.

Figure 1. Block Diagram of Total System Approach
Economic considerations dictate that frequency mixing be employed to reduce the VHF output frequency to a lower frequency where low-cost logic may be employed to lock the phase of the output frequency to the phase of a single low frequency reference crystal controlled oscillator.

The block diagram of the general system concept of the digital frequency synthesizer is presented in Figure 2.

The primary technical requirements for the synthesizer are:

1. Maximum time between channel changes should not exceed 100 milliseconds.
2. Spectral purity of the output of the voltage controlled oscillator must be maintained such that all frequencies except the carrier fundamental are suppressed greater than 60 dB.
3. The output level must be greater than +7.0 dBm across the band from 260.25 MHz to 287.50 MHz.

Figure 2. Block Diagram of General System Concept
1.2 PREDESIGN CONSIDERATIONS

The following electrical and mechanical guidelines shall apply in the design phase of the digital frequency synthesizer.

1. All digital integrated circuits shall be from the low cost 7400 series wherever possible.

2. The unit must function with required output level, frequency tolerance, and spectral purity over the temperature range from -40°C to +55°C.

3. Minimum size must be attained. The maximum size allotted for the synthesizer and code translator shall be 9.5" x 4.0".

4. Troubleshooting must be as simple as possible. No technique shall be used which will lead to expensive repair time.

5. All devices shall be low cost, solid state, and readily available.

The phase-locked digital loop shall employ a digital phase detector whose output is used to control a voltage sensitive oscillator. If the output frequency and the reference frequency are synchronous in phase, the system is said to be locked. If the phase of the VCO (voltage controlled oscillator) begins to either lead or lag the phase of the reference oscillator, a correction voltage is generated which restores the phase
synchronization. In this way a free running oscillator may be given crystal controlled stability.

Digital frequency synthesizers in general have certain problem areas which must be dealt with in a system concept. A complete awareness of these areas must be reached in order to begin a paper design. The major areas are presented here.

1. Any phase change in the high frequency oscillator is reduced in magnitude by the division ratio of the counters. Since the division ratio (modulus) changes from channel to channel, the phase error presented to the phase detector becomes a function of channel selection.

2. A voltage controlled oscillator using voltage sensitive capacitors, or varactors, has a non-linear frequency versus voltage characteristic resulting from the varactor's exponential voltage characteristic. As the control voltage changes across the band, the amount of control any correction voltage can exert will vary.

3. The characteristics of the digital phase detector employed must not be susceptible to false errors associated with harmonics of the input signals and must be able to detect frequency as well as phase differences. This allows the capture range of the
loop to be equal to the lock range. With this constraint, many limits imposed on the system by linear forms of phase detection are eliminated.

4. The output of any digital phase detector contains harmonics of the lowest frequency present which, in a locked condition, will be the reference frequency. If these harmonics are allowed to reach the VCO they will create undesired sidebands on the carrier and severely degrade the spectral purity.

5. While the system is acquiring lock, many undesired frequencies are present at the output. The transmitter must be prevented from turning on until the system becomes locked.

6. The phase of the various signals through both the digital and linear devices will be susceptible to noise on the supply voltage lines. The sensitivities of each device to supply voltage variations must be considered and additional regulation provided if necessary.

7. The time required to change output frequencies and reach a stable condition, or lock time, is usually a major constraint in digital synthesizers. However, for DME (distance measuring equipment) applications, where the system is not expected to respond instantaneously to a channel change, the lock time is not a
critical area. Other timing constraints in the system allow a synthesizer lock up time of at least 100 milliseconds, which is an order of magnitude longer than the state of the art is capable of. This relaxed constraint simplifies the trade-offs required to generate desirable closed loop transient performance.
1.3 INITIAL DESIGN

It is the purpose of a digital frequency synthesizer to generate a band of crystal controlled frequencies in the VHF (very high frequency) band from 260.25 to 287.50 MHz by using a voltage controlled oscillator (VCO) whose output frequency is phase locked to a low frequency standard. The approach used will take the form of a digital divider inserted in the feedback path of a phase locked loop. Such an approach is illustrated in Figure 3.

![Phase Locked Loop with Divider Network](image)

Figure 3. Phase Locked Loop with Divider Network

A low pass filter is inserted between the phase detector and the VCO for two reasons:

1. To filter the output of the phase detector and minimize any spurious frequencies which may be presented to the VCO.

---

2. To govern the transient response of the loop for both open and closed loop operation.

For the phase inputs of the phase detector to be synchronous, the output frequency must be $N$ times the reference frequency. By changing the division ratio $N$, the output frequency can be made to be any integral multiple of the reference frequency. In this manner a very high frequency can be made to step in increments and remain phase locked to the reference.

If the reference frequency is equal to the channel spacing (for this general model in Figure 3), the output channel frequency can be selected by choosing a proper division ratio ($N$) in the divider.

The reference source in the loop consists of a crystal controlled oscillator which is divided by means of a fixed divider to obtain the desired reference input. Because of a size and price tradeoff in crystals, it is generally desirable to use crystals above approximately three megahertz in reference oscillator designs. In this design, a 4 MHz oscillator was used as a source to be divided to the proper reference frequency.

The transistor-transistor (TTL) logic selected for use in the variable modulus counter will have an upper frequency range of approximately 20 MHz when used as a variable divider. It is desirable to shift the VCO frequency to this range without reducing the frequency error which is presented in the unlocked condition. This can be done by mixing the VCO frequency with a
crystal controlled frequency and using the resulting intermediate frequency as the effective input to the variable dividers.\textsuperscript{2} Since VCO output frequency is sensitive to variations in temperature, the mixing frequency must be removed from the output frequency band by as large a separation as possible to insure that the VCO frequency will not swing below the mixing frequency and provide a result which would generate a correction voltage of the wrong magnitude. However, in order to present a frequency to the variable divider which does not exceed the speed limitation of the logic, the mixing frequency should be selected to be as close to the band to be shifted as possible.

A compromise is made where the initial intermediate frequency is handled by the higher speed ECL family in a fixed divider whose output is then used to drive the programmable dividers (TTL).

Emitter-coupled logic was chosen for the fixed divider over the other forms available (Shottky, High-Speed TTL) because of the ease of constructing a suitable driving circuit. As the output of the mixer chosen will be typically 30 millivolts, (any higher levels may create a spurious output suppression problem) it is necessary to get this relatively low level signal into a logic form as quickly and as cheaply as possible.

As ECL requires a lower voltage swing to drive it, a driver was designed around an ECL triple line receiver with the first two sections biased in the linear mode. Typical performance with this low cost technique is to obtain reliable ECL output swings of less than 3 millivolts at frequencies in excess of 100 MHz over the full temp range. Furthermore, the cost of this arrangement is substantially the same as a discrete amplifier which could drive TTL at reduced performance levels. The extra margin on frequency response is desirable as the VCO will always overshoot when being channeled from the low end of the band to the high end, the amplifier divider chain must be able to accommodate this upper frequency limit or no signal at all would be sent to the variable divider. With these arguments, the ECL approach is used and is presented in Figure 4. Note that the highest frequency applied to the variable divider is now 9.4375 MHz which will allow substantial overshoot before the 20.0 MHz speed limit is approached.

![Figure 4. Frequency Scheme Using ECL Approach](image-url)
As a fixed divider has been inserted before the variable divider, the output frequency equation now becomes:

$$F_{\text{out}} = (4) (N) F_{\text{ref}}$$

The required reference frequency to produce a 250 kHz channel step becomes 62.5 kHz, a result of adding a fixed divider in the loop. Consequently, 62.5 kHz must be supplied at the reference input to the phase detector. Economic considerations reveal that a feasible approach is to use a crystal oscillator at a fundamental frequency of 4.0 MHz and a fixed divide by sixty-four circuit consisting of six T^2L flip-flops in two packages connected as ripple counters. The general block diagram for the synthesizer is presented in Figure 5.

Summing the frequencies involved around the loop and referring to Figure 6, an evaluation can be written for the output frequency.

$$F_{\text{out}} = (62.5 \text{ kHz}) (4 N) + (3 \times 83.250 \text{ MHz})$$

For an $F_{\text{out}}$ which ranges from 260.250 to 287.50 MHz, the required range of $N$ is from 42 to 151. However, the mechanics of the programmable divider are such that the actual count performed by the divider will be two greater than the count appearing on the data input lines. Thus the data input must be coded from $N = 40$ to $N = 149$.

The mixer employed will provide only limited isolation of the input frequencies from port to port. Additionally, the output of a low-cost VCO will not be sufficient to drive either
the multiplier which follows the synthesizer or the mixer employed, both of which require +7 dBm for proper operation. Therefore, two buffers will be used to provide increased isolation and gain.

To provide noise immunity from the supply voltage for the sensitive VCO and buffer circuitry, an internal voltage regulator will supply a stable source voltage for these elements.

The block diagram for the final synthesizer system is presented in Figure 6.
Figure 5. General Block Diagram of Frequency Synthesizer

- VCO: 260.250, 287.500
- Tripler (249.750)
- Offset Oscillator (83.250)
- Mixer: 10.5 + 37.75
- Low Pass Filter
- Wideband Amplifier
- Phase Detector
- Programmable Divider: N = 42 to 151
- ECL divided by 4: 9.4375, 2.625
- Reference Output (62.5 kHz)
- Output (62.5 kHz)
Figure 6. Block Diagram for Final Synthesizer System
2.1 VOLTAGE CONTROLLED OSCILLATOR

The purpose of the voltage controlled oscillator is to provide an output frequency which is a function of the control voltage presented to it. The circuit configuration chosen is a modified Clapp which uses a varactor in series with the tank inductance. As the output frequency must vary from 260.250 MHz to 287.50 MHz, the actual range of the VCO must be

![VCO Circuit Configuration](image-url)
greater to allow for overshoot of the phase lock loop during the
acquisition of the desired frequency. As stability and spectrum
purity are the major criteria here, we shall not be concerned
with power output at this point. Two buffers shall be used to
provide the required +7 dBm into the output load channel and
the synthesizer feedback channel. This approach eases the
design requirements upon the VCO and provides substantial
isolation between the load and the VCO and between the load
and the offset oscillator. The circuit configuration for the
VCO in simplified form is presented in Figure 7.

Appropriate bias levels are easily determined by the
design sheets of the transistor selected and the effort here
is primarily to arrive at suitable values for the tank components
in the VCO. The stray capacitance of the transistor base is
estimated to be about five picofarads which will appear across
the tank in the form of a fixed capacitance.

A varactor is normally specified at four volts reverse
bias and a wide range of standard values are available. The
capacitance versus voltage characteristics for a varactor is
of the form:

\[ C_V = (C_{\text{4volts}} - C_{\text{pkg}}) \left( \frac{V + .65}{4.65} \right)^{-N} + C_{\text{pkg}} \]

where \( V \) = applied reverse voltage

\( C_{\text{pkg}} \) = varactor package capacitance (typ. .2 pf)

\( N \) = a constant which will be in the neighborhood

of .47
The last arbitrary specification is the range of the input tracking voltage which is used to tune and control the VCO. The minimum reverse voltage which can be applied to a varactor, a DC level, should be greater than the highest voltage developed by the oscillations, which in turn is dependent upon the ratio of the feedback capacitance, $C_1$ and $C_2$ in Figure 7. As an operational amplifier will be incorporated in the low pass element which will provide the control voltage, there is some flexibility in this selection.

A computer program was written to calculate the values of inductance and fixed capacitance as a function of various ranges of tracking voltages and varactors available. A selection was then made based on the amount of fixed capacitance required versus the minimum reasonable inductance, a direct trade-off in this circuit configuration. The results are presented in Table 1.

If by arbitrary selection $C_1 = C_2 = 8$ pf, this gives a minimum fixed tank capacitance of 9 pf, without having an adjustment. Since an adjustment is desirable to compensate for tolerances, those varactors which require a fixed capacitance less than 9 pf can be eliminated.

The remaining constraint is the inductance value which should be made as large as possible to minimize the effect of track inductance when using printed circuit construction. This will yield a compromise value for the varactor by which all other circuit constraints may be met.
<table>
<thead>
<tr>
<th>Varactor $C_{4v}$ (pf)</th>
<th>Max Varicap C (pf)</th>
<th>Min Varicap C (pf)</th>
<th>Tot. Fixed C (pf)</th>
<th>Inductance (nh)</th>
</tr>
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<tr>
<td>6.8</td>
<td>6.8</td>
<td>4.05</td>
<td>3.4</td>
<td>164</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>7.08</td>
<td>5.8</td>
<td>96</td>
</tr>
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<td>15</td>
<td>15</td>
<td>8.83</td>
<td>7.2</td>
<td>77</td>
</tr>
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<td>22</td>
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<td>12.9</td>
<td>10.5</td>
<td>53</td>
</tr>
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<td>27</td>
<td>27</td>
<td>15.8</td>
<td>12.8</td>
<td>43</td>
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<td>33</td>
<td>19.3</td>
<td>15.6</td>
<td>35</td>
</tr>
</tbody>
</table>

Fixed constants:

Varactor exponent $N = 0.47$

Min tracking voltage = 4

Package capacitance = 0.2 pf

Max tank frequency = 288 MHz

Max tracking voltage = 14

Min tank frequency = 260 MHz

Table 1. Summary of Computer Survey of VCO Components
Having selected the circuit constants, the primary item of interest is the VCO transfer function. The nonlinear transfer function of the varactor yields a frequency output which has a changing relationship with respect to the control voltage. By differentiating the output frequency with respect to the control voltage we can find the VCO transfer function \( K_v \) at any point in the band of interest.

\[
K_v = \frac{f_1 - f_l}{V_l - \Delta V}
\]

For \( N' = 168 \), \( K_v = 5 \text{ MHz/v} = 31.5 \text{ MR/s} \)

For \( N' = 604 \), \( K_v = 2.5 \text{ MHz/v} = 15.7 \text{ Mr/s} \)

These transfer functions represent the VCO gain constant at the bottom end (\( N' = 168 \)) and top end (\( N' = 604 \)) of the band and will be useful when the loop characteristics are determined.

When channeling from the high end of the band to the low end, the control voltage will tend to overshoot the stable value as will be discussed in the section on loop characteristics. The voltage which biases the varicap will then fall to a value lower than the four volts which is required to establish lock at 260.250 MHz. In this range of reverse bias, the varactor capacitance is changing in value very rapidly and the possibility exists that the VCO frequency will go below the offset oscillator frequency of 249.75 MHz and form an erroneous product which will drive the system out of lock. To eliminate this possibility, a voltage clamp will be incorporated in the tracking line which will prevent any excursion capable of producing this effect.
2.2 PROGRAMMABLE DIVIDER

The purpose of the programmable divider is to provide an output frequency which is related to the input frequency by a fixed division ratio which may be selected by applying suitable inputs to a system of digital counters. There are many such devices available on the market with the selection of the 74190 based on purely economic considerations. The general outline of this device and an explanation of the various functions is presented in Figure 8.

In operation a pulse train is applied to the clock input. If at some point in time the "Load" input is brought low, the counter will assume the states of the data which is present on lines A, B, C and D. If the load signal is removed (brought high), the next positive edge of the clock pulse will decrement the counter until BCD zero (0000) is reached. At this point the "Max/Min" output goes high. As the clock goes low the ripple carry output will fall. The next positive clock transition resets the counters to BCD nine (1001), clears the ripple carry to high, and enters the normal down counting sequence of dividing by ten. This device is capable of being preset to any initial count from zero to nine by applying an initial count in BCD to the proper input lines.

---

Programmable Divider Chip Operations

Enable
"High" inhibits counting, disables R/C

Clock
Device triggers on low to high transition

D/U
"Down/Up" ("High" utilizes device as a down counter)

Max/Min
When BCD word in counters is zero (0000), this output goes "high" for full clock period.

A,B,C,D
Data inputs with "A" the least significant bit

Load
When held "low" data on A,B,C,D lines is jam loaded onto Qa, Qb, Qc, Qd independent of clock state.

Qa,Qb,Qc,Qd
Outputs of the four internal counters with Qa the least significant bit.

R/C
"Ripple carry". When Max/Min line goes high this output goes low for the width of the low portion of the clock pulse.

Figure 8. 74190 Programmable Divider Integrated Circuit
Two or more counters may be cascaded to give higher division ratios. Figure 9 illustrates the technique used when dividing by the integer 146.

![Diagram of cascade configuration for division by fixed integer]

**Figure 9. Cascade Configuration for Division by Fixed Integer**

This example is used to provide one low to high transition on output for every 146 low to high transitions on the input following a load pulse. After the load pulse disappears, the BCD words 6 (0110), 4 (0010), and 1 (1000) are present in the counters. The first positive transition of the clock pulse decrements counter #1 to five (1010). The sixth positive transition decrements counter #1 into the zero state. The negative transition of the sixth clock pulse forces the ripple carry low. The next positive clock transition clocks counter #1 to nine (1001) and raises the ripple carry to a high level, clocking counter #2 from 4 to 3. The seventeenth clock pulse
decrements counter \#2 from 3 to 2. The forty seventh clock pulse will decrement counter \#3 to zero and ninety-nine clock pulses later all counters are in the zero state. If the existence of this zero state is used as the output, 146 input pulses are required to produce an output state. If this output state is used to activate the load enable, the circuit will continuously divide the input pulse train by the BCD word present on the data terminals.

Since the highest division ratio required by the system shown in Figure 9 is less than 1999, a single flip-flop with appropriate gating for the load enable is used for counter \#3.

A divider of this type is limited by the maximum rate that the device can be made to load without missing a clock pulse. There is a delay in the Max/Min element which senses an all zero count, or terminal state, and a required time that the load enable must be low to ensure that all counters are fully loaded. By adding the delay times involved on a worst case basis (see Table 2), the maximum divide frequency can be obtained. Figure 10 illustrates a typical divider in which the terminal state is used to directly provide the loading pulse.

The procedure used in Table 2 is based on the typical and worst case specifications of the 74190 as can be obtained from the data sheet supplied by the manufacturer. The minimum time required between clock transitions relates to a typical maximum clock frequency of 14 MHz and a worst case clock
frequency of 8.1 MHz. Clearly an approach must be developed which will allow the divider to be used at the frequency required by the system in Figure 5 and allow adequate margin for any overshoot requirements.

![Diagram](https://via.placeholder.com/150)

**Figure 10. Worst Case Analysis of Direct Loading**

Thus far the design has centered on loading the counters between two adjacent clock pulses. In Figure 11 an approach is illustrated which is not subject to this limitation.

In this embodiment the terminal count clock pulse sets up the Max/Min count putting a low on the "D" input of

---

Parameter | Delay from last pulse to counter #1 Max/Min high | 25
| Delay in gate "G" (7410 used as typical example) | Typical 28 | Max 42
| Setup time required for load pulse (BCD - 7) | Typical 14 | Max 22
| Delay in gate "G" to release of load pulse | Typical 11 | Max 22
| Delay from release of load pulse to normal clock | Typical 11 | Max 22

Minimum time required between clock transitions | 71 ns 123 ns

Table 2. Worst Case Analysis of Direct Loading

a flip-flop via gate "G". The next clock pulse clocks the "Q" output of flip-flop #1 low, causing the load state. As the counters load, the Max/Min condition disappears on the counters and gate "G" output goes high. The next clock pulse will reset the "Q" output of FF #1 into a high state, disabling the load condition. Subsequent clock pulses will resume the normal system countdown operation. Note that FF1 is unaffected by clock pulses occurring at any time except when gate "G" has gone low (terminal count) due to the normal "D" action of the device. The timing diagram of this action is shown in Figure 12 and the worst case analysis is presented in Table 3.

Figure 12 illustrates the sequence of the various delays inherent in the system. The rising edge of the clock pulse causing the counters to reach the terminal state is Pl. The positive edge which clocks the control flip-flop into the load state is P2. Pulse P3 releases the control flip-flop from
Figure 11. Frequency Extender Technique for Programmable Divider

the load state and normal countdown operation continues with
the data words just loaded into the counters being decremented
by each clock pulse to another terminal state.

The limiting delay between P3 and P4 is the delay in
FF1 and the release of load information. This delay is
negligible when compared to the P2 - P3 delays and will be
disregarded.

A comparison of the delays from Table 3 shows that
the critical timing occurs between P2 and P3 which leads to
limiting clock frequencies of 16.6 MHz typical and 9.6 MHz
worst case. This will be adequate for operation in the system as a total worst case configuration is not likely. If a Shottky gate and a Shottky flip-flop were used delay "D" would be reduced to 7 ns, delay "F" would fall to 5 ns, and delay "G" would drop to 5 ns resulting in a worst case clock frequency of 25 MHz. However, the interval between P1 and P2 would become the limiting factor and would limit the maximum frequency to approximately 20 MHz which is certainly adequate for performance in this system. Since Shottky devices are interchangeable with conventional TTL devices they may easily be substituted if production quantities lead to a problem in timing.

Figure 12. Timing Diagram of Frequency Extender Operation
### Table 3. Worst Case Analysis With Frequency Extension

The final version of the variable divider is shown in Figure 13 with the additional circuitry which is required to provide for the loading operation. When channel 100 (divide by 100) is loaded into the programmable dividers, a problem occurs in the loading sequence. The occurrence of P2 enables the load state causing all zeroes to be loaded into the first two counters (74190) and a high to be loaded into the last counter, a single 7474 type "D" flip-flop. When P2 falls since the first two counters are still in the Max/Min condition, a negative transition occurs on the R/C line into the third counter.
When P3 occurs, going positive, two phenomena are taking place:

1. FF1 begins to remove the load state from the system.

2. The R/C is propagating through counters one and two and, after a certain delay, will cause a low to high transition at the input of counter three.

Figure 13. Final Version of Programmable Divider
If the 7474 load control clocks out of load before the R/C pulse arrives, the result is that FF1 is clocked from a high to a low by the pulse which was supposed to remove the load state. The solution is incorporated into Figure 13 and consists of disabling the R/C function during loading by utilizing the "Enable" function of the 74190.

Note that a system wired in this manner will always divide by two greater than the number which is loaded as data as the two additional clock pulses are used to enable and disable the load state. This presents no handicap in this system, however, as the count has been selected to range from 42 to 151 in the variable divider.
2.3 PHASE DETECTOR

It is desirable to develop a phase comparator which will perform the dual functions of providing a linear output as a function of the phase differences of two independent pulse trains when they are synchronous in frequency and providing a constant output whose polarity is determined by the higher frequency. In this manner, a frequency difference which exists upon channel change will cause the low pass filter to slew the VCO to the proper frequency where phase comparisons can be made. The transfer characteristics of an ideal phase – frequency comparator are presented in Figure 14.

![Figure 14. Idealized Frequency - Phase Comparator Response](image)

In order to accomplish this design, one must first examine what occurs in two pulse trains of different rates (frequency).
a) If $F_1$ is greater than $F_2$, at some point there will be two or more occurrences of a reference transition of $F_1$ which occurs in time between two reference transitions of $F_2$.

b) If $F_1$ is greater than $F_2$, at no time will two reference transitions of $F_2$ occur between two transitions of $F_1$.

These two basic ideas are illustrated in Figure 15 for pulse trains of different repetition rates (frequencies).

Figure 15. Pulse Rate Comparison
The problem of frequency comparison then reduces to the design of a network that requires two consecutive pulses on one of the inputs in order to change the output state from one state, \( F_1 \) greater than \( F_2 \), to the other state \( F_2 \) greater than \( F_1 \). The detection of these states can be used to determine the direction in which the voltage controlling the VCO must travel in order to arrive at the desired frequency.

For instance, if two consecutive pulses occur on the \( F_1 \) input (referenced to some transition point), the output is in STATE 1. This state tells the control voltage which way to go. If then two consecutive pulses occur on the \( F_2 \) input (caused by the VCO overshothing the proper frequency), the output switches to STATE 2 which forces the control voltage in the opposite direction.

This type of circuit can be implemented by inspection by using shift registers or flip-flop designs. One such design is presented in Figure 16 using two "D" positive edge triggered flip-flops and a Nand gate. The action map for the operation of Figure 16 is presented in Figure 17.

From the start-up condition \((A\text{-low}, B\text{-low}, Q_a\text{-low}, Q_b\text{-low})\) the sequence of operation can be determined. After \( A \) is set, two consecutive pulses are required at \( B \) to switch the STATE 2 line high. Then two consecutive pulses are required at \( A \) to switch the STATE 1 line high. Where alternating pulses appear after two consecutive pulses on either line, either the STATE 1 or the STATE 2 line will be high for the length of time between the
Flip-flops are leading edge triggered type "D"

Figure 16. Frequency/Phase Comparison Circuit

Figure 17. Action Map for Freq/Phase Comparator
positive edges of the input pulses. Furthermore, the output line which is pulsed high will be the same line which had the consecutive pulses prior to the alternating pulses.

For clarification, if at any time the A line is high in frequency (compared to the B line), at some point there will be two consecutive pulses on it. The first pulse will reset both A and B and the second pulse will set A (STATE 1). States of the output have been selected so that STATE 1 will begin to lower the frequency of A. If the next pulse arrives from B, both devices are reset. The next pulse arriving from A puts the STATE 1 line high again. B again resets the devices. STATE 1 continually acts to pump the frequency of A down. As the frequency approaches that of B, STATE 1 is pulsed high for shorter and shorter periods of time, ceasing to exist at all when the positive edges of the signal are locked. If the phases should drift out of synchronism, either STATE 1 or STATE 2 will pulse depending on which direction A must go to correct for the drift.

It appears then that this circuit may also be used to perform the phase comparison process, remaining in either STATE 1 or STATE 2 for the time interval between positive edges. The circuit then satisfies the criteria for an idealized frequency-phase detector set forth previously in Figure 14.

It is necessary to look at all possible states of the circuit in order to verify that the above analysis is correct.
and no states can be assumed which cannot be clocked back to a desireable loop. A complete state transition diagram is presented in Figure 18. Note that twelve of the sixteen possible states exist within the figure. The remaining states which are not accounted for are listed in Table 4.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>A  B</td>
<td>Q_a Q_b</td>
<td></td>
</tr>
<tr>
<td>0  0</td>
<td>1  1</td>
<td>Reset</td>
</tr>
<tr>
<td>0  1</td>
<td>1  1</td>
<td>Reset</td>
</tr>
<tr>
<td>1  0</td>
<td>1  1</td>
<td>Reset</td>
</tr>
<tr>
<td>1  1</td>
<td>1  1</td>
<td>Reset</td>
</tr>
</tbody>
</table>

Table 4. Unstable States of Phase Detector

However, at any time when Q_a and Q_b are both high, an unstable condition occurs which immediately rests both flip-flops. These reset conditions are illustrated on the transition diagram by the lines marked "R".

In order to apply this design to the system, B will be designated as the reference frequency input (62.5 kHz) and A will be the signal from the VCO - variable divider channel which is to be controlled. When A is greater than B, the VCO frequency is too high. STATE 1 will be assigned to reducing the VCO frequency by the label "Pump Down". When A is less than B and STATE 2 is high, the STATE 2 line will be used to "Pump Up" the VCO frequency.
Figure 18. State Transition Diagram for Figure 16
By combining the STATE 1 and STATE 2 outputs with a summing operation in the low pass filter, the desired correction voltage can be obtained.

In Figure 19, when the STATE 2 line is high, current flows through D1 into R1 forcing the control voltage output to fall. When the STATE 2 line is low, diode D1 is reverse biased and the output voltage remains at its last level (minus offset currents and leakage which will be dealt with later).

![Figure 19. Low Pass Filter Pumping Operation](image-url)
When the STATE 1 line is high, the inverter pulls current from R1 through D2, forcing the control voltage to rise. Similarly, when STATE 1 is low and the inverter output is high, diode D2 is reverse biased and the control voltage remains stable. The inverter is not necessary if the Q_a' output is used for STATE 1.

If the varactor in the VCO is biased so that an increase in control causes a decrease in reverse voltage, the frequency of the VCO is decreased. Hence STATE 2 can reduce the control voltage, increase the reverse bias, and raise the VCO frequency. Conversely STATE 1 will reduce the VCO frequency.

When the pulse rates are synchronous in frequency the action of the pump lines is to achieve a condition where the low to high transitions of the A and B lines will be locked together. When this occurs, the control voltage will remain at a stable level. If an error in phase should develop, one of the pump lines will pulse for a length of time related linearly to the error and the voltage on the control line will be adjusted accordingly.

Both TTL and CMOS devices are available from various sources which can replace the "D" flip-flops, the isolation diodes, and the inverter section. As the input signals provided by the variable modulus divider and the reference divider are all of the TTL variety, the Motorola MC4044 is selected as the frequency-phase comparator. This chip also contains a charge pump which compensates for the inability of a TTL
digital circuit to source as much current as it will sink, maintaining a balanced charging rate to the low pass filter during either pump up or pump down operation.\footnote{Phase-Locked Loop Systems, (Phoenix, Arizona: Motorola Semiconductor Products, Inc., 1973) p. 21.}

The state transition table in simplified form is supplied by the manufacturer and examination reveals that the internal operation is identical with that of our derived example. The specification sheet guarantees the operation to 8 MHz which is far more than adequate for the requirement of 62.5 kHz.

However, the cost of the item is approximately eight times the cost of the dual D flip-flop and single Nand gate arrangement. This factor will be disregarded in favor of the reduction in layout area required on the printed circuit board.
2.4 LOOP CHARACTERISTICS

At this point the closed loop performance of the system will be examined. This analysis will be accomplished by constructing a mathematical model of the loop under linear, locked conditions and solving for the response to specified inputs.

In Appendix C, the following functions were obtained to describe the closed system of Figure 20.

Examining the error function, it is noted that as time grows large, the system phase error, after a stimulus, approaches zero (final value theorem). The definition of a completely locked system may then be taken to be when the system has zero phase error:

**System Transfer Function:**

\[
\frac{O_o(S)}{O_i(S)} = \frac{2DW_n S + W_n^2}{S^2 + 2DW_n S + W_n^2}
\]

**System Error Function:**

\[
\frac{O_e(S)}{O_i(S)} = \frac{S^2}{S^2 + (2DW_n)S + W_n^2}
\]

Figure 20. Close Loop System with Defining Equations
There are two primary disturbances which must be anticipated in a solution for the performance of a locked system:

\[ o_1(s) = \frac{\Delta \theta}{s} \quad \text{A step in input phase as would normally be encountered when switching one channel increment.} \]

\[ o_1(s) = \frac{\Delta \omega}{s^2} \quad \text{A step in frequency also occurring during channel change.} \]

\[ o_1(s) \text{ in the system error function may be used as the input transient and the system error response calculated using the inverse Laplace of the result. For example, letting } D = 1 \text{ with a phase step } \frac{\theta}{s}, \]

\[ o_e(s) = \frac{o(s)}{s} \quad \frac{s^2}{s^2 + (2D \omega_n) s + \omega_n^2} = \frac{\Delta \theta}{(s + \omega_n)} - \frac{\Delta \omega \omega_n}{(s + \omega_n)^2} \]

Which yields (inverse Laplace): \[ o_e(t) = \Delta \theta (1 - \omega_n t) \exp^{-\omega_n t} \]

By evaluating in this manner with \( D \) taking on various values, a table can be constructed for the system error response to the selected input disturbances. 6

These functions, together with the loop phase error response versus frequency, are plotted on a computer to yield the graphs 7 in Figures 21, 22, and 23.


It is apparent from Figure 23 that if the phase error is changing in time at a frequency greater than $W_n$, there will be no correction voltage generated. This implies that in a channel change where the $W$ presented to the phase detector is above some limit, the loop will lose lock and the system will no longer be defined by our linearized model. Examining the frequencies encountered in single channel changes, it is found that with the loop initially locked on channel $N$, and the channel is changed instantaneously to $N + 1$ (actually $N + 4$ due to $+$ prescaler).

**Phase Step Error Response**

\[
\begin{align*}
D < 1 & \quad \Delta \varphi (\cos \sqrt{1-D^2} \frac{W_n t}{n} - \frac{D}{\sqrt{1-D^2}} \sin \sqrt{1-D^2} \frac{W_n t}{n}) e^{-W_n D t} \\
D = 1 & \quad \Delta \varphi (1 - W_n t) e^{-W_n t} \\
D > 1 & \quad \Delta \varphi (\cosh \sqrt{D^2 - 1} \frac{W_n t}{n} - D \sinh \sqrt{D^2 - 1} \frac{W_n t}{n}) e^{-W_n D t}
\end{align*}
\]

**Error Response to Frequency Step**

\[
\begin{align*}
D < 1 & \quad \frac{\Delta W}{W_n} \frac{1}{\sqrt{1-D^2}} \sin \sqrt{1-D^2} \frac{W_n t}{n} e^{-D W_n t} \\
D = 1 & \quad \frac{\Delta W}{W_n} W_n t e^{-W_n t} \\
D > 1 & \quad \frac{\Delta W}{\Delta n} \frac{1}{\sqrt{D^2 - 1}} \sinh \sqrt{D^2 - 1} \frac{W_n t}{n} e^{-D W_n t}
\end{align*}
\]

Table 5. Loop Error Response for Step Inputs
Figure 21. Error Due to Phase Step
Figure 22. Error Due to Frequency Step
Figure 23. Error Response of High Gain Loop
Therefore, one criteria for fast channel change is to select an $W_n$ for the loop which is greater than the maximum $\Delta W$ (9135 r/s) encountered with a single channel change. This selection ensures that the loop will never completely unlock as the channel is changed in single steps. However, a transient condition will exist as the loop servos the $W_{n+1}$ back to 62.5 kHz, the fully locked state. From Figures 21 and 22 it is shown that for a wide range of damping factors (D), the loop transient will almost completely die out in about six $W_n t$ units. If an $W_n$ of 9135 r/s is specified for the loop, the lock time expected would be on the order of:

$$W_n t = 6 \quad t = \frac{6}{9135} = .7 \text{ milliseconds}$$

If single channel steps were all that were to occur, the design for $W_n$ has been established. However, the lock time requirement must also be met when channeling from $N' = 168$ to $N' = 604$. Proceeding as before, the relationship is tabulated in Table 7.
It is apparent that the phase error from the phase detector is changing in time at a rate much greater than the reference frequency. For any reasonable value of $W_n$, therefore, our loop will always lose lock when large channel increments are presented to the system. As the foregoing analysis holds only for a system which remains in lock (linear), the nonlinear operation of the system must be used to determine the value for $W_n$. If a value can be found which will achieve lock-up in 50 ms for large channel separations, the incremental channel separations will of course be met.

The procedure for selecting the loop constants under nonlinear operation will be implemented by developing a scheme for using the frequency information from our phase detector to slew the VCO to the vicinity of the proper frequency. As the frequency approaches the desired rate, the phase error from the detector will be changing at some value which will lie within the bandwidth of the loop filter. From the foregoing analysis it is apparent that lock-up then will proceed rapidly, on the order of milliseconds.

<table>
<thead>
<tr>
<th>$N'$</th>
<th>$N'+436$</th>
<th>$F_n$ (Locked)</th>
<th>$F_{n+1}$ (Transient)</th>
<th>$\Delta F$</th>
<th>$\Delta W$</th>
</tr>
</thead>
<tbody>
<tr>
<td>168</td>
<td>604</td>
<td>62.5 kHz</td>
<td>17.384 kHz</td>
<td>54.116 kHz</td>
<td>$2.8 \times 10^5$ r/s</td>
</tr>
<tr>
<td>604</td>
<td>168</td>
<td>62.5 kHz</td>
<td>224.702 kHz</td>
<td>162.202 kHz</td>
<td>$10^6$ r/s</td>
</tr>
</tbody>
</table>

Table 7. Frequency Relationship for Band Edge Channel Change
Figure 24 illustrates the equivalent circuit of the phase detector, loop filter, and control voltage for an unlocked condition.

In order to slew the control voltage from one end of the band to the other, there must be a change of ten volts on the output. This stems from the VCO design which specified a tracking voltage range of ten volts. With a substantial frequency error into the phase detector a constant output of 2.25 volts will be provided to pump the low pass filter. As the non-inverting input to the amplifier is biased at 1.5 volts, there will be a potential of .75 volts tending to lower the control line. An analysis for the component values necessary to allow the .75 pump potential to lower the output 10 volts is easily arrived by using the Laplace technique.
\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{sC \cdot R2 + 1}{sC \cdot R1} = \frac{R2}{R1} \cdot \frac{1}{sC \cdot R1}
\]

(transient)  
(slew rate)

Taking the inverse Laplace of the slew rate,

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{T}{R1 \cdot C} \cdot \frac{10}{.75} = \frac{.05}{R1 \cdot C} \quad R1 \cdot C = 3.8 \times 10^{-3}
\]

Selecting a value for \( \frac{C}{10} \) based on economics and availability,

\( R1 = 3.6 \text{ K-ohms} \quad \text{(standard value)} \)

Referring to the equation for the loop frequency \( W_n \) and the damping factor, it is found that both quantities are dependent on VCO sensitivity and channel count \( N' \). The values for \( W_n \) at each end of the band are easily determined.

\[
K_d = .12 \text{ volts/rad} \quad R1 = 3.6k \quad C = 1.0 \text{ uf} \quad W_n^2 = \frac{K_v \cdot K_d}{N \cdot C \cdot R1}
\]

Channel \( N' \) (total)  

<table>
<thead>
<tr>
<th>( N' ) (total)</th>
<th>( K_v(VCO) )</th>
<th>( K_d )</th>
<th>( W_n^2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>168</td>
<td>31.5 mr/s</td>
<td>.12</td>
<td>2496 rad/sec</td>
</tr>
<tr>
<td>604</td>
<td>15.7 mr/s</td>
<td>.12</td>
<td>931 rad/sec</td>
</tr>
</tbody>
</table>

Table 8. Calculated Loop Parameters

Since \( D = \frac{W_n \cdot R2 \cdot C}{2} \), it is desirable to select a damping factor which will compromise the settling times at both extremes of \( N \).

Setting \( D_{\text{min}} = .5 \) which will occur at \( W_n \) min,

\[
R2 = \frac{(.5) \cdot (2)}{(10^{-6})(931)} = 1.1 \text{ K-ohms} \quad \text{(standard value)}
\]
With this value specified the damping factor $D$ will be .5 for $N' = 604$ and 1.35 for $N' = 168$, a spread which will give minimum overall settling times. The open loop performance when channeling from one end of the band to the other may now be summarized in Table 9.

<table>
<thead>
<tr>
<th>Initial Channel</th>
<th>± Next Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>168</td>
<td>604</td>
</tr>
<tr>
<td>604</td>
<td>168</td>
</tr>
</tbody>
</table>

Table 9. Summary of Loop Parameters

Assuming an initially locked system at the "initial channel", if the programmed divider is instantaneously changed to a count which represents the opposite end of the band, there will be a large frequency error presented to the input of the phase-frequency detector. The detector will respond to this frequency difference by providing an essentially constant "pump" to the low pass filter. The control voltage will then slew the VCO to the proper frequency at a rate determined by $R_1$ and $C$. When the output frequency of the VCO approaches the vicinity of the channel frequency, the frequency difference presented to the phase detector will fall within the capture range of the loop (in the vicinity of $W_n$) and phase lock will be rapidly acquired.
Comparing the $W_n$ at the extremes of the band to the $W_{error}$ existing for the single channel step case, it is apparent that lock may be lost momentarily even for single channel increments. However, this presents no problem as the time required to re-lock from such a small frequency separation is very low.

The value which was derived for $W_n$ is actually the minimum value which can be used if the lock time requirement is to be met. Obviously if a shorter lock time were required, $W_n$ could be increased. The tradeoff in this case would be the amount of filtering at the reference frequency provided by the loop. In order to keep the 62.5 kHz components generated by the phase detector from reaching the phase detector, $W_n$ should be as low as possible. The criteria for suppression of spectrum-widening modulation will be covered in the analysis of spurious outputs.
2.5 **SPURIOUS OUTPUTS**

One of the principle criteria for circuit operation was the requirement that spurious outputs—frequencies other than the primary carrier—can be reduced to 60 dB or more below the primary carrier level. These spurious outputs are caused by some external voltage reaching the VCO and modulating the frequency. This external voltage can be produced from several sources.

1) Ground currents causing a difference of potential along circuit paths that can create an effective time varying phase shift within the loop components.

2) Supply voltage lines which normally will be impressed with substantial TTL impulses from the logic.

3) Radiation into circuit components from devices which have a high RF field (transmitter, modulator).

4) Imperfections in the phase detector which will permit frequencies to enter the filter and VCO causing direct modulation on the control line.

Of the above, 1) and 3) can rarely be predicted and a mechanical layout with the shielding configuration based on experience with past designs must be relied upon. This is typically the greatest difficulty as there is no method to reliably predict what the effect of a particular method will be.
The supply voltage to the VCO, buffers, and loop filter should be supplied by an on-card regulator and maintained completely separated from busses which provide power to the digital functions.

The phase detector imperfections have a predictable effect and provide a means of determining the maximum performance which could be achieved if all mechanical and supply conditions were perfect. In the loop design, this effect is calculable and can have a great effect on the design chosen. The following analysis is presented to determine the sideband levels present in the design at this point and to determine if any modifications are required.

In the following analysis, the level of the first sideband will be assumed to be the worst case expected and the object shall be to reduce this value. Higher ordered sidebands could be investigated using the same techniques developed here.

\[
\text{Sideband level (1st)} = \frac{\text{Max. freq. deviation of VCO}}{\text{Carrier Level}} (\text{approx}) \times 2 \times (\text{modulating frequency})
\]

A frequency existing at the output of the phase detector and the effect on the loop output can be modeled as in Figure 25.

In this model, \( V_{\text{dist}} (W) \) is taken to be the pulse train from the phase detector occurring at \( W_{\text{ref}} \) rad/sec which is the resulting in a peak value \( V_{\text{pd}} (W) \).
Figure 25. Loop Model for Spurious Analysis

It can easily be shown that:

\[
\frac{\text{Sideband level}}{\text{Carrier level}} = \frac{V_{pd} W_n N D}{k_d} \frac{1}{\left(\frac{W_{ref}}{k_d}\right)^2 + \left(2 \frac{W_n ND}{k_d}\right)^2}^{1/2} \frac{1}{N'}
\]

For the system of interest, the right hand side can be reduced considerably.

Note that the variables \( W_n \) and \( D \) can be used to diminish the spurious level. However, the design has already specified the minimum level of \( W_n \) in anticipation of this restraint. Also,
any additional lowering of D severely degrades the damping characteristics. At this point an analysis must be made to determine the levels of $V_{pd}$ which will be encountered.

In Appendix 1C, it is shown that for a pulse relationship as is encountered in the output of the phase detector (Figure 26) the applicable relationships between the pulse width and the peak value of the fundamental may be determined by the Fourier series and simplified by assuming a small pulse width.

The average voltage is that voltage which the phase detector must supply to offset the leakage currents which are present in the summing junction of the low pass filter (Figure 27).

![Finite Pulse from Phase Comparator](image_url)

Figure 26. Finite Pulse from Phase Comparator
From the manufacturer's data sheet:

<table>
<thead>
<tr>
<th>Component</th>
<th>Il (Max)</th>
<th>Il (Typ)</th>
<th>Ib (Max)</th>
<th>Ib (Typ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC4044</td>
<td>5 ua</td>
<td>.1 ua</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM308</td>
<td>7 na</td>
<td>1.5 na</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For the circuit in Figure 30,

\[
V_{\text{average}} = (I_l + I_b) R_1 = 18 \text{ mV (max)} \quad \text{and} \quad .4 \text{ mV (typ)}
\]

This average voltage is generated by a finite pulse from the phase detector which results in a static phase error. This finite pulse has a frequency component existing at the reference frequency.

\[
V_{\text{peak ref.}} = 2 V_{\text{ave}} = 36 \text{ mV (max)} \quad \text{and} \quad .8 \text{ mV (typ)}
\]

With no additional filtering, the peak voltage results in a set of FM sidebands on the primary carrier.

\[
\frac{\text{Sideband level}}{\text{Carrier level}} (\text{dB}) = 20 \log_{10} \frac{V_{\text{peak}}}{{\text{Ref}}} = \frac{\text{V}_{\text{peak}}}{\text{Kd}} \frac{\text{W}}{\text{Ref}}
\]

- \(N = 168\)
- \(N = 604\)

<table>
<thead>
<tr>
<th></th>
<th>Max S/C (dB)</th>
<th>Typ S/C (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-7.2 dB</td>
<td>-40. dB</td>
</tr>
<tr>
<td></td>
<td>-13.3 dB</td>
<td>-46. dB</td>
</tr>
</tbody>
</table>

In view of these levels of suppression, there are two methods available for preserving the use of the MC4044 in the system.

1) The MC4044 must be selected to a leakage specification.
2) Additional filtering must be provided.
If additional filtering is used, the break frequency must be far removed from the loop corner frequency in order to prevent modification of the loop characteristics. The effect may be seen by a Bode plot analysis of the transfer function and with a determination of the gain-phase margin. A good rule of thumb, however, is to place the corner of the added filter at a minimum of about \( 5 \frac{\text{W}}{\text{n}} \) of the loop. If a single pole low pass filter were placed at about 2 kHz, this would provide additional suppression of the reference component of:

\[
\text{Additional Supp.} = n \, 20 \log \left( \frac{W_c}{W_{\text{ref}}} \right) = 30 \, \text{dB}
\]

This low pass filter is shown implemented into the input of the loop filter in Figure 28.

---

Motorola, Phase Locked Loop Systems, p. 29.
With this modification to the loop filter and the selection of the phase comparator to a leakage current specification, typical suppression will be greater than 70 dB.

Figure 28. Low Pass Network in Loop Filter
The following sections of the frequency synthesizer are not covered in the preceding sections on design as they represent a variety of disciplines which are not necessarily basic to the synthesizer design. For the sake of completeness however, a brief description of these circuits will be included here.

A) Offset Oscillator

The offset oscillator configuration chosen is a crystal controlled Colpitts oscillator using a fifth overtone crystal at 83.250 MHz. Bias values are selected to limit the amplitude of the oscillations by the available current providing a more predictable tuning response by maintaining the transistor out of saturation during all portions of the RF cycle.

b) Tripler

A PNP transistor is used as a tripler to raise the oscillator frequency of 83.250 MHz to the required frequency of 249.750 MHz. A double tuned circuit assures the suppression of other products which could otherwise reach the mixer.

C) Mixer

A double balanced mixer is employed which provides greater than 30 dB port to port isolation, preventing the offset oscillator frequency from reaching the VCO.
buffers and appearing on the desired output channel as an unwanted spurious output. The mixer intermediate frequency is fed into a 50 ohm low pass filter to allow only the desired difference frequency (10 - 39 MHz) to reach the logic sections.

D) Wideband Amplifier and Divide by Four

A cascaded triple line receiver (ECL) is biased with the first two sections in the linear mode. This approach enables full ECL logic level swings on the output with approximately 5 millivolts of input from the mixer. The last receiver section provides an input to an ECL divide by four which prescales the input frequency to the 2.5 to 10 MHz range required by the programmable divider.

E) ECL - TTL Converter

A base driven transistor circuit which is DC biased at the nominal TTL transition level is used to raise the ECL level logic swing to acceptable TTL levels. A Nand gate also biased at the transition point is used to buffer the output and provide drive capability for the various loads involved.

F) Reference Oscillator and Divider Chain

A crystal controlled Pierce oscillator operating in the fundamental mode at 4 MHz is used to drive a field effect device which is capable of clocking a TTL divide
by four ripple counter. The 1.0 MHz output is used to clock a divide by sixteen ripple counter which is decoded to provide a reference frequency output of 62.5 kHz. Another decoded output provides a comparison window for the lock detector.

G) VCO Buffers

Three common base amplifiers are cascaded to provide the required power gain and isolation in each of two channels. The first channel, which is used in the synthesizer loop, effectively isolates all mixer products from reaching the VCO. The second channel is used to provide the required bandwidth and power gain to drive the transmitter - multiplier chain.

H) Voltage Regulator

An integrated circuit voltage regulator is used to provide on-card regulation for the supply voltages of the VCO and buffers. Any undesirable noise on the +12 volt and the -12 volt lines is effectively eliminated on the +8 volt and the -8 volt lines.
Figure 29. Total System Schematic
SUMMARY

The frequency synthesizer designed in this report has been built and tested for all desired performance parameters from -45 degrees Centigrade to +55 degrees Centigrade. All specifications were met and the performance regarding lock times and spurious outputs were as predicted by the preceding derivations, allowing for component tolerance which created only minor and acceptable differences from calculated values.

Additionally, the synthesizer was installed into the total DME system mounted in an aircraft which was test flown to monitor performance. No deviation from expected results was created by the synthesizer operation and accurate measurements of the distance and speed information relative to a number of ground based stations were made confirming the system concept used in the design. Production of the system in quantity should begin in early 1976 and no synthesizer changes are anticipated.

In the course of the synthesizer development, two patent applications were disclosed to the Bendix Corporation in the name of the author. One disclosure was concerned with a method of detecting a locked loop in transient noise which is incorporated in the system. The second disclosure concerned and improved frequency-phase comparator which was a result of the research done on that portion of the system.
For small indices of modulation:

\[
\frac{J_1 (B)}{J_0 (B)} = \frac{B}{2} \quad \text{where } B = \text{index of modulation}
\]

\[
= \frac{\Delta f \text{ carrier (max)}}{\text{modulation freq.}}
\]

APPENDIX B - DERIVATION OF SIDEBAND TO CARRIER RATIO

\[ v_{\text{VCO}} = \text{Output phase of VCO} = 0_{\text{steady state}} + 0_{\text{disturbance}} \]

In this model the disturbance is occurring at \( f_{\text{ref}} \)

\[ v_{\text{VCO}} = v_{\text{ss}} + Od \sin (f_{\text{ref}} t) \]

\[ \frac{d}{dt} (v_{\text{VCO}}) = Od f_{\text{ref}} \cos (f_{\text{ref}} t) \]

Peak deviation = \( w_{pk} \) \( V\text{CO} = Od f_{\text{ref}} \)

From Figure 25,

\[ \frac{v_{\text{VCO}}}{v_{\text{dist}}} = \frac{F(s) K_v}{s + \left[ K_v K_d \frac{F(s)}{s N'} \right]} \]

Letting \( s = jw \)

\[ \frac{v_{\text{VCO}}}{v_{\text{dist}}} = F(s) K_v \left[ \frac{1}{w^2 + \left( \frac{K_v K_d F(s)}{N'} \right)^2} \right]^{1/2} \]

Solving for the response at the reference frequency:

\[ \frac{v_{\text{VCO}}}{v_{\text{dist}}} = F(f_{\text{ref}}) K_v \left[ \frac{1}{f_{\text{ref}}^2 + \left( \frac{K_v K_d F(f_{\text{ref}})}{N'} \right)^2} \right]^{1/2} \]

In this system, \( F(f_{\text{ref}}) = \frac{R_2}{R_1} \)

where \( R_2 = \frac{2 \cdot D}{W_n} \) \( C \)

\( R_1 = \frac{K_d K_v}{N' W_n^2} \)

\( \frac{R_2}{R_1} = \frac{2 N' W_n D}{K_d K_v} \)

Substituting:

\[ \frac{v_{\text{VCO}}}{v_{\text{dist}}} = \frac{N' W_n D}{K_d/2} \left[ \frac{1}{f_{\text{ref}}^2 + \left( \frac{2 W_n N D}{N'} \right)^2} \right]^{1/2} \]
The peak disturbance $O_d$ occurs when $V_{\text{dist}} = V_{pd}$ (peak)

$$O_{VCO} \text{ (peak)} = O_d = \frac{2 \frac{V_{pd} N' W_n D}{Kd}}{1 - \frac{2}{W_{\text{ref}} + (2 W_n D)^2}}^{1/2}$$

Since $W_{pk} = O_d \frac{W_{\text{ref}} 2 \frac{V_{pd} N' W_n D}{Kd}}{1 - \frac{2}{W_{\text{ref}} + (2 W_n D)^2}}^{1/2}$

Sideband level
Carrier level = $\frac{J_1 (B)}{J_0 (B)} = \frac{B}{2} = \frac{W_{pk}}{2 W_{\text{mod}}}$

$W_{\text{mod}} = W_{\text{reference}}$

Sideband level
Carrier level = $\frac{V_{pd} N' W_n D}{Kd} \left[ \frac{1}{W_{\text{ref}}^2 + (2 W_n D)^2} \right]^{1/2}$

For this system, $W_{\text{ref}}$ is much greater than $2 W_n D$.

Approximating,

Sideband
Carrier = $\frac{V_{pd} N' W_n D}{Kd W_{\text{ref}}}$

If $V_{\text{ref}}$ is the peak phase detector voltage on the control line,

$$V_{\text{ref}} = V_{pd} \frac{R_2}{R_1} = \left[ \frac{2 N' W_n D}{Kv Kd} \right] V_{pd}$$

Sideband
Carrier = $\frac{V_{\text{ref}} \frac{Kv}{2 W_{\text{ref}}}}{2 W_{\text{ref}}}$
APPENDIX C - DERIVATION OF AVERAGE VOLTAGE TO PEAK VOLTAGE
FOR SMALL PULSE

![Diagram of finite pulse](Image)

**Figure 30. Finite Pulse for Fourier Analysis**

The Fourier Series of the following pulse train is analyzed to arrive at a peak value of the frequency component of the repetition rate ($W_{ref}$).

\[
F(x) = \frac{A_0}{2} + \sum_{n=1}^{\infty} \left[ A_n \cos(\frac{2 \pi n x}{T}) + B_n \sin(\frac{2 \pi n x}{T}) \right]
\]

where

\[ A_n = \frac{2}{T} \int_{0}^{C} F(x) \cos(\frac{2 \pi n x}{T}) \, dx \]

\[ B_n = \frac{2}{T} \int_{0}^{C} F(x) \sin(\frac{2 \pi n x}{T}) \, dx \]

For $A_0$, $A_0 = \frac{2}{T} \int_{0}^{C} V \cos(0) \, dx = \frac{2}{T} \left[ \int_{0}^{C} xV \right] = \frac{2}{T} \left[ \frac{2}{C} \right]

Therefore, $V_{\text{average}} = \frac{A_0}{2} = \frac{cV}{T}$
For the fundamental, \( n=1 \)

\[
A_1 = \frac{2}{T} \int_0^C V \cos \left( \frac{2 \pi x}{T} \right) \, dx = \frac{V}{\pi} \sin \left( \frac{2 \pi c}{T} \right)
\]

\[
B_1 = \frac{2}{T} \int_0^C V \sin \left( \frac{2 \pi x}{T} \right) \, dx = \frac{V}{\pi} \left( 1 - \cos \left( \frac{2 \pi c}{T} \right) \right)
\]

The equation for the fundamental component therefore is:

\[
F(x) = \frac{V}{\pi} \sin \left( \frac{2 \pi c}{T} \right) \cos \left( \frac{2 \pi x}{T} \right) + \frac{V(1-\cos(2 \pi c/T))}{\pi} \sin \left( \frac{2 \pi x}{T} \right)
\]

If \( c \) is very much less than \( T \),

\[
\sin \left( \frac{2 \pi c}{T} \right) = (\text{approx.}) = \frac{2 \pi c}{T}
\]

\[
\cos \left( \frac{2 \pi c}{T} \right) = (\text{approx.}) = 1
\]

Substituting,

\[
F(x) = \left[ \left( \frac{V}{\pi} \frac{2 \pi c}{T} \right) \cos \left( \frac{2 \pi x}{T} \right) + 0 \right] = \frac{2 V c}{T} \text{ peak value}
\]

Comparing: \( V_{\text{peak}} = 2 V_{\text{average}} \) for very small \( c \).
APPENDIX D - LOOP DYNAMIC EQUATIONS

The derivation for the transfer functions for the various blocks of the digitally divided phase locked loop proceed as follows:

\[ G(s), \quad H(s) \]

Figure 31. General Phase Locked Loop

\[ G(s) \] -- VCO transfer function

\[ H(s) \] -- Transfer function of the feedback path from VCO output to phase detector input. In this model

\[ H(s) = \frac{1}{N'}, \] the division ratio of the divider.

From the servo theory, the following relationships are obtained:

\[ e(s), \quad VCO \] output signal

\[ o(s) \] -- Reference input signal
Expanding the model in Figure 31 to fit the basic model presented in Section 1.3 and using Laplace notation for the transfer functions of the various sections, Figure 32 is obtained.

![Digital Phase Locked Loop Diagram](image)

Figure 32. Digital Phase Locked Loop

The basic loop equations become:

\[
\frac{0_e(s)}{0_i(s)} = \frac{K_v \cdot K_d \cdot F(s)}{s + K_v \cdot K_d \cdot F(s)}
\]

\[
\frac{0_o(s)}{0_i(s)} = \frac{s}{N'}
\]

To determine the transfer function of the low pass filter, a configuration shall be employed using an operational amplifier. This configuration is presented in Figure 33. For a high gain
amplifier the transfer equation of the low pass filter becomes:

\[ F(s) = \frac{s C R2 + 1}{s C R1} \]

The loop transfer function then becomes:

\[
\frac{0_o(s)}{0_i(s)} = \frac{Kv Kd (s C R2 + 1)}{s^2 + Kd Kd (s C R2 + 1)} = \frac{Kv Kd (s C R2 + 1)}{s^2 C R1 + s(Kd Kd C R2) + Kd Kd \frac{N'}{N'}}
\]

Drawing on servo terminology, this has the form:\textsuperscript{10}

\[
H(s) = \frac{2 D W_n s + W_n^2}{s^2 + 2 D W_n s + W_n^2}
\]

Figure 33. Low Pass Filter

where \( W_n \) is the natural frequency of the loop and \( D \) is the damping factor.

\[ W_n^2 = \frac{Kd Kd}{N' C R1} \text{ and } D = \frac{R2 C W_n}{2} \]

\textsuperscript{10} Gardner, Phaselock Techniques, p. 9.
Note that here there are three components which can be independently selected to set both the natural frequency and damping factor.
BIBLIOGRAPHY


