The Design and Development of a Power Hybrid

Robert J. Albert

*University of Central Florida*

This Masters Thesis (Open Access) is brought to you for free and open access by STARS. It has been accepted for inclusion in Retrospective Theses and Dissertations by an authorized administrator of STARS. For more information, please contact STARS@ucf.edu.

**STARS Citation**


https://stars.library.ucf.edu/rtd/268
THE DESIGN AND DEVELOPMENT
OF A POWER HYBRID

BY

ROBERT J. ALBERT
B.S.E.E., University of New Haven, 1972

RESEARCH REPORT
Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Engineering
in the Graduate Studies Program of the
College of Engineering
of Florida Technological University

Orlando, Florida
1978
ABSTRACT

This report discusses the design, development and the fabrication of a power hybrid. Foldback current limiting which is self resetting is used whereby withstanding indefinitely a short circuit. Thermal design considerations and thermal analysis are described as well as stability analysis. The maximum current capability of this design is four amperes and forty watts can be dissipated in the power transistors over a wide range of temperatures.
TABLE OF CONTENTS

I. INTRODUCTION .............................................. 1

II. BACKGROUND .................................................. 2

III. DESIGN REQUIREMENTS ..................................... 6

   Hybrid Specifications .................................... 6
   Circuit Description ...................................... 8
   Hybrid Mechanization .................................. 13

IV. PERFORMANCE ANALYSIS .................................... 17

   Output Offset Analysis ................................... 18
   Amplifier Accuracy Analysis ............................ 20
   Output Current Capability ............................... 23
   Cold Temperature Limit .................................. 25
   Hot Temperature Limit ................................... 27
   Maximum Output Current Required .................... 30
   Power Dissipation ......................................... 33
   Expression for the Power Supply Voltage ............ 35
   Amplifier Power Dissipation Three Phase AC . . . 36
   Amplifier Power Dissipation Power Supply is 28VDC . . . 39
   Fault Conditions .......................................... 40
   AC Stability Analysis .................................... 42
   Thermal Analysis .......................................... 52

V. RESULTS AND EVALUATION ................................... 67

   Thermal Resistance Measurements .................... 67
   Gain Accuracy ............................................. 74
   Closed Loop Frequency Response ....................... 75

VI. CONCLUSIONS AND RECOMMENDATIONS ....................... 77

APPENDIX 1 ..................................................... 79
APPENDIX 2 ..................................................... 80
APPENDIX 3 ..................................................... 82
APPENDIX 4  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .  84
APPENDIX 5  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .  87
APPENDIX 6  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .  90
REFERENCES  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .  92
### LIST OF ILLUSTRATIONS

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Discrete version of the power amplifier</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>Hybrid version of the power amplifier</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>Unlidded power amplifier hybrid</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>Power amplifier schematic</td>
<td>9</td>
</tr>
<tr>
<td>5</td>
<td>Simplified flow chart of the hybrid manufacturing process</td>
<td>15</td>
</tr>
<tr>
<td>6</td>
<td>Equivalent representations of offset sources</td>
<td>18</td>
</tr>
<tr>
<td>7</td>
<td>Gain accuracy model</td>
<td>20</td>
</tr>
<tr>
<td>8</td>
<td>DC Output current model</td>
<td>24</td>
</tr>
<tr>
<td>9</td>
<td>Synchro torque receiver model</td>
<td>30</td>
</tr>
<tr>
<td>10</td>
<td>Full-wave power supply waveform</td>
<td>34</td>
</tr>
<tr>
<td>11</td>
<td>Current limiting waveform</td>
<td>40</td>
</tr>
<tr>
<td>12</td>
<td>Model used for the first stage analysis</td>
<td>42</td>
</tr>
<tr>
<td>13</td>
<td>AC open-loop model</td>
<td>43</td>
</tr>
<tr>
<td>14</td>
<td>Model used for the second stage analysis</td>
<td>45</td>
</tr>
<tr>
<td>15</td>
<td>Calculated open-loop response</td>
<td>50</td>
</tr>
<tr>
<td>16</td>
<td>Calculated closed-loop response</td>
<td>51</td>
</tr>
<tr>
<td>17</td>
<td>Cross-sectional model for a square heat source</td>
<td>54</td>
</tr>
<tr>
<td>18</td>
<td>Cross-sectional model for a rectangular heat source</td>
<td>54</td>
</tr>
<tr>
<td>19</td>
<td>Flow chart showing the different methods for the fabrication of the hybrid by Manufacturer 1</td>
<td>60</td>
</tr>
<tr>
<td>20</td>
<td>Thermal conduction model for Manufacturer 1</td>
<td>61</td>
</tr>
<tr>
<td>21</td>
<td>Flow chart showing the different methods for the fabrication of the hybrid by Manufacturer 2</td>
<td>64</td>
</tr>
<tr>
<td>22</td>
<td>Thermal conduction model for Manufacturer 2</td>
<td>65</td>
</tr>
<tr>
<td>23</td>
<td>Test set-up for measuring $\theta_{JA}$ (NPN)</td>
<td>68</td>
</tr>
<tr>
<td>24</td>
<td>Test set-up for measuring $\theta_{JA}$ (PNP)</td>
<td>68</td>
</tr>
<tr>
<td>25</td>
<td>Measured closed-loop response</td>
<td>76</td>
</tr>
<tr>
<td>26</td>
<td>Current limit waveform</td>
<td>85</td>
</tr>
</tbody>
</table>
LIST OF TABLES

1. Operating electrical specifications .......................... 7
2. Frequency response - computer printout ...................... 49
3. Thermal conductivity of materials ............................ 57
4. Eutectic solder properties .................................... 58
5. Hybrid test measurements ..................................... 70
6. Change in base-emitter voltage ............................... 71
I. INTRODUCTION

With hybrid microcircuit technology, both discrete and deposited thick-film elements are combined into a miniature circuit. The component parts are interconnected and sealed in a hermetic package resulting in a reliable circuit capable of withstanding adverse environmental conditions.

The small physical size of the hybrid contributes to system miniaturization. The hybrid also contributes to lower the total number of interconnections and reduces system costs and provides better system maintenance. The cost advantages over conventional circuit board packaging techniques are due principally to the lower piece-part cost of the components in the chip versus packaged form.

Further advantages of hybrid microcircuit miniaturization is in smaller and lighter equipment, lower system assembly and test cost, and ease of equipment maintenance.
II. BACKGROUND

The decision to hybridize the power amplifiers was primarily due to weighing the advantages and disadvantages of hybrid microcircuit packaging design and conventional component part packaging. It was important that the considerations be based on total system cost rather than only the cost of the hybrid circuit versus the discrete components. Some of the advantages of the hybrid are: smaller and lighter equipment, lower system assembly, test cost and maintenance.

In previous systems the discrete version of the power amplifiers when assembled required two printed circuit card positions due to the large heat sinks required. (See figure 1.) The hybrid version of the power amplifiers requires only one card position and also allows the mounting of a fourth power amplifier as shown in figure 2.

Figure 3 is an unlidded hybrid showing the internal construction and layout of the components. The power darlington transistors are mounted in each of the corners to ensure minimal heat transfer from one to another.
Fig. 1. Discrete version of the power amplifier
Fig. 2. Hybrid version of the power amplifier
III. DESIGN REQUIREMENTS

Hybrid Specifications

The specifications and function of the power amplifiers were detailed in an in-house document. The amplifiers are to provide buffering between the synchro loads and the D/A converters. Synchro signals are 11.8 Vrms line-to-line and are referenced to phase C of the three phase power supply. The phase shift shall not exceed ± 0.5°. The amplifiers shall not be damaged when operated with any load from open circuit, maximum load specified and a short circuit. Some waveform and accuracy degradation is acceptable while slewing through large angles. Full performance is required in the steady state condition. The operating electrical specifications for the hybrid are listed in Table 1.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain, Channel 1 (Pins 5 &amp; 8)</td>
<td>D.C., Load=1kΩ, 25°C</td>
<td>-1.674</td>
<td>-1.669</td>
<td>-1.663</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>400Hz Sine Wave, Load=26Ω/79°</td>
<td>-1.677</td>
<td>-1.669</td>
<td>-1.660</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>+25°C to +85°C</td>
<td>-1.683</td>
<td>-1.669</td>
<td>-1.655</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>+25°C to +85°C</td>
<td>-1.677</td>
<td>-1.669</td>
<td>-1.660</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>-55°C to +125°C</td>
<td>-1.683</td>
<td>-1.669</td>
<td>-1.655</td>
<td>V/V</td>
</tr>
<tr>
<td>Gain, Channel 2 (Pins 6 &amp; 9)</td>
<td>D.C., Load=1kΩ, 25°C</td>
<td>-1.916</td>
<td>-1.910</td>
<td>-1.904</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>400Hz Sine Wave, Load=13Ω/79°</td>
<td>-1.920</td>
<td>-1.910</td>
<td>-1.900</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>+25°C to +85°C</td>
<td>-1.926</td>
<td>-1.910</td>
<td>-1.894</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>+25°C to +85°C</td>
<td>-1.920</td>
<td>-1.910</td>
<td>-1.900</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td>-55°C to +125°C</td>
<td>-1.926</td>
<td>-1.910</td>
<td>-1.894</td>
<td>V/V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Full Power, Eout=11.8 Vrms</td>
<td>20</td>
<td></td>
<td></td>
<td>KHz</td>
</tr>
<tr>
<td></td>
<td>Small Signal, -3dB</td>
<td>200</td>
<td></td>
<td></td>
<td>KHz</td>
</tr>
<tr>
<td>Output Offset Voltage</td>
<td>25°C</td>
<td>-30</td>
<td>±8</td>
<td>+30</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>-55°C to +125°C</td>
<td>-40</td>
<td>±10</td>
<td>+40</td>
<td>mV</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>Inverting Input (Pins 5 &amp; 8)</td>
<td>5.983</td>
<td>5.992</td>
<td>6.001</td>
<td>KΩ</td>
</tr>
<tr>
<td></td>
<td>Inverting Input (Pins 6 &amp; 9)</td>
<td>5.228</td>
<td>5.236</td>
<td>5.244</td>
<td>KΩ</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>-65°C to +125°C</td>
<td>11.8</td>
<td></td>
<td></td>
<td>Vrms</td>
</tr>
<tr>
<td>Current Limit</td>
<td>-65°C to +125°C</td>
<td>1.25</td>
<td>2.6</td>
<td>4.2</td>
<td>Apk</td>
</tr>
<tr>
<td>C Load</td>
<td></td>
<td>3000</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>At rated load</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pin 1</td>
<td>23</td>
<td></td>
<td></td>
<td>Vpk</td>
</tr>
<tr>
<td></td>
<td>Pin 2</td>
<td>-30</td>
<td></td>
<td>-26.2</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td>Pin 3</td>
<td>26.2</td>
<td></td>
<td>30</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td>Pin 11</td>
<td>-24.8</td>
<td></td>
<td>-23</td>
<td>Vpk</td>
</tr>
</tbody>
</table>
Circuit Description

The hybrid microcircuit assembly consists of two independent power amplifier circuits. These amplifiers are used to drive a 3-wire, X-Y-Z synchro load. Each amplifier can provide 11.8 Vrms at 400 Hz into its rated load.

Both circuits are inverting amplifiers with two possible gain configurations. The gain is selected by applying the input voltage to the appropriate pin as shown in figure 4.

The output circuit of each amplifier is current limited (foldback current limiting is used) to provide protection against overloads.

The inputs to the amplifiers are from digital to analog converters. The signal inputs are in a synchro format, \( E_{IX} = K \sin(\theta-120^\circ) \sin \omega t \) and \( E_{IY} = K \sin(\theta-60^\circ) \sin \omega t \), where \( K \) is the peak input voltage) so that both amplifiers will not be required to simultaneously dissipate maximum power.

The accuracy of the amplifier is due primarily to the thin film resistor networks U3 and U4. To ensure high accuracies, resistors R3/R14 were specified to a maximum initial tolerance of 0.1% and a temperature coefficient of ±25 ppm/°C. Resistors R1/R12 and R2/R13 were specified
Fig. 4. Power amplifier schematic
with nominal values of 5.992K and 5.236K respectively; and, more importantly, the ratio values of 1.66877 ± 0.05% and 1.90998 ± 0.05% and temperature tracking of ± 5 ppm/°C were required. Also, the use of a thin film network will simplify changing the gain of the amplifier for future use.

Resistors R4 and R15 are needed to help reduce the output offset voltages due to input bias currents.

A high voltage operational amplifier (National LM143 or Motorola MC1536) is used because of its output voltage swing of ± 22 V min and its output current capability of ± 4.4 mA. The current regulator diodes CR1, 2, 5 and 6 are used as a constant current source supplying the bias current to the transistors minimizing cross-over distortions in class B emitter-follower stage. Resistors R1 and R16 serve a dual role. The first is short circuit protection for the operational amplifier by limiting the power dissipation in the op-amp. The second is a part of the dominant pole (in conjunction with C2 and C4) in the base circuit to increase the stability of the circuit. (See the stability analysis section) The zener diodes (VR1-4) are part of the biasing network during normal operation. They also have a second function when the circuit is in current limiting as discussed later.

The silicon power darlington transistors (Q 1, 2, 7 and 8) were chosen for their collector current capability
(I_C = 8.0 Adc) and high breakdown voltages (V_CB = 80 Vdc, V_CEO = 80 Vdc). They are complementary darlington transistors and have built-in base emitter shunt resistors. The DC current gain of these transistors at low temperatures enables the circuit to meet all output current requirements.

Diodes CR3, 4, 7 and 8 suppress the voltage spikes due to the inductive load.

Capacitors C1 and C3 increase the stability of the amplifier by decoupling the output of the amplifier from the output stage and provide a controlled gain bandwidth product in conjunction with the parallel combination of R1 or R2 and R3 and Rl2 or Rl3 and Rl4 respectively.

Resistors R10, 11, 21 and 22 are the output current sense resistors for the current foldback circuit. (Discussion will be held to only one of the circuits). Foldback is initiated when the voltage drop across resistor R10 (due to load current) exceeds the base-emitter voltage sufficiently to turn-on transistor Q4. As Q4 turns on some of the base current of transistor Q1 is shunted through resistor R6 and the collector-emitter of Q4 to the output. The voltage developed across resistor R6 biases the base-emitter junction of Q3 and it turns on. The remaining base current of Q1 is shunted through Q3 and becomes the base drive current for Q4. Transistor Q4 will continue to conduct independently from the output current.
This technique is similar in principle to an SCR (silicon controlled rectifier) crowbar with the exception that power shutdown is not required to reset the circuit. Zener diode (VR2: $V_z = 3.6V$) ensures that the base emitter breakdown voltage ($V_{EB} = 5.0\text{ Vdc}$) is not exceeded when the current limiting circuit is conducting. (The opposite is true for VR1). The output voltage of the op-amp can in theory be nearly that of its power supply ($\pm 28\text{Vdc}$; for this circuit). On the alternate half of the cycle, transistors Q3 and Q4 will turn off and Q5 and Q6 will turn on if the overload still exists. Otherwise, the circuit will return to normal operation.
Hybrid Mechanization

After the circuit was designed, breadboarded and tested, and the circuit met all the design requirements, the circuit specifications and the schematic were forwarded to the hybrid manufacturers to begin the layout of the circuit.

In the development of the power hybrid, the thermal resistance must be held to a minimum to ensure that the maximum junction temperature of the transistors is not exceeded. Proper selection of the materials used will minimize the thermal resistance. Reduction is accomplished by eutectically bonding the chip to the substrate (material: gold/germanium) or by using a tin/lead solder preform. Conductive epoxies are not recommended for high power applications. The use of a heat sink, such as molybdenum ("molytab") is an alternate approach. The choice between beryllia and alumina (ceramic) for the substrate material is a major factor in the thermal design. Even though the thermal conductivity of beryllia is nearly seven times higher than alumina, beryllia requires a controlled closed environment if laser or sand abrasive trimming is necessary for resistors. Trimming processes on beryllia creates a dust which is lethal. The most important thermal junction occurs between the substrate
and the hybrid case. Eutectic bonding or solder preforms are strongly recommended rather than the use of conductive or non-conductive epoxies. The hybrid case, kovar or steel, is also important in thermal resistance reduction.

Once it has been decided what materials will be used, and the dimensions of the case are established, the circuit is partitioned and the layout begins. A simplified flow chart is shown in figure 5.

Layouts are made at twenty times scale on a clear sheet of mylar overlaying an accurate tenth-inch grid. The tenth-inch grid represents 5 mils on the actual circuit. The high current conductors (amplifier output stage) are specified to a minimum width of 30 mils and ground conductors to be 15 mils. All other conductor widths are to be 10 mils minimum with 10 mil spacing. Wire bonding pad size is 10 x 10 mils for 1 mil wire and 20 x 20 mils for 2 mil wire. The wire type is specified as gold with a 1 mil diameter except for the wire bonds on the power chips. Two 2 mil wires are used. After the layout is completed, "rubies" are then cut. A ruby is two laminations of mylar—the first is clear and the second is ruby red which is photographically opaque. The ruby is a precision artwork trace of the conductor pattern, crossovers and resistors. A separate ruby for each resistor ink is needed. The artworks are prepared by the
Fig. 5. Simplified flow chart of the hybrid manufacturing process
"cut-and-peel" method. The rubies are then photographically reduced down to a 1:1 scale and reproduce their image on 2-by-2 inch glass plates. The inks are then applied through the screen and then fired to 850°C. The process is repeated until all the layers are finished.

The resistors on the substrate are trimmed using a laser or sand abrasive trimmer to the tolerances required. The components are then mounted on the substrate and are connected together via wire bonds. The hybrid is then tested, hermetically sealed and retested.
IV. PERFORMANCE ANALYSIS

This section discusses the detailed circuit analysis of the power amplifiers. Errors due to amplifier imperfections and components are analyzed ensuring the accuracy requirements.

The output current is calculated for the power amplifier since it must be capable of supplying the required load current over the specified temperature range.

To reduce the power dissipation in the transistors, a three-phase AC power supply is used whereby reducing the total package dissipation when compared to a DC supply. Also, the power dissipation is calculated for short circuits using current foldback and compared to standard current limiting techniques. With the inductive load, frequency stability is required to prevent the amplifier from oscillating.

To verify that the maximum transistor junction temperature is not exceeded, a thermal analysis calculating the thermal resistance of the junction is performed.
Output Offset Voltage

Operational amplifiers may produce a constant output voltage even when both inputs are grounded. This output voltage is primarily caused by the imperfections in the input circuitry of the operational amplifier. To determine these effects, equivalent current and voltage sources are introduced at the input of the amplifier. The remaining portion of the amplifier will be treated as ideal (i.e. $A = \infty$).

The circuit of figure 6 is used to determine the effect of the offset sources under closed loop conditions.

![Fig. 6. Equivalent representations of offset sources](image-url)
Considering one source at a time, the output can be written by inspection as:

\[ V_{os} = I_1 R_3 - I_2 R_4 (1 + R_3 / R_1) + V (1 + R_3 / R_1) \]  

(1)

which can be rearranged as:

\[ V_{os} = (I_1 - I_2) R_3 + I_2 (R_2 - R_4 (1 + R_3 / R_1)) + V (1 + R_3 / R_1) \]  

(2)

This shows that the effective input voltage offset due to the offset current, \( I_{os} = I_1 - I_2 \), is dependent only upon \( R_3 \). The effective input offset due to the offset voltage, \( V \), is dependent upon \( 1 + R_3 / R_1 \) which is the closed-loop gain. The input offset due to the bias current, \( I_2 \), is dependent upon the resistance unbalance between the operational amplifier inputs.

From the specifications\(^3\) for an LM143 or an MC1536 operational amplifier:

- \( |V| = 7.0 \text{ mV} \)
- \( |I_2| = 35 \text{ nA} \) \((-55^\circ \text{C to } +125^\circ \text{C})\)
- \( |I_{os}| = 7.0 \text{ nA} \)

and substituting into equation 2 yields an output offset voltage due to the input \( V_{os} = 18.8 \text{ mV} \).
Amplifier Accuracy Analysis

From the stability analysis response curves it is seen that the poles and zero's due to the output stage and load do not affect the loop-gain \((A\beta)\) for frequencies around 400 Hz. Therefore, they can be neglected without error when calculating the gain accuracy at 400 Hz. The resulting model is shown in figure 7:

\[
\begin{align*}
E_i &\rightarrow \left(\frac{R_1}{R_1'+R_2'}\right) \rightarrow R_3 \rightarrow C_1 \rightarrow A_1 \rightarrow E_o \\
&= \left(\frac{1}{A_1(s)}\right) + \left(\frac{1}{1+sR_3C_1}\right)
\end{align*}
\]

Fig. 7. Gain accuracy model

And the transfer function can be written:

\[
\frac{E_o(s)}{E_i(s)} = \left[\frac{-R_3}{R_1(1+sR_3C_1)}\right] \left[\frac{1}{1 + \frac{1}{A_1(s)\beta(s)}}\right]
\tag{3}
\]

where

\[
A_1(s) = \frac{A_o}{1 + sA_o/\omega_{TA}} \quad \text{and} \quad \beta(s) = \frac{R_i}{R_1 + \frac{R_3}{1 + sR_3C_1}}
\]

where \(A_o\) and \(\omega_{TA}\) are the DC open loop gain and the unity gain bandwidth of the operational amplifier.

The overall closed loop response can be rewritten as:
\[
\frac{E_0(s)}{E_1(s)} = \left[ \frac{-A_0 R_3}{(A_0 + 1) R_i + R_3} \right] \times \left\{ \frac{1}{1 + \left[ \frac{(A_0 + 1) R_i R_3 C_5 + A_0 (R_i + R_3) / \omega_{TA}}{(A_0 + 1) R_i + R_3} \right] s + \left[ \frac{A_0 R_i R_3 C_5}{(A_0 + 1) R_i \omega_{TA} + R_3 \omega_{TA}} \right] s^2} \right\}
\]

The worst-case feedback configuration is for the closed loop gain equal to -1.91, where \( R_i = R_2 = 5.23566 \text{K}\Omega \) since this requires the most open-loop gain. Upon substitution of the typical component values into equation 4:

\[ R_3 = 10 \text{K}\Omega; \quad R_i = 5.23566 \text{K}\Omega; \quad C_5 = 47 \text{pF}; \quad A_0 = 5(10)^4; \quad \omega_{TA} = 2\pi 400 \text{Hz} \]

\[
\frac{E_0(s)}{E_1(s)} = \frac{-1.90991}{1 + 1.6278(10)^{-6} s + 1.867(10)^{-13} s^2}
\]

\[
= \frac{-1.90991}{\left[ 1 + \frac{s}{2\pi(105.8 \text{KHz})} \right] \left[ 1 + \frac{s}{2\pi(1.28 \text{MHz})} \right]}
\]

From equation 6 it is seen that the higher frequency closed loop pole will have negligible effect on the accuracy at 400Hz. Therefore, equation 6 will reduce to:

\[
\frac{E_0(s)}{E_1(s)} = \frac{-1.90991}{1 + \frac{s}{2\pi(105.8 \text{KHz})}}
\]

Letting \( s = \text{j}\omega \), the magnitude of the gain can be written as:

\[
\frac{\text{E}_0(\text{j}\omega)}{\text{E}_1(\text{j}\omega)} = \frac{-1.90991}{\sqrt{1 + \left( \frac{2\pi f}{2\pi(105.8 \text{KHz})} \right)^2}}
\]
The worst case gain at 400Hz, due to the amplifier is

\[
\left| \frac{E_o(400Hz)}{E_i(400Hz)} \right| = 1.90989
\]

which is an error equal to 0.0047%, and the maximum gain error due to the resistors is ±0.05%, which yields the maximum overall error of ±0.055%.
Output Current Capability

The output current of the amplifier will be calculated at the two temperature extremes to guarantee the requirements of the load. The DC model of the amplifier shown in figure 8 will be used in the analysis.

There are two limiting modes on the output current capability for the circuit:

1) Beta ($\beta$) of the buffer transistors Q1/Q2 times their potential base drive current, which is the lesser of the current diodes current, $I_{CR'}$, or the operational amplifiers output drive, $I_{OA}$.

$$I_B = I_{CR'}, \text{ if } I_{CR} < I_{OA} \quad (9)$$

or

$$I_B = I_{OA'}, \text{ if } I_{OA} < I_{CR} \quad (10)$$

2) Turn-on of the current limit circuit is composed of (Q3, Q4, R6, R7, R10) and (Q5, Q6, R8, R9, R11) and this limit occurs sooner at hot temperatures than cold.

It was determined that the maximum peak current during slewing is:

$$I_{I_p} \text{ (MAX) } = 0.813 \text{ Arms or 1.15 Apk}$$

(See Maximum Output Current Required).
Fig. 8. DC Output current model
Cold Temperature Limit

The maximum output current, $I_{\text{OPK}}$, can be expressed as:

$$I_{\text{OPK}} = \beta I_B = (\beta I_{\text{CR}} \text{ or } \beta I_{\text{OA}}) \quad (11)$$

Condition: The base drive is the lesser of $I_{\text{CR}}$ or $I_{\text{OA}}$.

From the minimum specifications of the operational amplifier:

$$I_{\text{OA}} \geq \frac{V_{\text{O min}}}{R_{\text{L min}}} \geq \frac{22V}{5\Omega} = 4.4 \text{ mA} \quad (12)$$

For the current diode, $I_{\text{CR1}} \geq 3.51 \text{ mA}$ minimum at $\pm 25^\circ \text{C}$. To calculate the current at $-65^\circ \text{C}$, the change due to temperature is

$$\Delta I_p = \Delta I_{\text{CR}} / \Delta T \quad -0.5\% / ^\circ \text{C} \quad (13)$$

$$I_{\text{CR1}} \geq I_{\text{CR1 \ Min.}} \text{ at } +25^\circ \text{C}(1 + (\Delta I_p / 100\%))(\Delta T) \quad (14)$$

$$I_{\text{CR1}} \geq 5.1 \text{ mA} \text{ at } -65^\circ \text{C}$$

At room temperature $I_{\text{CR1}} = 3.51 \text{ mA}$ which is less than the output current of the operational amplifier since $I_{\text{OA}} = 4.4 \text{ mA}$, the output current is:

$$I_{\text{Opk}} \geq \beta I_{\text{CR1}} = 750(3.51 \text{ mA}) = 2.63 \text{ Ampere at } +25^\circ \text{C} \quad (15)$$

At $-65^\circ \text{C}$, $I_{\text{CR1}} > I_{\text{OA}}$, therefore, the limiting parameter of the output current is:

$$I_{\text{Opk}} \geq (\beta \text{ at } -65^\circ \text{C})(I_{\text{OA}}) \quad (16)$$

To compute the minimum beta at $-65^\circ \text{C}$ from the transistor specifications it can be shown that $\beta = 328$ at $-65^\circ \text{C}$.
(see Appendix 1). The resulting output current using equation 16 is:

\[ I_{Opk} = (328)(4.4\text{mA}) = 1.44 \text{ Amperes at } -65^\circ\text{C} \quad (17) \]

Therefore, the circuit is capable of supplying a minimum output current of 1.44 Amperes at -65°C.
Hot Temperature Limit

Current limiting occurs when the voltage drop on R10(R11) causes sufficient collector current in Q4(Q6) to turn-on Q3(Q5) via R6(R7).

To determine the base-emitter voltage required to turn-on the transistor at +125°C the Ebers-Moll relationship for forward-biased junctions will be used.\(^6\)

\[
V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}
\]

where \(k\) = Boltzman's constant = \(1.38 \times 10^{-23}\) joules/°K

\(T\) = absolute temperature

\(q\) = electron charge = \(1.6 \times 10^{-19}\) coulombs

\(I_C\) = forward current

\(I_S\) = saturation current

The saturation current, \(I_S\), is also a function of temperature and is approximately\(^7\)

\[
I_S = BT^3 \exp \left(-\frac{qV_{go}}{kT}\right)
\]

where \(V_{go}\) = bandgap voltage at 0°C = 1.11 V

\(B\) = temperature-independent constant related to doping levels and junction geometry.

Combining the above equations it can be shown how the base-emitter voltage at any specified collector current and temperature (\(I_{CO}\) and \(T_0\) respectively)\(^8\) can be calculated.

\[
V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_{CO}} \frac{T_0}{T} + T \left(\frac{V_{BEO} - V_{go}}{T_0}\right) + V_{go}
\]
where $V_{BEO} = V_{BE}$ at $I_{CO}$ and $T_0$

Differentiating equation 20 with respect to temperature for a constant collector current will show the temperature variation per °C.

$$\left( \frac{dv_{BE}}{dT} \right)_{I_c=constant} = \frac{V_{BEO} - V_{GO}}{T_0} - \frac{3k}{q} \left( 1 + \ln \frac{T}{T_0} \right) \quad (21)$$

Evaluating equation 21 at 298.15°K (+25°C) and with a typical $V_{BEO} = .64$ volts yields a temperature coefficient approximately equal to $-1.84$ mV/°C. Therefore, at +125°C the base-emitter voltage required at turn-on is 456 mV, and a collector current

$$I_{C4} = \frac{V_{BE}}{R_6} = \frac{456\text{mV}}{1\text{K}\Omega} = 0.456 \text{mA} \quad (22)$$

is where Q3(Q5) starts to conduct. The required voltage drop on $R_{10}$ is calculated using equation 22

$$V_{BE} = 0.426 \text{ volts at +125°C}$$

and the minimum current limit is then

$$I_0 \text{ Limit} > \frac{426\text{mV}}{0.3\Omega} = 1.42 \text{ Amperes at +125°C} \quad (23)$$

which is 19% greater than the absolute worst case output current required.

The cold and hot temperature output current limits determined are absolute minimums at those temperatures; and typically the gain of the transistors, $\beta$, and the operational amplifier output current will be greater.

The maximum current limit will be calculated to ensure
that the maximum current capability of the output transistors is not exceeded at room temperature for output short circuits.

\[
I_0 \text{ Limit Max.} < \frac{V_{BE \, Max.}}{R_{10 \, Min.}} = \frac{750\,mV}{0.2\Omega} = 3.75 \, A \quad (24)
\]

which is less than the rated continuous current of 8 amperes.
Maximum Output Current Required

The load on the hybrid is a synchro torque receiver and can be modeled as shown in figure 9:

![Synchro torque receiver model](image)

**Fig. 9. Synchro torque receiver model**

Writing the loop equations for $I_{LX}$ and $I_{LY}$ yields:

\[
E_X = I_{LX}(2Z) + I_{LY}(Z) \tag{25}
\]

\[
E_Y = I_{LX}(Z) + I_{LY}(2Z) \tag{26}
\]

where

\[
E_X = E_{OX} \sin(\theta-120^\circ) \tag{27}
\]

\[
E_Y = E_{OY} \sin(\theta-60^\circ) \tag{28}
\]

\[
Z = (2/3)Z_{so}
\]

$Z_{so}$ is the stator impedance with the rotor open at electrical zero

$\theta$ = transmitted data angle, degrees

Solving for $I_{LX}$ and $I_{LY}$ and substituting equations 27 and 28 into equations 25 and 26

\[
I_{LX} = \frac{\sqrt{3}}{4} \frac{E_{OX}(\sqrt{3} \sin\theta+\cos\theta)}{Z_{so}} \tag{29}
\]
and

\[ I_{LY} = -\sqrt{3} \frac{E_{OY}}{4} \left[ \sqrt{3} \sin\theta - \cos\theta \right] \]  

(30)

Differentiating the line current equations with respect to \( \theta \) and solving for the maximum current yields:

\[ I_{LX \ Max} = \frac{\sqrt{3} E_{OX}}{2 Z_{SO}} \text{ at } \theta = 60^\circ \]  

(31)

\[ I_{LY \ Max} = \frac{\sqrt{3} E_{OY}}{2 Z_{SO}} \text{ at } \theta = -60^\circ \]  

(32)

Therefore, the maximum magnitude of any line current is

\[ I_{L \ Max} = \frac{\sqrt{3} E_{O}}{2 Z_{SO}} \]  

(33)

The synchro load for the amplifiers are two torque receivers connected in parallel. The equivalent load impedance is equal to the parallel combination where

\[ Z_{SO1} = 3.12 + j17 \text{ and } Z_{SO2} = 10 + j45. \]

Therefore, \( Z_{SO} = 12.57 \Omega /79^\circ \)

and the worst case maximum required output current is

\[ I_{L \ Max} = \frac{\sqrt{3} (11.8 \text{ Vrms})}{2 (12.57\Omega)} = 0.813 \text{ Arms} \]  

(34)

It should be noted that the maximum line current of 0.813 Arms occurs when the output voltage is 10.2 Vrms. Also, since the torque receiver (TR) is similar to a transformer with voltages applied to both the primary and secondary ratioed to match the "transformation ratio", the line currents will be much less when the rotor position
comes to null. Only during the slewing time will the load current be maximum.

Laboratory data indicates that the maximum steady-state line current when the rotor position is in null will be 0.37 Arms for voltage ratio and transformation-ratio errors up to 10%. When the rotor angle is 30°,

\[ E_{OX \, Max} = 11.8 \text{ Vrms} \text{ (the maximum output voltage)} \text{ and the slewing current will be} \]

\[
I_{LX} (\theta=30°) = \frac{\sqrt{3}(11.8 \text{ Vrms})[\sqrt{3} \sin30° + \cos30°]}{4(12.57\Omega)}
\]

\[ I_{LX} = 0.704 \text{ Arms, Max} \]

The continuous "null current" will be

\[ I (\text{calculated-null}) = \frac{I (\text{measured-null})}{X \text{ (calculated-slewing) Max} \text{ (calculated-slewing)}} \]

\[ = \frac{0.37 \text{ Arms}}{0.813 \text{ Arms}} \times 0.704 \text{ Arms} \]

\[ I (\text{null}) = 0.32 \text{ Arms} \]

Therefore, when the amplifier is required to deliver rated output voltage of 11.8 Vrms, the maximum load current is 0.704 Arms during slewing and 0.32 Arms continuous.
Power Dissipation

The power dissipation in the amplifiers is calculated for each power supply. It will be shown that the use of the AC power supply is more efficient than the conventional DC supply and a greater power reduction can be realized.

The equivalent or average DC voltage of the AC supply is 16.67 volts (see Appendix 2). The supply voltage waveform (see figure 10) is generated from the three-phase AC power. All three phases are diode OR-ed with phase A and B used as the "filler" voltages. The filler voltages are needed to maintain a minimum supply voltage across the output transistors.
Fig. 10. Full-wave power supply waveform
Expression for the Power Supply Voltage

From figure 10 the input voltage can be expressed as:

\[
E_{IN} = E_{Slpk} \sin\omega t\left|_{\phi}^{(\pi-\alpha)} \right. + E_{S2pk} \sin(\omega t-\pi/3)\left|_{(\pi-\alpha)}^{\pi} \right. \\
+ E_{S2pk} \sin(\omega t-2\pi/3)\left|_{\pi}^{(\pi-\alpha)} \right. + E_{Slpk} \sin(\omega t-\pi)\left|_{(\pi-\alpha)}^{(\pi+\alpha)} \right.
\]

for \(\alpha \leq \phi \leq (\pi-\alpha)\)

The value of \(\alpha\) can be determined by solving the intersection of the \(\Phi_C\) and \(\Phi_A\) components of the power supply voltage.

Letting \(\alpha = \omega t\)

\[
E_{Slpk} \sin\alpha = E_{S2pk} \sin(\alpha+\pi/3) \\
= E_{S2pk} \cos\alpha\sin\pi/3 + E_{S2pk} \sin\alpha\cos\pi/3
\]

\[
\alpha = \tan^{-1}\left[ \frac{\sqrt{3} E_{S2pk}}{2 E_{Slpk} - E_{S2pk}} \right]
\]

(38)

Substituting typical values into equation 38 where

\(E_{Slpk} = 23\) Volts and \(E_{S2pk} = 12.5\) Volts

\(\alpha = 32.9^\circ; 0.574\) rad
Amplifier Power Dissipation - Three Phase AC

The average power dissipation in the output stage of the amplifier, \( P_A \), is defined as:

\[
P_A = P_{\text{IN}} - P_{\text{OUT}}
\]

or

\[
P_A = \frac{1}{\pi} \int_{\phi}^{(\phi+\pi)} [E_S(\omega t) - E_O(\omega t)] I_O(\omega t) d(\omega t)
\]

where \( E_S = \) power supply voltage
\( E_O = \) output voltage of the amplifier
\( I_O = \) output current (or line current)

The integral can be broken into parts

\[
P_A = \frac{1}{\pi} \left\{ \int_{\phi}^{(\pi-\alpha)} E_{S1} \sin(\omega t) I_O \sin(\omega t - \phi) d(\omega t) \\
+ \int_{(\pi-\alpha)}^{\pi} E_{S2} \sin(\omega t - \pi/3) I_O \sin(\omega t - \phi) d(\omega t) \\
+ \int_{(\pi-\alpha)}^{(\pi+\alpha)} E_{S2} \sin(\omega t - 2\pi/3) I_O \sin(\omega t - \phi) d(\omega t) \\
+ \int_{(\pi+\alpha)}^{(\pi+\phi)} E_{S1} \sin(\omega t - \pi) I_O \sin(\omega t - \phi) d(\omega t) \\
- \int_{(\pi+\phi)}^{(\pi+\phi)} E_O \sin(\omega t) I_O \sin(\omega t - \phi) d(\omega t) \right\}
\]

where the constants \( E_{S1}, E_{S2}, E_O \) and \( I_O \) are peak values.
Equation 41 will be solved using the integral equation (see Appendix 3 for the derivation).

\[
\int \sin(A-B)\sin(A-C)dA = \frac{1}{4} \sin(B+C-2A) + \frac{A}{2} \cos(B-C)
\]

(42)

Integrating equation 41 using equation 42

\[
P_A = \frac{E_{S1}I_Q}{4\pi} \left\{ \sin(\phi-2\omega t) + 2\omega \cos(\phi) \right\}_{\phi}^{(\pi-\alpha)}
\]

\[
+ \left[ \sin(\pi+\phi-2\omega t) + 2\omega \cos(\pi-\phi) \right]_{(\pi+\alpha)}^{(\pi+\phi)}
\]

\[
+ \frac{E_{S2}I_Q}{4\pi} \left\{ \frac{\sin(\frac{\pi+\phi-2\omega t}{3}) + 2\omega \cos(\phi)}{3} \right\}_{\frac{\pi}{3}}^{(\pi-\alpha)}
\]

\[
+ \left[ \frac{\sin(\frac{2\pi+\phi-2\omega t}{3}) + 2\omega \cos(\frac{2\pi-\phi}{3})}{3} \right]_{\frac{\pi}{3}}^{(\pi+\alpha)}
\]

\[
- \frac{E_{L}I_L}{4\pi} \left\{ \sin(\phi-2\omega t) + 2\omega \cos(2\phi) \right\}_{\phi}^{(\pi+\phi)}
\]

(43)

Making the necessary substitutions

\[
P_A = \frac{E_{S1}I_Q}{2\pi} \left[ (1+\cos 2\alpha) \sin \phi + (\pi-2\phi) \cos \phi \right]
\]

\[
+ \frac{E_{S2}I_Q}{4\pi} \left\{ \sin(60^\circ+\phi) - \sin(120^\circ+\phi) + \sin(120^\circ+\phi-2\alpha)
\right.
\]

\[
- \sin(60^\circ+\phi+2\alpha) + 2\alpha \left[ \cos(60^\circ-\phi)+\cos(120^\circ-\phi) \right]
\]

\[
- \frac{E_{L}I_L}{2\pi} \cos \phi
\]

(44)
Inserting the typical values into equation 44 where,

\[ E_{S1} = 23 \text{ V}; \quad E_{S2} = 12.5 \text{ V}; \quad \alpha = 32.9^\circ, \quad 0.574 \text{ rad}; \]
\[ E_O = \sqrt{2} \text{ 11.8 V}; \quad \phi = 79^\circ, \quad 1.379 \text{ rad}. \]

\[ P_A = 5.95 I_{Orms} - 0.191 E_{Orms} I_{Orms} \quad \text{(45)} \]

For the calculated load current, \( I_{Orms} = 0.32 \text{ Arms} \) the power dissipated in the amplifier is 1.18 Watts.
It will be shown that the use of a DC power supply greatly increases the power dissipation in the amplifier. For this reason the AC supply was developed thereby increasing the overall efficiency of the amplifier.

\[
P_A = \frac{1}{\pi} \int_{\phi}^{(\phi+\pi)} E_S - E_O(\omega t) I_O(\omega t) d(\omega t) \tag{46}
\]

where \( E_S \) = power supply voltage, DC
\( E_O \) = output voltage of the amplifier
\( I_O \) = output current (or line current)

\[
P_A = \frac{1}{\pi} \int_{\phi}^{(\phi+\pi)} E_S I_O \sin(\omega t - \phi) d(\omega t)
- \int_{\phi}^{(\phi+\pi)} E_O \sin(\omega t) I_O \sin(\omega t - \phi) d(\omega t) \tag{47}
\]

\[
= \frac{E_S I_O}{\pi} \left\{ - \left[ \cos(\omega t - \phi) \right]_{\phi}^{\phi+\pi} \right\} - \frac{E_O I_O \cos \phi}{2} \tag{48}
\]

\[
P_A = \frac{2E_S I_O}{\pi} - \frac{E_O I_O \cos \phi}{2} \tag{49}
\]

Inserting typical values into equation 49 where, \( E_S = 28 \) V
\( \phi = 79^\circ, 1.379 \) rad.

\[
P_A = 17.825 I_O - 2.25 I_{Orms} \tag{50}
\]

Using the calculated load current, \( I_{Orms} = 0.32 \) Arms,
the power dissipated in the amplifier is 7.35 Watts.
Fault Conditions

If a short circuit defined as a one ohm load exists at the output of the amplifier, the foldback current limit circuit will turn-on. A typical output voltage waveform is shown in figure 11.

![Typical output voltage waveform](image)

**Fig. 11.** Current limiting waveform

The average power dissipation in the amplifier, $P_{ACL}$, is defined as:

$$P_{ACL} = \frac{1}{\pi} \int_{0}^{t_o} \left[ E_S \sin(\omega t + 2\pi/3) - E_0 \sin(\omega t) \right] \times I_{CL} \sin(\omega t) d(\omega t)$$  \hspace{1cm} (51)

For the nominal current limit the turn-on point of the foldback circuit, $I_{CL} = 2.6$ Amperes, the power in the amplifier is then,
Upon substituting the typical values into equation 52 where $E_S = 12.5V$; $E_O = 11.8\sqrt{2}V$ and $t_o = 0.062$ ms. the average power dissipation in the amplifier is 0.084 Watts.

If a conventional current limiting circuit were used the power dissipation in the amplifier if the same current limiting point was held would be 43.36 Watts (see Appendix 4). This power dissipation is exceedingly high and the current limit threshold would be lowered (e.g., one ampere). This would then lower the amplifier power dissipation to approximately 17 Watts.
AC Stability Analysis

The AC open-loop model shown in figure 13 indicates that the analysis can be done in two stages, the integrator first stage (figure 12) and the output buffer stage (figure 14).

The gain $E_o/E_i$ is the "loop-gain" (Aβ) and its nature at OdB determines the closed-loop stability.

Fig. 12. Model used for the first stage analysis

Where

$$R_{IN} = R_1 || R_3 \quad \text{and} \quad E' = E_i \frac{R_{IN}}{R_{IN} + R_3}$$ (53)

$$E_x(s) = A_1(s) E_a(s)$$ (54)

and letting $Z = 1/C_1$ (55)

and writing the current expressions

$$E_i - E_a = E_a - E_x$$ (56)
Fig. 13. AC open-loop model
Solving for $E_a$

$$E_a = \frac{(E_i'Z + E_xR_{IN})}{(Z + R_{IN})}$$

and substituting equation 54 into equation 57

$$E_a = \frac{(E_i'Z)}{(Z + R_{IN} - AR_{IN})}$$

Let $K_o = \frac{Z}{R_{IN}} = \frac{1}{sC_1R_{IN}}$

and substitute equation 59 into equation 58 and rearranging terms yields

$$\frac{E_a}{E_i'} = -K_o \left[ \frac{1}{1 + K_o - A_1} \right]$$

Using equation 54 where $E_a(s) = \frac{E_x(s)}{A_1(s)}$, equation 60 can be written as:

$$\frac{E_x(s)}{E_i'(s)} = -K_o \left[ \frac{-A_1(s)}{1 + K_o - A_1(s)} \right]$$

For the amplifier a one-pole rolloff model will be used.

$$A_1(s) = -A_o\frac{\omega_a}{s + \omega_a}$$

where $A_o = \text{DC open-loop gain}$

$\omega_a = 3\text{dB frequency}$

Upon substituting equation 62 into equation 61 can be written as:

$$\frac{E_x(s)}{E_i'(s)} = -K_o \left[ \frac{A_o\omega_a/(1+K_o)}{(s + \omega_a) + A_o\omega_a/(1+K_o)} \right]$$

With the substitution of equation 59, for $K_o$, and equation 53, for $E_i'$ into equation 63 and rearranging terms the first stage transfer function is:

$$\frac{E_x(s)}{E_i(s)} = \left( \frac{-R_1A_o}{R_1 + R_3} \right) \frac{1}{1 + sC_1R_{IN}(1+A_o) + 1/\omega_a + s^2R_{IN}C_1/\omega_a}$$
Inserting the component values into equation 64 where
\[ A_0 = 10^5; \quad R_1 = 5.235\ \Omega; \quad R_3 = 10\ \Omega; \quad R_{IN} = 3.436\ \Omega; \]
\[ C_1 = 47\text{pF} \text{ and } \omega_a = 20\pi \text{ radians}. \]
\[ \frac{E_x(s)}{E_i(s)} = \frac{-3.436(10)^4}{1 + 3.206(10)^{-2} + 2.57(10)^{-9}s^2} \] (65)

In factored form equation 65 becomes
\[ \frac{E_x(s)}{E_i(s)} = \frac{-3.436(10)^4}{\left[1 + \frac{s}{2\pi(10\text{Hz})}\right] \left[1 + \frac{s}{2\pi(2.0\text{MHz})}\right]} \] (66)

Second stage

The second stage can be remodeled as shown in figure 14.

Fig. 14. Model used for the second stage analysis
Where \( C_T = C_2 + C_{obl} + C_{ob2} \), and \( I_B(s) \) is the complex base current of the darlington transistor, and \( I_E(s) \) is the output emitter current. The transistor transfer function can be accurately modeled as having two poles at the same frequency resulting in an overall unity-gain bandwidth of 4MHz from a DC gain of 2000.
Solving for the current gain

\[ \frac{I_E(s)}{I_B(s)} = (h_{fe}(s) + 1) = \frac{h_{feo}}{(1 + s\sqrt{h_{feo}/\omega_{TQ}})^2} + 1 \]  \hspace{1cm} (67)

\[ \frac{I_E(s)}{I_B(s)} = h_{feo} \left[ 1 + \frac{2s/(\omega_{TQ}\sqrt{h_{feo}}) + s^2/\omega_{TQ}^2}{(1 + s\sqrt{h_{feo}/\omega_{TQ}})^2} \right] \]  \hspace{1cm} (68)

since \( h_{feo} \gg 1 \)

Upon substitution of the values for \( h_{feo} \) and \( \omega_{TQ} \) where \( h_{feo} = 2000 \) and \( \omega_{TQ} = 2\pi(4\times10^6) \) radians.

\[ \frac{I_E(s)}{I_B(s)} = 2(10)^3 \left[ 1 + 1.7794(10)^{-9}s + 1.583(10)^{-15}s^2 \right] \left[ 1 + \frac{s}{2\pi(89.4\text{KHz})} \right] \]  \hspace{1cm} (69)

In factored form equation 69 becomes

\[ \frac{I_E(s)}{I_B(s)} = 2(10)^3 \left[ 1 + \frac{s}{2\pi(89.4\text{KHz}+j4\text{M}\text{Hz})} \right] \left[ 1 + \frac{s}{2\pi(89.4\text{KHz}-j4\text{M}\text{Hz})} \right] \]  \hspace{1cm} (70)

The effective capacitance \( C_T \) is the sum of \( C_2 \) and \( C_{ob} \) of transistors Q1 and Q2; where the average \( V_{CB} \) is 15 Volts.

\( C_{obl} = 80\text{pF} \); \( C_{ob2} = 140\text{pF} \) and therefore, \( C_T = 610\text{pF} \).

Two cases exist for the output load:

Case 1 - No capacitive load

Case 2 - \( C_L = 0.003\mu\text{F} \)

Note that at high frequencies the synchro load is essentially an open circuit since the inductance becomes a high impedance.
Case 1 - No capacitive load

\[ Z_B = \infty \text{ and } R_5 = 270 \Omega \]

\[
\frac{E_o(s)}{E_x(s)} = \frac{1}{1 + sR_5C_T} \left[ 1 + \frac{s}{2\pi(970 \text{ KHz})} \right] \tag{71}
\]

Case 2 - \( C_L = 0.003 \mu F \)

Then

\[
Z_B = \frac{I_E(s)}{I_B(s)} \left( R_10 + \frac{1}{sC_L} \right) = \frac{I_E(s)}{I_B(s)} \left( \frac{1 + sR_10C_L}{sC_L} \right) \tag{72}
\]

Substituting for \( I_E(s)/I_B(s) \) into equation 72

\[
Z_B = h_{feo} \left[ \frac{1 + 2s/\omega_{TQ}h_{feo} + s^2/\omega_{TQ}^2}{sC_L[1 + s\sqrt{h_{feo}/\omega_{TQ}}]^2} \right] \left[ 1 + sR_10C_L \right] \tag{73}
\]

\[
Z_{C_T || Z_B} = \frac{Z_C}{Z_C + Z_B}
\]

\[
= h_{feo} \left[ \frac{1 + 2s/\omega_{TQ}h_{feo} + s^2/\omega_{TQ}^2}{sC_L[1 + s\sqrt{h_{feo}/\omega_{TQ}}]} \right] \left[ 1 + sR_10C_L \right] \times \frac{1}{sC_Lh_{feo} \left[ 1 + 2s/\omega_{TQ}h_{feo} + s^2/\omega_{TQ}^2 \right] \left[ 1 + sR_10C_L \right]} \tag{74}
\]

The gain expression can now be written for the second stage:

\[
\frac{E_o(s)}{E_x(s)} = \frac{Z_C}{Z_C + Z_B} \tag{75}
\]
Substituting into equation (76) the component values where 

\[ C_L = 0.003 \mu F; \quad C_T = 610 \mu F; \quad R_5 = 270 \Omega; \quad R_{l0} = 0.25 \Omega; \]

\[ h_{feo} = 2000 \] and \( \omega_{TQ} = 2\pi(4\times10^6) \) radians.

\[
\begin{align*}
\frac{E_o(s)}{E_x(s)} & = \left[ \frac{1+2s/\omega_{TQ}\sqrt{h_{feo}}+s^2/\omega_{TQ}^2}{1+2s/\omega_{TQ}\sqrt{h_{feo}}+s^2/\omega_{TQ}^2} \right] \left[ \frac{1+sR_{10}C_L}{1+sR_{10}C_L} \right] \\
& \times \frac{l}{sR_5C_I \left[ \frac{1}{\sqrt{h_{feo}}} + \frac{s}{\omega_{TQ}} \right]}
\end{align*}
\]

(76)

and rewriting equation (77)

\[
\begin{align*}
\frac{E_o(s)}{E_x(s)} & = \left[ \frac{1+2.25(10)^{-9}s}{1+1.779(10)^{-9}s+1.583(10)^{-15}s^2} \right] \\
& \times \frac{5.867(10)^{-3}1.547(10)^{-2}3.69(10)^{-15}s^2}{1.69(10)^{-7}s+1}
\end{align*}
\]

(77)

The overall open-loop response: loop-gain

\[
\frac{E_o(s)}{E_i(s)} \bigg|_{OL} = \frac{E_x(s) \times E_o(s)}{E_i(s) \times E_x(s)}
\]

(79)

and the closed-loop response is

\[
\frac{E_o(s)}{E_i(s)} \bigg|_{CL} = \frac{-1.91}{1 + \frac{E_o(s)}{E_i(s)} \bigg|_{OL}}
\]

(80)

A computer program was written to calculate the loop-gain and phase shift; closed-loop gain and phase shift. The computer print-out is shown in Table 2, and the data is plotted for both the open and closed-loop gains in figures 15 and 16 respectively.
TABLE 2
FREQUENCY RESPONSE - COMPUTER PRINTOUT

2 DIM C(4)
4 C(1)=1, C(2)=2+C(3)=4+C(4)=7
10 COMPLEX A,B,C,S,U
11 PRINT "********LOOP-GAIN ******", "********CLOSED-LOOP GAIN ******"
12 PRINT
15 PRINT GAIN (DB)'*', PHASE (DEG)'*', GAIN (DB)'*', PHASE (DEG)'*', "FREQ"
16 PRINT
17 E=100
18 FOR I=1 TO 4
20 F=E*C(I)
30 A0=3.434E4
40 A=A0/(2.5687E-9*S^2+1.62056E-2*S+1)
50 B=(1.9225E-9*S*(1.5851E-15*S^2+1.7794E-9*S+1)/(5.8667E-31*S^4+1.547E-21*S^3+1.6913E-7*S+1))
60 C=A*B
61 D=-1.91/(1/C(I))
70 PRINT 20*LDG10(CABSCC)>>180/PI*PHASE(C)>20*LOG10(CABSCD), 180/PI*PHASE(D)>F
80 NEXT I
90 IF E>1E7 THEN END ELSE E=10*E
100 GO TO 18
>RUN

********LOOP-GAIN ******

<table>
<thead>
<tr>
<th>GAIN (DB)</th>
<th>PHASE (DEG)</th>
<th>GAIN (DB)</th>
<th>PHASE (DEG)</th>
<th>FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>64.613428</td>
<td>-87.166475</td>
<td>5.6204134</td>
<td>179.96636</td>
<td>100</td>
</tr>
<tr>
<td>58.606844</td>
<td>-89.595605</td>
<td>5.6204113</td>
<td>179.93271</td>
<td>200</td>
</tr>
<tr>
<td>52.50225</td>
<td>-91.324178</td>
<td>5.620407</td>
<td>179.86542</td>
<td>400</td>
</tr>
<tr>
<td>47.721938</td>
<td>-93.655421</td>
<td>5.620379</td>
<td>179.76449</td>
<td>700</td>
</tr>
<tr>
<td>44.624008</td>
<td>-95.803817</td>
<td>5.620343</td>
<td>179.66536</td>
<td>1000</td>
</tr>
<tr>
<td>38.603472</td>
<td>-97.034333</td>
<td>5.620125</td>
<td>179.32173</td>
<td>2000</td>
</tr>
<tr>
<td>32.598269</td>
<td>-98.202015</td>
<td>5.619275</td>
<td>178.65431</td>
<td>4000</td>
</tr>
<tr>
<td>27.271898</td>
<td>-99.573344</td>
<td>5.616920</td>
<td>177.64527</td>
<td>7000</td>
</tr>
<tr>
<td>24.632591</td>
<td>-100.854351</td>
<td>5.613022</td>
<td>176.63662</td>
<td>10000</td>
</tr>
<tr>
<td>18.601409</td>
<td>-101.751142</td>
<td>5.592012</td>
<td>173.27932</td>
<td>20000</td>
</tr>
<tr>
<td>12.574484</td>
<td>-102.621774</td>
<td>5.507530</td>
<td>166.60684</td>
<td>40000</td>
</tr>
<tr>
<td>7.6964055</td>
<td>-103.162633</td>
<td>5.286062</td>
<td>156.78714</td>
<td>70000</td>
</tr>
<tr>
<td>4.571875</td>
<td>-104.767299</td>
<td>4.944387</td>
<td>147.31013</td>
<td>100000</td>
</tr>
<tr>
<td>1.599363</td>
<td>-105.35607</td>
<td>3.2449632</td>
<td>119.20163</td>
<td>200000</td>
</tr>
<tr>
<td>3.147054</td>
<td>-106.09995</td>
<td>1.313942</td>
<td>79.538669</td>
<td>400000</td>
</tr>
<tr>
<td>-1.948129</td>
<td>-107.77682</td>
<td>-1.9688409</td>
<td>46.573132</td>
<td>700000</td>
</tr>
<tr>
<td>-1.679866</td>
<td>-109.67094</td>
<td>-10.996308</td>
<td>30.074668</td>
<td>1000000</td>
</tr>
<tr>
<td>-27.256167</td>
<td>-111.642425</td>
<td>-21.791472</td>
<td>115.80822</td>
<td>2000000</td>
</tr>
<tr>
<td>-87.597081</td>
<td>-113.726264</td>
<td>-81.976718</td>
<td>-147.29864</td>
<td>4000000</td>
</tr>
<tr>
<td>-79.105232</td>
<td>-115.13951</td>
<td>-73.484218</td>
<td>-88.864614</td>
<td>7000000</td>
</tr>
<tr>
<td>-68.530076</td>
<td>-116.740708</td>
<td>-80.909277</td>
<td>-71.261575</td>
<td>10000000</td>
</tr>
<tr>
<td>-103.24679</td>
<td>-119.255337</td>
<td>-97.626102</td>
<td>-70.746999</td>
<td>20000000</td>
</tr>
<tr>
<td>-120.21228</td>
<td>-121.15579</td>
<td>-114.59161</td>
<td>-62.844259</td>
<td>40000000</td>
</tr>
<tr>
<td>-133.0583</td>
<td>-122.90671</td>
<td>-127.43763</td>
<td>-52.993301</td>
<td>70000000</td>
</tr>
<tr>
<td>-140.65542</td>
<td>-123.56136</td>
<td>-135.03475</td>
<td>-47.438849</td>
<td>1E+08</td>
</tr>
<tr>
<td>-154.58673</td>
<td>-125.64696</td>
<td>-148.96607</td>
<td>-44.353039</td>
<td>2E+08</td>
</tr>
<tr>
<td>-186.92375</td>
<td>-126.63371</td>
<td>-163.30309</td>
<td>-53.362836</td>
<td>4E+08</td>
</tr>
<tr>
<td>-181.07685</td>
<td>-115.33021</td>
<td>-176.08619</td>
<td>-64.669794</td>
<td>7E+08</td>
</tr>
</tbody>
</table>
Fig. 16. Calculated closed-loop response.

- Closed-loop Phase
- Closed-loop Gain

Frequency (Hz)

Gain (dB)

Phase Shift (Degrees)
Thermal Analysis

Several factors are to be considered prior to the thermal calculations. Heat transferred by radiation and convection is not calculated but is considered as a safety margin. It should be noted that convection and radiation can be difficult to control but that their effects in the model are negligible. The effect of heat transfer has the same form as three resistances in parallel. The lowest resistance is that caused by conduction and the other resistances, being high in value, are caused by convection and radiation.

From the Second Law of Thermodynamics it is known that heat flows from a higher to a lower temperature. If a heat source (transistor die) is attached to one surface of the substrate and if the opposite surface of the substrate is at a lower ambient temperature, heat will flow to the lower temperature side. The heat continues to flow as long as there is a temperature gradient.

The maximum heat transfer for a given condition occurs when the surface areas and thermal conductivities are maximized and the thickness is minimized. Thermal conduction models will be developed as an aid in the analysis.

The equations that describe thermal spreading are quite complicated. The assumption that the heat flow
diverges to approximately 45 degrees has been shown to be conservatively valid for most design calculations. This makes the model look like a truncated pyramid. A good approximation of cross-sectional area (see figure 17) comes about through integrating equation 81

\[ \Theta = \frac{1}{K} \int_{0}^{X} \frac{dx}{Area} \]  

(81)

where

- \( \Theta \) = thermal impedance, \(^{\circ}\text{C}/\text{watt} \)
- \( K \) = thermal conductivity, \( \text{watts}/\text{\ensuremath{^\circ}\text{C}-inch} \)
- Area = \( F(X) = \) surface area, square-inch
- \( X \) = thickness, inch

Substituting Area = \((a+2y)^2\) into equation 81 and solving

\[ \Theta = \frac{1}{K} \int_{0}^{X} \frac{dy}{(a+2y)^2} \]  

(82)

\[ \Theta = \frac{x}{Ka(a+2x)} \]  

(83)

equation 83 is valid only for a square heat source.

If the heat source were rectangular (see figure 18) the area would be Area = \((a+2y)(b+2y)\).

Substituting the above area into equation 81 the thermal impedance is

\[ \Theta = \frac{1}{2K(a-b)} \left[ \ln \left( \frac{a}{b} \right) \left( \frac{2x+b}{2x+a} \right) \right] \]  

(84)
Fig. 17. Cross-sectional model for a square heat source

Fig. 18. Cross-sectional model for a rectangular heat source
A further assumption is made that the cross-sectional area through which the heat flows remains nearly constant for bonds using eutectic alloys or conductive adhesives. Therefore, equation 81 will reduce to

$$\theta = \frac{x}{KA}$$

(85)

Two manufacturers built the hybrid and each had a slightly different approach. One manufacturer bonded the power transistor die on a molybdenum heat sink (usually called a "molytab") and then bonded the molytab to the substrate (see figure 20). The second manufacturer bonded the power transistor die directly to the substrate, but this created some difficulties.

The first difficulty occurred in the case of transistor failure. The number of times the die can be replaced is limited. When the transistor die is lifted, some of the gold is removed from the pad.

Secondly, the die does not have a gold backing, but rather a chrome-silver backing. This means that eutectic bonding of the die, preferred method, could not be used unless special techniques were utilized. That is, the bonding pad must have a second layer of gold. The reason being is that during the eutectic bonding process the gold is absorbed into the die and electrical continuity may be broken. However, the second layer which is not absorbed insures electrical continuity.
Die with chrome-silver backing are bonded to the substrate using a solder preform. The preform consists of lead (92.5%), indium (2.5%) and silver (5.0%).

The thermal impedances for each junction are calculated for the sake of comparison. It will become evident that the eutectic bonding approach is the preferred method. Also, it will be shown that the major thermal junction is that of the substrate to the case.

In the final selection of the bonding materials, a second consideration is necessary other than thermal properties. The materials must have approximately the same temperature coefficient of expansion. This is necessary or else fractures will occur in the bond. Tables 3 and 4 show both the thermal conductivities and linear expansion coefficients for materials generally used in hybrids.

As evidenced in Table 3 the thermal expansion coefficient of such materials as beryllia and kovar are so widely different that these materials are not used together so as to prevent substrate fracturing.
<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Conductivity Δ</th>
<th>Linear Expansion Coefficient *</th>
<th>Solderability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>10.0</td>
<td>17.6</td>
<td>Excellent</td>
</tr>
<tr>
<td>Gold</td>
<td>6.9</td>
<td>14.3</td>
<td>Fair</td>
</tr>
<tr>
<td>Beryllia</td>
<td>6.0</td>
<td>9.0</td>
<td>Fair</td>
</tr>
<tr>
<td>Aluminum</td>
<td>4.9</td>
<td>28.7</td>
<td>Fair</td>
</tr>
<tr>
<td>Isomet</td>
<td>4.4</td>
<td></td>
<td>Poor</td>
</tr>
<tr>
<td>Gold silicon eutectic</td>
<td>6.2</td>
<td></td>
<td>Poor</td>
</tr>
<tr>
<td>Molybdenum</td>
<td>3.6</td>
<td>6.0</td>
<td>Good</td>
</tr>
<tr>
<td>Silicon</td>
<td>2.4</td>
<td>4.7</td>
<td>Good</td>
</tr>
<tr>
<td>Nickel</td>
<td>1.5</td>
<td>15.5</td>
<td>Good</td>
</tr>
<tr>
<td>Steel</td>
<td>1.2</td>
<td>15.0</td>
<td>Poor</td>
</tr>
<tr>
<td>Solder (Pb/Sn) 60/40</td>
<td>1.25</td>
<td></td>
<td>Poor</td>
</tr>
<tr>
<td>Epoxy, conductive</td>
<td>0.48</td>
<td>6.2</td>
<td>Poor</td>
</tr>
<tr>
<td>Kevlar</td>
<td>0.46</td>
<td></td>
<td>Poor</td>
</tr>
<tr>
<td>Alumina 96%</td>
<td>0.78</td>
<td>6.0</td>
<td>Poor</td>
</tr>
<tr>
<td>Epoxy, non-conductive</td>
<td>0.0276</td>
<td></td>
<td>Poor</td>
</tr>
<tr>
<td>Glass</td>
<td>0.026</td>
<td></td>
<td>Poor</td>
</tr>
</tbody>
</table>

Source: Dietterle, Robert E. "A 1kW Hybrid Thin-Film DC Switch." Proceedings of the 1976 International Microelectronics Symposium (October 1976):170-77, Table II.

$\Delta = W/IN^2 - ^\circ C/IN$

* - $IN/IN ^\circ C \times 10^{-6}$
<table>
<thead>
<tr>
<th>Material</th>
<th>Melting Temperature</th>
<th>Required Flux</th>
<th>Compatible Metalizations</th>
<th>Die Backing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gold/Tin</td>
<td>280°C</td>
<td>Nitrogen Atm. no flux</td>
<td>Tungsten, Nickel, Gold</td>
<td>Gold</td>
</tr>
<tr>
<td>Gold/Silicon</td>
<td>370°C</td>
<td>Nitrogen Atm. no flux</td>
<td>Tungsten, Nickel, Gold</td>
<td>Gold or Scrubbed Silicon</td>
</tr>
<tr>
<td>Lead/Tin</td>
<td>180°C</td>
<td>Rosin flux KL35/KL197</td>
<td>Tungsten, Nickel, Gold, and Copper</td>
<td>Chrome-Silver</td>
</tr>
<tr>
<td>Lead/Indium</td>
<td>180°C</td>
<td>Rosin flux KL35/KL197</td>
<td>Tungsten, Nickel, Gold</td>
<td>Chrome-Silver</td>
</tr>
<tr>
<td>Gold/Germanium</td>
<td>356°C</td>
<td>Nitrogen Atm. no flux</td>
<td>Tungsten, Nickel, Gold</td>
<td>Gold</td>
</tr>
<tr>
<td>Indium/Silver</td>
<td>230°C</td>
<td></td>
<td></td>
<td>Chrome-Silver</td>
</tr>
</tbody>
</table>

Thermal calculations - Manufacturer 1

The manufacturing techniques available by this manufacturer are discussed below. Dimensions for the material thickness were supplied by the manufacturer. The flow chart showing all the different material and bonding techniques is shown in figure 19. The thermal conduction model shown in figure 20 was developed as an aid in the calculation of the thermal resistance with the assumption that the heat flow diverges to approximately 45 degrees.

a) Die - The power darlington die are 2N6301 and 2N6299. Both are a square die whose dimensions are: .115"L x .115"W x .012"T

b) Die bond - Eutectic bonding is used to bond the die to the "molytab" which is coated with a layer of gold and dipped with either an N or P type material. This bond is controlled to a maximum thickness of 0.0005".

c) Molytab - Molybdenum material. Dimensions are .125"L x .125"W x .005"T.

d) Molytab bond - The molytab is solder bonded to the substrate using a solder paste. The material thickness is less than .004".
Fig. 19. Flow chart showing the different methods for the fabrication of the hybrid by Manufacturer 1.
Fig. 20. Thermal conduction model Manufacturer 1
e) Substrate
   i) Alumina - A 96% pure ceramic substrate is used whose thickness is 0.016" maximum.
   ii) Beryllia - A 99.5% pure beryllia substrate can be used whose thickness is 0.025" maximum.

f) Substrate bond
   i) Solder paste - (Sn 62 alloy) maximum thickness .004".
   ii) Non-conductive Maximum thickness .004".

   epoxy

g) Case
   i) Kovar - Maximum case thickness is .04".
   ii) Steel - Maximum case thickness is .04".

The technique that was used by this manufacturer was to eutectically bond the transistor die to the molytab and solder it to the substrate. The substrate was then soldered to the Kovar case. It should be noted that the case material was not left as an option on his part.
The resulting thermal impedance, $\Theta_{JA} = 5.04^\circ C/Watt$. The mathematical calculations can be found in Appendix 5. If the substrate had been epoxied to the case then the thermal impedance would have been more than double.

The maximum transistor junction temperature at an ambient temperature of 85°C will be:

$$T_J \left( ^\circ C \right) = T_{AMB} \left( ^\circ C \right) + \Theta_{JA} \left( ^\circ C/W \right) P_A \left( W \right)$$

$$T_J \left( ^\circ C \right) = 85^\circ C + \left( 5.04^\circ C/W \right) \left( 1.18W/2 \right) = 87.97^\circ C$$
Thermal Calculations - Manufacturer 2

The manufacturing techniques available by this manufacturer are similar to the other manufacturer and are discussed below. Dimensions for the material thickness were supplied by the manufacturer. The flow chart showing all the different material and bonding techniques is shown in figure 21. The thermal conduction model shown in figure 22 was developed as an aid in the calculation of the thermal resistance with the same assumption as before that the heat flow diverges to approximately 45 degrees.

a) Die

The power darlington die are 2N6301 and 2N6299. Both are a square die whose dimensions are:

.115"L x .115"W x .012"T.

b) Die bond

i) Epoxy - The die is bonded to the substrate using a conductive epoxy. The thickness of the bond is controlled to a maximum of .004".

ii) Eutectic - Later development lead to eutectic bonding with a maximum thickness of .002".

c) Substrate

i) Alumina - A 96% pure ceramic substrate is used
Die bond

- Epoxy \( \theta_{\text{EAi}} \)
- Eutectic \( \theta_{\text{EAii}} \)

Substrate

- Alumina \( \theta_{\text{AEi}} \)
- Beryllia \( \theta_{\text{AEii}} \)

Substrate bond

- Non-cond E. \( \theta_{\text{ECi}} \)
- Cond. Epoxy \( \theta_{\text{ECii}} \)
- Eutectic \( \theta_{\text{ECiii}} \)

Case

- Kovar \( \theta_{\text{CAi}} \)
- Steel \( \theta_{\text{CAii}} \)

Fig. 21. Flow chart showing the different methods for the fabrication of the hybrid by Manufacturer 2
Fig. 22. Thermal conduction model Manufacturer 2

- \( \theta_{JE} \) - Junction to Eutectic
- \( \theta_{EA} \) - Eutectic to Alumina
- \( \theta_{AE} \) - Alumina to Eutectic
- \( \theta_{EC} \) - Eutectic to Case
- \( \theta_{CA} \) - Case to Ambient
whose maximum thickness is .025".

ii) Beryllia - A 99.5% pure beryllia substrate is used whose maximum thickness is .025".

d) Substrate bond

i) Non-conductive Maximum thickness is .004".
   epoxy -

ii) Conductive Maximum thickness is .004".
   epoxy -

iii) Eutectic Maximum thickness is .002".

e) Case

i) Kovar - Maximum case thickness is .04".

ii) Steel - Maximum case thickness is .04".

The technique that was used by this manufacturer was to eutectically bond the transistor die to the substrate. The substrate was then eutectically bonded to the Kovar case. Similar to the other manufacturer, a Kovar case was specified. The resulting thermal impedance, 

\[ \Theta_{JA} = 5.12^\circ C/Watt \]

The mathematical calculations can be found in Appendix 6.

The maximum transistor junction temperature at an ambient temperature of 85°C will be:

\[
T_J \ (\circ C) = T_{AMB} \ (\circ C) + \Theta_{JA} \ (\circ C/W) \ P_A \ (W) \tag{87}
\]

\[
T_J \ (\circ C) = 85^\circ C + (5.12^\circ C/W)(1.18W/2) = 88 \ ^\circ C
\]
V. RESULTS AND EVALUATION

Thermal Resistance Measurement

Tests were performed on the hybrid to verify the thermal impedance calculations. Hybrids from each manufacturer were used in the measurements.

Wire bonds added to the hybrid for the tests were necessary because the case had no spare pins. The test set-ups are shown in figures 23 and 24. Measurement of the base-emitter voltage ($V_{BE}$) for a known power condition established the quiescent condition used as the reference. The power dissipation in the transistor was increased ten-fold and the change in the base-emitter voltage was noted. Based upon the change in $V_{BE}$ and the temperature coefficient ($\theta_v$, mV/°C), the junction temperature was calculated.

Verification of the test procedure was accomplished by noting the change in $V_{BE}$ as a function of temperature and comparing the results to the calculated rise in junction temperature. Secondly, discrete transistors subjected to the same test procedure were compared to the transistor manufacturer's predicted thermal resistance. Data was taken on four different hybrids (see Tables 5 and 6) and the thermal impedances were calculated as follows:
Fig. 23. Test set-up for measuring $\Theta_{JA}$ (NPN)

Fig. 24. Test set-up for measuring $\Theta_{JA}$ (PNP)
Sample Calculation

With the collector at ground potential

\[ I_L = \frac{V_{EE} - V_{BE}}{R_L} = \frac{20.040 - 1.3617}{62.579} = 0.298 \text{ Adc} \]  (88)

The transistor power dissipation is calculated as follows:

\[ P_{QL} = I_L V_{BE} = (0.298 \text{ Adc})(1.3617 \text{ Vdc}) = 0.406 \text{ Watts} \]  (89)

With the collector at +10 Vdc

\[ V_{BE} = -1.18 \text{ Vdc} \]

\[ \Delta V_{BE} = (1.368 - 1.18) \text{ Vdc} = 0.1817 \text{ Vdc} \]

The transistor manufacturer specifies the temperature coefficient \( \theta_V = 3.8 \text{ mV/°C} \); therefore,

\[ \Delta T_J = \frac{\Delta V_{BE}}{\theta_V} = \frac{0.1817 \text{ Vdc}}{3.8 \text{ mV/°C}} = 47.82°\text{C} \]  (90)

The transistor power dissipation is now

\[ P_{QL} = I_L (V_{CC} - V_{BE}) = (0.298 \text{ Adc})(10 - (-1.18)) = 3.33 \text{ Watts} \]  (91)

The thermal resistance for the hybrid is determined using the following equation:

\[ T_J = \theta_{JA} (°C/W) P_Q (W) \]  (92)

\[ \theta_{JA} (°C/W) = \frac{\Delta T_J (°C)}{\Theta_P (°C/W)} = \frac{47.82°\text{C}}{(3.33 - 0.406) \text{W}} = 16.31 (°C/W) \]  (93)
<table>
<thead>
<tr>
<th>Test Number</th>
<th>Mfg.</th>
<th>$V_{BE}$ Volts Measured</th>
<th>Collector Potential</th>
<th>$\Theta_{JC}$ °C/W Calculated</th>
<th>$\Theta_{JC}$ °C/W Measured</th>
<th>Transistor Type</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>-1.3617</td>
<td>Gnd</td>
<td>13.12</td>
<td>16.31</td>
<td>NPN</td>
<td>Proto-type</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>-1.1800, 1.4060</td>
<td>Gnd</td>
<td>13.12, 13.12</td>
<td>15.82, 15.82</td>
<td>PNP</td>
<td>Proto-type</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>-1.382, 1.2162</td>
<td>Gnd</td>
<td>5.31, 5.31</td>
<td>6.45, 6.45</td>
<td>NPN</td>
<td>Production</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>-1.309, 1.374</td>
<td>Gnd</td>
<td>5.31, 5.31</td>
<td>7.15, 7.15</td>
<td>PNP</td>
<td>Production</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>-1.368, 1.2652</td>
<td>Gnd</td>
<td>6.24, 6.24</td>
<td>9.16, 9.16</td>
<td>NPN</td>
<td>Proto-type</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>1.4060, 1.2162</td>
<td>Gnd</td>
<td>6.24, 6.24</td>
<td>7.9, 7.9</td>
<td>PNP</td>
<td>Proto-type</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>-1.366, 1.287</td>
<td>Gnd</td>
<td>5.12, 5.12</td>
<td>6.97, 6.97</td>
<td>NPN</td>
<td>Production</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>-1.392, 1.317</td>
<td>Gnd</td>
<td>5.12, 5.12</td>
<td>6.63, 6.63</td>
<td>PNP</td>
<td>Production</td>
</tr>
<tr>
<td>9</td>
<td>Motorola</td>
<td>-1.311</td>
<td>Gnd</td>
<td>2.33</td>
<td>3.74</td>
<td>NPN</td>
<td>TO-66</td>
</tr>
<tr>
<td>10</td>
<td>Motorola</td>
<td>-1.27</td>
<td>+10V</td>
<td>2.33</td>
<td>4.4</td>
<td>PNP</td>
<td>TO-66</td>
</tr>
<tr>
<td>Temperature (°C)</td>
<td>Duration (Minutes)</td>
<td>$V_{BE}$ (Volts)</td>
<td>Load</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------------</td>
<td>-------------------</td>
<td>-----------------</td>
<td>-------</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>0</td>
<td>-1.2464</td>
<td>62.579</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>2</td>
<td>-1.1800</td>
<td>62.579</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>5</td>
<td>-1.1708</td>
<td>62.579</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>20</td>
<td>-1.1590</td>
<td>62.579</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Test performed with the collector at ground potential. Temperature was allowed to settle for 15 minutes before the measurements were taken.
The transistor was then subjected to temperature testing (see Table 6 for data). As the sample calculation shows the NPN transistor when the power dissipation was increased, the change in $V_{BE}$ reflects 48°C junction temperature rise. Therefore, if the ambient temperature were raised by 48°C, the expected $V_{BE}$ should be the same as when the power was increased. At 80°C, the measured voltage $V_{BE}$ was 1.18 VDC which verifies the technique.

Secondly, using the assumption that the base-emitter voltage changes with temperature by 3.8mV/°C will show a change in $V_{BE}$ for the 55°C rise equal to 0.209 volts. Therefore, the predicted voltage for the base-emitter is 1.153 volts.

It was found that after twenty minutes the voltage measured was 1.159 volts. This again verified the technique.

The differences in the predicted thermal impedance to that measured can be easily explained.

For Manufacturer 1, the substrate was epoxied to the case causing high thermal impedances. A 0.001 inch variation in thickness increases the thermal impedance by 2°C/watt. Typical material thickness is 0.004 inches. In the production hybrid, the substrate is soldered to the case lowering the thermal impedance. Due to the variation in this junction, slight differences in the thermal
impedances are expected.

The prototype supplied by Manufacturer 2 was not too different from the production hybrid. The transistor die was bonded to the substrate with conductive epoxy. The final version was eutectically bonded to the substrate, yielding a lower thermal impedance.
Gain Accuracy

Gain tests were performed on the hybrid at different temperatures to verify compliance with the specification. The temperature range was from -55° to +125°C. The hybrids not only met the requirements, but in most cases they exceeded them.
Closed Loop Frequency Response

The closed loop frequency response was performed on the prototype hybrid. Figure 25 is a plot of the frequency response. A simulated load was used in place of the synchro load. There was excellent correlation between the measured and calculated frequency responses.
Fig. 25. Measured closed-loop response
VI. CONCLUSIONS AND RECOMMENDATIONS

The hybrid microcircuits reduced the total weight of the card assembly more than ten-fold and also provided space for an additional card assembly. Precautions were necessary in the system to ensure that adequate heat transfer was provided.

The hybrid case that was chosen (standard product) created several problems because of the different size pins and lead spacing. A special connector had to be constructed for testing and care had to be exercised in the system wiring of the smaller case pins.

Minimization of the thermal impedance was not obtained in this design due to the restrictions imposed on both manufacturers (e.g., the case material). This was proven in both the calculations and measurements of the thermal impedance.

Discrepancies in the calculated and measured impedances can be contributed to variations in the thickness of the bonding materials, substrate and the case bottom.

Thermal impedances with less than 2°C/Watt can be obtained with the use of a beryllia substrate and a steel case. If the steel case is eliminated and the beryllia
substrate is used for the case as well as the substrate, then the thermal impedance will be further reduced to approximately 1°C/Watt. This technique will be used in future orders. Also, the case pin configuration will be changed to that of uniform spacing and the same size pins.

The power amplifiers exceeded all the system requirements and the accuracies that were obtained will allow more uses of the hybrid in future applications.
APPENDIX 1

Calculation for the Minimum Beta

To compute the minimum beta at -65°C using the transistor specifications:

**Q1:** \( \beta_G > 750 \) at 4A, 25°C   Guaranteed minimum
\[
\begin{align*}
\beta_{T1} & \geq 3200 \text{ at } 4A, 25°C \quad \text{Typical} \\
\beta_{T2} & \geq 3200 \text{ at } 1A, 25°C \quad \text{Typical} \\
\beta_{T3} & \geq 1600 \text{ at } 1A, -55°C \quad \text{Typical}
\end{align*}
\]

\[
\beta_1 > \beta_G (\beta_{T2}/\beta_{T1}) = 750 \times \frac{3200}{3200} = 750 \text{ at } 1A, 25°C \quad (94)
\]

\[
\beta_2 > \beta_1 (\beta_{T3}/\beta_{T2}) = 750 \times \frac{1600}{3200} = 375 \text{ at } 1A, -55°C \quad (95)
\]

\[
\beta > \beta_1 - (\beta_1 - \beta_2)(25°C - (-65°C))/(25°C - (-55°C)) \quad (96)
\]

\[
\beta = 750 - (750 - 375)(90°C/80°C) \quad (97)
\]

\[
\beta = 328 \text{ at } 1A, -65°C \quad (2N6301) \quad (98)
\]

**Q2:** \( \beta_G > 750 \) at 4A, 25°C   Guaranteed minimum
\[
\begin{align*}
\beta_{T1} & \geq 2500 \text{ at } 4A, 25°C \quad \text{Typical} \\
\beta_{T2} & \geq 3500 \text{ at } 1A, 25°C \quad \text{Typical} \\
\beta_{T3} & \geq 1500 \text{ at } 1A, -55°C \quad \text{Typical}
\end{align*}
\]

\[
\beta_1 > \beta_G (\beta_{T2}/\beta_{T1}) = 750 \times \frac{3500}{2500} = 1050 \text{ at } 1A, 25°C \quad (99)
\]

\[
\beta_2 > \beta_1 (\beta_{T3}/\beta_{T2}) = 1050 \times \frac{1500}{3500} = 450 \text{ at } 1A, -55°C \quad (100)
\]

\[
\beta > \beta_1 - (\beta_1 - \beta_2)(25°C - (-65°C))/(25°C - (-55°C)) \quad (101)
\]

\[
\beta = 1050 - (1050 - 450)(90°C/80°C) \quad (102)
\]

\[
\beta = 375 \text{ at } 1A, -65°C \quad (2N6299)
\]
APPENDIX 2

Average Voltage of 3 Phase Unfiltered Power Supply

\[ E_{AV} = \frac{1}{\pi} \int_{\alpha}^{\alpha+\pi} E_s(\omega t) \, d(\omega t) \]  \hspace{1cm} (103)

The above integral can be broken into parts. See figure 10 for the voltage waveform.

\[ E_{AV} = \frac{1}{\pi} \left\{ \int_{\alpha}^{\pi-\alpha} E_{s1} \sin(\omega t) \, d(\omega t) + \int_{\pi-\alpha}^{\pi} E_{s2} \sin(\omega t - \pi) \frac{d(\omega t)}{3} \right\} \]

\[ + \int_{\pi}^{\alpha+\pi} E_{s2} \sin(\omega t - 2\pi \frac{3}{3}) \, d(\omega t) \} \]

\[ = -\frac{1}{\pi} \left\{ E_{s1} \left[ \cos(\omega t) \right]_{\alpha}^{\pi-\alpha} + E_{s2} \left[ \cos(\omega t - \pi) \frac{3}{3} \right]_{\pi-\alpha}^{\pi} \right. \]

\[ + E_{s2} \left[ \cos(\omega t - 2\pi \frac{3}{3}) \right]_{\pi}^{\alpha+\pi} \} \]  \hspace{1cm} (104)

\[ E_{AV} = -\frac{1}{\pi} \left\{ E_{s1} \left[ \cos(\pi - \alpha) - \cos\alpha \right] \right. \]

\[ + E_{s2} \left[ \cos(\pi - \pi \frac{3}{3}) - \cos(\pi - \alpha - \pi \frac{3}{3}) \right] \]

\[ + E_{s2} \left[ \cos(\alpha + \pi - \pi \frac{3}{3}) - \cos(\pi - 2\pi \frac{3}{3}) \right] \} \]  \hspace{1cm} (105)
Inserting typical values into equation 106 where, \( E_{s1} = 23 \text{V} \); \( E_{s2} = 12.5 \text{V} \) and \( \alpha = 32.9^\circ \). Then, \( E_{AV} = 16.67 \text{V} \).
APPENDIX 3

Derivation of the Integral Equation

\[ I = \int \sin(A-B)\sin(A-C) \]  \hspace{1cm} (107)

Applying the angle-difference relationships,

\[ \sin(A-B) = -\cos A \sin B + \sin A \cos B \]  \hspace{1cm} (108)
\[ \sin(A-C) = -\cos A \sin C + \sin A \cos C \]  \hspace{1cm} (109)

multiplying equations and

\[ \sin(A-B)\sin(A-C) = \cos^2 A \sin B \sin C - \sin A \cos A \sin B \cos C \]
\[ - \sin A \cos A \sin C \cos B + \sin^2 A \cos B \cos C \]  \hspace{1cm} (110)

\[ = \sin B \sin C \cos^2 A + \cos B \cos C \sin^2 A \]
\[ - (\sin B \cos C + \cos B \sin C) \sin A \cos A \]  \hspace{1cm} (111)

Note that: \( \sin B \cos C + \cos B \sin C = \sin(B+C) \) \hspace{1cm} (112)
and \( \sin A \cos A = \frac{1}{2} \sin 2A \) \hspace{1cm} (113)

\[ I = \sin B \sin C \int \cos^2 A \, dA - \frac{1}{2} \sin(B+C) \int \sin 2A \, dA \]

\[ + \cos B \cos C \int \sin^2 A \, dA \]  \hspace{1cm} (114)

Let

\[ I_1 = \int \cos^2 A \, dA = \frac{A}{2} + \frac{1}{4} \sin 2A \]  \hspace{1cm} (115)
\[ I_2 = \int \sin 2A \, dA = -\frac{1}{2} \cos 2A \]  
\hspace{1cm} (116)

and

\[ I_3 = \int \sin^2 A \, dA = \frac{A}{2} - \frac{1}{4} \sin 2A \]  
\hspace{1cm} (117)

then,

\[ I = \sin B \sin C \left( I_1 \right) + \frac{1}{2} \sin (B+C) \left( -I_2 \right) + \cos B \cos C \left( I_3 \right) \]  
\hspace{1cm} (118)

\[ = \frac{1}{4} \sin 2A (\sin B \sin C - \cos B \cos C) + \frac{1}{4} \sin (B+C) \cos 2A \]  
\[ + \frac{A}{2} \left( \sin B \sin C + \cos B \cos C \right) \]  
\hspace{1cm} (119)

\[ = \frac{1}{4} \sin (B+C) \cos 2A + \frac{1}{4} \cos (B+C) \sin 2A + \frac{A}{2} \cos (B-C) \]  
\hspace{1cm} (120)

\[ I = \frac{1}{4} \sin (B+C-2A) + \frac{A}{2} \cos (B-C) \]  
\hspace{1cm} (121)

Therefore,

\[ \int \sin(A-B) \sin(A-C) = \frac{1}{4} \sin(B+C-2A) + \frac{A}{2} \cos(B-C) \]  
\hspace{1cm} (122)
APPENDIX 4

Amplifier Power Dissipation for
Conventional Current Limiting

3 Phase Supply

The current waveform shown in figure 26 is assumed to be a rectangular pulse. The power dissipation in the amplifier output stage, \( P_{ACL} \), is defined as:

\[
P_{ACL} = \frac{1}{123} \int_{\phi}^{\phi+\pi} E_s(\omega t) I_{CL} \, dt
\]  

The integral can be broken into parts before integrating equation 123.

\[
P_{ACL} = \frac{I_{CL}}{\pi} \left\{ \int_{\phi}^{\pi-\alpha} E_{s1} \sin \omega t \, dt + \int_{\pi-\alpha}^{\pi} E_{s2} \sin(\omega t - \pi) \, dt \right. \\
+ \int_{\pi}^{\pi+\alpha} E_{s2} \sin(\omega t - 2\pi) \, dt + \int_{\pi-\alpha}^{\phi+\pi} E_{s1} \sin(\omega t - \pi) \, dt \\
- \int_{\phi}^{\pi+\phi} E_0 \sin \omega t \, dt \right\}
\]

\[
= \frac{I_{CL}}{\pi} \left\{ E_{s1} \cos \omega t \left|_{\phi}^{\pi-\alpha} + E_{s2} \cos(\omega t - \pi) \right|_{\phi}^{\pi-\alpha} \right. \\
\left. + E_{s2} \cos(\omega t - 2\pi) \right|_{\pi}^{\pi+\alpha} + E_{s1} \cos(\omega t - \pi) \right|_{\pi+\alpha}^{\phi+\pi} - E_0 \cos \omega t \right|_{\pi+\phi}^{\phi} \right\}
\]

\[
= \left\{ \begin{array}{c}
E_{s1} \cos \omega t \left|_{\phi}^{\pi-\alpha} + E_{s2} \cos(\omega t - \pi) \right|_{\phi}^{\pi-\alpha} \right. \\
\left. + E_{s2} \cos(\omega t - 2\pi) \right|_{\pi}^{\pi+\alpha} + E_{s1} \cos(\omega t - \pi) \right|_{\pi+\alpha}^{\phi+\pi} - E_0 \cos \omega t \right|_{\pi+\phi}^{\phi} \right\}
\]
Fig. 26. Current limit waveform
Inserting typical values into equation 125
where, $E_{s1} = 23V$; $E_{s2} = 12.5V$; $\alpha = 32.9^\circ$; $\phi = 79^\circ$;
and $I_{CL} = 2.6A$, the power dissipation in the amplifier
is 43.36 Watts.
Thermal Calculations for Manufacturer 1

a) Die

\[ JE = \frac{x}{K(a+2x)} = \frac{0.012''}{(2.4W/^\circ C-IN)(.091'')(.091''+2(.012''))} \]

\[ JE = 0.4778 \, ^\circ C/W \]

b) Die bond

\[ EM = \frac{x}{K^{2}} = \frac{0.005''}{(5.76W/^\circ C-IN)(.115'')^{2}} \]

\[ EM = 0.0066 \, ^\circ C/W \]

c) Molytab

\[ ME = \frac{x}{K(a+2x)} = \frac{0.005''}{(3.4W/^\circ C-IN)(.115'')(.115''+2(.005''))} \]

\[ ME = 0.0118 \, ^\circ C/W \]

d) Molytab bond

\[ EA = \frac{x}{K^{2}} = \frac{0.004''}{(1.25W/^\circ C-IN)(.125'')^{2}} \]

\[ EA = 0.205 \, ^\circ C/W \]

e) Substrate

i) Alumina

\[ AEi = \frac{x}{K(a+2x)} = \frac{0.016''}{(.78W/^\circ C-IN)(.125'')(.125''+2(.016''))} \]

\[ AEi = 1.045 \, ^\circ C/W \]

ii) Beryllia

\[ AEii = \frac{x}{K(a+2x)} = \frac{0.025''}{(6.0W/^\circ C-IN)(.125'')(.125''+2(.025''))} \]

\[ AEii = 0.1905 \, ^\circ C/W \]

87
f) Substrate bond

i) Solder - Alumina substrate

$$\theta_{ECiA} = \frac{x}{k_A} = \frac{0.004''}{(1.25\text{W/°C-IN})(.157'')}^2 = 0.1298 \text{ °C/W}$$

Solder - Beryllia substrate

$$\theta_{ECiB} = \frac{x}{k_A} = \frac{0.004''}{(1.25\text{W/°C-IN})(.175'')}^2 = 0.1045 \text{ °C/W}$$

ii) Epoxy - Alumina substrate

$$\theta_{ECiiA} = \frac{x}{k_A} = \frac{0.004''}{(.0276\text{W/°C-IN})(.157'')}^2 = 5.98 \text{ °C/W}$$

Epoxy - Beryllia substrate

$$\theta_{ECiiB} = \frac{x}{k_A} = \frac{0.004''}{(.0276\text{W/°C-IN})(.157'')}^2 = 4.732 \text{ °C/W}$$

g) Case

i) Kovar - Alumina substrate

$$\theta_{CAiA} = \frac{x}{k_a(a+2x)} = \frac{0.04''}{(.34\text{W/°C-IN})(.157'')(.157''+2(.04''))} = 3.162 \text{ °C/W}$$

Kovar - Beryllia substrate

$$\theta_{CAiB} = \frac{x}{k_a(a+2x)} = \frac{0.04''}{(.34\text{W/°C-IN})(.175'')(.175''+2(.04''))} = 2.636 \text{ °C/W}$$

ii) Steel - Alumina substrate

$$\theta_{CAiiA} = \frac{x}{k_a(a+2x)} = \frac{0.04''}{(1.2\text{W/°C-IN})(.157'')(.157''+2(.04''))} = 0.8958 \text{ °C/W}$$
Steel - Beryllia substrate

\[ \Theta_{CAiiB} = \frac{x}{K_{a}(a+2x)} = \frac{.04"}{(1.2W/^\circ C-IN)\times(1.175")\times(1.175"+2\times.04")} \]

\[ \Theta_{CAiiB} = .747 \text{ °C/W} \]

The thermal impedance is therefore,

\[ \Theta_{JA} = \Theta_{JE} + \Theta_{EM} + \Theta_{ME} + \Theta_{EA} + \Theta_{AEi} + \Theta_{ECiA} + \Theta_{CAiiB} \]

\[ \Theta_{JA} = .4778 + .0066 + .0118 + .205 + 1.045 + .1298 + 3.163 \]

\[ \Theta_{JA} = 5.04 \text{ °C/W} \]
APPENDIX 6

Thermal Calculations for Manufacturer 2

a) Die

\[ \theta_{JE} = \frac{x}{K_a(a+2x)} = \frac{0.012''}{(2.4W/^\circ C-IN)(.091'')(.091''+2(.012''))} \]

\[ \theta_{JE} = 0.4778 ^\circ C/W \]

b) Die bond

i) Epoxy

\[ \theta_{EAi} = \frac{x}{K_A} = \frac{.004''}{(.48W/^\circ C-IN)(.115'')^2} = 0.63 ^\circ C/W \]

ii) Eutectic

\[ \theta_{EAii} = \frac{x}{K_A} = \frac{.002''}{(5.76W/^\circ C-IN)(.115'')^2} = 0.0263 ^\circ C/W \]

c) Substrate

i) Alumina

\[ \theta_{AEi} = \frac{x}{K_a(a+2x)} = \frac{.025''}{(2.78W/^\circ C-IN)(.115'')(.115''+2(.025''))} \]

\[ \theta_{AEi} = 1.689 ^\circ C/W \]

ii) Beryllia

\[ \theta_{AEii} = \frac{x}{K_a(a+2x)} = \frac{.025''}{(6.0W/^\circ C-IN)(.115'')(.115''+2(.025''))} \]

\[ \theta_{AEii} = 0.2196 ^\circ C/W \]

d) Substrate bond

i) Non-conductive epoxy

\[ \theta_{ECi} = \frac{x}{K_A} = \frac{.004''}{(.0276W/^\circ C-IN)(.165'')^2} = 5.323 ^\circ C/W \]
ii) Conductive epoxy

\[ \theta_{ECii} = \frac{x}{KA} = \frac{.004''}{(.48W/^\circ C\cdot IN)(.165'')^2} = 0.3061 \, ^\circ C/W \]

iii) Eutectic

\[ \theta_{ECiii} = \frac{x}{KA} = \frac{.004''}{(5.76W/^\circ C\cdot IN)(.165'')^2} = 0.0128 \, ^\circ C/W \]

e) Case

i) Kovar

\[ \theta_{CAi} = \frac{x}{Ka(a+2x)} = \frac{.04''}{(.34W/^\circ C\cdot IN)(.165'')((.165''+2(.04''))} \]
\[ \theta_{CAi} = 2.91 \, ^\circ C/W \]

ii) Steel

\[ \theta_{CAii} = \frac{x}{Ka(a+2x)} = \frac{.04''}{(1.2W/^\circ C\cdot IN)(.165'')((.165''+2(.04''))} \]
\[ \theta_{CAii} = 0.825 \, ^\circ C/W \]

The thermal impedance is therefore,

\[ \theta_{JA} = \theta_{JE} + \theta_{EAii} + \theta_{AEi} + \theta_{ECiii} + \theta_{CAi} \]

\[ \theta_{JA} = .4778 + .0263 + 1.689 + .0128 + 2.91 \]
\[ \theta_{JA} = 5.12 \, ^\circ C/W \]
REFERENCES


