Analysis And Design Of A Modular Solar-fed Fault-tolerant Power System With Maximum Power Point Tracking

2005

Hussam Al-Atrash

University of Central Florida

Find similar works at: http://stars.library.ucf.edu/etd

University of Central Florida Libraries http://library.ucf.edu

Part of the Electrical and Electronics Commons

STARS Citation

http://stars.library.ucf.edu/etd/272

This Masters Thesis (Open Access) is brought to you for free and open access by STARS. It has been accepted for inclusion in Electronic Theses and Dissertations by an authorized administrator of STARS. For more information, please contact lee.dotson@ucf.edu.
ANALYSIS AND DESIGN OF A MODULAR SOLAR-FED FAULT-TOLERANT POWER SYSTEM WITH MAXIMUM POWER POINT TRACKING

by

HUSSAM J. AL-ATRASH
B. S. University of Jordan, 2003

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the Department of Electrical and Computer Engineering in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

Spring Term
2005
© 2005 Hussam J. Al-Atrash
ABSTRACT

Solar power is becoming ever more popular in a variety of applications. It is particularly attractive because of its abundance, renewability, and environment friendliness. Solar powered spacecraft systems have ever-expanding loads with stringent power regulation specifications. Moreover, they require a light and compact design of their power system. These constraints make the optimization of power harvest from solar arrays a critical task.

Florida Power Electronics Center (FPEC) at UCF set to develop a modular fault-tolerant power system architecture for space applications. This architecture provides a number of very attractive features including Maximum Power Point Tracking (MPPT) and uniform power stress distribution across the system.

MPPT is a control technique that leads the system to operate its solar sources at the point where they provide maximum power. This point constantly moves following changes in ambient operating conditions. A digital controller is setup to locate it in real time while optimizing other operating parameters. This control scheme can increase the energy yield of the system by up to 45%, and thus significantly reduces the size and weight of the designed system.

The modularity of the system makes it easy to prototype and expand. It boosts its reliability and allows on-line reconfiguration and maintenance, thus reducing down-time upon faults.

This thesis targets the analysis and optimization of this architecture. A new modeling technique is introduced for MPPT in practical environments, and a novel digital power stress distribution scheme is proposed in order to properly distribute peak and thermal stress and improve reliability.
A 2kW four-channel prototype of the system was built and tested. Experimental results confirm the theoretical improvements, and promise great success in the field.
To the minds that dream,
the hands that build,
and the hearts that give.

To the homeland, for her everlasting grace...
ACKNOWLEDGEMENT

I wish to express deep gratitude to all people and firms that contributed to the work presented in this thesis. Particularly, I thank my advisor, Dr. Issa Batarseh, for his numerous discussions and unwavering support and guidance, Drs. Kasemsan Siri and Peter Kornetzky for their enlightening technical observations and suggestions, and Drs. Takis Kasparis, Chris Ianello and Murad Qahwash for serving on my committee and providing helpful comments.

I am deeply debited to all the team members from ApECOR and UCF that made the completion of the project possible: Khalid Rustom, Nattorn Pongratananukul, Feng Tian, Yangyang Wen, and Adje Mensah.

Hussam Al-Atrash

March 2005
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter / Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABSTRACT</td>
<td>iii</td>
</tr>
<tr>
<td>ACKNOWLEDGEMENT</td>
<td>vi</td>
</tr>
<tr>
<td>TABLE OF CONTENTS</td>
<td>vii</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>xi</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>xv</td>
</tr>
<tr>
<td>CHAPTER 1: INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>Solar cell structure and characteristics</td>
<td>1</td>
</tr>
<tr>
<td>Power harvesting efficiency ((P_o/P_{sun}))</td>
<td>3</td>
</tr>
<tr>
<td>Power system architectures</td>
<td>4</td>
</tr>
<tr>
<td>Load types</td>
<td>4</td>
</tr>
<tr>
<td>Topology options</td>
<td>5</td>
</tr>
<tr>
<td>MPPT</td>
<td>6</td>
</tr>
<tr>
<td>System reliability</td>
<td>7</td>
</tr>
<tr>
<td>Fault tolerance</td>
<td>7</td>
</tr>
<tr>
<td>Modular architectures</td>
<td>8</td>
</tr>
<tr>
<td>Uniform power stress distribution</td>
<td>8</td>
</tr>
<tr>
<td>Research objectives</td>
<td>9</td>
</tr>
<tr>
<td>Thesis outline</td>
<td>9</td>
</tr>
<tr>
<td>CHAPTER 2: OVERVIEW OF SOLAR POWER HARVESTING TECHNIQUES AND SYSTEMS</td>
<td>11</td>
</tr>
<tr>
<td>Introduction</td>
<td>11</td>
</tr>
<tr>
<td>System architecture</td>
<td>11</td>
</tr>
<tr>
<td>Section</td>
<td>Page</td>
</tr>
<tr>
<td>------------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>The Digital Controller</td>
<td>47</td>
</tr>
<tr>
<td>The Controller Area Network (CAN) Bus</td>
<td>48</td>
</tr>
<tr>
<td>Maximum Power Point Tracking</td>
<td>49</td>
</tr>
<tr>
<td>Experimental Results</td>
<td>52</td>
</tr>
<tr>
<td>Parallel Channel Operation</td>
<td>53</td>
</tr>
<tr>
<td><strong>CHAPTER 4: STATISTICAL NATURE OF HILL-CLIMBING MPPT ALGORITHMS</strong></td>
<td>55</td>
</tr>
<tr>
<td>Statistical Equilibrium at the MPP</td>
<td>55</td>
</tr>
<tr>
<td>Effect of Noise</td>
<td>56</td>
</tr>
<tr>
<td>Spiky noise in voltage measurements</td>
<td>57</td>
</tr>
<tr>
<td>Quantization noise in current measurements</td>
<td>58</td>
</tr>
<tr>
<td>Statistical Modeling of MPPT Operation in a Noisy Environment</td>
<td>58</td>
</tr>
<tr>
<td>Noisy voltage measurement ($n_i=0$)</td>
<td>60</td>
</tr>
<tr>
<td>Noisy current measurement ($n_i=0$)</td>
<td>62</td>
</tr>
<tr>
<td>Noisy voltage and current measurements</td>
<td>63</td>
</tr>
<tr>
<td>Effect of Noise on Steady-State Tracking as Predicted by the Statistical Model</td>
<td>64</td>
</tr>
<tr>
<td>Effect of voltage measurement noise</td>
<td>66</td>
</tr>
<tr>
<td>Effect of current measurement noise</td>
<td>68</td>
</tr>
<tr>
<td>Effect of measurement noise in both signals</td>
<td>69</td>
</tr>
<tr>
<td>Noisy System Simulation</td>
<td>71</td>
</tr>
<tr>
<td>Voltage noise vs. current noise</td>
<td>73</td>
</tr>
<tr>
<td>Statistical model verification</td>
<td>77</td>
</tr>
<tr>
<td>Digital filtering enhancement</td>
<td>81</td>
</tr>
</tbody>
</table>
LIST OF FIGURES

Figure 1-1 Typical terminal characteristics of a solar array (a) irradiance variations (b) temperature variations......................................................................................................................... 2

Figure 2-1 Resistive loading of the solar array............................................................................................................ 12

Figure 2-2 Constant power loading of the solar array.................................................................................................. 13

Figure 2-3 Unregulated bus topology......................................................................................................................... 14

Figure 2-4 Regulated bus topology.......................................................................................................................... 16

Figure 2-5 Battery dominated MPPT bus topology.................................................................................................. 17

Figure 2-6 Modular MPPT-enabled architecture......................................................................................................... 19

Figure 2-7 Current-mode control............................................................................................................................ 21

Figure 2-8 Basic flowchart of the PnO algorithm........................................................................................................ 27

Figure 2-9 Basic flowchart of the IncCond algorithm.................................................................................................. 29

Figure 2-10 Voltage regulation schemes (a) tight regulation (b) programmed droop ............................................. 32

Figure 2-11 Current sharing control structures (a) outer-loop regulation (b) inner-loop regulation (c) Dual-loop regulation.......................................................................................................................... 34

Figure 2-12 Typical current sharing bus configurations............................................................................................... 36

Figure 3-1 Modular system architecture.................................................................................................................. 37

Figure 3-2 Typical terminal characteristics of a solar cell.......................................................................................... 39

Figure 3-3 Electrical model of a solar cell................................................................................................................ 40

Figure 3-4 Configuration of solar cells in an array....................................................................................................... 42

Figure 3-5 Typical characteristics of the constructed solar arrays........................................................................... 43

Figure 3-6 Solar powered channel structure............................................................................................................. 45

Figure 3-7 Basic PnO algorithm............................................................................................................................... 49
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-22</td>
<td>Discarded regions when using a hysteresis window on the (a) LHS (b) RHS and the di/dv test on the (c) LHS (d) RHS</td>
</tr>
<tr>
<td>4-23</td>
<td>Experimental MPPT results (a) P-V curve (b) basic PnO (c) with dv hysteresis (d) with di/dv test (e) with analog LPF for voltage signal (f) with digital filters</td>
</tr>
<tr>
<td>5-1</td>
<td>Block diagram of a single solar channel with MPPT</td>
</tr>
<tr>
<td>5-2</td>
<td>Dc Output characteristics of a solar powered channel with MPPT</td>
</tr>
<tr>
<td>5-3</td>
<td>Scalable solar-powered system model</td>
</tr>
<tr>
<td>5-4</td>
<td>Power stress distribution among channels in the system</td>
</tr>
<tr>
<td>5-5</td>
<td>Controller model of the parallel-pin based current sharing algorithm</td>
</tr>
<tr>
<td>5-6</td>
<td>Output characteristics with the OVR_MOD function</td>
</tr>
<tr>
<td>5-7</td>
<td>Current distribution among two channels in OVR</td>
</tr>
<tr>
<td>5-8</td>
<td>Controller model of the trim-pin based current sharing algorithm</td>
</tr>
<tr>
<td>5-9</td>
<td>OVR_MOD hardware setup</td>
</tr>
<tr>
<td>5-10</td>
<td>Trimmed and untrimmed output voltage values</td>
</tr>
<tr>
<td>5-11</td>
<td>Control flow of a system with trim-based current sharing</td>
</tr>
<tr>
<td>5-12</td>
<td>Current distribution model</td>
</tr>
<tr>
<td>5-13</td>
<td>OVR_MOD circuitry with programmed $R_o$</td>
</tr>
<tr>
<td>5-14</td>
<td>Overall system simulation model</td>
</tr>
<tr>
<td>5-15</td>
<td>Capacitive constant current simulation model</td>
</tr>
<tr>
<td>5-16</td>
<td>Single PV powered channel simulation model</td>
</tr>
<tr>
<td>5-17</td>
<td>Solar array simulation model</td>
</tr>
<tr>
<td>5-18</td>
<td>Converter simulation model</td>
</tr>
<tr>
<td>5-19</td>
<td>Input voltage regulator model</td>
</tr>
</tbody>
</table>
Figure 5-20 Output voltage regulator model with OVR_MOD and output droop ............... 112
Figure 5-21 Digital controller simulation model ......................................................... 113
Figure 5-22 Perturb and Observe algorithm simulation model ................................. 114
Figure 5-23 OVR mode detector model ..................................................................... 114
Figure 5-24 Current sharing algorithm simulation model ........................................... 115
Figure 5-25 Simulation results for the four channel system with trim-based current sharing .... 115
Figure 5-26 Experimental prototype ........................................................................... 117
Figure 5-27 Experimental results for a two channel system ....................................... 117
Figure 5-28 Experimental results for a four-channel system ...................................... 119
LIST OF TABLES

Table 2-1: Application-specific considerations affecting MPPT algorithm choice..................... 22
CHAPTER 1: INTRODUCTION

Solar power is gaining increasing attention as a power alternative for the 21st century. In addition to being abundant and renewable, solar power is particularly attractive because of its clean, environment-friendly nature. Its use, however, has been limited in commercial applications due to the high initial cost of solar systems, as well as the low conversion efficiency of state-of-the-art solar modules. The feasibility of solar systems has been further limited by the fluctuating nature of the source, and the low reliability of associated power conversion systems.

In order to deliver the great advantages of solar power to the new century, the designers of such systems face the challenges of significantly increasing the overall reliability and conversion efficiency of solar harvesting systems.

For space applications, photovoltaic arrays have long been the most popular sources for energizing satellites and space exploration missions. The reliance of the space industry on such sources has accelerated research directed at solar energy. The designers of terrestrial solar systems can largely benefit from the experience accumulated by their peers in the aerospace industry.

Solar cell structure and characteristics

Solar cells are semiconductor device that are capable of producing voltage and associated current when exposed to sunlight. They show highly nonlinear terminal voltage-current characteristics that are dependent on multiple factors. Cells are connected in series and parallel to produce solar arrays of different voltage and current ratings. These arrays are then used as power sources for different systems. Typical terminal characteristics of a solar array at different operating conditions are shown in the Fig. 1-1 below.
Ambient operating conditions have a significant effect on the cell characteristics. Most important of those, intuitively, is the amount of irradiance incident on the surface of the cell. Irradiance is commonly measured as the average power incident per unit area. Bright sunlight perpendicular to a cell surface placed on the face of the earth has typical irradiance of 1000W/m². Temperature is another key player. Higher temperature decreases the energy yield of a solar cell.

There are two main operating regions for a solar array. The right hand side (RHS) is the region where the current drawn is fairly small, and the operating voltage is relatively constant. Within this region, the power delivered increases with the current and decreases with voltage. On the left hand side (LHS) of the curve, the current saturates and becomes relatively constant while the voltage decreases quickly. The power in this region increases with voltage and decreases with current.
The maximum power point (MPP) separates these two operating regions. At this point, the solar array is matched to its load. The incremental resistance of the solar array is equal in magnitude to its absolute resistance. Operation at this point will yield the maximum power output from the array. The location of this point on the curve keeps changing following variations in the operating conditions of the array.

Power harvesting efficiency ($P_o/P_{sun}$)

The power from the sun goes through multiple conversion processes before reaching the actual load. The utilization of power from the solar array is dependent on a multitude of factors including the ambient operating conditions of the solar array, load type and state, as well as power system configuration and control strategy.

The array converts solar power directly into voltage and current. The efficiency of this conversion stage is defined as the maximum power value in the terminal characteristics curve relative to the total input irradiance power. This efficiency is typically in the range of 15%. Intensive efforts are being put by solar cell manufacturers to increase this figure. Encouraging results have been recently reached with prospective doubling of this figure [1].

\[
\text{ArrayEfficiency} = \frac{P_{mpp}}{P_{ph}}
\]

(1.1)

The solar array operating point is dependent on what is connected to its terminals. Different load types, and difference control strategies, will result in operating the array at different points on the curve, and will draw an average power less or equal to the maximum power available. The closer the operating point is to the MPP, the higher the utilization efficiency of that array is. This value heavily depends on the load type and power system architecture. It typically ranges from 40 to 99%.
Most solar power systems include an electronic power conversion stage for power conditioning and/or load regulation. Again, these converters contribute to some power loss. Depending on the number of power processing stages, and regulation bandwidth requirements, such converters can be designed with efficiencies ranging from 80 to 97%.

\[
\text{ArrayUtilizationEfficiency} = \frac{P_{\text{avg}}}{P_{\text{MPP}}} \quad (1.2)
\]

Factoring in all of the efficiency figures mentioned here, the overall sun to load conversion efficiency is:

\[
\text{OverallEfficiency} = \frac{P_{\text{avg}}}{P_{\text{photo}}} = \frac{P_{\text{MPP}} \cdot P_{\text{avg}} \cdot P_{\text{photo}}}{P_{\text{MPP}} \cdot P_{\text{photo}} \cdot P_{\text{avg}}} = \text{ArrayEfficiency} \cdot \text{ArrayUtilizationEfficiency} \cdot \text{ConverterEfficiency} \quad (1.4)
\]

**Power system architectures**

The type of the load being supported by the system is a primary factor affecting the choice of system architecture.

**Load types**

A wide variety of loads can be applied to a solar array system. A particularly useful classification for designers of such systems groups these loads into:

1. Flexible, unregulated loads: loads that can handle and operate with a large variation in their voltage, current, and power values. Examples of such loads are certain types of light bulbs and dc-motors.
2. Constant voltage loads: loads that can sink a variable current while keeping their input voltage relatively constant. Batteries and battery dominated buses are a good example such loads.

3. Constant current loads: these sink in almost constant current at different voltage levels. These are not very common in practical systems, and were listed here for the sake of completeness.

4. Constant power loads: sensitive regulated loads are generally interfaced to solar arrays through power electronic converters. These converters are controlled to supply a regulated voltage/current to their loads. Observing these converters from the input (solar array side) shows a constant power sink behavior. These types of loads are widely used, and are particularly important to consider and analyze as their characteristics have significant implications regarding system stability and reliability.

**Topology options**

All four types of loads described above can be directly connected to a solar array with acceptable voltage and current ratings. The design of the system should target the maximization of the array utilization efficiency, while assuring that the source is capable of holding the load for all conditions both in beginning of life (BOL) and end of life (EOL) periods.

In this case, the operating point of the solar array is heavily dependent on different parameters of the load characteristics. There are limited control actions that can be taken to choose the operating point. Predictions of the operating conditions have to be made in the worst case, and then used to design the system. Dissipative shunt regulators can be added for protecting the load subsystem from over-voltages in times of limited load capacity.
It is also possible to interface these loads to the solar source via power electronics converters. These converters become control agents that enable a controller to choose the operating point of the solar array. If enough intelligence is added to this controller, it can locate the MPP, and force the solar array to operate at it. This process is called Maximum Power Point Tracking (MPPT).

Note in this case that the power value becomes a function of the source. This is the reason why the load in this case needs to be one of a flexible (variable) power type. Anything but a constant power sink is conceptually suitable in this case.

To accommodate the power variance of solar energy, stand-alone solar power systems usually have a battery sub-system. This battery is charged in times of available sunlight, and is then used to maintain the load in times of low irradiance.

MPPT

As described earlier, the characteristics of the solar array are constantly changing following changes in operating conditions. Temperature, irradiance, shading, ageing, and module damage are examples of those. The MPP thus moves all the time. Different approaches have been developed over the years for achieving MPPT. One class of algorithms is model-based. These depend on some study and modeling of the solar array characteristics as well as some measurements in the field in order to locate the MPP.

Another class of algorithm is called hill-climbing algorithms. It includes algorithms that perform some type of search algorithm in real time in order to locate the MPP. Different search algorithms and implementations exist, ranging from discrete component-based controllers to complex neural network realizations.
Hill-climbing algorithms are particularly popular in the field because they do not require prior study or modeling of the source characteristics, and can account for characteristics’ drift resulting from ageing, shadowing, or other operating irregularities.

As described earlier, the implementation of MPPT requires a power processing stage to allow control over the operating point of the array. This conversion stage is generally implemented using switch mode power supplies which generate large amounts of noise. The nature of hill-climbing MPPT algorithms makes them very sensitive to measurement noise. Analysis and modeling of the effect of noise on these algorithms is thus a very important topic and is targeted in chapter 4 of this thesis.

System reliability

High system reliability is an important issue for system designers in general. Solar power is popular in space applications. This industry has extreme reliability standards because of the high cost of launching space crafts, and the difficulty –impossibility in some cases- of providing maintenance and repair operations. Extra care is generally taken to provide system architectures and operating techniques that maximize the reliability of such systems.

Fault tolerance

Fault tolerance can be achieved through the use of slightly over-rated systems with intelligent controllers. If these controllers are intelligent enough to anticipate and/or detect the occurrence of a problem, and find the optimal method for avoiding or solving it, or at least taking measures for avoiding long term or permanent complications, then the system could be described as fault-tolerant.
MPPT itself can be considered a fault-tolerance measure. Moreover, different procedures the controller follows at undesirable operating conditions are also classified under fault-tolerance measures.

Modular architectures

The utilization of the concept of modular systems can also significantly improve system reliability. An excellent example would be the utilization of multiple solar array sources, as well as multiple paralleled power converters per solar array. The use of such systems has the advantage of relieving stress off the design of power stages, and reducing voltage and current stresses at critical components in the system. It also significantly increases the chances of system recovery upon incidents. Modular architectures also significantly increase system scalability and adaptability. While these advantages come at the cost of increased control complexity, this challenge is not enough to abandon this design philosophy.

Uniform power stress distribution

Thermal stress is one of the primary concerns for a system designer when considering reliability. The rate of device or module failure rapidly increases with rise in operating temperature. In most cases, the larger portion of temperature rise in power processing systems is caused by power losses. These losses are very strongly correlated with the value of the current and power being sourced by solar arrays or processed by power converters.

In many modular parallel-structured systems, paralleled modules do not naturally share the power processing stress. This causes different modules to significantly heat more than others causing their reliability to deteriorate.
Additional control features can be added to such systems to force these paralleled systems to uniformly distribute the power and current stress among them. This enables an intelligent controller to find and direct the system to the optimal operating conditions that would increase the overall reliability of the system, and maximize the mean time between failures.

The channels paralleled in this channel are only paralleled at the output side, and are sourced from independent power-limited sources. This makes the concept and implementation considerations of uniform current distribution different and more complicated. Chapter 5 of this thesis targets this subject and introduces a novel implementation scheme. This scheme takes advantage of the flexibility and processing power of the digital controller to provide high performance at low incremental cost.

Research objectives

The objective of the research work presented here is the design and implementation of a solar system with high conversion efficiency and maximized reliability. This work was largely inspired by the experimental challenges faced while prototyping the system. Therefore, recommendations made here directly address the real-world issues associated with the implementation of such a system. Different design and implementation challenges are shown, explained and analyzed. Solutions are then proposed, and are thus backed by thorough experimental tests that confirm their validity and relevance.

Thesis outline

In chapter 1, a brief introduction to solar powered systems and applications is provided. Different design challenges faced are described and the research objectives are stated. Chapter 2 contains a review of existing techniques published in literature and used in the field. The
designed solar powered system for space applications is described in chapter 3. Chapter 4 introduces a detailed operational model of hill-climbing MPPT algorithms in noisy environments. Chapter 5 presents a novel digital uniform current distribution scheme for the system.
CHAPTER 2: OVERVIEW OF SOLAR POWER HARVESTING

TECHNIQUES AND SYSTEMS

Introduction

As solar energy is used for different application and with different primary design objectives in different application fields, numerous system architectures, control philosophies, and performance optimization techniques can be found.

Basic architectures targeting reduced system component count and complexity have been used, bringing down the development and initial installation costs of such systems. Other more sophisticated architectures and techniques were also developed to maximize the harvest efficiency and reliability of solar systems.

This chapter provides an overview of existing and proposed practices for solar array system design. Comparisons of different techniques are made in order to make the choice of the architecture and control method a more systematic task, and uncover bottlenecks at which research work is an immediate necessity.

System architecture

System architecture refers to the configuration and interconnection topologies of major components in the system, as well as the control scheme applied to force these components into desired modes of operation. The choice of architecture is always heavily influenced by the intended application as performance versus cost and complexity compromises become a function of user preferences and objectives.

Traditional power system design engineers have long been accustomed to the interface of rigid low impedance voltage sources to various loads. It is therefore no surprise that a large
number of solar system designers lean toward operating the solar array in its RHS region where its characteristics follow the behavior of a voltage source.

The direct connection of the load to the solar array is only suitable to loads that are fairly flexible in terms of their operating voltages. The voltage drop generally accelerates with increasing load, and high voltage drops are expected if the arrays are loaded beyond the MPP. It is then the responsibility of the designer to make sure that this drop is within the acceptable range for the load. Figure 2-1 shows typical source and load characteristics for such a configuration.

![Figure 2-1 Resistive loading of the solar array.](image)

A more challenging situation is encountered once regulated loads are applied [2-4]. Regulated loads are interfaced to the source through tightly regulated power converters. These load subsystems appear as constant-power loads from the perspective of the array. Large signal instability will be encountered whenever the power sink value of such loads exceeds the maximum power value available from the array [2], that is, the MPP power value. The operating
point of the solar array is expected to collapse to a point far on the LHS where the delivered power is very small, and the interface power converters fail to startup.

![Figure 2-2 Constant power loading of the solar array.](image)

It is the responsibility of the designer in this case to make sure that the arrays are suitably sized to handle full load power in EOL situations, and worst expected ambient operating conditions. This generally results in severe over-sizing of such arrays which greatly reduces the average utilization factor and efficiency of these arrays. This choice is one of high cost since solar cells are generally the bulkiest and most expensive parts of such systems.

Due to the large variance in available solar power caused by variations in irradiance and other operating conditions, solar systems often include another power source or storage unit. A battery is very popular for stand-alone and UPS applications. The battery is used to store the extra energy available from the solar sources when abundant, and to supply the load in times of scarcity.
Various system architectures can be constructed by changing the way the three main components of the system -arrays, battery, and load- are interfaced [5].

The unregulated bus topology

The battery can be directly connected at the terminals of the solar array to form the primary bus. In this case, the state of charge of the battery determines the voltage at the bus and the operating point of the solar array. The load can then be directly connected to the bus or interfaced using power electronic converters.

It is necessary to provide a mechanism for protecting the battery from over-charge. Over-charging the battery can damage it or limit its life span, and can also damage the solar source or load due to excessive voltage value. A dissipative (linear) shunt regulator is provided to achieve active clamping of the battery voltage by shunting excessive current from the array whenever the battery is fully charged.

This topology has two main advantages:

1. It eliminates the negative impedance instability mechanism mentioned earlier since the bus is now masked as a voltage sink due to the presence of the battery.
2. The solid connection between the solar source and the battery eliminates the use of power converters. This means that the system cost is lowered, power conversion losses are reduced, and reliability increased.

The main disadvantages of this architecture are:

1. Cannot achieve bus voltage regulation. The bus voltage changes significantly following the battery state of charge.

2. The solar array voltage is always clamped by the battery. No MPPT operation can be performed. The system should be designed such that the operating point is in the vicinity of the maximum power point. Worst case parameters should be used for design to ensure proper operation at EOL situations.

*The regulated bus topology*

To prevent the battery from dominating the voltage of the bus, it can be interfaced to it via charge controllers. These are power electronic converters controlled to regulate the state of charge of the battery by controlling the charge and discharge current.

The solar array is still directly connected to the system bus. The voltage of this bus is tightly regulated using a dissipative shunt regulator.
Advantages of this topology include:

1. Tight regulation of the bus enables it to directly power a large variety of load subsystems. This relatively constant voltage also simplifies the design challenge of sizing the array to match its MPP to the bus voltage.

2. Independent regulator for battery charge and discharge currents. This feature enables the proper charging of the battery while regulating the bus, provided that the solar array has enough available power to do that at the specified regulation voltage.

Some drawbacks of this architecture are:

1. Additional power converter modules decrease reliability and introduce more losses.

2. More complicated control scheme.

3. Does not offer MPPT functionality.
**Battery dominated bus with MPPT functionality**

Depending on ambient and loading condition patterns, MPPT can increase the overall energy yield of a solar power system by 10-45%. However, MPPT functionality has structural requirements in a system for it to be carried out. Two basic requirements for it are:

1. A control method over the solar array operating point. This is usually a variable voltage gain power converter. It basically tunes the voltage gain to force the solar array to its MPP.
2. A power flexible bus. Note that when MPPT is active, the power delivered to the system bus becomes a function of the array itself. This means that the system bus should be able to accommodate a large range of power values. A system bus connected only to a limited load cannot be the receiving end.

The simplest architecture that provides both of these functions for a stand-alone solar system is called the battery dominated MPPT bus architecture [5, 6]. This has the PV array interfaced to the system bus through a dc-dc converter unit. A battery is directly connected to the bus. The battery in this case acts as the power absorber or backup supply depending on the strength or weakness of the solar source.

![Figure 2-5 Battery dominated MPPT bus topology.](image)

The main advantages of this architecture are obvious:
1. The system maximizes the utilization efficiency of the solar power through the use of MPPT. This means that more power can be extracted from smaller sources, and that lower storage capacities are needed to handle the fluctuations in solar power. It thus allows considerable down-sizing of the solar arrays and the system battery.

2. Does not use dissipative regulators. Dissipative regulators are bad for power efficiency, and for system reliability. The heat generated from these regulators has to be properly disposed of. Moreover, the extra energy dissipated by these regulators adds unnecessary power stress at the solar array. Note that it is undesirable to stress the solar source by drawing high current especially when that is not contributing to the energy yield.

3. The battery is not interfaced through converters. This means that there is no power conversion loss associated with charging and discharging it.

Drawbacks of this architecture are similar to those of the unregulated bus topology in terms of the absence of bus voltage and battery current regulation mechanisms.

**Modular COTS architecture**

A novel flexible system architecture was proposed in [7] and [8] for solar applications. This system architecture uses commercial-off-the-shelf (COTS) converters and aims at constructing a modular power system. The system is constructed by paralleling multiple MPPT-ready solar powered channels. This architecture is shown in the Fig. 2-6 below.
This provides numerous benefits including, but not exclusive to:

1. Rapid development and prototyping.
2. Easy scalability of the system for different levels of power.
3. Increased reliability.
4. N+1 redundancy.
5. Easy repair and maintenance.
6. Possibility of independent MPPT processes for multiple solar arrays. This is particularly important since the maximum power available from multiple connected solar arrays is always less or equal to the sum of maximum power values individually available from each.
7. Provides tight output voltage regulation when the system battery is fully charged and available solar power is higher than load demand.

This topology is particularly attractive because of the modularity principle. It was adopted as the operating topology for the system considered throughout this work.

**Grid-connected systems**

Another major field of solar systems is targeted through a set of different system architectures. This field is distributed generation through grid-connected solar inverter systems in terrestrial applications. A grid-connected inverter will reduce the power bill and relieve stress off the utility power system. When allowed by law and the utility company, a solar inverter can also sell power back to the utility company if it generates more power than is needed by the consumer.

In these systems, the solar array has to be interfaced to the utility grid through an inverter. Moreover, the grid is a flexible power consumer. These provide the two basic requirements for accommodating MPPT. This is why most grid-connected inverters have MPPT.

For safety reasons, as well as standards satisfaction requirements, most inverter systems have galvanic isolation between the solar array and the grid. This is done through a power transformer. Early designs have this transformer at their output, operating at line frequency. This transformer is hence heavy and relatively inefficient. State of the art designs use a two stage inverter system [9]. The first stage is an isolated high frequency switching dc-dc converter, and the second stage is a non-isolated power inverter that generates line frequency current. This makes the overall design considerably lighter and more efficient.
New topologies were introduced that use a single high-frequency power stage for isolation, MPPT, and unity-power-factor line frequency generation [10, 11].

*Current-mode control (CMC)*

Current mode control is a control method that uses a current feedback-based control to modulate the switching patterns of switch-mode power supplies (SMPS). Voltage regulation control can then be built around this CMC controller, see Fig. 2-7. This control scheme has been shown to have a stabilizing effect especially for power systems with wide variations in input and output voltage levels. CMC was recommended for MPPT systems by numerous papers [3, 7, 8, and 12].

![Current-mode control](image)

**Figure 2-7 Current-mode control.**

**MPPT techniques**

MPPT is a very effective method for boosting the energy yield of solar power systems. Throughout the years, several MPPT approaches have been suggested, tested, and applied. Some approaches depend on prior study and modeling of the solar arrays. These utilize model parameters and characteristics along with some field measurements to approximate the MPP
location. Others perform real-time search algorithms in order to accommodate larger variances in operating conditions and module characteristics. Some available MPPT techniques are:

1. Ambient measurement based MPPT.
2. Open/short circuit test algorithms.
3. Curve scanning method.
4. Pilot cell method.
5. PnO (Perturb and observe) algorithm.
7. Parasitic capacitance algorithm.

Solar arrays were introduced to a variety of applications of different nature. These include aerospace and satellite applications, solar-powered vehicles, and household power generation. Each of these applications has different requirements and limitations, and thus requires the utilization of a certain algorithm or a certain variation.

For the proper choice of algorithms, the application is an important factor. The design objectives of the targeted system directly affect the choices made.

Table 1 summarizes important issues to be considered for some popular applications of PV arrays.

<table>
<thead>
<tr>
<th>Application</th>
<th>Atmospheric variation</th>
<th>Partial damage</th>
<th>shading/dirt accumulation</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aerospace applications</td>
<td>very slow and regular</td>
<td>possible damage</td>
<td>frequent</td>
<td>not a critical factor</td>
</tr>
<tr>
<td>Solar-powered vehicles</td>
<td>quick and irregular</td>
<td>accumulation</td>
<td>frequent</td>
<td>important to consider</td>
</tr>
<tr>
<td>Household generation</td>
<td>slow but irregular</td>
<td>less probable</td>
<td></td>
<td>critical factor</td>
</tr>
</tbody>
</table>
Targeted MPPT characteristics

1. Compatibility with a wide variety of PV arrays, and power sources of similar characteristics.
2. Ability to cope with varying environmental conditions.
3. Tolerance of array characteristics’ drift due to ageing and dirt accumulation.
4. Tolerance of partial shading or damage of the PV array.

These objectives describe the most general, dynamic and adaptive system requirements. It assumes no forehand knowledge about the source characteristics whatsoever.

Although many of the requirements above do not apply to the satellite application intended for this project, these requirements are taken into consideration to allow extension of the results to a multitude of other applications.

Model based algorithms

Ambient model based MPPT: for a given type of solar arrays, the MPP location can be approximated given measurements of the insolation level and operating temperature of the array. MPPT can then be carried out by sensing these two quantities, and using the measurements with a model to approximate the MPP voltage or current value [15].

Advantages of this technique are that it is instantaneous, and can be relatively easy to implement if some approximations are made here and there. However, this technique is largely inaccurate, uses too many sensors, requires prior study and modeling of the solar array, and cannot account for variations in source characteristics due to factors such as ageing and partial shading.
Open/short circuit test based MPPT

Studying solar sources shows that the short circuit current at a given time is proportional to the MPP current \([16, 17]\). MPPT is performed in this case by periodically short circuiting the array and measuring its current in that time. The short circuit current is then calculated from:

\[
I_{\text{app}} = k_i \cdot I_{\text{sc}}
\]  

(2.1)

\(k_i\) is a constant decided by the solar array type. Characteristics of the solar array are then assumed constant for a period of time, and the solar array is operated at the approximated MPP position. This continues until the next short circuit test instant.

Another very similar algorithm open circuits the solar source terminals and uses the following relation:

\[
V_{\text{app}} = k_v \cdot V_{\text{oc}}
\]  

(2.2)

Although this method is very simple, it has a number of major drawbacks:

1. Requires forehand knowledge of the characteristics of the source used.
2. Assumes uniform solar cell characteristics for the entire array, and cannot account for partial shading or damage effects.
3. Require periodic interruption of the system current: this is especially difficult for large arrays with high current ratings.
4. Might present some problem if used with COTS converters because of the switching involved.
5. Power is lost during the disconnection/test period.
6. If utilized in systems with fast atmospheric changes, the testing is required to be more frequent, and the power losses will become large.
Exhaustive measurement algorithms

Two algorithms that perform extensive measurements on the cells in real time are mentioned in literature, these are:

Curve scanning method

This method is an improvement of the open-circuit-test-based algorithm. The load is temporarily disconnected from the array. This time, the characteristics are quickly swept to read the entire curve of the array, and the absolute maximum of the curve can now be easily determined.

This method provides two major advantages over the open circuit testing algorithm:

1. Does not require any forehand knowledge of the source characteristics.
2. Works for uniform and non-uniform characteristics array. It can find the absolute maximum of the curve, no matter what its shape is.

Unfortunately, the following disadvantages still exist:

1. Requires periodic interruption of the system current, for intervals longer than those of the open-circuit-test-based algorithm.
2. MPP location becomes erroneous if high slew rate of scanning is used for an array with significant capacitance.
3. Power is lost during the disconnection/test period.
4. If utilized in systems with fast atmospheric changes, the testing is required to be more frequent, and the power losses will become large.

Pilot cell method

The pilot cell method uses a solar cell with characteristics matching the cells in the solar array. This cell is used solely for measurement purposes. The P-V characteristics of this cell are
continuously searched for the maximum power point. Then VMPP for the array can be
| calculated from VMPP of the pilot cell. Generally if n cells are connected in series in each string
| within the array then:
| \[
| V_{\text{MPP}}(\text{array}) = n \cdot V_{\text{MPP}}(\text{pilot } \text{cell})
| \]
| (2.3)
| Again, this method is really simple but has the following drawbacks:
| 1. Requires an additional cell solely for measurement purposes.
| 2. Assumes uniform solar cell characteristics for the entire array, cannot account for partial
| shading or damage effects.

**Hill-climbing algorithms**

This class includes the Perturb and Observe (PnO) and some of its variations.

**PnO**

The PnO algorithm is a widely used algorithm [18-23]. Its wide application is due to the
| following reasons:
| 1. Relative theoretical simplicity.
| 2. Ease of implementation.
| 3. No requirement of prior study of source characteristics.
| 4. General applicability for a wide range of different applications.

This algorithm determines the relative position of the maximum power point by
| considering the values: \( \Delta V \) and \( \Delta P \). If the power increases with increasing voltage, the algorithm
| further increases the voltage reference with a constant voltage step \( V_{\text{STEP}} \). If the power decreases
| with increasing voltage, the reference voltage is decreased by the same value.
This method requires successive measurements of array current and voltage. The power drawn from the array is then calculated from these values. The changes in power and voltage are then calculated from two consecutive measurement cycles.

![Figure 2-8: Basic flowchart of the PnO algorithm.](image)

Main disadvantages of the PnO algorithm are:

1. Oscillates around the maximum power point (MPP) once that is reached. It is not capable of detecting the arrival at the MPP, and keeps changing the voltage back and forth. This oscillation accounts for a steady-state power loss even under stable atmospheric conditions.
2. Susceptibility to noise is a big issue for this algorithm. This is due to the derivative at its front end and its high nonlinearity.
3. Can be trapped within a local maximum point for curves that have multiple local maxima. These curves can occur if an array is partially shaded or damaged.
Incremental Conductance (IncCond)

The IncCond algorithm was developed as an attempt to overcome the oscillation problem of the PnO algorithm. The IncCond algorithm tests the input arguments to determine if the MPP has been reached. Once that is verified, the IncCond method stops changing the reference voltage. The operating point is then kept constant until the I-V characteristics of the array change, and the conditions for the MPP are violated, the search for the MPP then starts over again [18, 19, 23, and 24].

The IncCond method is based on the fact that, at the MPP, the following relations hold:

\[
\frac{dp}{dv} = 0 = \frac{d(v \cdot i)}{dv} = v \cdot \frac{di}{dv} + i 
\]

or:

\[
\frac{di}{dv} + \frac{i}{v} = 0 \quad \text{and hence the name IncCond.} 
\]

The incremental conductance \( \frac{di}{dv} \) is approximated by \( \frac{\Delta i}{\Delta v} \) from two consecutive measurements. For practical reasons, the answer above will rarely be 0. Whenever the answer is less in magnitude than a small value \( \varepsilon \), the system is considered at the MPP. If this condition is not satisfied, the values calculated are used to decide to increment or decrement the reference voltage.
According to its introduction paper, [24], the IncCond algorithm is theoretically expected to be more stable under quickly varying environmental conditions. It is expected to have less steady state losses than the PnO algorithm. However, its use is limited for the following factors:

1. Complicated implementation: mathematical manipulations done on the signal require a large calculation time and slow the algorithm down.

2. Local maxima problem: this method does not offer an advantage over PnO regarding this issue.

**Parasitic capacitance**

The parasitic capacitance method is a refinement of the incremental conductance method that takes into account the parasitic capacitance of the solar array. Parasitic capacitance uses the switching ripple to perturb the array. To account for the parasitic capacitance, the average ripple
of the array power and voltage, generated by the switching frequency, are measured using a series of filters and multipliers and then used to calculate the array conductance. The incremental conductance algorithm is then used to determine the direction to move the operating point of the MPPT.

Main disadvantages include:

1. The parasitic capacitance in each module is very small, and will only be significant in very large arrays.
2. The input capacitance of the dc-dc converters interfacing the array to its load can be large enough to mask the overall effects of the parasitic capacitance of the array.

Dithering for hill-climbing

To enable hill-climbing algorithms to escape the local maximum points, a dither signal (sinusoidal perturbation signal) can be added to the reference control voltage of the array. This signal -if of enough amplitude- can drive the systems into the region leading to the absolute maximum of the P-V curve [7, 8].

If the amplitude of this dither signal is high enough, the system will operate far from the MPP for a fair percentage of time even when it properly locates the MPP. This dither signal can thus be switched on and off in order to better utilize the source.

Current sharing

Parallel converter structures and load distribution

Loads applied to electrical power systems are ever increasing, requiring the design of stable, reliable, high power-rated systems that often exceed the practical design limits of a single
converter. A single power converter rating is limited by component ratings and efficiency considerations.

These converters can be fed from a single or multiple independent sources. They are all paralleled from the output side to form a regulated bus. Such converters are often controlled as voltage sources in order to regulate the voltage of this common bus.

Paralleled converter structures provide an excellent approach for meeting high power demand. Main advantages of using these parallel converter structures include:

1. Lower component stresses.
2. Scalability and expandability.
3. Higher reliability.
4. Easier maintenance.

Due to tight output voltage regulation, these converters behave as near-ideal voltage sources in steady state. That is, the output resistance of each voltage source is very small, typically in milliOhms and can even go all the way to zero or a negative value. With voltage regulation reference tolerances, and without additional control, this leads to a largely non-uniform load current distribution among these paralleled modules.

Non-uniform current distribution is undesirable in such systems. It results in different component stresses, and a non-uniform thermal loss distribution throughout the system. This phenomenon degrades system reliability, and will generally result in a lower mean time between failures for channels that tend to process more power.

Implementing a current sharing scheme to force these paralleled channels to equally contribute power is very desirable. It will enhance both peak and thermal stress distribution. It
can also alleviate some stress from protective circuit design since it reduces the probability and severity of false over-current alarms.

*Droop sharing techniques*

Severe non-uniform current distribution is a result of near-ideal voltage regulation for the paralleled channels in steady-state. Dc current distribution can be enhanced by allowing some output resistance. If enough resistance is allowed, the current distribution error can be brought down to a low value, especially at higher load conditions [31, 32].

Output resistance can be physically added to the output of the regulated power supply, however, this is not recommended for efficiency reasons. This resistance can alternatively be programmed into the controller characteristics. In this case, the voltage regulation reference is adjusted with negative linear correlation with the output current measurements, see Fig. 2-10. Doing this avoids power losses in the resistance of the converter.

![Figure 2-10 Voltage regulation schemes](image)

This method is very simple and reliable. It requires no communication among the converter controllers, and will enhance the current distribution both during transients and in
steady-state. Unfortunately, this method has two major disadvantages. It has low accuracy particularly at lower loading conditions, and bus voltage regulation is degraded. Design largely becomes a tradeoff matter between tight voltage regulation and steady-state load distribution error.

**Active sharing techniques**

More accurate current sharing can be achieved without compromising output voltage regulation by applying more active methods for load sharing. Current sharing can be achieved by introducing an additional control loop within the controller structure. This control loop utilizes information about the current contributions of other channels in the system. This information is collected using an information network often dubbed the current-sharing bus, and is used to provide a targeted value for the current distribution of the channel, serving as a reference for current regulation.

**Control structures**

As mentioned earlier, current mode control is a popular control technique in a wide variety of converters used for parallel structured systems. It involves a voltage regulation error amplifier that provides an error signal output used as a current reference.

The current sharing loop can be added to such a system in three different structural schemes: [31]

1. Outer loop regulation: the current sharing control loop is introduced at the outermost level and given control over the voltage regulator reference. This means that current sharing can be introduced without breaking into the internal structure of high-bandwidth regulation loops. This is particularly useful when using COTS products. It also allows the use of a low-
bandwidth current sharing bus in order to reduce noise pickup on that sensitive bus [31, 33]. Several commercial IC’s for realizing such control are commercially available [34, 35].

2. Inner-loop regulation: current sharing is directly interfaced to the innermost current control loop. This requires breaking into the internal control structure of these converters and can be provided by the manufacturer of COTS modules as an added feature. Among the advantages of this scheme is that the current sharing loop can be combined with the innermost current feedback loop as one [31]. Moreover, its speed does not have to be limited by the relatively low-bandwidth voltage regulation loop.

3. Dual loop regulation: the current sharing loop and the voltage regulation loops are arranged in this case in parallel. This allows these two loops to be independently designed with less concern for their interaction. This gives more freedom to the choice of the bandwidth allowed for the current sharing loop. The bandwidth can then be increased to achieve faster response or reduced to increase noise immunity.

Figure 2-11 Current sharing control structures (a) outer-loop regulation (b) inner-loop regulation (c) Dual-loop regulation.
The current sharing bus

The current sharing bus provides a communication backbone for reference generation for the current sharing regulators. This bus typically holds a single value that is transmitted throughout the system and represents the current at which each channel should settle in order to achieve the targeted distribution.

The value posted at the current sharing bus is programmed in different ways, these include:

1. Dedicated master program: the output current measurement of one of the channels is constantly present on the current sharing bus. All other channels follow this signal and regulate their current to match it. During that process, this current value changes and moves to a proper level representing the balanced share for that channel. This program is the simplest. Unfortunately, this program presents a reliability problem since current sharing is lost if the master unit fails. Additionally, this program cannot be used for independently sourced channels that have limited power resources.

2. Automatic master program: this bus program chooses the minimum or maximum current contribution at any point in time to be posted at the sharing bus. This method is very attractive for its fault tolerance. An inherent problem in this case is wandering of the master channel. A method is described in [35] for solving this problem that insignificantly compromises sharing accuracy.

3. Average bus program: this bus program uses the average value of all current contributions as the reference posted on the current sharing bus. The averaging function can be very easily realized in analog electronics. The problem associated with this scheme is that sharing is lost
upon failure of any paralleled channel. The use of this bus is further limited because it is patented.

Figure 2-12 Typical current sharing bus configurations.

The choice of the control structure and the bus program is dependent on the application and the characteristics targeted. A digital scheme can introduce flexibility and allow fault tolerance procedures to be implemented.
CHAPTER 3: SCALABLE PARALLEL-STRUCTURED SYSTEM FOR SPACE APPLICATIONS WITH INNOVATIVE CONTROL

Following the ever-increasing need for flexible, scalable, and reliable power for space applications, a number of concepts have emerged that provide improved architectures and control schemes.

In close coordination with the Advanced Power Electronics Corporation (APECOR), Florida Power Electronics Center (FloridaPEC) at UCF initiated a project to design a solar-powered, scalable, modular, parallel-structured system for space power applications that incorporates these emerging concepts.

The system architecture is shown in Fig. 3-1 below:

Figure 3-1 Modular system architecture.
The system is composed of a number of standardized solar-powered converter channels. These channels are independently sourced from their corresponding solar arrays, and are paralleled from their output side to form a common bus.

Systems of different power ratings can be configured by paralleling a suitable number of these channels. An extra channel can also be added to achieve so-called N+1 redundancy. This enables hot swap functionality for real time maintenance and reconfiguration. Each solar powered channel is independently sourced, operated, and controlled. It can either work alone, or in conjunction with other channels or power sources, such as a battery, paralleled at the same output bus.

Each solar powered channel is composed of three main components: the solar array, the power stage, and the controller unit. The solar array channel is used to source power to the system at variable voltage levels depending on the insolation and other operating conditions. The power stage processes incoming power from the solar arrays to provide a suitable output voltage at the output bus. It also provides an active control tool over the system operation and particularly over its corresponding solar source. This control is then carried out by the controller unit which is responsible for optimizing the operating parameters and ensuring reliable operation in conjunction with other channels and subsystems in the power system.

The different components of the system were modeled and analyzed in order to find the optimal configuration and control strategy for the system under design.

Solar cell characteristics

Solar cells are basically made out of specially manufactured and doped semiconductor material. This material is properly doped and setup to form a p-n junction that, when bombarded by light of particular frequency content, generates free electrons. The presence of the junction
also produces an intrinsic electric field and an associated potential difference that pushes these electrons to move and form an electric current if a circulation (loading) path is present.

The value of the voltage that appears between the terminals of a solar cell is dependent upon a number of factors ranging from cell and load characteristics to ambient operating conditions. At a particular irradiance and temperature, the terminal cell voltage starts from a maximum value, the open circuit voltage ($V_{oc}$), at zero current. The terminal voltage drops slowly with increased loading current. Beyond a certain point, the current levels off and the voltage drops quickly until it reaches zero. The cell then supplies its maximum current, called its short circuit current ($I_{sc}$).

![Typical terminal characteristics of a solar cell.](image)

Figure 3-2 Typical terminal characteristics of a solar cell.

The intensity of incident light directly affects the number of free electrons generated in the cell, and thus has a direct effect on the short circuit current value. Irradiance is thus effectively directly proportional to the maximum power value in the characteristics curve.
Solar cells need to be mounted in a way that maximizes the power incident at their surfaces [40]. The setting of the array should avoid shading effects, as it decreases the effective value of irradiance at the solar cell surface.

Temperature is another important factor. Temperature has a direct effect on the voltage level produced by the semiconductor junction, and thus affects the open circuit voltage value. The open circuit voltage decreases with increasing temperature.

The electrical model of a solar cell is shown in the figure below.

![Electrical model of a solar cell](image)

**Figure 3-3 Electrical model of a solar cell.**

This model consists of four main components, these are:

1. \( I_{\text{photo}} \): the photo current component which represents the internally generated electrical current resulting from the freed electrons within the cell. Its value is directly proportional to the amount of sunlight incident on the surface of the cell semiconductor. This current is the key variable determining the short circuit value of solar cell current.

2. Diode \( D \): this diode accounts for the nonlinear semiconductor material characteristics. This diode cannot be seen as simply on or off since the operating range of the solar cell voltage covers its transition region. The thermal voltage constant for this diode reflects the major effect of temperature on cell characteristics. Its value directly affects the open-circuit value of the cell voltage.
3. **R\_shunt**: this resistor accounts for the leakage current lost within the semiconductor device. This current is generally insignificant and the resistor value is fairly high.

4. **R\_series**: accounts for ohmic losses in the semiconductor material and connection terminals of the cell. This resistance is generally low in value.

The values and parameters for these model components are all dependent upon a number of variables. These include parameters of the semiconductor material as well as operating conditions such as illumination, operating temperature, and cell ageing.

Following the model presented above, the terminal current of the solar cell is related to its terminal voltage by the following equation:

\[
I = I_{photo} - I_0 \cdot \left( \exp\left(\frac{q}{AKT} \left(V + I \cdot R_{series} \right) - 1\right) - 1 \right) - \frac{V}{R_{shunt}}
\]

where:

- \(I_{photo}\) = photo current generated due to insolation
- \(I_0\) = reverse saturation current of semiconductor material
- \(R_{series}\) = series ohmic resistance of the cell
- \(R_{shunt}\) = leakage resistance
- \(K\) = Boltzmann’s constant
- \(T\) = absolute operating temperature
- \(q\) = charge of a single electron
- \(A\) = ideality factor of the p-n junction
Constructing Solar Arrays

The output voltage of a solar cell is generally small. Larger operating voltages are needed in order to optimize their bundled power converters efficiencies. A number of cells are generally connected in series to form solar strings capable of generating larger voltages. Multiple strings are then paralleled to form solar arrays of desirable power and current rating.

![Figure 3-4 Configuration of solar cells in an array.](image)

The shape of the terminal electrical characteristics of a solar array is very similar to that of its cells. The open circuit voltage of a solar array is the sum of the open circuit voltages of cells in series, while its short circuit current is the sum of the short circuit currents of its paralleled strings. See Fig. 3-5.
As is immediately evident from its terminal characteristics, a solar array is a highly non-linear power source. The characteristic curves are generally split into two regions, the right hand side (RHS), and left hand side (LHS) of the curve. The RHS is the region where the array behaves as a non-ideal voltage source. In this region, a load draws more current in order to increase the power delivery, which results in a voltage drop at the array terminals. On the other hand, the array behaves as a current source at the LHS. Voltage rapidly increases, and current slowly decreases with increasing power. Separating the two regions is the maximum power point (MPP). Operation at this point will result in the largest amount of power harvest from the array.

Partial shading of a solar array will cause different cells in the same array to have significantly different characteristics. This can cause serious degradation in the power output capabilities of the whole array.

Figure 3-5 Typical characteristics of the constructed solar arrays.
Power Stage and Analog Control

As described earlier, power converters are needed to interface the solar arrays to the system bus in order to enable control over the operating point of the solar arrays. In this system, the primary system bus is chosen to be operated at 28V dc. This voltage is achieved through a dc-dc conversion stage.

In order to accelerate the development and prototyping phase of the project, commercial-off-the-shelf (COTS) dc-dc converters were used. The converters used have the following features:

1. Wide input voltage range: this allows the system to handle different solar array modules that are commercially available. It can also tolerate large variances in the operating voltage of these solar arrays.
2. Tightly regulated output: automatic regulation of the output voltage when abundant power is available. Note that these converters can be operated at different output voltages if proper control is applied.
3. Electrically isolated topology: the input return path and the output bus ground are isolated. This is sometimes required in such systems. It can also reduce design complexity due to ground loops and noise coupling.
4. Current-mode-controlled: provide robust control over their current by utilizing peak current mode control. This feature is also available to outside control through the parallel pin.
5. Parallel pin: these converters provide a control pin that can be used to override output voltage regulation, and limit their current. This parallel pin is the focal point of the control strategy presented here.
6. Automatic current sharing: when paralleled both at the input and the output sides, these converters can perform very fast, accurate, and reliable current sharing. This is done by shorting their parallel pins together to form a current-sharing bus. When operated in this way, multiple paralleled converters can be seen and dealt with as a single converter of a higher power rating.

7. Trim pin: this is a control pin that is used to modify the feedback voltage measurement signal in order to change the regulation voltage of the output. This pin is also utilized within the control structure.

Solar channels of different ratings are needed to interface solar arrays of different sizes. This can be done by paralleling as many COTS converters within a single channel. These are all paralleled at the input and the output sides, and automatically share current. These converters can then be seen as a single converter with an output voltage regulator, and a current limit terminal.

Figure 3-6 Solar powered channel structure.
**OVR and IVR**

The output voltage regulator (OVR) is built into these modules. It is programmed in a very traditional way to fit a multitude of applications. This voltage regulator senses the output voltage and modifies the current command in order to regulate it. The current drawn by these converters from their input, which is proportional to the parallel pin signal, is increased when the load voltage drops, and decreased when that voltage surges.

Operation in OVR is maintained as long as the basic positive relationship between input current and power is valid. This is true on the right-hand side of the P-V curve. Whenever the power demanded from the input is larger than is available, operation is shifted to the left hand side of the P-V curve. Large-signal instability then results in the input voltage settling at a very low value where the converters cannot start.

In this case, this channel cannot be responsible for regulating the bus voltage since it does not have enough power. The proper control action would be to disable the output voltage controller, and force the channel to operate at the MPP in order to push the maximum power attainable to the output bus. The output voltage is this case will depend on other channels or subsystems tied to the bus.

The output voltage regulation can be disabled by pulling the parallel pin voltage down. This has to be done in such a way that will regulate the input voltage to a reference value that hopefully represents the MPP voltage. The input voltage regulator (IVR) is introduced for this goal. This is an error amplifier that senses the input voltage, compares it to a reference, and applies the error signal to the parallel pin.

In general, the channel operates in OVR mode whenever that causes its input voltage to settle at a voltage larger than that commanded to the IVR. If more power is demanded, the
voltage drops and is soon clamped by the IVR regulator to its reference, while the OVR saturates and becomes naturally inactive.

This IVR controller has to be designed to stabilize the loop for a wide range of source resistance and voltage levels. At the same time, its time constant should be low enough to avoid instability in the outer control loop, namely MPPT.

IVR functionality does not interfere with current sharing within the channel. This is because the error signal is still applied to all paralleled COTS converters.

**Input measurements**

Input voltage and current sensing circuitry are needed to provide measurement signals for the DSP realizing MPPT. It is important that these values have accurate dc values, as well as matched delay for their ac components. Voltage sensing is done using a voltage divider while current sensing can be achieved resistively or using a hall-effect sensor.

**The Digital Controller**

A digital controller is needed for proper control and monitoring of this system. TI’s tms320lf2407a was chosen to realize this controller. The main control functions it carries are:

1. **MPPT**: the digital controller receives scaled solar array voltage and current measurements from the analog conditioning circuits. It senses these measurements through an analog-to-digital converter (ADC) and processes them to locate the MPP. This controller then provides a voltage reference through a digital-to-analog converter (DAC) that corresponds to the MPP. The IVR is then responsible for matching the operating point of the solar array to it.

2. **Fault tolerance**: the digital controller should always ensure operation of the channels within the recommended ranges. The controller should limit converter operation within the specified
input voltage range, and also perform de-rating of the power converters at higher temperatures.

3. Data collection: the digital controller is interfaced to other controllers in the power system of the space-craft, as well as to other mission control equipment. It can provide data logging and analysis services to these controllers in order to allow better optimization of system operation.

4. Inter-channel current sharing: intra-channel current sharing, between converters in a single channel, is automatically achieved; however, current sharing among multiple channels in the system is more elaborate. Inter-channel sharing was introduced to the system through the digital controller. This is described in chapter 5.

*The Controller Area Network (CAN) Bus*

As mentioned earlier, the digital controllers of different channels are digitally interfaced to each other and to other mission control processors. This is achieved using a CAN bus. This protocol is chosen for a number of reasons:

1. Provides multi-nodal communication.

2. Network flexibility: provides dynamic addressing and broadcast capability.


4. Available core within the digital controller used.

5. Easy electrical isolation.
Maximum Power Point Tracking

The MPPT algorithm chosen was the PnO due to its simplicity and generality. It is theoretically able to cope with wide variations in the P-V characteristics, and does not require any prior knowledge of the characteristics of the source.

The PnO algorithm flowchart for a single iteration is shown below:

```
start

calculate
\[ \Delta v = v(k)-v(k-1) \]
\[ \Delta p = p(k)-p(k-1) \]

sign(\Delta p) = sign(\Delta v)

v_{ref} =
\begin{align*}
& v_{ref} + V_{STEP} & v_{ref} = v_{ref} - V_{STEP}
\end{align*}

end
```

**Figure 3-7 Basic PnO algorithm.**

In order to achieve stable, reliable, and fault-tolerant MPPT operation, a number of blocks, operations, and limits are added to the basic PnO algorithm. The MPPT block performs the following:

1. Dither generation and perturbation: many publications recommended the introduction of a sinusoidal dither signal to MPPT. This is superimposed at the input voltage reference to perturb the system and enhance the measurements Signal-to-Noise ratio. It is important that this signal is a smooth sinusoid. Glitches and steps in the sinusoid cause the input and output currents and voltages to be spiky and noisy.
2. IIR filtering: to enhance both the steady-state and transient response of MPPT, voltage and current signals are passed through identical 3rd order IIR digital filters. The system function of these filters is of the form:

\[
H(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2} + b_3 \cdot z^{-3}}{1 + a_1 \cdot z^{-1} + a_2 \cdot z^{-2} + a_3 \cdot z^{-3}}
\]  

(3.2)

The necessity of adding these filters is thoroughly discussed in chapter 4. Their design should be cautious, and should consider the following:

a. Near-unity gain up to double or triple the dither frequency,

b. Near-linear phase in the unity gain range,

c. Stability issues,

d. Register saturation issues.

The reason why unity gain and linear phase are stressed for the 0-3fdither range is that the current is non-linearly related to the voltage. Whenever the voltage has a 100Hz dither signal, the current is expected to have multiples of that frequency. The 2nd –maybe 3rd- harmonic is important for proper MPP tracking.

3. Power calculation: the filtered current measurement is multiplied by voltage to get a reading for the power.

4. Operating mode detection: It is important for the DSP controller to determine if the channel is operating in MPPT or in OVR mode. This enables the DSP to disable MPPT when the load is light. This measure is important to stop the MPPT algorithm from interfering with normal OVR operation of the system. OVR detection is also important for a number of others blocks such as current sharing.
The method used for OVR detection is comparing the measured voltage of the solar array to the commanded set-point provided by the DSP. In MPPT mode, the two voltages should be equal. In OVR mode, the measured voltage is expected to be larger than the reference voltage.

5. Open circuit recovery: if the open circuit voltage of the solar array drops quickly, or if the MPPT algorithm is mistakenly initialized beyond the open-circuit voltage of the array, the IVR regulator loses control of the array operating point. Any dither induced by the DSP is not passed to the input voltage, and there is not enough information for the PnO algorithm for it to decrease its voltage reference. In that case, the current of the array drops, and that can be used as an indication for the DSP to retreat. This is done by comparing the current reading to a predetermined threshold. This threshold should exceed the no-load drain current of the channel from its corresponding solar array.

6. Reference conditioning: in order to avoid operation at a voltage unacceptable for the dc-dc converters as well as register saturation/resetting problems, the voltage reference is clipped to a proper operating range.

Figure 3-8 MPPT control block diagram.
Experimental Results

A prototype was built in order to experimentally verify the operation of this architecture. A standardized channel of 500W was built by paralleling two 28V, 250W COTS dc-dc converters, and adding the necessary control.

A single channel was tested independently to verify MPPT operation, as well as control stability under different load transient conditions across OVR and IVR (MPPT) modes.

![Experimental waveforms of a single MPPT channel.](image)

**Figure 3-9** Experimental waveforms of a single MPPT channel.
Figure 3-9.a shows a capture for a constant load that drives the channel to MPPT. Trace 1, solar array voltage, is maintained at 48V which corresponds to the MPP voltage. Sinusoidal dither is superimposed on it to allow robust MPPT. Trace 2 represents the solar array current which also has this dither component in response to its presence in the voltage. Trace 3, output voltage, is not regulated and has a ripple component due to the dithering process. Trace A represents solar array power, it has ripple at double the dither frequency, which is a special signature of the MPP.

Figure 3-9.b shows a load current transient, trace 4, between two loading values in MPPT. The array voltage and current traces are virtually intact, while the output voltage has ripple that corresponds to both the dither frequency and the load transient. Figure 3-9.c shows a similar condition at a higher load transient frequency.

Figure 3-9.d shows a load transient between MPPT and OVR. At light load, the output voltage is regulated at 28V, while the array voltage and current settle at a point on the RHS of the curve (high voltage, low current) with no dither component. Upon load increase, the output voltage loses regulation, and the input voltage drops far to the LHS. MPPT then kicks in and raises the input voltage until it reaches the MPP.

Multiple prototypes were constructed and tested together. The results of those tests are discussed in chapter 5.

Parallel Channel Operation

As described earlier, multiple of these MPPT-enabled, independently sourced, solar-powered channels are connected to a single output bus in order to construct a power system of the desired rating. When paralleled, these channels can simply work together. No added control is required to provide the basic functionality.
At any point of time, some of these channels are fully loaded and operate in MPPT mode. Other channels on the bus might be partially loaded, those are then responsible for output voltage regulation. These channels operate in OVR.

If excessive loading is applied, the output voltage will drop. An auxiliary power supply, typically a battery, should kick-in in such a case to hold the bus voltage from collapsing.

In order to provide added features and optimize the system, the controllers of all channels on the bus are connected through a CAN bus network. These controllers can share information among them to perform system level functions. A system-level function of particular interest for reliability is inter-channel current-sharing. This is introduced in chapter 5.
CHAPTER 4: STATISTICAL NATURE OF HILL-CLIMBING MPPT ALGORITHMS

Among the most practical and most attractive MPPT algorithms are the so-called Hill-Climbing Algorithms. This class basically covers the basic PnO algorithm and all others derived from it: incremental conductance, parasitic capacitance, and other modified PnO versions.

Hill climbing algorithms are generally very easy to understand in their simplest form. These algorithms depend on two or more consecutive measurements of voltage and current. These measurements are used to estimate the rate of change of power with respect to change in the control variable. The control variable is then changed in the direction that would increase power.

The practical implementation of these algorithms is not straight-forward. Practical MPPT setups tend to have a lot of noise due to the use of switch-mode power converters. The derivative operation on the front-end of these algorithms (slope estimation mentioned above) acts as a noise amplifier. Moreover, delays involved in the system might make it difficult to relate changes in power at one instant to the change in the control variable that must have occurred in advance.

Statistical Equilibrium at the MPP

In the ideal –noise and delay free- implementation of hill-climbing algorithms, the algorithm always increases (decreases) the control variable when dP/dControl is positive (negative). The algorithm stops at the MPP because dP/dControl keeps changing signs from positive to negative every other iteration.
In the practical setup, and if the system is tracking properly, the algorithm takes the correct decision more often than the wrong one, and converges in the statistical sense: the control variable is increased (decreased) more frequently when \( \frac{dP}{dControl} \) is positive (negative). The control variable is increased as many times as it is decreased when the system is at the MPP. In other words, the system always stops at the point of statistical equilibrium.

**Effect of Noise**

As mentioned above, MPPT usually runs in a noisy environment. Noise here is used to refer to any deviation from the I-V curve in the current and voltage measurement. These deviations might be random conducted or radiated noise, or simply deviations induced by delays in the control loop and the measurement circuitry.

The voltage and current measurements tend to be very noisy. Extensive filtering might destroy the information content in these signals. Some noise will always find its way to the core MPPT process.

If the noise injected to these measurements is unbiased, i.e., it causes the MPPT algorithm to make control variable increments as frequent as decrements at all operating points, then it should have no steady-state effect on the overall operation of the system. Unfortunately, this is rarely the case. The highly non-linear nature of the algorithm makes it take many biased decisions in the presence of noise. Whenever the equilibrium between control increment and decrement instances is destroyed at the MPP, the system would depart from it. The system would always search for a point of statistical equilibrium. The point of equilibrium might be close to or far from the MPP depending on the severity of the noise and the level of intelligence in the algorithm.
Two examples of noise that are particularly destructive to the MPPT setup built at UCF are mentioned below:

**Spiky noise in voltage measurements**

Spiky noise in the voltage measurement signal is a source of many problems in the practical MPPT setup. The reason of the severity of damage done by noise in the voltage over that in the current is that the implemented algorithm depends on $dp/dv$ rather than $dp/di$ (voltage is taken to be the control variable).

Whenever the voltage measurement changes due to a burst of noise, the current measurement is not expected to change accordingly. If the current is almost constant, then $p$ would become directly proportional to $v$, and $dp$ will tend to follow the sign of $dv$. This condition will make the algorithm tend to increase the reference voltage supplied to the system. The point of equilibrium would be shifted to the right hand side (RHS) of the P-V curve.

A similar problem is observable when the channel is operating in OVR mode. In that case, both voltage and current should be constant (given a constant load) or slowly varying. The MPPT algorithm should theoretically keep the reference voltage constant and not interfere with system operation. In the practical setup, the phenomenon described above causes the reference voltage of the MPPT algorithm to keep increasing slowly but steadily until it starts interfering with normal system operation. It induces mode transitions from OVR to IVR and back, and introduces ripple to input voltage and current. If there is not enough information in the voltage and current measurements to cause the MPPT to back down to the left, the reference would keep increasing until the dc-dc converters are shut-off.
Quantization noise in current measurements

The quantization effect in the current measurement signal is more observable because the voltage is not allowed to drop below 36 V (minimum input voltage for the dc-dc COTS units), and because the ac content in the voltage is constant and primarily determined by the dither signal added to the reference.

When the sun insolation is low, the solar array current becomes small in magnitude. The changes in the current can easily become comparable in magnitude to the quantization step of the ADC. This observation might seem irrelevant in the presence of other sources of noise. However, if the signals are properly filtered, a signal clear enough might result that has an ac component lower than the quantization level.

A problem generally starts appearing when the ac component of the current measurement is in the range of 4-6 quantization levels. It is difficult to predict the direction to which this type of noise biases the system. However, when the signal ripple is too low, lower than one quantization level, making the current measurement constant most of the time, the system is usually biased to the RHS of the P-V curve.

Statistical Modeling of MPPT Operation in a Noisy Environment

In order to allow proper design of the MPPT algorithm –in terms of dither amplitude and reference bias point step size-, different parameters of MPPT need to be quantitatively related to tracking efficiency and transient response.

In a noisy MPPT environment, the voltage step size –determined by the dither signal shape and amplitude– is the primary design parameter that can be optimized given a certain measurement noise statistical characteristics.
From the statistical perspective, the MPPT control variable update direction and speed are directly affected by the probability of decision errors. On average, the following equation holds for a voltage-based MPPT process:

\[
\frac{dV_{\text{ref}}}{dt} = V_{\text{STEP}} \cdot f_{\text{update}} \cdot (P_{\text{pve}} - P_{\text{nve}})
\]  

(4.1)

where:

- \( V_{\text{STEP}} \) = reference bias point step size,
- \( f_{\text{update}} \) = frequency at which the MPPT takes decisions and updates output,
- \( P_{\text{pve}} \) = probability of a decision made to increment the voltage reference,
- \( P_{\text{nve}} \) = probability of a decision made to decrement the voltage reference.

The best performance that can be achieved using hill-climbing MPPT algorithms corresponds to the case when:

- \( P_{\text{pve}} = 1.0, P_{\text{nve}} = P_{\text{zero}} = 0.0 \) on the LHS of the PV curve,
- \( P_{\text{nve}} = 1.0, P_{\text{pve}} = P_{\text{zero}} = 0.0 \) on the RHS of the PV curve,
- \( P_{\text{pve}} = P_{\text{nve}} = 0.5, P_{\text{zero}} = 0.0 \) at the MPP.

where:

- \( P_{\text{zero}} \) = probability of a decision made to keep the voltage reference unchanged.

For simplifying the analysis, \( P_{\text{zero}} \) is taken to be zero; however, in a quantized system, it might have some value especially if a voltage step window is implemented.

Naturally, the system stops when \( \frac{dV_{\text{ref}}}{dt} = 0 \). Neglecting \( P_{\text{zero}} \), this happens whenever \( P_{\text{pve}} = P_{\text{nve}} = 0.5 \). Noisy measurements can easily make this condition hold at some point away from the MPP causing bad tracking and decreased extracted power from the array.
The conditions on the noise leading to decision errors are discussed next for three cases: voltage noise only, current noise only, and noise is both signals. If these condition expressions are used along with a proper statistical model of the noise, $P_{pv}$ and $P_{ps}$ can be estimated.

**Noisy voltage measurement ($n_i=0$)**

Given a noisy voltage measurement, the calculated power of the solar array is:

$$\Delta \tilde{p} = i_{sa} (\Delta v_{sa} + \Delta n_v) + (v_{sa} + n_v)\Delta i_{sa}$$

(4.2)

since $i_{sa}$ is always positive:

$$sign(\Delta \tilde{p}) = sign[\Delta v_{sa} + \Delta n_v + \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v)]$$

(4.3)

On the LHS, and assuming $\Delta v_{sa} > 0$, $\Delta p_{sa} > 0$ follows. The algorithm takes a wrong decision if:

Case 1: $\Delta \tilde{v} > 0$, and $\Delta \tilde{p} < 0$:

$$\Delta n_v + \Delta v_{sa} + \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) < 0$$

(4.4a)

and

$$\Delta n_v + \Delta v_{sa} > 0$$

(4.4b)

$$\therefore -\Delta v_{sa} < \Delta n_v < -\Delta v_{sa} - \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v)$$

(4.4c)

or if:

Case 2: $\Delta \tilde{v} < 0$, and $\Delta \tilde{p} > 0$:
This case is impossible because $\Delta i_{sa} < 0$, and that means that both the voltage and current readings have decreased, and the power reading should decrease too.

It can be shown that a condition with the same probability follows by assuming $v_{sa} < 0$.

On the RHS, assuming $\Delta v_{sa} > 0$, $\Delta p_{sa} < 0$ follows. The algorithm takes a wrong decision if:

Case 1: $\Delta \tilde{v} < 0$, and $\Delta \tilde{p} < 0$:

$$\Delta n_v + \Delta v_{sa} + \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) < 0$$

and

$$\Delta n_v + \Delta v_{sa} < 0$$

(4.5a)

(4.5b)

The first expression follows from the second since the sign of $\Delta i_{sa}/i_{sa}(v_{sa} + n_v)$ is negative given a small voltage noise amplitude.

The condition for a decision error in this case becomes:

$$\Delta n_v < -\Delta v_{sa}$$

(4.5c)

or if:

Case 2: $\Delta \tilde{v} > 0$, and $\Delta \tilde{p} > 0$:

$$\Delta n_v + \Delta v_{sa} + \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) > 0$$

and

$$\Delta n_v + \Delta v_{sa} > 0$$

(4.6a)

(4.6b)
In this case, the second expression follows from the first one since the sign of \( \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) \) is negative given a small voltage noise amplitude.

The condition for a decision error in this case becomes:

\[
\Delta n_v > -\Delta v_{sa} - \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v)
\]  

(4.6c)

**Noisy current measurement \((n_v=0)\)**

Given a noisy current measurement, the calculated power of the solar array is:

\[
\Delta \tilde{p} = v_{sa} (\Delta i_{sa} + \Delta n_i) + (i_{sa} + n_i) \Delta v_{sa}
\]

(4.7)

since \( v_{sa} \) is always positive:

\[
\text{sign}(\Delta \tilde{p}) = \text{sign}[\Delta i_{sa} + \Delta n_i + \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i)]
\]

(4.8)

On the LHS, and assuming \( \Delta v_{sa} > 0 \), \( \Delta p_{sa} > 0 \) follows. The algorithm takes a wrong decision if \( \Delta \tilde{p} < 0 \):

\[
\Delta n_i + \Delta i_{sa} + \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i) < 0
\]

(4.9a)

\[
\therefore \Delta n_i < -\Delta i_{sa} - \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i)
\]

(4.9b)

On the RHS, and assuming \( \Delta v_{sa} > 0 \), \( \Delta p_{sa} < 0 \) follows. The algorithm takes a wrong decision if \( \Delta \tilde{p} > 0 \):

\[
\Delta n_i + \Delta i_{sa} + \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i) > 0
\]

(4.10a)
Noisy voltage and current measurements

Given noisy voltage and current measurements, the calculated power of the solar array is:

\[
\Delta \tilde{p} = (v_{sa} + n_v) \cdot (\Delta i_{sa} + \Delta n_i) + (i_{sa} + n_i) \cdot (\Delta v_{sa} + \Delta n_v) + (\Delta i_{sa} + \Delta n_i) \cdot (\Delta v_{sa} + \Delta n_v)
\]  

(4.11a)

neglecting the last term:

\[
\Delta \tilde{p} \cong (v_{sa} + n_v) \cdot (\Delta i_{sa} + \Delta n_i) + (i_{sa} + n_i) \cdot (\Delta v_{sa} + \Delta n_v)
\]  

(4.11b)

On the LHS, and assuming \( \Delta v_{sa} > 0 \), \( \Delta p_{sa} > 0 \) follows. The algorithm takes a wrong decision if:

Case 1: \( \Delta \tilde{v} > 0 \), and \( \Delta \tilde{p} < 0 \):

\[
\Delta n_v + \Delta v_{sa} > 0
\]  

(4.12a)

and

\[
\Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) + \Delta i_{sa} \cdot (v_{sa} + n_v) + \Delta v_{sa} \cdot (i_{sa} + n_i) < 0
\]  

(4.12b)

\[
\therefore \Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) < -\Delta i_{sa} \cdot (v_{sa} + n_v) - \Delta v_{sa} \cdot (i_{sa} + n_i)
\]  

(4.12c)

or if:

Case 2: \( \Delta \tilde{v} < 0 \), and \( \Delta \tilde{p} > 0 \):

\[
\Delta n_v + \Delta v_{sa} < 0
\]  

(4.13a)

and

\[
\Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) + \Delta i_{sa} \cdot (v_{sa} + n_v) + \Delta v_{sa} \cdot (i_{sa} + n_i) > 0
\]  

(4.13b)

\[
\therefore \Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) > -\Delta i_{sa} \cdot (v_{sa} + n_v) - \Delta v_{sa} \cdot (i_{sa} + n_i)
\]  

(4.13c)

63
On the RHS, again assuming $\Delta v_{sa} > 0$, $\Delta p_{sa} < 0$ follows. The algorithm takes a wrong
decision if:

Case 1: $\Delta \tilde{v} > 0$, and $\Delta \tilde{p} > 0$:

$$\Delta n_v + \Delta v_{sa} > 0$$

(4.14a)

and

$$\Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) + \Delta i_{sa} \cdot (v_{sa} + n_v) + \Delta v_{sa} \cdot (i_{sa} + n_i) > 0$$

(4.14b)

$$\therefore \Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) > -\Delta i_{sa} \cdot (v_{sa} + n_v) - \Delta v_{sa} \cdot (i_{sa} + n_i)$$

(4.14c)

or if:

Case 2: $\Delta \tilde{v} < 0$, and $\Delta \tilde{p} < 0$:

$$\Delta n_v + \Delta v_{sa} < 0$$

(4.15a)

and

$$\Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) + \Delta i_{sa} \cdot (v_{sa} + n_v) + \Delta v_{sa} \cdot (i_{sa} + n_i) < 0$$

(4.15b)

$$\therefore \Delta n_i \cdot (v_{sa} + n_v) + \Delta n_v \cdot (i_{sa} + n_i) < -\Delta i_{sa} \cdot (v_{sa} + n_v) - \Delta v_{sa} \cdot (i_{sa} + n_i)$$

(4.15c)

Effect of Noise on Steady-State Tracking as Predicted by the Statistical Model

The conditions derived above for noise to produce errors in the MPPT decision can be
used to analyze the effect of noise on the system both qualitatively and quantitatively. A number
of assumptions need to be made in order to simplify the analysis:

The voltage change, $\Delta v_{sa}$, is always taken to be positive. In fact, it can be shown that if
the noise is completely random and the measurements are not affected by loop and regulation
delays, the probability of error is the same for positive and negative voltage steps, the probability
of error need only be considered for positive voltage changes.
The error conditions give constraints on the change in noise in two consecutive measurements, namely, $\Delta n_v$ and $\Delta n_i$; however, they are difficult to analyze due to the presence of the absolute noise terms $n_v$ and $n_i$. On the statistical sense, these terms can be dropped because they are small compared to voltage and current actual values, and have zero-means.

The noise signals added to the measurements are considered independent both from each other and from the states of the system.

The probability density function of the noise changes ($\Delta n_i$ and $\Delta n_v$) is symmetric. A Gaussian distribution function is typical for this kind of noise.

![Figure 4-1 Typical probability density function of noise increments.](image)

The voltage step $|\Delta v_{in}|$ is taken to be a constant, implying a triangular dither signal.

As discussed earlier, the system reaches steady-state whenever $P_{\text{ve}}=P_{\text{ve}}$. If operation at one side only is considered, one of them becomes $P_{\text{error}}$ and the other $P_{\text{correct}}$. Neglecting $P_{\text{zero}}$, the system stops at one side of the curve if a point is found where $P_{\text{error}}=0.5$. 

65
Effect of voltage measurement noise

On the LHS, the expression derived for a decision error is:

$$-\Delta v_{sa} < \Delta n_c < -\Delta v_{sa} - \frac{\Delta i_{sa}}{i_{sa}} (v_{ma} + n_c)$$

(4.16)

The area under the probability density curve in the interval shown in the condition represents the probability of error. This is shown in Fig. 4-2 below.

![Error conditions for voltage noise on the LHS.](image)

Since both bounds are negative, and the curve is symmetric, it follows that $P_{\text{error}} < 0.5$. This means that random noise in the voltage only cannot shift the steady-state operating point to the LHS of the P-V curve.
On the RHS, a decision error occurs if:

\[ \Delta n_v < -\Delta v_{sa} \]  \hspace{2cm} (4.17a)

or

\[ \Delta n_v > -\Delta v_{sa} - \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) \]  \hspace{2cm} (4.17b)

As can be seen from the curve in Fig. 4-3, the probability of error can easily become larger or equal to 0.5. In fact, this happens for higher noise amplitudes, or for lower absolute values of \( \Delta v_{sa} \) and \( \Delta v_{sa} + \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) \).

The term \( -\Delta v_{sa} - \frac{\Delta i_{sa}}{i_{sa}} (v_{sa} + n_v) \) is positive in this case and increases with increasing power-to-voltage slope, that is, for a sharper curve, and further from the MPP. On the RHS, there should be at least one point that satisfies the condition \( P_{\text{error}} = 0.5 \) which represents the point of equilibrium.

![Figure 4-3 Error conditions for voltage noise on the RHS](Image)

**Figure 4-3 Error conditions for voltage noise on the RHS**
Effect of current measurement noise

On the LHS, an error occurs whenever:

\[ \Delta n_i < -\Delta i_{sa} - \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i) \]  

(4.18)

The probability of error is shown in figure 4-4.

![Figure 4-4 Error conditions for current noise on the LHS](image)

The boundary, \(-\Delta i_{sa} - \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i)\), is negative on the LHS and positive on the RHS for a positive voltage step, \(\Delta v_{sa}\). This means that the probability of error in this case is always less than 0.5. The measurement noise in the current does not push the steady-state operating point to the LHS.

On the RHS, the condition for an error becomes:

\[ \Delta n_i < -\Delta i_{sa} - \frac{\Delta v_{sa}}{v_{sa}} (i_{sa} + n_i) \]  

(4.19)
Again, the probability of error cannot exceed 0.5 for random noise, and the system cannot get trapped on the RHS either.

It is notable that random noise in the current measurement does not cause a steady-state error in MPPT. However, a significant probability of error means that tracking becomes slower. In fact, as the operating point becomes closer to the MPP, the absolute value of the term 

\[-\Delta i - \frac{\Delta v}{v}(i_n + n)\]

decreases, allowing the probability of error to increase. This means that in the presence of random current noise, the tracking process becomes slower as the operating point approaches the MPP.

**Effect of measurement noise in both signals**

The conditions for decision errors in this case present conditions for \(\Delta n\) alone and others with both \(\Delta n\) and \(\Delta n\). Better understanding of the joint effect of these signals requires the consideration of their joint pdf.
Figure 4-6 below shows a typical joint pdf of $\Delta n_i$ and $\Delta n_i$. The highest probability is usually associated with the (0, 0) neighborhood region.

Figure 4-7 shows the regions that cause a decision error when the operating point is on the LHS. If $\Delta n_i$ is taken to be zero, the curve reduces to that of the uni-variable pdf of $\Delta n_i$, the error conditions reduce to those of a noisy voltage signal only (compare with Fig. 4-2). As current noise increases, the hill becomes wider along the $\Delta n_i$ axis and the probability of error increases making the tracking slower.

Figure 4-7 Error-producing regions on the LHS
Figure 4-8 shows the error-producing regions on the RHS of the P-V curve. It can be noted that increasing the current noise makes the peak region wider and might cause it to cover a larger area in the error regions. This means that even though current noise doesn’t drive the system to the RHS, it can increase the shift to the right if that was initiated by noise in the voltage.

![Error-producing regions on the RHS](image)

**Figure 4-8 Error-producing regions on the RHS**

**Noisy System Simulation**

Figure 4-9 shows the system-level simulation model of the system. A fairly simple model is used for the solar array. The details of the solar panel model are shown in Fig. 4-10.
The power stage and control loop delays are modeled using simple first order transfer functions with relatively low time constants.
The DSP algorithm was reduced to the part active while operating in MPPT mode. The quantization effect is simulated using simple linear quantizers, and the digital filters are added for the voltage and current measurements.

![Figure 4-11 DSP algorithm model](image)

For the simulation results shown, and unless otherwise indicated, injected noise in current and voltage measurements has $1e^{-8}$ power level.

*Voltage noise vs. current noise*

Figure 2-12 shows the tracking characteristics in an ideal, noise-free system. It is observed that the MPPT algorithm climbs the curve at a high and constant rate until it reaches the MPP. Upon arrival at the MPP, the algorithm stops and no observable fuzziness or excursions exist.
Figure 4-12 Tracking diagram for a noise-free system

With noise added to the voltage, as shown in the Fig. 4-13, the tracking behavior on the LHS of the curve is not altered. The climbing rate of the algorithm is almost equal to that in the case of no noise (this is true on the LHS only). However, after reaching the MPP, the algorithm continues moving to the right and settles at a point on the RHS. The algorithm shows some excursions from time to time after reaching steady state.
Noise in the current has a different effect on the operation of the system. As can be seen in Fig. 4-14, tracking is slowed down and becomes slower as the operating point becomes closer to the MPP. However, the steady-state equilibrium point of the system in not changed, and the system closes in on the MPP.
When noise is added to the voltage and current measurements, the steady state operating point is shifted to the RHS due to voltage noise, and the transient response is slower than that of the ideal case due to current noise. It is notable that the climbing rate is faster than that when noise is inserted to current only, this can be related to the acceleration effect of the voltage noise on the LHS of the P-V curve.
The simulation results shown here follow the expected behavior using the statistical model; furthermore, the results resemble those of the experimental setup. However, it is preferable to verify that the model can actually predict the point of equilibrium. If it does, it can then be trusted.

Statistical model verification

A simple test was carried out to verify the derived equations for the probability of decision errors, and its effect on steady-state operation of the MPPT algorithm. The system is simulated with noise in the voltage measurement only. The results are shown in figure 4-16 below. The operating point moves to the RHS as expected.
According to the statistical model of the MPPT process, the system is expected to find a point at which the probability of increments equals that of decrements of the control variable.

Assuming operation on the RHS, the system stops at the point where the probability of error equals the probability of a correct decision. Assuming a negligible probability of the “NO CHANGE” condition, the system stops when the probability of a correct decision equals 0.5.

As was previously shown, a correct decision is taken in this case if:

$$-\Delta v_{\text{ref}} < \Delta n_r < -\Delta v_{\text{ref}} - \frac{\Delta i_{\text{ref}}}{i_{\text{ref}}} \cdot (v_{\text{ref}} + n_r)$$  \hspace{1cm} (4.20)

In order for this equation to be easily utilized, the $n_r$ term is dropped since it has zero mean, and $\Delta v_{\text{ref}}$ is taken to be a constant. Taking $\Delta v_{\text{ref}}$ as a constant implies using a triangular dither signal in simulation as opposed to a sinusoidal signal as in the experiments.
Figure 4-17 shows the probability density function of the noise signal step injected to the voltage measurement. Figure 4-18 shows the integral of this probability starting at \( \Delta n = \Delta v_{n0} \) (= 6e-3 in simulation).

![Figure 4-17 Probability density function of voltage noise step](image1)

![Figure 4-18 Cumulative probability of voltage noise step](image2)
The probability of a correct decision can be read from Fig. 4-18 by reading the value of the curve at the point: \( \Delta n_i = -\Delta v_{m} - \frac{\Delta I_{m}}{i_m} (v_{m} + n_r) \). At the point of statistical equilibrium, this should be 0.5.

From the curve in Fig. 4-18, \(-\Delta v_{m} - \frac{\Delta I_{m}}{i_m} (v_{m} + n_r)\) at equilibrium is around 0.013. This makes \(\left| \frac{\Delta I_{m}}{\Delta v_{m}} \right| \frac{v_{m}}{i_m} = (0.013+0.006)/0.006 = 3.17\).

![Figure 4-19 Absolute and incremental conductance estimation at the point of equilibrium](image)

From the I-V characteristics shown in Fig. 4-19, this value can be estimated at the point of equilibrium. \(\left| \frac{\Delta I_{m}}{\Delta v_{m}} \right| \frac{v_{m}}{i_m} = (0.68 - 0.47)/(0.938 - 0.847) (0.89/0.6) = 3.42\) which is very close to 3.17 given the level of approximation used.
**Digital filtering enhancement**

In the presence of ground loops, supply noise, and EMI interference, it is difficult to attenuate the noise effectively in the analog domain. Digital filters provide a very powerful tool for that purpose.

Figure 4-20 below shows the frequency response of a 3rd order digital IIR filter used for voltage and current measurements both in simulation and in the experimental setup.

![3rd order digital filter response](image)

**Figure 4-20 Phase and gain of a 3rd order digital filter used in the DSP**

The design of the filter shown took into consideration the minimization of attenuation applied to the signals up to 200 Hz which corresponds to twice the dither frequency. Moreover, near-linear phase was achieved for that range of frequencies.

Figure 4-21 shows the simulated behavior of the system when the filter is applied. The system climbs to the MPP at a high rate, almost equal to that of the ideal system; moreover, the system stops at the MPP with minimum deviations and excursions. The filter certainly enhances
both the steady-state and the transient response of the MPPT process. These enhancements delivered by the digital filter were also noticed in the experimental setup.

![Tracking diagram of a noisy system with the filter applied](image)

**Figure 4-21 Tracking diagram of a noisy system with the filter applied**

Anti-Noise Recommendations

The point of origin of the \((\Delta n, \Delta n)\) plane –corresponding to noise free measurements- naturally falls in the correct decision region at all times. The system performance is enhanced when noise probability is concentrated around that point. As seen earlier, the system becomes better if:

1. The noise had less amplitude, allowing a narrower pdf and a lower probability of error. A very effective way of achieving that is using digital low-pass filters for the measured voltage and current signals.
2. The error-producing regions were pushed away from origin. This can be achieved by increasing the effective $|\Delta v_\omega|$ value. That, in turn, can be achieved by perturbing the system using a zero-mean dither signal added to the MPPT reference.

Moreover, the statistical model predicts that at least two apparently attractive methods can seriously harm the system performance. These are:

1. Hysteresis constraint for $\Delta \bar{v}$: this constraint prevents the algorithm from taking a decision for updating the reference voltage if the measured change in voltage is less in magnitude than a pre-determined value. Figure 4-22 (a and b) shows the values of the noise that cause the readings to be discarded. The discarded areas in the correct-decision areas are closer to the origin and correspond to higher probability. This means that on average, this constraint discards more correct decisions than bad ones!

2. Impossible slope cancellation: this test is based on the fact that for solar arrays, the incremental conductance $\frac{di}{dv}$ is always negative. If $\Delta \bar{v}$ and $\Delta \bar{i}$ of the same sign are detected, that iteration is discarded. The problem with this condition is that it only rejects noise urging increments in the reference voltage. It never rejects erroneous decrements in the reference. This works wonderfully on the RHS, but unfortunately produces a problem on the LHS. With this condition in place, the system can settle on the LHS.
Experimental Results

The statistical model was put to the ultimate test by investigating its predictions in the experimental setup. After verifying the basic predictions, the anti-noise recommendations were applied to enhance the system performance. Experimental results showed close correspondence to the model.
Figure 4-23 below shows experimental voltage (top) and current (bottom) waveforms obtained for different conditions. In order to observe the transient response of MPPT, the load is momentarily decreased, driving the channel out of MPPT, and allowing the MPPT to be reset. That is followed by an increased load that allows the MPPT algorithm to take control.

Figure 4-23.a shows that the MPP voltage is around 46V. Basic MPPT –Fig. 4-23.b- settles on the RHS at around 50V. Adding a hysteresis window to the voltage does not enhance the settling point, and only slows the climbing down; see Fig. 4-23.c. Figure 4-23.d shows that the di/dv test totally destroys MPPT. With an analog LPF before sampling the voltage, noise is lowered and the algorithm settles at the MPP, however, the response is slow and fuzzy, see Fig. 4-23.e. Finally, Fig. 4-23.f shows near-ideal performance when digital low-pass filters are added to the DSP code.
Figure 4-23 Experimental MPPT results (a) P-V curve (b) basic PnO (c) with dv hysteresis (d) with di/dv test (e) with analog LPF for voltage signal (f) with digital filters

Understanding this model can greatly help developers of such system in debugging MPPT and designing extra fault tolerance procedures for avoiding unexpected behavior in severe situations.
CHAPTER 5: PARALLEL OPERATION AND CURRENT-SHARING FOR
THE MODULAR SOLAR POWER SYSTEM WITH MPPT

Single channel structure

The basic building block of the system is a solar-powered MPPT channel. The basic block diagram of the channel is shown in Fig. 5-1 below.

![Figure 5-1 Block diagram of a single solar channel with MPPT](image)

Each channel has a number of input and output paralleled COTS converters, each with its own OVR controller. However, only one OVR controller takes control, and competes with the IVR controller to win command over all peak current controller modules. Since all converters share a single current command signal at all times, uniform current sharing is always maintained within the channel (intra-channel sharing). The competition between the OVR and IVR controller loops is settled depending on the loading condition. The IVR controller wins control...
whenever the OVR attempts to drive the solar array voltage (input voltage) below the command set point provided by the system controller. This condition occurs whenever the loading applied to the channels exceeds its available power causing its input voltage to collapse, or when the system controller raises its command set point signal in attempt to limit the power processed by that channel.

Typical output characteristics of a single channel are shown in Fig. 5-2. Operation in OVR follows the lower right part of the curve. The slope of that portion of the curve depends on the dc output resistance of the converter. If that is zero, the line becomes vertical. In IVR, the channel basically becomes a constant power source. That is depicted by the inverse I-V curve to the upper left.

![Figure 5-2 Dc Output characteristics of a solar powered channel with MPPT](image)

Multi channel system structure and model

Independently sourced solar channels are paralleled at the output side to form the output bus. Also connected to the output bus are the load, and the battery subsystems. At any particular
point in time, a number of solar-powered channels operate in IVR, while the others operate in OVR. The system model is shown in Fig. 5-3.

**Figure 5-3 Scalable solar-powered system model**

A channel operating in OVR can generally be modeled by a voltage source in series with a small output resistance, as well as an ideal diode to account for unidirectional power flow. Channels operating in IVR are virtually independent from the load, and provide constant power to the output bus. This constant power translates to constant current given that the output bus voltage is tightly regulated by other channels at the same bus. The amount of current they deliver is primarily dependent on the command set point provided by the DSP (channel controller) to the input voltage regulator module, and the amount of input power available at that particular point on the curve.

**System operation with no current sharing**

Assuming negligible output channel resistance, which is a justified assumption especially if remote sensing is utilized, load current distribution is not uniform among different channels (inter-channel sharing). In fact, channels are sequentially activated depending on their output voltage regulation reference tolerances. One channel, the one with the highest OVR reference,
processes all power for very light loads. With increasing load, that channel switches to MPPT and operates in IVR while another gets partially loaded. The latter channel operates in OVR, and regulates the bus. A third is then activated once the load demand drives the second into MPPT, and so on. At any point in time, a number of channels behave as current sources (IVR), one channel behaves as a voltage source and supplies current, and regulates the bus voltage, while the others behave like voltage sources that are blocked by their diodes and supply no current.

**Targeted current sharing characteristics**

To achieve maximum reliability and stability, channels need to be simultaneously activated, that is, process the same amount of power at light loads. For the system in concern, limited power resources are available for each channel. If the required value of output current drives a particular channel into MPPT (due to limited available input power), that channel should keep operation at the MPP while uniform current-sharing is maintained among other channels not in MPPT, see Fig. 5-4 below.

![Figure 5-4](image)

(a) sequential activation (natural)  
(b) targeted current sharing

*Figure 5-4 Power stress distribution among channels in the system*
While achieving this power stress distribution, the current sharing scheme should preserve the attractive features of the system. The current sharing scheme should accommodate MPPT operation and should as well preserve tight output bus voltage regulation whenever the combined loading power is less than that available from the sun.

Proposed current-sharing implementation schemes

The DSP controller already present in the system can be used to achieve current sharing if adequate hardware and software modules are added to the system. Four main components are needed:

1. Output current measurement/estimation method.
2. A current-sharing bus.
3. Current-sharing algorithm (software).
4. DSP control over processed power distribution.

Since the input power is readily available to the DSP chip for use in MPPT, and assuming positive incremental efficiency at all operating points, output current sharing can be achieved by input power matching. If this assumption proves not accurate enough for a specific application, additional output current sensing circuitry can be used. Such a change would only have marginal effects on the algorithm implementation.

The current sharing algorithm is heavily dependent on the method by which the DSP controls the amount of power being processed by its corresponding power stage. Two main control pins available on the COTS converters can be used to achieve DSP control over processed power. These are the parallel pin, and the trim pin. A current-sharing scheme can be tailored around either pin.
Parallel pin based scheme

The IVR controller present in the system uses the parallel pin to clamp the solar array voltage to a minimum value determined by the DSP chip. Whenever the DSP chip generates a reference voltage on the RHS of the PV curve, the power processed by that channel cannot exceed the amount of power available at that point in the curve. If the OVR circuitry attempts to drive the power stage to a point of higher power, the IVR circuitry takes control and that channel behaves as a current source as discussed earlier.

Current sharing can be achieved by pushing the input voltage of the channels processing too much power to the RHS, thus limiting their processed power, and allowing other channels to catch the remaining power. During current sharing operation, increasing the input voltage reference will decrease the amount of power being processed by that channel. This is valid on the RHS side of the PV curve.

If the amount of power the channel needs to process to achieve current sharing is higher than the available power at its input, the algorithm keeps decreasing its IVR reference. When that happens, that channel should switch to MPPT operation. This can be achieved if the DSP outputs the maximum of the MPPT reference voltage, and the voltage set point calculated by the current sharing algorithm. This basically means that the channel is only allowed to operate on the RHS of the input PV curve or at the MPP.

In order to preserve tight output voltage regulation, all channels should not be allowed to operate in power limit (PL) mode at the same time. One channel should always be allowed to operate in OVR mode and regulate the output bus.

Upon application of a light load, one channel catches it while the others process no power. The current sharing algorithm then forces that channel to power limit mode, thus enabling
other channels to be activated and pick up the rest of the power. This process continues until all channels process the same power. The last channel to be activated is the one with the lowest OVR reference. That channel is the only one to operate in OVR, it regulates the bus, and its processed power value serves as the reference power to which all other channels limit their power. As the load increases, some channels might eventually switch to MPPT whenever the power required is higher than their available input power. These channels need to declare the highest possible number as their processed power in order to avoid other channels trying to limit their power to follow them.

If the channel with the lowest OVR reference, the one in OVR, has limited power resources, it switches to MPPT. When this occurs, channels in power limit should retreat and allow more power to be processed in order not to lose output voltage regulation. However, that retreat action would cause the last channel to go back to OVR, and thus lose current sharing. It is important to ensure that it stays in MPPT while another picks up output voltage regulation. This can be done by increasing its OVR reference. Therefore, it is important that the DSP gets at least 2-level control over the OVR voltage reference of its corresponding power stage. This can be achieved by manipulating the trim pins of the COTS converters.

To sum up, the Fig. 5-5 below shows the parallel-pin based current sharing algorithm.
This scheme can achieve the targeted power distribution characteristics while preserving output voltage regulation in steady state. Unfortunately, this scheme is complicated, involves multiple operating modes, and is not easy to stabilize in times of transient loading. Moreover, for relatively large load transients, if the channel regulating the bus switches to MPPT, the output voltage regulation is lost for a relatively long time. This time is needed for detecting this mode transition, and for the power limiting channels to allow more power flow.

This scheme is suitable for systems in which a battery is present at the output bus, and for which output voltage regulation is not a sensitive issue.

Trim pin based scheme

For channels operating in output voltage regulation (OVR) mode, non-uniform current distribution is caused by tolerances in OVR references and droop characteristics. Given enough output droop resistance, real-time adjustment of the OVR reference through the manipulation of the feedback voltage sense signal can force the system into desired power distribution patterns.
The steady-state output characteristics of a single solar-powered channel with OVR_MOD functionality is depicted in the Fig. 5-6 below.

![Output characteristics with the OVR.MOD function](image)

**Figure 5-6 Output characteristics with the OVR.MOD function**

The effect of changing the output voltage reference of a single channel on the output current distribution is shown in Fig. 5-7. This figure assumes that the total output current is not enough to drive either channel into IVR.

![Current distribution among two channels in OVR](image)

**Figure 5-7 Current distribution among two channels in OVR**
For current sharing operation, these channels should be operated in the transition region. Fine tuning of the reference voltages of these channels can achieve the desired power distribution.

Given positive output resistance of all channels, the power being processed by a certain channel increases with increasing OVR reference. If a channel runs out of input power, it switches to MPPT, and other channels naturally continue regular current sharing operation. Channels operating in MPPT should not be allowed to increase their OVR references further since that would increase the transient period needed for the system to settle after the load decreases again to a point where these channels should operate in OVR.

The basic trim-pin based current sharing algorithm is shown below.

The OVR_MOD function, namely, fine DSP control over the OVR reference can be achieved using the circuit in Fig. 5-9. Since the DSP is referenced to the input ground, while the trim is referenced to the output, an opto-coupler is important to preserve the input/output isolation provided by the COTS converters.

Figure 5-8 Controller model of the trim-pin based current sharing algorithm
The trim pin based scheme has a very important advantage over the parallel pin scheme; it doesn’t have the power limit mode. This means that all the input power available from the input sources is almost instantaneously available to the output, and is only delayed by the relatively high bandwidth OVR regulation loop as opposed to the significantly slower digital current-sharing loop as for the parallel pin scheme. This scheme is not heavily operating-mode dependent, is easy to stabilize, and allows very fast output voltage regulation.

Detailed analysis of trim pin based scheme

Detailed analytic and numerical analyses of different system parameters and control gains are needed to enable the design of an optimal control loop given the resources available.

Control range requirements

The open circuit voltage of each channel is set to a nominal value of 28V with no output voltage trimming. There is certain tolerance to this value. That means that all channels’ open circuit voltage values would fall between two values, \( V_{L_{\text{min}}} \) and \( V_{L_{\text{max}}} \).

The OVR modifier circuit is designed to trim the output voltage up. At the maximum DAC voltage applied to it, it would add some increment \( \Delta \) to the open circuit voltage, raising it
to another value ranging between two values, $V_{Hmin}$ and $V_{Hmax}$. Assuming small tolerance in the OVR modifier board components, it follows that $V_{Hmin} - V_{Lmin} = V_{Hmax} - V_{Lmax} = \Delta$.

![Figure 5-10 Trimmed and untrimmed output voltage values](image)

The designed value for $\Delta$ should be determined to allow current sharing at all loading conditions and with worst conditions assumed in terms of output voltage reference tolerances and output resistance variations.

$V_{oHmin}$ and $V_{oLmax}$

Assume a number of channels have already achieved successful current sharing. There is a limited range over which the output voltage at the bus, $V_o$, can be swept. The worst case scenario is such that this control range is narrowest. It is then important to find $V_{oLmax}$ and $V_{oHmin}$.

$V_{oL}$ is the output bus voltage given that all channels are attempting to decrease their voltages while preserving current sharing. In the worst case, at least one channel has $V_{Lmax}$ as its $V_L$ value, and the lowest possible output resistance. Since proper current sharing is assumed, it processes its share of the output current, $I_{sh}$. It follows that:

$$V_{oLmax} = V_{Lmax} - R_{omin} I_{sh}$$

(5.1)
Similarly, $V_{oh}$ is the output bus voltage given that all channels are attempting to increase their voltages while preserving current sharing. In the worst case, at least one channel has $V_{h_{\text{min}}}$ as its $V_h$ value, and the highest possible output resistance. Since proper current sharing is assumed, it again processes its share of the output current, $I_{sh}$. It follows that:

$$V_{oh_{\text{min}}} = V_{h_{\text{min}}} - R_{\text{omax}} I_{sh}$$

(5.2)

$V_{h_{\text{min}}}$, $V_{L_{\text{max}}}$, and $\Delta$

With another channel added, two worst case scenarios can be assumed:

1. Added channel has $R_o = R_{\text{omin}}$, and $V_L = V_{L_{\text{max}}}$, to achieve sharing:

$$V_{L_{\text{max}}} - V_{oh_{\text{min}}} = R_{\text{omin}} I_{sh}$$

(5.3a)

substituting for $V_{oh_{\text{min}}}$ from (5.1):

$$V_{L_{\text{max}}} - V_{h_{\text{min}}} = (R_{\text{omin}} - R_{\text{omax}}) I_{sh}$$

(5.3b)

or

$$V_{h_{\text{min}}} - V_{L_{\text{max}}} = (R_{\text{omax}} - R_{\text{omin}}) I_{sh}$$

(5.3c)

2. Added channel has $R_o = R_{\text{omax}}$, and $V_h = V_{h_{\text{min}}}$, to achieve sharing:

$$V_{h_{\text{min}}} - V_{oL_{\text{max}}} = R_{\text{omax}} I_{sh}$$

(5.4a)

substituting for $V_{oL_{\text{max}}}$ from (5.2):

$$V_{h_{\text{min}}} - V_{L_{\text{max}}} = (R_{\text{omax}} - R_{\text{omin}}) I_{sh}$$

(5.4b)

Both worst case conditions yield the same design requirements, given in (5.3c). $\Delta$ is the immediate design parameter, governing the design of the OVR_MOD board, it can be expressed as:

$$\Delta = V_{h_{\text{min}}} - V_{L_{\text{min}}} = (V_{h_{\text{min}}} - V_{L_{\text{max}}}) + (V_{L_{\text{max}}} - V_{L_{\text{min}}})$$

(5.4)

The second term directly relates to the COTS converters voltage reference tolerance and can be determined from their datasheet. Combining that with the value found for the first term
from equation (5.3), the $\Delta$ value for which the OVR_MOD should be configured can then be determined.

**Stability analysis, and control loop design recommendations**

The current-sharing algorithm should be investigated from a control system perspective. A simple diagram is depicted in the Fig. 5-11 below.

![Figure 5-11 Control flow of a system with trim-based current sharing](image)

**$V_{OVR\_MOD}$ to $P_{in\_k}$ transfer function**

This block models the effect of a change in the DAC voltage controlling the trim pin on the input power processed by that same channel. The dc transfer characteristics can be derived from the following model:

![Figure 5-12 Current distribution model](image)
This model consists of three branches: the OVR channel \( k \) for which the analysis is being conducted, the combined model of all other channels operating in OVR, and the effective combined loading on the OVR channels. This loading current is the difference between the actual loading current and the combined contribution of all channels operating in IVR. Note that for this scheme, all IVR channels are basically operating in MPPT since there is no power limit mode. These IVR channels do not directly affect the current distribution and are thus combined with the load.

\[
\frac{dP_m}{dV_{\text{OVR\_MOD}}} = d\left[ \frac{P_m}{P_m} \cdot I_o \cdot V^k_{\text{out}} \right] = \frac{dV_{\text{OVR\_MOD}}}{dV_{\text{OVR\_MOD}}} = \frac{1}{\text{Eff}} \cdot \left( I_o + V^k_{\text{out}} \cdot \frac{dI_o}{dV^k_{\text{out}}} \right) \cdot \frac{dV^k_{\text{out}}}{dV_{\text{OVR\_MOD}}} = \frac{k_{\text{control}}}{\text{Eff}} \cdot \left( I_o + V^k_{\text{out}} \cdot \frac{dI_o}{dV^k_{\text{out}}} \right)
\]

(5.5)

\( I_o \) is generally negligible compared to \( V^k_{\text{out}} \cdot \frac{dI_o}{dV^k_{\text{out}}} \) because \( R_o \) is very small:

\[
\frac{dP_m}{dV_{\text{OVR\_MOD}}} \approx \frac{k_{\text{control}}}{\text{Eff}} \cdot \frac{V^k_{\text{out}}}{\text{Eff}} \cdot \frac{dI_o}{dV^k_{\text{out}}} = K \frac{dI_o}{dV^k_{\text{out}}}
\]

(5.6)

from the model shown in the figure above, \( \frac{dI_o}{dV^k_{\text{out}}} \) can be shown to be:

\[
\frac{dI_o}{dV^k_{\text{out}}} = \frac{1}{R_o^i + R_e^i \parallel R_e^i \parallel \ldots \parallel R_e^i} \\
\approx \frac{1}{R_{\text{typical}} + \frac{R_{\text{typical}}}{m-1}}
\]

101
\[ V_{\text{OVR MOD}} \text{ to } P_{\text{in}}^\text{other} \text{ and } P_{\text{bus}} \text{ transfer function} \]

This block models the effect of a change in the OVR modifier voltage of one channel on the amount of power being processed by other channels operating in OVR. This has a direct effect on the Pbus reference being targeted by that particular channel.

An incremental change in \( V_{\text{OVR MOD}} \) generally produces limited current variation in that channel. This produces a small change in the net loading applied to the other channels. This small change in loading is not expected to have a pronounced effect on the power distribution over other channels in OVR. Generally, it is expected that the change would be distributed among those channels.

Since the amount of change in the Pbus value is directly related to changes in the power being processed by those OVR channels, an approximation of that change would be:

\[ \Delta P_{\text{bus}} \approx \frac{\Delta P_{\text{in}}^k}{m-1} \]

where:

\( \Delta P_{\text{in}}^k \) = the amount of power change in the channel itself due to the change in its OVR modifier control voltage.

\( m \) = the total number of channels operating in OVR, and supplying load current at that point in time.
Effect of the number of OVR channels on system gains

The overall loop gain starting from a change in the control variable induced by the algorithm and ending at the amount of change of the input to the algorithm is a key factor for algorithm stability.

The input to the algorithm is the difference between the calculated power signal and the \( P_{bus} \) reference, it follows that:

\[
\Delta(p^i - P_{bus}) \approx \frac{\Delta P^i}{m-1} + \frac{\Delta P^i}{m-1}
\]

\[
= \frac{m}{m-1} \cdot \Delta P^i
\]

(5.9)

using the estimate found before for Iok and Pink:

\[
\Delta(p^i - P_{bus}) \approx \frac{m}{m-1} \cdot K \cdot \frac{\Delta V_{OVR\_MOD}}{R_{\text{sys}}} \]

\[
= K \cdot \frac{\Delta V_{OVR\_MOD}}{R_{\text{sys}}} \]

(5.10)

Since \( K \) was found to be virtually a constant, the overall gain from the output of the algorithm, \( \Delta V_{OVR\_MOD} \), to its input, \( \Delta(p^i - P_{bus}) \), is virtually independent from the number of channels operating in OVR and the net loading current applied to them. This property can greatly simplify the design.

Control loop design recommendations

The control loop design can be designed and tested for a two channel system. With enough design margins, the loop is expected to perform well for a multi-channel system. In order to improve both stability and transient response, a PID controller is preferred rather than comparative control. That also linearizes the loop and simplifies analysis.
It is important to ensure high control resolution, and low feedback resolution to avoid limit-cycle-related instability. 8-bit values for `p_share` and `P_{bus}` where experimentally shown to be sufficient to achieve good results. In addition to other system parameters, output droop resistance and OVR_MOD board gain affect forward control resolution by affecting the coefficient K in the analysis results presented earlier.

*Ensuring output droop*

As seen in the stability analysis section, the minimum and maximum permitted output resistance values are critical for design and stability insurance. Output resistance of 5-10 mΩ presents a good range given the design requirements for this system: it provides good control resolution, and low maximum output voltage drop at high loading (around 0.2Volts).

Output resistance can be physically introduced; it would be the sum of all connector and power stage resistances present between the output bus and the voltage sensing point. Using this configuration, a minimum output resistance can be insured, but the maximum depends on the length of the cables. Large output resistance values will slow down the current sharing response—for a system designed for lower resistances— and deteriorate output voltage regulation.

On the other hand, if the sense pins of the power stage are taken all the way to the output bus, the output resistance is reduced to an unacceptably small value. That will destabilize the current sharing control loop.

The trim pin can again be used, with simple added circuitry to introduce output droop, while the sense pins are taken all the way to the bus. That is to say, sufficient output resistance can be introduced to the output of the power stage that is independent on the connector cables.
and other largely variable parasitics. This can be achieved by using a modified version of the OVR_MOD board shown here.

![Figure 5-13 OVR_MOD circuitry with programmed $R_o$](image)

This circuit basically gets a measurement of the output current through the $I_{sen}$ connector, differentially amplifies it, and draws a dependent current from the trim pin. The circuit is configured to sink more current from the trim pin for less output current, that is, increase the output voltage for less output current. This operation ensures pre-designed output resistance values while leaving the remote sense pins free to go all the way to the bus.

Proposed sharing bus programs

A current sharing bus is required for inter-channel information exchange. A digital bus scheme is preferred for a number of reasons, some of which are:

1. Easy electrical isolation.
2. Enhanced noise immunity.
3. Reconfiguration flexibility.
4. Ability to avoid pitfalls of existing analog approaches.
At the two-channel experimental stage, digital communication was provided by an isolated Serial Communication Interface (SCI) bus. However, this configuration only provides point-to-point communication and cannot be used for a larger system. For a scalable power system, a digital network needs to be created that links the DSP chips. The Controller Area Network (CAN) bus protocol was used for the following reasons:

1. Core module available on DSP chip used, TMS320LF2407a.
2. High bit-rate.
3. Support for large number of nodes.
4. Broadcast operation possible.

A broadcast scheme is adopted for the bus. Depending on the bus program selected, one or more channels keep broadcasting their \( P_{\text{share}} \) values. Each channel collects all the values broadcast within one sampling period and processes them to take a decision.

In order to accommodate MPPT and achieve targeted operation, channels in MPPT for which \( P_{\text{bus}} \) is higher than the processed power do not declare their presence in the system. They constantly monitor the \( P_{\text{bus}} \) value. Whenever \( P_{\text{bus}} \) becomes lower than the power they process, they start posting their power values on the bus, and contributing to the calculation of \( P_{\text{bus}} \). Different bus programs can be used to explicitly or implicitly generate a value for \( P_{\text{bus}} \), these include:

[1] Average bus program: for this bus program, \( P_{\text{bus}} \) is the arithmetic average value of power measurements collected from the communication bus. The calculation of an exact value of that requires the division by the number of channels posting their power values on the bus, which is an arbitrary number that dynamically changes for different system sizes and loading conditions.
Since the division operation is computationally intensive, an alternative realization uses the fact that the current-sharing algorithm can rely on comparison rather than proportional error control techniques:

\[
\text{sign}(P_{in} - P_{bus}) = \text{sign}(P_{in} - \frac{\sum P_{other}}{m-1})
\]

\[
= \text{sign}((m-1)P_{in} - \sum P_{other})
\]

This can be efficiently realized in a DSP-based computational environment. It requires no division. However, if the DSP has enough bandwidth, implementing division can yield an explicit average value and enable PID implementation of the algorithm.

The main disadvantage of this scheme is that the bus bandwidth needed is directly proportional to the number of channels on the bus; congestion is a serious issue for large power systems.

[3] Median bus program: this scheme does not really generate a value for \( P_{bus} \). Instead, each channel counts the number of channels processing more power than it does, and those processing less. A decision for control increment or decrement is based on comparing those two numbers. This program is named the “median program” since it results in making the median power value among OVR channels the point of attraction for all channels in the system.

This scheme requires high communication bus bandwidth, and is not suitable for PID implementation due to its implicit \( P_{bus} \) result.

[4] Min-max bus program: this bus program basically keeps track of two power values, the minimum and maximum power being processed. Comparative control is used, the channel with maximum power attempts to decrease its power, while the one with minimum power
attempts to increase its own. Other channels do not produce control decisions, and wait until they become minimums or maximums.

An important advantage of this bus program is that the same communication bus bandwidth is needed for systems of different sizes, since two channels only broadcast their power values at any point in time. An important disadvantage is that it produces a slower current sharing response for larger systems.

[5] Min-max average bus program: this is similar to the previous program in that it keeps track of both the minimum and maximum processed powers. However, the average value of these two values is taken to be $P_{bus}$. This can then be used with either PID or comparative control techniques.

For the experimental prototype, the explicit average bus program has been selected, with division carried out by the DSP chip in order to enable PID control.

Paralleled Channel Simulation

A model of the system was built in Matlab’s Simulink in order to simulate the current sharing algorithm. This model is detailed, and can account for a number of non-idealities in the system. The experimental results later collected closely match the results this simulation platform yields.

The basic simulation setup is shown here.
The simulation platform consists of four solar powered channels. Each channel takes the open circuit voltage and short circuit current values as inputs. It produces a value representing the output current it delivers. All the output currents are summed up and fed to a constant current (CC) load simulator, with finite capacitance. The load simulator uses the current values to
calculate the output voltage, this is fed back to the solar channels in order for them to determine the output currents, and to run in OVR when required to.

![Figure 5-15 Capacitive constant current simulation model](image) In order to realize current sharing, the current sharing bus is constructed. To simulate the transmission enabling/disabling feature of the applied scheme, two signals are generated per channel; these are the p_share value, and the psh_flag. Each signal type is collected from all four channels and summed. The two resultant values are then fed back to all channels.

Each solar powered channel contain three main blocks, these are the solar array simulator (SAS), the power stage, and the digital control algorithm.

![Figure 5-16 Single PV powered channel simulation model](image)
The solar array simulator model produces a value for the solar array voltage based on the current drawn from the array and the curve parameters, namely, open-circuit voltage, and short-circuit current. Its model is shown below.

![Solar array simulation model](image)

**Figure 5-17 Solar array simulation model**

The power stage takes the voltage and current values from the SAS, and uses them to determine the output current, and to update the input current value.

![Converter simulation model](image)

**Figure 5-18 Converter simulation model**

The power stage model basically uses the power conservation concept to determine the output current based on the input power, and the output voltage values. The output voltage value
is generated by the load simulator as described before. The input current drawn from the input is basically determined as the minimum of the two commanded values of the two competing controllers of the converters, the OVR and IVR controllers.

The input voltage regulator (IVR) is a simple error amplifier that basically attempts to regulate the input voltage to the value commanded by the digital controller.

![Figure 5-19 Input voltage regulator model](image)

The output voltage regulator is a little more complicated. It basically consists of an error amplifier too, but the voltage reference consists of three main components. These are the untrimmed voltage reference, 28+/-.28V, the OVR modifier command provided by the digital controller, and the output resistance emulation term, which is a value directly proportional to the output current.

![Figure 5-20 Output voltage regulator model with OVR_MOD and output droop](image)
The third and last block inside the single channel model is the digital controller. The basic setup for that is shown below.

![Digital controller simulation model](image)

**Figure 5-21 Digital controller simulation model**

The digital controller has solar array voltage and current values as input. These directly pass through quantizers and low pass filters. Three main subsystems are found within this controller simulator.

The PnO algorithm simulator basically runs the Perturb and Observe algorithm to achieve MPPT, it generates the input voltage reference signal.
Another block is the OVR detection block, which basically checks for the operating mode, and supplies the rather critical signal, OVR_flag, to both the PnO (MPPT) model and the current sharing model. This block declares OVR operation whenever the measured input voltage exceeds the MPPT commanded voltage by a certain predetermined threshold value.

Last but not least, is the current sharing algorithm simulator. This block takes the measured power value, as well as the resultant $P_{bus}$ value from the current sharing bus, and processes them to generate the OVR modifier value used to compensate the output voltage reference of the converters in order to achieve the targeted power distribution.
The simulation results for the four channel model shown and described above are shown here.

Figure 5-25 Simulation results for the four channel system with trim-based current sharing
The upper figure of the simulation results represents the amount of input power being processed for each of the four channels in the system. At low power values, all the traces follow each other. As the total power (load power) increases, different channels switch to MPPT and their power values settle to the maximum available power values from their corresponding solar arrays, while other channel still in OVR continue to achieve current sharing. The bottom figure represents shown the output voltage ripple. Note that the ripple is within the ripple amount expected from a single channel.

It is also noticeable that there is a dip in the processed power values of different channels as they switch from MPPT to OVR, however, that dip is quickly recovered. Most importantly, this interval of loss in current sharing does not present a problem for output voltage regulation. The output voltage is regulated to satisfaction at all times.

Experimental results

Shown in Fig. 5-26 below are two identical PV-powered channel prototypes. Each channel has 2 COTS converters, each rated at 28V, 250W, totaling to 500W/channel, as well as the digital control board. The digital controller realizes both MPPT and current sharing control, and handles communication with other controllers in the system through the CAN bus.
Figure 5-26 Experimental prototype

Figure 5-27 below shows experimental waveforms captured for a two channel system with no battery when loaded by a triangular constant-current-sink load.

Figure 5-27 Experimental results for a two channel system

Traces 1 and 2 represent the input power values for both channels as measured by their DSP’s. The power traces match at the lower values signifying proper load sharing. As the
loading increases, channel 2 switches into MPPT mode, and thus its power value levels off at a value corresponding to its maximum available input power. As the load increases further, channel 1 enters MPPT mode too, and its power value levels off.

Trace 3 represents the output voltage at the bus. It can be seen that it is tightly regulated to 28V, and is not affected by current sharing. However, the voltage drops when both channels operate in MPPT. This is due to the limited input power resources, and the absence of a battery at the output bus. Trace 4 shows the total output current of system.

A total of four channel prototypes were constructed in order to demonstrate the controller functionality for a scalable power system. Figure 5-28 shows the power waveforms as seen by the DSP’s for the four different channels when a ramp load is applied to the system. It can be seen that the distribution of processed power among all channels matches the targeted characteristics described earlier. It is important, however, to note the sharp transient in the power distribution whenever a channel exits MPPT into OVR. This latency is caused by both the latency in mode transition due to the competing control loops (OVR and IVR), and the delay in mode detection by the DSP.
The experimental results show very good correspondence to the simulation results as well as the targeted system characteristics. It was also experimentally shown that the different time constants in the system are virtually indifferent to the number of channels in the system.
CHAPTER 6: SUMMARY AND CONCLUSIONS

Solar energy is a promising technology for meeting the ever-increasing power demand. It is an abundant, renewable, and environment friendly power source. These merits of solar energy, however, were countered by its fluctuating nature, low utilization efficiency, and high initial investment requirement. These challenges were further toughened by the scarcity of engineering experience with solar sources. In many practical designs, the average power extracted from solar arrays can be as low as 10% from the power incident at their surfaces. The development of new techniques for solar cell manufacturing and efficient power extraction and processing is very critical for bringing down the cost of solar energy to the range where it is feasible. This thesis provides an overview of common practices for the design of solar power harvest systems, and proposes new approaches and recommendations for enhancing practical designs in terms of utilization efficiency and reliability.

Traditional power system concepts led designers to approximate a solar source by a voltage source. This approximation yielded very simple systems with low complexity and cost. Unfortunately, because solar arrays exhibit largely non-linear terminal I-V characteristics, such systems yielded very bad voltage regulation. The introduction of tightly regulated power converters to stabilize load voltage has introduced the problem of negative impedance instability, which can be directly related to the limited value of power available from these sources. Maximum Power Point Tracking (MPPT) was introduced as a control strategy that avoids this failure mechanism and controls the system to extract the maximum attainable power form the source. A number of system architectures were introduced in literature and in the field for accommodating MPPT.
As the power demand applied to such systems increases, the design of modular parallel-structured systems becomes an imminent necessity. Systems that accommodate a number of solar arrays and power converters that operate in parallel provide merits such as system scalability, redundancy, fault-tolerance, and hot-swap capabilities. An attractive architecture was chosen to construct a modular MPPT-compatible solar power system for space applications. This architecture is studied in chapter 3, discussing the practical design challenges and implementation issues. System operation is verified experimentally by constructing a multi-channel prototype.

Numerous MPPT algorithms can be found in literature. Among the most popular of those are the so-called hill-climbing algorithms. This class covers the PnO algorithm and several modified versions of it. These algorithms rely on continuous measurements of voltage and current of the solar array to locate the Maximum Power Point (MPP). They provide a flexible scheme that can be applied to various sources and handle large drifts in terminal characteristics. Due to their high non-linearity, they are particularly susceptible to measurement noise. Careful understanding of the effect of noise is important to facilitate debugging of these algorithms in practical setups. This is the focus of chapter 4. It introduces a new statistical model that is employed to evaluate a number of noise-fighting techniques for validity and performance. Recommendations are then given that are backed by the results in the experimental setup mentioned earlier.

As is common in paralleled converter systems, the modular paralleled system architecture chosen for the system does not provide uniform current and power stress distribution among the paralleled channels. System reliability can be significantly enhanced by introducing active control to distribute this stress. Many traditional current/power sharing techniques cannot be
directly applied to this system. This is because of the limited input power resources available for these different channels, and the need for accommodating MPPT. Chapter 5 introduces a practical scheme for achieving current sharing control while preserving the attractive features of the system: modularity, MPPT, and tight bus voltage regulation. This is achieved by depending on the flexibility and functionality of digital control. The result is a flexible, fault-tolerant, modular power system with optimized reliability at very low incremental cost.

The system presented here is an attractive design since it combines efficient resource utilization, reliability, cost effectiveness, and accelerated design and development.

Many of the concepts and design challenges addressed here are common with other solar-powered applications. An important field is terrestrial distributed generation using solar-powered grid-connected inverters. The design of such inverters is targeted by the following research project.
REFERENCES


124


