Effect Of Annealing On Copper Thin Films: the Classical Size Effect And Agglomeration

2005

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EFFECT OF ANNEALING ON COPPER THIN FILMS:
THE CLASSICAL SIZE EFFECT AND AGGLOMERATION

by

PARAG GADKARI
B.E. Rajiv Gandhi Technical University, INDIA, 2001

A thesis submitted in partial fulfillment of the requirements
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With continued shrinking of CMOS technology to reduce the gate delay times, an increase in the resistivity of the metal corresponding to the wire dimension is a concern. This phenomenon of increase in resistivity with decreasing dimension of the thin metallic film or interconnect is known as the “classical size effect”.

Various theories have been postulated to explain the phenomenon of classical size effect; these theories can be broadly classified as resistivity due to scattering arising from surface and grain boundaries. The total resistivity of metals depends on the electron scattering due to impurities, phonons, surfaces, grain boundaries, and other crystal defects.

Managing the size effect in a practical and manufacturing way is of major concern to the microelectronics industry. Since each of the processes (phonon, surface and grain boundary scattering) adds to the resistivity and are interrelated, it further complicates managing the size effect. However, these effects have been separately studied.

In this work, the effect of annealing on the classical size effect in Cu thin films deposited on SiO$_2$ substrate is investigated. Polycrystalline Cu thin films having thicknesses in the range of 10nm to 200nm were ultra high vacuum sputter deposited on thermally grown SiO$_2$ surfaces. The films were annealed at temperatures in the range of 150°C to 800°C in argon and argon+3% hydrogen gases.

The un-annealed Cu thin films exhibit higher resistivity than the annealed films. The resistivities of un-annealed films were in good agreement with Mayadas and Shatzkes model.
When annealed the films undergoes grain growth resulting in lowering the resistivities by about 20%-30% thereby confirming the role of grain size on resistivity of the film. However, there is a limit to annealing, i.e. agglomeration phenomenon.

Agglomeration is a thermally activated process resulting in a reduction of the free energy of the film–substrate system and can occur well below the melting point of the material by surface and interfacial diffusion. The reduction of film-substrate interfacial energy, film-surface interfacial energy and stresses within the film are possible driving forces for agglomeration.

This work also includes the study of agglomeration phenomenon. The agglomeration behavior of Cu is investigated and compared with that of Ru, Au and Pt thin films with thicknesses in the range of 10 nm to 100 nm UHV deposited on thermally grown SiO$_2$ substrate. The films were annealed at temperatures in the range of 150°C to 800°C in argon and argon+3% hydrogen gases. Scanning electron microscopy was used to investigate the agglomeration behavior, and transmission electron microscopy was used to characterize the microstructure of the as-deposited and annealed films.

The agglomeration sequence in all the films is found to follow a two step process of void nucleation and void growth. However, void growth in Au and Pt thin films is different from Cu and Ru thin films. Residual stress and adhesion were observed to play important part in deciding the mode of void growth in Au and Pt thin films.

Lastly, it is also observed that the tendency for agglomeration can be reduced by encapsulating the metal film with an oxide overlayer, which in turn improves the resistivity of the thin film due to prolonged grain growth without film breakup.
Dedicated to my parents
ACKNOWLEDGMENT

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CHAPTER ONE: INTRODUCTION

1.1 Overview

Since the discovery of transistors in 1947 there has been a rapid development of the field of microelectronics. The motivation for higher performance through greater functionality in integrated circuits has led to device miniaturization. The reduction in the size of the transistors leads to increase in the transistor density on a finite chip area, which results in an increasing density of wires connecting the transistors. These wires, also known as interconnects, provide the metal connection between different devices on a chip. Interconnects are formed by patterning and selective etching a thin metallic film. The function of the interconnects is to provide clock or other signals and to provide power to and among the various components, circuits, and systems on the chip.

Rapidly increasing the density of transistors on a chip has resulted in more complex interconnect geometries and the degree of complexity is expected to increase with time\textsuperscript{1,2}. Figure 1.1 illustrates an example of a complex interconnect design having seven layers of interconnect wiring. However, the complexity and miniaturization has adversely affected the performance and reliability of the interconnects.

The performance and reliability of interconnects has become an important issue since the signal propagation speed and device reliability issues are now determined by that of interconnects rather than be the transistors themselves. Several interconnect issues are discussed in the following section.
1.2 Interconnect Issues

While device miniaturization favors device performance, it can lead to slower signal propagation because of increased sheet resistance of the interconnects. Table 1, which is an excerpt from International Technology Roadmap for Semiconductor (ITRS 2003) roadmap, shows the way interconnects can be expected to change in the near future (2009). As can be seen from the table, additional metallization levels and increasing current densities in the interconnects are expected. Both of these issues result in reliability concerns. An integrated circuit, apart for performing as desired, must also work for an extended period of time without failing. Therefore, the interconnect metal should also address to the reliability issues. The performance and reliability issues in interconnect are discussed in the following subsections.
Table 1. Table showing an excerpt from ITRS 2003\textsuperscript{4}: Microprocessor interconnect technology requirements (near term).

<table>
<thead>
<tr>
<th>Year of Production -&gt;</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
</tr>
<tr>
<td>Number of metal levels</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Number of optional levels.</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Total interconnect length (m/cm\textsuperscript{2}) – active wiring only.</td>
<td>579</td>
<td>688</td>
<td>907</td>
<td>1002</td>
<td>1117</td>
<td>1401</td>
<td>1559</td>
</tr>
<tr>
<td>Jmax (X10\textsuperscript{5}A/cm\textsuperscript{2}) - intermediate wire (at 105°C).</td>
<td>3.7</td>
<td>5.0</td>
<td>6.8</td>
<td>7.8</td>
<td>10</td>
<td>14</td>
<td>25</td>
</tr>
<tr>
<td>Interconnect RC delay (ps) for 1mm intermediate line</td>
<td>105</td>
<td>139</td>
<td>182</td>
<td>224</td>
<td>229</td>
<td>288</td>
<td>358</td>
</tr>
<tr>
<td>Conductor effective resistivity (µm-cm) – Cu intermediate line</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
<td>2.2</td>
</tr>
</tbody>
</table>
1.2.1 Interconnect Speed and RC Delay

The miniaturization paradigm results in an aggressive shrinking/scaling of interconnect cross-sectional area. When coupled with the trend of some interconnects to have a longer length and the large increase in the density of interconnects, this trend leads to some interconnections having higher resistance and capacitance and thus a longer RC delay and slower signal propagation between different devices on the chip. RC delay is the main component affecting the speed of interconnects thereby affecting the performance of integrated circuits. High speed causes increases in inductance related issues and electromagnetic interference problems. This scenario is termed as the “interconnect crisis”\(^5\).

Interconnect speed, once an insignificant issue, is quickly becoming a performance bottleneck for achieving higher speed of integrated circuits. Parameters like cost, delay, power, reliability and turnaround time of future integrated circuits would be determined by interconnects and not transistors. Figure 1.2, from reference \([6]\), illustrates such scenario.

Apart from speed, signal integrity is also becoming a major performance bottleneck in integrated circuits. As the interconnects are scaled down and are placed closed together in complex designs, the coupling capacitance increases between them. Increased coupling capacitance in between interconnects gives rise to problems like crosstalk noise and large delay fluctuation.
Efforts are being made to reduce the resistance of interconnect by experimenting on different materials and by using low $k$ dielectrics for the isolation materials to reduce the capacitance.

### 1.2.2 Electromigration

In a perfect lattice, there is no resistance. Electrons move about in a periodic potential with no other interaction with the metal atoms. But a perfect lattice cannot exist above absolute zero due to atomic vibrations, vacancies, and chemical impurities. Grain boundaries, and
Dislocations are also usually present. Perhaps even more important, at any temperature above 0 °K, the atomic vibrations become larger. The collective vibrations of the atoms are also called phonons, and they pull a metal atom out of its thermal equilibrium position, disturbing the periodic potential of the lattice, and causing electron scattering by the atoms. The force due to collisions of electrons to metal atoms is called the momentum exchange. This phenomenon can result in motion of the atoms which is termed as electromigration.

Electromigration is defined as motion of ions/atoms of a thin film or interconnect in response to the passage of high current thought it. Such motion can lead to the formation of "voids or holes” and “hillocks” in the thin film, which can grow to a size where the conductor is unable to pass current or is shorting other interconnect line.

Discovered more than a century ago, it became a concern only when the relatively severe conditions necessary for operation of integrated circuits made it painfully visible. Figure 1.3 from reference [7] illustrates a scenario of electromigration in interconnects. Copper is known to be more resistive to electromigration than aluminum.
Figure 1.3. Effect of electromigration on interconnects.
1.2.3 Thermomechanical Failure: Agglomeration

The initial structure of an interconnect can change upon subsequent annealing, in use or as part of the device fabrication process. These changes include grain growth, and morphological instabilities such as void or “pinhole” formation and the breakup of the film into isolated islands on the substrate surface. This phenomenon of island formation is known as agglomeration. Figure 1.4 shows an example of the initially continuous and fully agglomerated Au thin film.

Agglomeration is a thermally activated process that reduces the free energy of the thin film or interconnects. It does so by rearranging the film-substrate interface, grain boundaries and film surface. An agglomerated film or interconnect can effect signal integrity, RC delay, and can cause device failure by having no conduction, figure 1.4(ii).

Figure 1.4. Effect of agglomeration: SEM images of 20nm Cu thin film; (i) continuous – as deposited; (ii) percolated.
1.2.4 Other Issues

Other, non-trivial, interconnect performance and reliability issues include diffusion and adhesion properties, scaling properties, and oxidation issues of the interconnect metal. At higher processing temperature, interconnect metal atoms can diffuse in a dielectric or semiconductor, thus effecting the performance of the integrated circuit. To prevent the diffusion, a barrier or liner layer is introduced between the interconnect metal and dielectric or semiconductor. This additional fabrication process adds to the cost of the integrated circuit. Moreover, due to electron scattering in interconnect at the interface, this can also effect the resistance of the interconnect and thus affect its speed.

Some metals, like Au and Pt, do not adhere well to the dielectrics. Poor adhesion when coupled with the residual stress in film can lead to film bulging or delamination\(^8\) which can result in poor performance of the integrated circuits.

1.3 Aluminum vs Copper Interconnect

In the past, semiconductor industries were heavily dependent on aluminum alloys for interconnects. Aluminum alloys are provided for low cost and high throughput. Aluminum alloys also shows good adhesion to most of the dielectrics used in the semiconductor industry. Moreover, aluminum alloys are known to form native oxide which acts as a passivation layer and aluminum can be easily patterned or etched.
However, aluminum alloys cannot cope with the increasing demands of shrinking device dimensions and scaling interconnects because of higher RC delay. Copper was seen as the attractive alternative to aluminum for interconnects because of its lower resistivity and better electromigration and scaling properties than aluminum. The lower resistivity of copper (1.72µm-cm) results in smaller RC delay. Typically, using copper instead of aluminum as interconnects reduces 40% resistance of interconnects, resulting in better signal integrity and smaller RC delay.

The electromigration activation energy for copper is higher than that of aluminum. Since aluminum is known to be reliable until the 0.18µm linewidth design point, these potential failures limit the minimum thickness and width of interconnect making copper a better choice at dimensions smaller than 0.18µm. However, copper also suffers from reliability and other issues which are discussed in the next section.

1.4 Copper Interconnect: Challenges

The larger electromigration activation energy and lower resistivity of copper (Cu) as compare to aluminum (Al) has allowed Cu interconnects to operate at higher current densities and for longer times. Thus Cu has been readily accepted as the metallization of choice for high performance interconnects. However, scaling Cu interconnects also arises questions regarding its performance and reliability. Different performance and reliability related issues of Cu interconnect are listed below.
• **The Size Effect:** The “size effect” in metallic films has been a key issue since the advent of microelectronics and has been studied for little more than a century\(^9\). This effect or phenomenon deals with the increase in the resistivity of metallic conductors with decreasing their dimensions, and applied directly to the case of Cu interconnects. This effect becomes important when the thickness of Cu thin film or thickness and width of Cu interconnect approaches near the room temperature mean free path of electron-phonon scattering, which for Cu is 39 nm.

• **Metallic Diffusion:** Cu is known to diffuse rapidly in semiconductors and dielectrics, even at the room temperature. In order to prevent this problem, a barrier layer is required. Tantalum based diffusion barrier processing has been one of the major breakthroughs in Cu interconnect manufacturability. The integrity of the barrier layer should be closely examined, particularly in regions where the line or interconnect changes direction. Any opening in the barrier layer would permit Cu diffusion onto other metal lines or active device areas.

• **Agglomeration or Thermomechanical Failure:** The structures of an as-deposited Cu interconnect can change upon annealing which would eventually result in film breakup causing failure of device. The Cu thin films are known to agglomerate well below their melting temperature.
1.5 The Classical Size Effect

The electrical resistivity of metals is known to be higher in thin films and wires than in bulk. This phenomenon of increase in resistivity with decreasing dimension of the thin metallic film or interconnect is known as the “size effect”. In thin films it is possible to observe two kinds of size effects: a quantum size effect and the classical size effect. The quantum size effect arises when the thickness of the film is comparable to the de Broglie wavelength of electron. In the quantum size effect, an oscillatory dependence of kinetic coefficients appears on the thickness of the film because the energy spectrum in the direction of thickness becomes discrete. However, to analyze the quantum size effects requires films thickness to be in quantum regime (a few nanometers). Such films are more prone to defects and therefore make the verification of these models difficult. The classical size effect has been more relevant to the resistivity of interconnects because it occurs at larger sizes, closer to that of interest to interconnect designs. In classical size effect, increases in resistivity and changes of kinetic characteristics of the film is observed when the thickness of the metallic film is commensurate with mean free path of electron in the film.

1.5.1 Background

Thompson, in 1901, was the first to discuss the inverse relationship between the resistivity and size of a thin metallic film. Later in 1938 Fuchs\textsuperscript{10} described this dependence of resistivity on the thickness in terms of bulk and surface contributions to the electron scattering in
the thin film. The Fuchs size effect theory is based on semi-classical concept of relaxation time. It postulates that external surface of the film imposes a boundary condition on the electron distribution function, and when coupled with the ordinary scattering mechanism in bulk (phonon scattering) can enhance the thickness independent bulk resistivity to provide a thickness dependent total resistivity. The Fuchs theory was derived from Boltzmann transport equation, a powerful tool for analyzing transport phenomenon within a system that involves density and temperature gradients.

Since the time Fuchs introduced his theory of size effect, numerous extensions of his work have been developed\textsuperscript{11,12,13,14}, all of which concluded that surface morphology has the main contribution to the size effect in metallic thin films.

The aforementioned Fuchs theory and its extensions hold well for the single crystal films. However, many metallic thin films are deposited as polycrystalline in nature. The impact of grain size and grain boundaries on the resistivity of polycrystalline thin metallic film was first described in detail by Mayadas and Shatzkes\textsuperscript{15} in 1970, where it was shown that a “size effect” due to grain boundary scattering is also expected, since the thinner films tend to have smaller grains and hence a higher density of grain boundaries.

Numerous theories based on Fuchs and Sondheimer (FS) theory of surface scattering and Mayadas and Shatzkes (MS) theory of grain boundary scattering have been proposed till date, but our scientific understanding of size effect is still limited.
1.5.2 Importance in Copper Thin Films

Copper was introduced to mitigate the problems arising from the miniaturization paradigm on the RC delay of interconnects. In the International Technology Roadmap for Semiconductors (ITRS 2003), it is assumed that the resistivity of Cu thin films or interconnects at intermediate level would remain same in the near term, as can be seen from table 1.1, and long term even when the intermediate interconnects continue to scale down. However, this would mean completely specular scattering of conduction electrons at film surface and grain boundaries. As the interconnect dimensions of Cu are scaled down the conduction electrons will suffer more scattering due to the surfaces, arising from the large surface to volume ratio, and from grain boundaries, arising from polycrystalline nature of the film.

Figure 1.5, from reference [16], shows the resistivity of Al and Cu versus line width as a function of the fraction of electrons that are elastically scattered. From the figure it can be seen that Cu is more sensitive to change in dimension than Al. In fact, for very narrow linewidths, when the fraction of elastically scattered electrons in Cu are greater than for Al, Cu could exhibit a larger total resistivity.

As the interconnection technology is evolving from Al based conductors to Cu based conductors, the increase of resistivity of Cu with reduction in film dimensions is of great concern. It will be important to develop a better understanding of the combined effects of surface morphologies and grain boundaries on the resistivity of Copper for future interconnection technologies.
1.6 Objectives

At room temperature the electrical resistivity of metallic thin film depends on the rate of collision of the conduction electrons with phonons or with imperfections in lattice, and thus both have their contribution on the resistivity of the metal films. The electrical resistivity arising from electron scattering from phonon is temperature dependent and the resistivity caused by lattice imperfections is independent of temperature. It is often assumed that both of these resistivities are independent of each other and therefore the total resistivity is the summation of the two resistivities. It is also believed that phonon scattering is eliminated at low temperatures and thus the resistivity at low temperature is due solely to the electron scattering at lattice imperfections, such as grain boundary and surface roughness.
The objective of this work is to study the electrical resistivity both at the low temperature of 4 K and at room temperature. This study involves the effect of annealing on the resistivity of the thin films. Annealing results in increase in the size of grains of the film, thereby reducing the resistivity of the film. However, annealing also causes the film-substrate system to minimize its free energy by breaking the metallic film, resulting in agglomeration. Since this phenomenon is equally important to the study of the classical size effect in thin metallic films, the objective of this thesis also includes the study of agglomeration in order to achieve the lowest resistivity with annealing but without breaking the film.
CHAPTER TWO: LITERATURE REVIEW

Since the time when Fuchs introduced the concept of surface scattering to explain the size effect, many other theories and models have came into existence. Many of the theories derive from the Fuchs theory of surface scattering and the Mayadas and Shatzkes theory of grain boundary scattering. This chapter begins with explaining the Boltzmann transport equation, which is the base of numerous size effect theories, and later reviews the existing theories of size effect in metallic thin films.

2.1 Boltzmann Transport Equation

The Boltzmann transport equation (BTE) is a powerful tool for analyzing the transport phenomenon within a system that involves density and temperature gradient. The application of this equation includes analysis of general currents within a system, thermally induced diffusion and calculation of transport coefficients in a system.

The BTE is a semi-classical equation and describes the time-dependent position and momentum or electron and holes in a conductor or semiconductor in terms of a distribution function \( f(\mathbf{r}, \mathbf{p}, t) \), where vector \( \mathbf{r} \) is the position, vector \( \mathbf{p} \) is the momentum and \( t \) is the time. The BTE can be obtained from the conservation principle that the change in \( f(\mathbf{r}, \mathbf{p}, t) \) with respect to time is the sum of the change in \( f \) with respect to the space, the change in \( f \) with respect to the momentum and the change in \( f \) with respect to time.
Consider a system with non-uniform particle density. Now consider the system of randomly moving particle within a medium across x axis. Whenever a particle is scatters or collides with the medium its velocity after the collision will be that of equilibrium distribution, $f_0$ at collision point. A particle moves in the $\xi$ direction at an angle $\theta$ with respect to x-axis and moving with a velocity $v$ as shown in figure 2.1. The projection of $\xi$ on x-axis is given by:

$$\Delta x = \Delta \xi \cdot \cos \theta \quad \text{(Equation 2.1)}$$

![Figure 2.1. Particle moving within a medium in a $\xi$ direction](image)

The probability, $dP$, that a particle will collide the medium along the distance element $d\xi$ is proportion to the length $d\xi$, the density and scattering centers $n_s$ and the scattering cross sections $\sigma_s$.

$$dP = -P \cdot d\xi \cdot \sum_s n_s \cdot \sigma_s = -P \cdot \frac{d\xi}{\lambda} \quad \text{(Equation 2.2)}$$
The summation occurs for all \( s \) accounts and \( \lambda ( = 1 / (\Sigma n_s \sigma_s)) \) is the mean free path of the particle. The probability that last collision of the particle, before reaching \( \xi \), was along the element \( d\xi_1 \), at a position \( \xi_1 (\xi_1 < \xi \text{ in figure 2.a}) \), is:

\[
\frac{P(\xi_1) \cdot d\xi_1}{\lambda} = e^{\frac{(\xi - \xi_1)}{\lambda}} \cdot \frac{d\xi_1}{\lambda} \quad \text{(Equation 2.3)}
\]

\( \lambda \) is determined by the properties of the medium and is the probable distance of where the particle comes from and is given by,

\[
\int_{-\infty}^{\xi} \left( \xi_1 - \xi \right) \cdot P(\xi_1) \cdot d\left( \frac{\xi_1}{\lambda} \right) = \lambda \quad \text{(Equation 2.4)}
\]

The velocity distribution, \( v \), of a particle at \( \xi \) is obtained by integrating the local velocity distribution along the line up to \( \xi \). Each distribution is multiplied by the probability that the particle comes from that distance, namely, that it has collided for the last time with the medium at that place:

\[
f(\xi, v) = \int_{-\infty}^{\xi} f_0(\xi_1, v) \cdot P(\xi_1) \cdot d\left( \frac{\xi_1}{\lambda} \right) \quad \text{(Equation 2.5)}
\]

Where \( v = |v| \) and \( f_0(\xi_1, v) \) is the local equilibrium distribution. If the equilibrium distribution does not change significantly along the mean free path \( l \), it will be possible to use the first terms of Taylor series:
\[ f_0(\xi_1,v) = f_0(\xi,v) + \frac{\delta f_0}{\delta \xi}(\xi_1 - \xi) + \frac{\delta f_0}{\delta v}(v(\xi_1) - v(\xi)) \]  
(Equation 2.6)

The change in velocity is a result of force acting on the particle, such as a gravitational field or an electric field for a charged particle. Assuming that the force acts in the x-direction, the velocity change will be:

\[ v(\xi_1)^2 - v(\xi)^2 = 2v \cdot (v_1 - v) = 2a(\xi_1 - \xi) \cos \theta \]  
(Equation 2.7)

where \( a \) is the acceleration, equal to \( eE/m \) for an electric field \( E \). Substituting equation 2.6 and equation 2.5 into equation 2.4 and integrating over \( \xi_i \), and finally substituting \( x \) and \( \theta \) for \( \xi \), then according to equation 2.1 we get:

\[ f(x,v,\theta) = f_0(x,v) - \lambda \cdot \cos \theta \left( \frac{\delta f_0}{\delta x} + \frac{a}{v} \frac{\delta f_0}{\delta v} \right) \]  
(Equation 2.8)

The non-equilibrium distribution in equation 2.8 is the linear Boltzmann transport equation in a somewhat non-traditional form. \( f_0(x,v) \) is the local equilibrium distribution given by Maxwell-Boltzmann or Fermi-Dirac distributions. The medium properties enter through the mean free path \( \lambda \), and external forces through the acceleration \( a \). The standard form of the linear Boltzmann transport equation includes a constant relaxation time \( \tau \) and is given by:

\[ \frac{\delta f}{\delta t} + v \frac{\delta f}{\delta x} + a \frac{\delta f}{\delta v} = \frac{(f - f_0)}{\tau} \]  
(Equation 2.8)
Where relaxation time $\tau$ is given by:

$$\tau = \frac{\lambda}{v} \quad \text{(Equation 2.9)}$$

Boltzmann transport equation relates the properties of a non-equilibrium system, expressed by a non-equilibrium distribution, in terms of local equilibrium distributions. The equation is derived by assuming random movement of particles within a medium. The equation 2.8 was used by Fuchs to describe the transport phenomenon of electrons in metallic thin films.

2.2 Existing Theories and Models

2.2.1 Surface Scattering Theories

In the past, researchers have used Fuchs and Sondheimer theory to analyze the size effect arising from surface scattering. Fuchs-Sondheimer\textsuperscript{10,11} theory is based on semi-classical Boltzmann transport equation. Fuchs postulated that the residual resistivity of the metallic film is due to the electron scattering at the surface of the metallic thin film. The electron scattering at the surface is defined as either diffuse or specular scattering. The scattering is said to be completely specular when all the electrons undergo perfect reflection at the surface of the thin film without losing its momentum. Whereas a perfectly diffuse scattering occurs when all the electrons that strikes the surface loses all the memory of their velocity before scattering.
Figure 2.2 shows the two different event of specular and diffuse scattering. When scattering event is specular the resistivity of the metallic film is that of bulk. The result of the Fuchs theory for thin films is:

\[
\rho = \rho_i \left[ 1 - \left( \frac{3}{2\kappa} \right) (1 - p) \right] \cdot \left( \frac{1}{t^3} \frac{1}{t^5} \frac{1 - e^{-\kappa t}}{1 - pe^{-\kappa t}} \right) \right]^{1/3} \\
\] (Equation 2.10)

Where \( \kappa (=d / \lambda_i) \) is the ratio between the film thickness, \( d \), and intrinsic mean free path, \( \lambda_i \). And \( p \), also known as the specularity coefficient, is the probability that an electron will be specularly reflected upon scattering from the film surface and varies from 0, perfectly diffuse scattering, to 1, perfectly specular scattering. The expression of size dependent resistivity was simplified by Sondheimer. The simplified model is given by:

\[
\rho = \rho_i \left[ 1 + \left( \frac{\lambda_i}{d} \right) (1 - p) \left( \frac{3}{8} \right) \right] \\
\] (Equation 2.11)
The equation contains three unknown quantities \( \rho_i, \lambda_i \) and \( p \). However, \( \rho_i \) and \( \lambda_i \) are not independent since:

\[
\rho_i \cdot \lambda_i = \frac{12 \pi^3}{q^2 S_F} h \tag{Equation 2.12}
\]

Where \( q \) is the electron charge and \( S_F \) is the free area of Fermi surface. The simplified model by Sondheimer had been used extensively and therefore the size effect theory by Fuchs has been collectively called as Fuchs and Sondheimer theory.

Generally it is assumed that the product \( \rho_i \cdot \lambda_i \) is constant. However, Mayadas et al. have shown that this assumption is not correct for Al thin films and \( \rho_i \) decreases with increasing thickness. Later, it was found that decrease in \( \rho_i \) was due to increasing grain size. The work of Mayadas and Shatzkes is reviewed in the next section.

Later in 1950, Chambers\(^{17} \) developed the theory of transport from the point of view of kinetic theory. His theory was also based on surface scattering. He postulated that the energy of an electron passing through point \( r_0 \) at time \( t_0 \) had had its energy modified by \( \Delta E \), where:

\[
\Delta E(r_0, t_0) = \int_{-\infty}^{t_0} v \cdot (-e \varepsilon(r, t)) e^{-\frac{(t-t_0)}{\tau}} \, dt \tag{Equation 2.13}
\]

If the electrons were initially in equilibrium before their energy was modified by the applied field then:
The equation 2.17 is a particular solution to Boltzmann transport equation. Chamber derived an integral expression of resistivity of wire with a rectangular wire cross-section based on the above mentioned kinetic theory which is given by:

\[
\frac{\rho_0}{\rho} = \frac{3}{4 \pi s} \int_s ds \int_0^{2\pi} d\phi \int_0^{\pi} d\theta \sin \theta \cos \theta \left[ 1 - \frac{(1 - p) e}{-\frac{\lambda_a}{\Lambda_i}} \right]^n \left( \frac{-\lambda_b}{\Lambda_i} \right) \left( 1 - p e \right) \sum_{n=1}^{\infty} n \cdot p^{n-1} \left( \frac{\rho_0}{\rho} \right)_{p=0, n \kappa} \]

(Equation 2.15)

Where \( \lambda_a \) is the mean distance traveled before colliding with the wall/surface and \( \lambda_b \) is the mean distance traveled between two successive collisions if the reflection is specular. The angle \( \theta \) is the angle between the direction give by \( \lambda_a \) and the z-axis and angle \( \phi \) is the azimuth angle. A simple expression of equation 2.15 was gives as:

\[
\left( \frac{\rho_0}{\rho} \right)_{p, \kappa} = \left( 1 - p^2 \right) \sum_{n=1}^{\infty} n \cdot p^{n-1} \left( \frac{\rho_0}{\rho} \right)_{p=0, n \kappa} \]

(Equation 2.16)

In this equation, \( \kappa \) is the ratio between the film thickness and mean free path of electrons in the metal films. The equation 2.16 given by Chambers is the exact in framework with Fuchs theory and does not rely on approximation for the limiting cases.
In Fuchs and Sondheimer\textsuperscript{10,11} theory, however, the specularity coefficient, $p$, was independent of the angle of incidence of the conduction electron with the film surface. Soffer\textsuperscript{18}, extended the work of Ziman\textsuperscript{19}, to introduce a specularity coefficient, $p$, that depend on the angle of incidence in the limit of no lateral surface correlation. The expression of specularity coefficient is given as:

$$p_s(\cos \theta) = e^{-\left[\left(\frac{4\pi}{\lambda_e}\right)^2 \left(\cos \theta\right)^2\right]^2}$$  \hspace{1cm} (Equation 2.17)

Here $r = a / \lambda_e$, $a$ being the r.m.s. surface roughness and $\lambda_e$ the Fermi wavelength. This model assumes similar wavelength of surface roughness and conduction electrons, which for most metals is around the inter-atomic spacing. Soffer’s theory is in good agreement with the thickness range of several hundreds of angstroms. However, as the film thickness decreases, the deviation of theory from experimental results appears more clearly, particular when substrate is heated during film deposition\textsuperscript{20}.

In nearly all the instances, it has been observed that single crystal films show higher resistivity than polycrystalline films. All the abovementioned surface scattering models does not take into account the resistivity arising from the conduction electron scattering at grain boundaries.

\subsection*{2.2.2 Grain Boundary Scattering Theories}

In the past it was commonly believed that there was no affect of grain size on the resistivity of thin films. However, this was the case when grain sizes were bigger than the mean
free path of the electron and therefore the contribution of grain boundaries can be neglected. But this assumption is not valid in case of thin films where the grain sizes are lesser than mean free path of the bulk.

Figure 2.3. Grain boundary scattering in metallic thin films: (i) Specular scattering event and (ii) Diffuse scattering event.

Mayadas and Shatzkes, in 1970, extended the Fuchs and Sondheimer model to include the contribution of electron scattering at grain boundaries to the total resistivity of the thin metallic film. According to their theory, the mean free path of electron is decreased by the existence of additional scattering sites that are assumed to be statistically distributed in the conductor. Their model assumed fully columnar grains oriented perpendicular to the film. Figure 2.3 illustrates electron reflection at grain boundaries. They calculated the resistivity arising from the grain boundary, $\rho_g$:

$$\frac{\rho_i}{\rho_g} = 3 \left( \frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln \left( 1 + \frac{1}{\alpha} \right) \right)$$

(Equation 2.18)
Where $\alpha$ is given by:

$$\alpha = \frac{\lambda_i}{D} \cdot \frac{R}{1-R} \quad \text{(Equation 2.19)}$$

The equation 2.18 can be simplified to more general form:

$$\rho = \rho_i \left[ 1 + \left( \frac{3}{2} \right) \frac{\lambda_i}{D} \left( \frac{R}{1-R} \right) \right] \quad \text{(Equation 2.20)}$$

In the above equations, $D$ is identified as the mean grain width and $R$ is known as reflection coefficient and, like $p$ in Fuchs and Sondheimer theory, ranges from 0 to 1. The resistivity of the thin film is that of bulk when $R$ is 0 i.e no electrons are reflected. And resistivity is infinite when all the electrons are reflected and $R$ is 1.

Landauer\textsuperscript{21} obtained the same result of resistivity being proportional to $(R / (1-R))$ term even before Mayadas et al., in 1957. Landauer assumed the reflectivity coefficient, $R$, to be dependent on the angle of incidence. However, unlike Soffer, no expression was given for the angular dependency of $R$.

Several theories have attempted to predict the influence of the grain boundaries on the resistivity but Mayadas and Shatzkes remains the most commonly used theory. However, Vancea\textsuperscript{22} et al pointed out inconsistency in Mayadas and Shatzkes theory. They showed that, in Mayadas and Shatzkes theory, evaluation of mean free path from the size effect is done independent of the absolute value of the resistivity which is incoherent with the Matthiessen’s rule of additive resistivity.
2.2.3 Combined Surface and Grain Boundary Scattering

Mayadas and Shatzkes were the first to use the combination of Fuchs size effect theory and their grain boundary theory to derive an expression of total resistivity of the thin film. However, they assumed equivalence of the grain size and film thickness and did not experimentally study the microstructure of their samples.

Sambles et al\textsuperscript{23}, in 1982, studied the combined effect of Soffer’s surface scattering theory and Mayadas and Shatzkes’ grain boundary theory on the total resistivity of small and large grained Au thin films. They assumed that the total resistivity would follow a Matthiessen’s additive resistivity rule; however, some deviation was expected from Matthiessen’s rule due to temperature dependent part of resistivity. The temperature dependent phonon contribution to the resistivity was approximated using Bloch and Gruneisen formula given by:

\[
\rho_P = \rho' \left( \frac{T}{\Theta} \right)^5 J_N \left( \frac{\Theta}{T} \right) \tag{Equation 2.21}
\]

Where \( \rho' \) is the constant chosen to give ice point resistivity, \( \rho_{273} \), and \( \Theta \) is the Debye temperature associated with phonon scattering and \( J_N(x) \) is the Debye integral. Although they were able to explain the size effect in the small grained Au film but their model did not worked for the large grained film instead surface scattering model alone was used to predict the total resistivity suggesting the grain boundary scattering mechanism to be dominant in metallic thin films.

Steinhögl et al\textsuperscript{24}, in 2002, studied their experimental results on Cu interconnects using combination of Fuchs and Sondheimer’s surface scattering theory and Mayadas and Shatzkes
grain boundary theory. Like Sambles et al, their combination was also based on the assumption of Matthiessen’s rule of additive resistivity. They described the total resistivity in terms of combined relaxation time due to surface scattering, grain boundary scattering and background electron and phonon scattering. Steinhögl et al study shows that the grain boundary scattering is the dominant source of resistivity increase in polycrystalline Cu thin films.

Durkan and Welland\textsuperscript{25}, in 1999, followed the approach due to Chambers to combine both the Fuchs size effect theory and Mayadas and Shatzkes grain boundary theory, using Matthiessen’s rule, to study the size effect in polycrystalline Au nanowires. They modified the Mayadas and Shatzkes model to incorporate grain size distribution as a function of linewidth of the wire. Durkan and Welland, unlike Steinhögl et al, pointed out that both the mechanism of surface and grain boundary scattering are equally important to predict the total resistivity of metallic thin film.

Similar study was done by Marom and Eizenberg\textsuperscript{26} recently. However, they developed an analytical expression to study the temperature dependence of resistivity of thin metallic film based on Mayadas and Shatzkes model. They also concluded that the scattering of electron arising from surface and grain boundaries collectively can, only, explain the resistivity of thin films and not just grain boundary scattering.
2.2.4 Other Theories

Many theories based on non-classical quantum physical treatments of surface roughness and film resistivity have been developed over past thirty years. The motivation of such theories has been the evolution of conceptual difficulties in semi-classical Boltzmann transport equation while dealing with length scales comparable to de Broglie wavelength, such as relaxation time approximation. Most of the quantum size effect theories are based on Kubo\textsuperscript{27} and Greenwood\textsuperscript{28} linear response theory and is often called as “Kubo formalism”\textsuperscript{29}. Linear response theory describes the zero-temperature dc conductivity as the average over configuration of quantum states that are eigen-functions of a particular configuration of the random potential in a system.

The quantum size effect in semimetal films with perfect surfaces was first studied by Sandomirskii\textsuperscript{30} in 1967. According to his theoretical calculations for a film with perfect surface, an increase in film layer thickness would lead to decrease in density of states eventually resulting in increased relaxation time and mobility. He also expected the transport coefficients to show an oscillatory behavior in quantum regime. Govindaraj and Devanathan\textsuperscript{31} studied the quantum size effect using Kubo formalism by considering randomly distributed scattering centers. They found that in quantum limits the conductivity becomes an oscillatory function of thickness, which for Cu and Al were found to be one half of the de Broglie wavelength. This oscillatory behavior was attributed to density of states exhibiting quantum character, i.e. a step-like function with respect to energy of the film, and was found to be in agreement with Sandomirskii’s theory.

Camblong and Levy derived an expression for conductivity in multilayer metallic film by making semi-classical approximation to Kubo formula. They showed an explicit connection
between the semi-classical theories based on Boltzmann transport equation and quantum theories based on Kubo formulism. They also suggested a novel way of treating diffuse scattering at the interface by inserting additional thin layer at interface with small mean free path.

Various theories and models based on Kubo formulism have been developed until now. These models or theories have considered atomic scale roughness, atomic and longer wavelength roughness, small and large wavelength roughness and impurity potentials. However, to analyze these models requires films thickness to be in quantum regime, such films are more prone to defects and therefore making the verification of these models difficult. Also model or theories based on quantum size effects either take into account the electron scattering due to rough surface or due to grain boundaries; there is still a lack of a model which includes background, surface and grain boundary scattering to explain the total resistivity of a thin film.

2.3 Failure of Matthiessen’s Rule

The total resistivity of metals depends on the electron scattering due to impurities, phonons, surfaces, grain boundaries, and other crystal defects. It is often assumed that the contribution due to phonons and due to lattice imperfections (surface and/or grain boundary) are additive in nature. Matthiessen’s rule has, therefore, long been used to analyze their contributions. Such an approach was implemented by Bloch and Gruneisen. However, Matthiessen’s rule is invalid for thin films.
The contribution of surface and grain boundaries on the net resistivity of the thin film depends upon the mean free path of the electron. Landauer pointed out that velocity distribution, including incident electrons and reflected electrons, in thin films does not vary with the angle of incident of an electron; therefore, there would be no single relaxation time for whole conduction process. Thus, Matthiessen’s rule would not be applicable if the reflecting wall exists with thermal scattering. Vancea et al also supported this idea, he pointed out that background or phonon scattering and scattering due lattice imperfection are not independent and therefore Matthiessen’s rule might be inapplicable in such cases.

Munoz et al\textsuperscript{37}, while analyzing the residual resistivity in thin films of CoSi\textsubscript{2}, found that Matthiessen’s rule is seriously violated in thin films regardless of theoretical models, either based on Kubo formalism or semi-classical Boltzmann transport equation. He also pointed out that for resistivities due to background and lattice imperfections to be additive the film thickness must be in the range of few hundreds of nanometer.

2.4 Alteration of Resistivity

Managing the size effect in a practical and manufacturing way is of major concern to the microelectronics industry. Since each of the processes (phonon, surface and grain boundary scattering) adds to the resistivity and are interrelated, it further complicates managing the size effect. However, these areas have been separately studied to alter the resistivity of Cu thin films.
Egelhoff, et. al,\textsuperscript{38} have shown that the diffuse scattering event will dominate at the metal surfaces unless special care is taken to prepare extremely flat surfaces. They pointed out that the level of diffuse electron scattering from the surface will relate to the level of opportunities for the electrons to scatter to alternate surfaces. He suggested of using oxide surfactant would greatly enhance the specular scattering event at the surface of the film. Similar results were obtained by Sakakima et al\textsuperscript{39} and Rossanagel and Kuan\textsuperscript{40}.

On the other hand grain growth in thin films have been extensively studied and modeled\textsuperscript{41,42,43,44,45,46}. In Cu films grains are known to grow even at room temperature and in thick films this effect can lead to resistance change of -25\% or more. This is an interesting phenomenon to consider and can have impact in altering the resistivity of Cu; however, as described in earlier chapter, Cu can agglomerate well below its melting temperature during processing and can seriously affect the performance. Therefore, the study of the surface morphologies of Cu at high annealing temperatures is as important as the physics of the size effect.

2.5 Agglomeration

Thin metallic films are basic components of most semiconductor and magnetic devices. Such films are often deposited at low temperature with microstructures far from equilibrium. The initial film structure can change upon subsequent heating of the film, in use or as part of the device fabrication process. These changes include grain growth, and morphological instabilities.
such as void or “pinhole” formation and the breakup of the film into isolated islands on the substrate surface. The morphological instabilities can result in device failure and are the subject of this work. These instabilities have long been studied\textsuperscript{47} and are still of practical and scientific interest. Films that have a high surface to volume ratio and a weak chemical interaction with their substrate are most susceptible to morphological change. The process of the uncovering of the substrate or dewetting of an initially continuous film is known as agglomeration.

Agglomeration is a thermally activated process resulting in a reduction of the free energy of the film–substrate system and can occur well below the melting point of the material by surface and interfacial diffusion. The reduction of film-substrate interfacial energy, film-surface interfacial energy and stresses within the film are possible driving forces for agglomeration.

Agglomeration can be considered a two step process, void nucleation and subsequent void growth. The nucleation of voids can be homogeneous or heterogeneous in nature. While the possibility of homogeneous nucleation of voids has been considered\textsuperscript{48,49}, heterogeneous nucleation of voids at defects is an accepted means of void formation. Mullins\textsuperscript{47} has demonstrated, via linear stability analysis, that an initially flat surface is stable against small amplitude perturbations and therefore would not form holes spontaneously.

Film defects, such as grain boundary triple points\textsuperscript{47,48}, pinholes\textsuperscript{50}, and gas bubbles\textsuperscript{51}, can act as sources for heterogeneous nucleation of voids. Grain boundary grooving describes the tendency of the free surface of a film to form a depression along the intersection of the free surface with a boundary between two adjacent grains. This tendency is typically justified as satisfying a force balance among the two surface/grain and the grain/grain interfacial tensions.
A triple point, where three grains meet, represents a preferred site along the grooved grain boundary for heterogeneous nucleation of voids. Upon annealing, voids are formed in the thin film that exposes part of the substrate surface. With further annealing these voids grow and impinge upon each other resulting in a porous yet partially continuous film. Further annealing eventually forms isolated islands of the film material. This common process based on capillarity$^{52,53}$ has been reported for Cu$^{51}$, Pd$^{54}$, Au$^{52,53,55}$, Pt$^{56}$, and Ag.

Recently, Kwon et al observed a somewhat different agglomeration process in Au thin films and proposed a different mechanism of “fractal growth.” They reported that Au thin films agglomerate through void nucleation and a subsequent fractal growth of the void. According to fractal growth mechanism, the void nucleates at areas with high stress, not necessarily at grain boundaries, and then voids in the film grow laterally through surface diffusion and undergo perturbations creating void branches.

Such branch groups eventually impinge upon each other resulting in the formation of isolated islands similar to those formed in the capillary process. However, no detailed explanation of why the normal capillary process was not observed for their Au thin films was given.

Stresses within the film are also expected to play an important role in kinetics of agglomeration. Srolovitz and Goldiner reviewed that a film in tensile stress favors agglomeration, whereas a film in compressive stress would lead to formation of holes or hillocks on the surface of the film.
However, a film in compressive stress could still agglomerate as result of film thinning or exposing part of substrate due to formation of holes or hillocks. Moreover, a compressive stress can also lead to transverse buckling of film creating blisters on the surface of thin film\textsuperscript{57}. Apart from classical size effect, a study of agglomeration of Cu and its comparison with other noble metals such as Au, Pt and Ru is also done as part from of this work.
CHAPTER THREE: METHODOLOGY

Various microstructures of Cu, Ru, Pt and Au were made using Ultra High Vacuum (UHV) Sputtering system for low temperature resistivity measurements of Cu and for studying and comparing the agglomeration behavior of Cu with that of Ru, Pt and Au. The films were then annealed at different temperature in Argon (Ar) and Argon + 3% H₂ ambient. Small samples were made from a larger 3” wafer for resistivity measurements. Resistivity measurements were done using Liquid Helium cold stage, Kiethley Instruments Nanovoltmeter and Kiethley Sourcemeter. Brief description of all the process is given below.

3.1 Sputter Deposition

“Sputtering” is a vacuum process used to deposit very thin films on substrates for a wide variety of commercial and scientific purposes. It is similar to a billiard ball event. Ions are accelerated in an electric field towards the target of material to be deposited, where they knock off or “sputter” the target atoms. It is performed by applying a high voltage across a low-pressure gas to create “plasma,” which consists of electrons and gas ions in a high-energy state. Argon is typically used as the sputtering gas because it is inert and readily available in a pure form and also it has a high sputtering yield. Table 2 shows the comparison of sputtering yield of Argon with other gases.
Table 2: Illustrating sputtering yields of various gases

<table>
<thead>
<tr>
<th>Sputtering gas (energy in keV)</th>
<th>He (0.5)</th>
<th>Ne (0.5)</th>
<th>Ar (0.5)</th>
<th>Kr (0.5)</th>
<th>Xe (0.5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>0.20</td>
<td>1.77</td>
<td>3.12</td>
<td>3.27</td>
<td>3.32</td>
</tr>
<tr>
<td>Al</td>
<td>0.16</td>
<td>0.73</td>
<td>1.05</td>
<td>0.96</td>
<td>0.82</td>
</tr>
<tr>
<td>Au</td>
<td>0.07</td>
<td>1.08</td>
<td>2.4</td>
<td>3.06</td>
<td>3.07</td>
</tr>
<tr>
<td>Cu</td>
<td>0.24</td>
<td>1.80</td>
<td>2.35</td>
<td>2.35</td>
<td>2.05</td>
</tr>
<tr>
<td>Ni</td>
<td>0.16</td>
<td>1.10</td>
<td>1.45</td>
<td>1.30</td>
<td>1.22</td>
</tr>
</tbody>
</table>

During sputtering, energized plasma ions strike a “target,” composed of the desired coating material, and cause atoms from that target to be ejected with enough energy to travel to, and bond with, the substrate. This process is shown in figure 3.1.

![Figure 3.1. The sputtering process.](image-url)
To increase the ion density and hence the sputtering deposition rate a magnetic field is used to capture and spiral electrons, thereby increasing their ionizing efficiency, in the vicinity of the sputtering target. This technique is referred to as magnetron sputtering and has found widespread application of deposition of metals and insulators at high rates.

To study the resistivity of Cu at low temperature, thin films of thickness in the range of 10nm to 200nm were deposited in an ultra high vacuum AJA ATC1800 magnetron sputtering system. The substrates used were 3” Si wafers with 100 nm of thermally grown SiO₂. The system base pressure was approximately 3 X 10⁻⁸ Torr.

The depositions were done in Argon with flow rate of 20 SCCM and chamber pressure set to 4mTorr. The Cu target was fired with a DC source with power set to 200W, which gave a deposition rate of 2.80 Å/sec. Some microstructures were prepared with 3nm to 30nm overlayers and underlayers of SiO₂. The SiO₂ layers were RF sputtered at 250W with deposition rate of 0.81 Å/sec. Small samples of 1cm X 1cm were prepared from 3” wafer and annealed at different temperatures.

To study and compare the agglomeration behavior of Cu, thin films of Cu, Ru, Pt and Au were also deposited in an ultra high vacuum ATC2200V magnetron sputtering system. Again the substrate used here was Si with 100nm thermally grown SiO₂. The substrate was in-situ cleaned with RF plasma at 30W and 10mTorr Ar gas pressure for 15min as it was found that such pre-deposition cleaning prevented the occurrence of pinholes in the thin films. The Cu, Ru, Pt and Au were deposited using DC power source set to 200W; the deposition rates were in the range of 6 Å/sec to 2 Å/sec.
To study the effect of encapsulation layer, some samples were deposited with 3nm and
10nm SiO$_2$ encapsulation layers with SiO2 deposited at 250W with deposition rate of 0.81 Å/sec.
Furthermore, to study the effect of residual film stress on agglomeration, additional samples of
Au and Pt were deposited at higher sputtering gas pressure of 20mTorr. These samples were also
annealed at different temperatures ranging from 50 °C to 1000 °C.

3.2 Annealing

For studying the electrical resistivity of Cu films, samples were annealed in two gases,
Ar and Ar+3%H$_2$, in a quartz tube furnace. Temperatures were in the range of 150 °C to 600 °C
and films were annealed for 30 min.

To study the agglomeration behavior, annealing was performed on the thin films of Cu,
Ru, Pt and Au in an ambient of one atmosphere of an Ar + 3%H$_2$ reducing gas mixture in a
quartz tube furnace. Temperatures in the range of 50 °C to 1000 °C were explored and a
common annealing time of 30 min was used.

3.3 Film Characterization

The basic film morphology of the annealed and as deposited films was observed using
JEOL 6400F scanning electron microscope (SEM) and the grain structures of some selected
films were studied using transmission electron microscope (TEM).
The TEM study was performed by a colleague, Rumy Petrova. One of two techniques was used to prepare plan view TEM specimens: focused ion beam in-situ lift out and chemical etching. For the chemical etching, hydrofluoric acid was used to remove the SiO$_2$ under layer and float off the metal film onto a TEM grid. Analysis was carried out in an FEI Tecnai F30 TEM operating at 300 KeV and the images were recorded on a CCD camera.

3.4 Low Temperature Measurements

Low temperature resistivity measurements of Cu thin films were performed in a liquid Helium cold storage maintained at 4K. Sheet resistance was measured using Keithley 2400 current sourcemeter and Keithley 2182 nanovoltmeter and the temperature was monitored using Lakeshore 331s temperature controller. Software was designed and coded in Visual Basic to operate the nanovoltmeter and sourcemeter through IEEE 488 general purpose interface bus (GPIB) and to get the temperature reading from temperature controller using the serial port of the computer. A multiplexer was designed using relays to do measurements on four different samples and the multiplexer was also controlled by the software through the parallel port. Figure 3.3 show the layout of the experimental setup.

Sheet resistance was measured using a four point probe based on van der Pauw’s$^{58}$ method, as shown in figure 3.4. The resistivity of the thin films was calculated by solving following expression; where $R_A$ and $R_B$ are illustrated in figure 3.d.
\[
\left( -\pi \cdot d \cdot \frac{R_A}{\rho} \right) + \left( -\pi \cdot d \cdot \frac{R_B}{\rho} \right) = 1 \quad \text{(Equation 3.1)}
\]

Figure 3.3. Shown in the figure is the layout of experimental setup for low temperature resistivity measurement.

Figure 3.4. van der Pauw arrangement of Cu samples for low temperature resistivity.
CHAPTER FOUR: RESULTS AND DISCUSSIONS

4.1 Grain Growth with Annealing

Fig. 4.1 show bright field TEM images of the 50 nm thick Au, Pt, Cu and Ru film samples before and after annealing at 300 °C. Only modest grain growth was observed for the Ru film, while a significantly larger grain growth was observed for the other metals. The largest percentage increase in grain size, more than 200%, was observed for the Au thin films, from a 22nm average grain size in as-deposited film to a 69nm grain size in annealed film. Grains in Pt films were observed to grow by about 100%, from a 17nm average grain size in as-deposited film to a 34nm average in annealed film. Grain growth in the Cu films was almost 180% after annealing, from an average grain size of 35nm in the as-deposited films to 98nm in the annealed film. In the Ru thin film, the grain growth was a modest 18%, from 12.1 nm to 14.6 nm. This reduced extent of grain growth in Ru is consistent with Ru having the highest melting temperature of the four metals.

The electron diffraction patterns from all four metals were observed in order to determine the extent of crystallographic texture present in these polycrystalline specimens, i.e., if there was one special plane common to most of the grains. The samples were α-tilted from -45° to 45° and diffraction patterns recorded on the CCD camera. It was found that Au and Pt films showed some texture whereas Cu and Ru did not.
Figure 4.1. TEM bright field images of 50nm thick Au, Pt, Cu and Ru films deposited at 4mTorr: as-deposited film before annealing (a) Au, (c) Pt, (e) Cu and (g) Ru; and after annealing for 30 min at 300°C (b) Au, (d) Pt, (f) Cu and (h) Ru.
From this study it was confirmed that, upon annealing, the thin films undergo normal grain growth and form a typical metallic thin film microstructure consisting of a single layer of equiaxed grains in the plane of the film.

4.2 Temperature Dependence of Resistivity

Figure 4.2 illustrates electrical resistivity of a 50nm Cu thin film in the range of 300K to 6K. In the temperature range 300K – 25K the electrical resistivity of Cu thin film was observed to linearly decrease with decreasing temperature. When normalized to resistivity at 273K, the slope of the temperature dependent part of resistivity corresponds to the temperature coefficient $\alpha_{273K}$ of the resistivity.

![Resistivity vs Temperature](image)

Figure 4.2. The temperature dependence of electrical resistivity of 50nm thick Cu films.
However, at temperatures lower than 25K electrical resistivity of Cu was seen to be independent of temperature and almost constant. From hereon the resistivity at this point, when it is no longer temperature dependent, will be referred to as “residual resistivity”.

It can, therefore, be plausibly assumed in the temperature range 300K - 25K the resistivity was dominated by the electron-phonon interactions and at temperatures less than 25K the resistivity was due to scattering of electrons from surface and/or grain boundaries as phonons freezes at such low temperature.

4.3 The Size Effect

Both the total resistivity and the residual resistivity of the Cu film were observed to decrease with increasing thickness. The figure 4.3 shows this trend of decreasing resistivity with increasing thickness of Cu thin films at 300K and 4K. The resistivity was observed to rise from 1.98\(\mu\)ohm-cm for the thickest film to 6.83 \(\mu\)ohm-cm for the thinnest film whereas the resistivity of the bulk Cu is 1.72\(\mu\)ohm-cm. This phenomenon is termed as size effect.

4.3.1 The Temperature Dependent Resistivity

The temperature dependent results are shown in the figure 4.4 for the range from 77K to 300K. The temperature dependent part of the resistivity is normalized to resistivity value at 273K for better comparability. All the curves are linear over the entire temperature range and the slope of these curves gives the information about the temperature coefficient of resistivity.
The characteristics show dependence of temperature coefficient on film thickness with thicker films exhibiting steeper slope. Figure 4.5 shows dependence of temperature coefficient of resistivity on film thickness. The thinner films exhibit less temperature dependence when compared to the temperature coefficient of the bulk Cu ($4.33 \times 10^{-3} \text{ K}^{-1}$).

Figure 4.3. The “Size Effect”: Electrical resistivity as a function of thickness.
Figure 4.4. Temperature dependence of normalized resistivity of Cu thin films.

Figure 4.5. Temperature coefficient as a function of thickness.
4.3.2 The Residual Resistivity

The residual resistivities in the range of 30K to 3K are shown in figure 4.6. It is evident from the figure that, for all the thicknesses, resistivity is almost constant in the temperature range of 3K to 15K. The residual resistivity could be helpful in determining the mean free path of electrons in the thin films at lower temperature as at such lower temperatures the total resistivity of the film is given by the residual resistivity of the film.

4.3.3 Modeling the Total Resistivity

The thickness dependent resistivity was compared with existing models of Fuchs size effect theory from equation (2.10), Sondheim’s approximation to Fuchs theory from equation (2.11) and Mayadas and Shatzkes grain boundary theory from equation (2.18). For all the models the value of bulk resistivity of the Copper was taken to be 1.75 $\mu\Omega$-cm and mean free path of electrons in Cu was approximated to 39nm. The Fuchs size effect theory and Sondheim’s approximation theory was modeled assuming purely diffuse scattering, i.e. $p=0$. For Mayadas and Shatzkes theory it was assumed that the grain size is equal to film thickness and fraction of electron reflected from grain boundaries to be 0.5. Figure 4.7 illustrates comparison of the aforementioned models with the thickness dependent resistivity results.
Figure 4.6. The residual resistivity of the Cu thin films

Figure 4.7. Comparison of existing models with the thickness dependent resistivity.
As can be seen from the figure no model fully explains the size effect results, however, the Mayadas and Shatzkes model seems to be the closest fit to the experimental results. If these models are accepted as valid, it can plausibly be assumed that scattering due to grain boundary is dominating factor in deciding the total electrical resistivity of the abovementioned Cu thin films.

4.4 Alteration of Copper Resistivity

4.4.1 Resistivity as a Function of Annealing Temperature

Copper thin films were annealed for 30 min at various temperatures. The room temperature electrical resistivity as a function of annealing temperature is shown in figure 4.8. As can be seen in the figure, the resistivity is observed to initially decrease with an increase in annealing temperature, reaches a minimum, and ultimately increases. In 50nm and 100nm films the highest %change in resistivity of 26% and 22%, respectively, was observed in the range of 200 °C to 400 °C. Further annealing, however, results in an increase in resistivity and eventually results in zero conductivity.

This can be explained in terms of morphological changes. The thin films have high surface to volume ratio energy and when annealed the films undergoes morphological changes to reduce the free energy of the system. These changes include grain growth, rearranging grain boundaries and grooving at triple junctions, where three grains meet, which leads to void formation eventually resulting in film breakup. The initial decrease in resistivity with increasing
annealing temperature can be attributed to grain growth, increase in grain size with annealing temperature. Subsequently there is a void growth phase of agglomeration, where the total electrical resistivity increases with further increasing in temperature. Ultimately the film breaks and is no longer continuous and conductive. This phenomenon is also dependent on the size or thickness of the film and is described later in this chapter.

Figure 4.8. Effect of annealing on electrical resistivity of the Cu thin films.
If we now compare the thickness dependence of the films annealed at 150°C with the existing models, the resistivity data is a better fit to Fuchs size effect theory than Mayadas and Shatzkes theory, as was the case before annealing. And therefore it can be stated here that post annealing resistivity is apparently dominated by surface scattering events. Figure 4.9 illustrates these comparisons.

![Resistivity vs Thickness](image)

Figure 4.9 Comparison of total resistivity of Cu thin films annealed at 150°C.

4.4.2 Resistivity as a Function of Cap Layer Thickness

Figure 4.10 shows the resistivity of Cu thin films as a function of encapsulation layer thicknesses. Samples with three different SiO$_2$ cap layer thicknesses of 3nm, 10nm and 30nm. It
was observed that the increase in cap layer thicknesses have small but significant effect on the total resistivity of the thin film. When in contact with SiO₂, Cu is known to form oxides. The formation of copper oxide on the surface of the film could result in increase surface scattering resulting in the higher resistivity than films without cap. The dependence of resistivity of Cu on encapsulation layer thickness could be explained in terms of grain growth in encapsulated films, with thicker encapsulated films having smaller grain sizes. However, more work is needed to understand this phenomenon.

Figure 4.10. The effect of encapsulation layer on the room temperature resistivity of 50nm, 20nm, and 10 nm thick Cu thin films.
When annealed these films exhibit lower resistance than the films without cap. This observation can be explained in terms of the tendency of the cap layer to resist dewetting of the films and/or promote grain growth. The figures 4.11 and 4.12 illustrate the total resistivity at room temperature as a function of annealing temperature and their comparison with the resistivity of films without a cap layer. The decreasing resistance could be explained in terms of the grain growth in the Cu thin films resulting from annealing similar to that of films without cap layer.

![Figure 4.11. The behavior of resistivity of 50nm thick Cu film with 3nm, 10nm and 30nm of SiO_2 encapsulation layer.](image)

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Looking in the figure 4.11 and 4.12 it can be stated that at higher annealing temperatures the encapsulation SiO$_2$ layer resist the agglomeration helping grain growth in the film thereby resulting in lower resistivity than the films without cap layer. It is therefore important to study the effect of encapsulation layer on the kinetics of agglomeration.

![Graph showing the behavior of resistivity of 20nm thick Cu film with 3nm, 10nm and 30nm of SiO$_2$ encapsulation layer.](image)

Figure 4.12. The behavior of resistivity of 20nm thick Cu film with 3nm, 10nm and 30nm of SiO$_2$ encapsulation layer.

4.5 Agglomeration

This section covers the study of the agglomeration of Cu thin films and its comparison with Ru, Au and Pt thin films. The section also includes the effect of encapsulation or cap layer,
annealing temperature, thickness and residual stress on the agglomeration kinetics and/or behavior.

4.5.1 The Process

While thin metallic films are routinely produced and employed in various industries as interconnects, gate electrodes etc, a number of questions arise on their long term stability. One interesting general problem relates to stability against shape changes in the thin films, particularly when shape changes tend to break up the continuous film into group of islands. This phenomenon is termed as agglomeration.

Agglomeration is a thermally activated, two step process of void nucleation and void growth which eventually leads to film breakup forming islands on the film. Figure 4.13 illustrates this process in a 20nm Pt thin film. In the figure 4.13(a), at first the voids forms or nucleates in the film. Further annealing results in the growth and impingement of these voids, figure 4.13(b), leading to film breakup and formation of islands, figure 4.13(c).

The resistivity of the thin films of 20nm Cu, Au, Pt and Ru were observed to increase with the annealing temperature during growth of voids, figure 4.14 illustrates resistivity of these films as a function of annealing temperature. The highest percentage change in resistivity before agglomeration was observed in Au (44%) followed by Cu (26%), Pt (12%) and Ru (9%). The agglomeration process remains the same for all the metals, however, a difference in growth modes was observed for some metals which would be discussed later in this section.
4.5.2 Film Thickness and Agglomeration

For each metal, thicker film samples required a higher annealing temperature to be used to achieve the same extent of agglomeration as the thinner films. One criterion for the extent of agglomeration is island formation, i.e., the percolation threshold, the point at which the film becomes discontinuous and is no longer electrically conductive end to end. This criterion is relevant to device applications of metal films and was also used by us to summarize the effect of film thickness and annealing temperature upon agglomeration. This data is shown graphically in figure 4.15(a), where the thickness at which the percolation limit was exceeded is shown as a function of the temperature of anneal for each of the four metals.

Figure 4.13. The “Agglomeration Process” in 20nm thick Pt thin film.
Figure 4.14. Illustrating resistivity as a function of annealing temperature for 20nm of Cu, Au, Ru and Pt films.

The monotonic increase in thickness with anneal temperature is expected. Other criterions for studying the agglomeration were based on void formation and void growth. For this work void formation was defined as a point where 5% of 1µm² substrate area was uncovered or exposed and void growth as a point where an average of 40% of 1µm² substrate area was exposed. Figure 4.15(b) and 4.15(c) illustrates similar data, but for these slightly different criteria.
We can infer from these graphs that thicker films tend to maintain morphological stability at higher annealing temperatures. The entire agglomeration sequence for 50nm and 100nm thick Ru films could not be studied, as is apparent from the graph, because the range of anneal temperatures explored was not high enough to generate discontinuous Ru films.

4.5.3 Annealing Temperature and Agglomeration

The annealing temperature was varied from 350 °C to 900 °C with a fixed annealing time of 30min to study the effect of temperature on agglomeration. The average island diameter and density as a function of annealing temperature is presented in fig.4.16.

Fig.4.16(a) presents the surface morphologies of 10nm thick Ru and Pt films and figure 4.16(b) illustrates 20nm thick Cu and Au films. From fig.4.16 we learn that with increases in annealing temperature the density of islands decreases and the size of the islands increases. This dependence can be credited to the coalescence of islands at high temperatures.
Figure 4.15. Effect of thickness on agglomeration behavior. Graph showing thickness vs temperature of films deposited at 4mTorr: (a) when film is no longer continuous; (b) when 5% of surface is uncovered per $\mu m^2$; (c) when 40% of surface is uncovered per $\mu m^2$. 
Figure 4.16. Island density and island diameter as a function of anneal temperature of films deposited at 4mTorr.
4.6 The Void Growth Modes

4.6.1 The Capillary Agglomeration Process

The normal, capillary agglomeration process was observed for all of our Ru and Cu thin film samples and an example of this is illustrated by the SEM images of figure 4.17 for the case of a 20nm Cu thin film. Figure 4.17(a) shows the featureless as-deposited thin film. Figure 4.17(b) shows the image of a film annealed at 250°C, where some rough texture can be observed along with initial voids, the latter presumably nucleated at grain boundaries. Further annealing to 350°C results in the initial voids growing to form obvious holes in the film that expose parts of the substrate, as shown in figure 4.17(c). At 450°C this process is further developed, and these holes have grown to impinge upon each other, as shown in figure 4.17(d), and film finally breaks up at 550 °C forming small islands on the substrate surface, as shown in figure 4.17(e). At this point film is no longer continuous.

Annealing at yet higher temperature, 700°C, shows a reduction of island density and increasing island size as shown in figure 4.17(f). This process was common to all of the Cu and Ru samples studied, however the annealing temperature needed to generate a given extent of film agglomeration was found to vary systematically with film thickness and encapsulation, and to be different for the two metals, as described below.
Figure 4.17. The capillary growth mode: SEM images of 20nm thick annealed Cu thin film deposited at 4mTorr: (a) as-deposited before annealing; (b) 250 °C; (c) 350 °C; (d) 450 °C; (e) 550 °C; (f) 700 °C.
4.6.2 The Fractal Growth Process

Voids in the Au and Pt thin films were typically observed to grow in branched manner, described as “fractals”. The main feature of which is that the voided regions appear to be initially elongated, linear, structures and not the regions of minimum perimeter associated with capillary forces. An illustrative example is shown in figure 4.18, which consists of SEM images of a 20nm thick Au film. The as-deposited Au film is shown in figure 4.18(a). After annealing at 300 °C, as shown in figure 4.18(b), voids were found to nucleate in Au thin films creating a hole in the film and exposing the substrate. Figure 4.18(b) also shows large circular blisters in the Au film that will be covered later in this section. Figures 4.18(c), 4.18(d), and 4.18(e), corresponding to anneal temperatures of 400°C, 450°C, and 500°C respectively, show the distinctive fractal appearance of the voids as they grow larger in size. Eventually, island morphology similar to that of the capillary agglomeration process results, as shown in figure 4.18(f) for a sample annealed to 700°C.

This fractal agglomeration process was observed for all the Au and Pt thin films we studied except the thinnest, 10 nm thick, Au films and the Au and Pt films deposited at higher Ar pressure.
Figure 4.18. SEM images of 20nm of annealed Au thin film deposited at 4mTorr: (a) as-deposited before annealing; (b) 300 °C; (c) 400 °C; (d) 450 °C; (e) 550 °C; (f) 750 °C.
The circular blisters that can be seen in Figure 4.18(b) were usually present on the Au and Pt films deposited at low pressure (4 mTorr), but were always absent on the Cu and Ru films that were similarly deposited. The blisters were present on almost all of the annealed thin films of Au and Pt and on the as-deposited films of Au and Pt, except for the 10nm thick as-deposited Au film. They were also observed to grow with time on the as-deposited films. The case of the 10nm Au film is discussed later in the next section. The blisters are believed to areas of film delamination.

Kwon et al and Hummel et al also observed blisters in their films and they credited Ar collecting at the film-substrate interface as the cause for this delamination. They assumed the blisters to be Ar bubbles formed from Ar gas atoms incorporated in the film during sputter deposition and further concluded that these blisters had no effect on the agglomeration sequence\(^5\). While trace Ar amounts can usually be found in sputtered films, the diffusion of Ar atoms over the micron-scale distances required to collect Ar at a blister location seems unlikely compared to the Ar atoms simply diffusing the 10nm - 50nm required to escape from the top surface of the film.

Instead, these blisters were interpreted to be circular regions of film delamination resulting from the combination of residual compressive stress in the film and poor adhesion of Au and Pt to the SiO\(_2\) substrate. Only the as-deposited thinnest Au film, at 10 nm, failed to develop blisters with time, consistent with this model.
Also consistent with this model are the separate observations of film adhesion using a qualitative “scotch tape test,” which indicated stronger film-substrate adhesion for Cu and Ru films, where blisters were not observed, compared to the Au and Pt films.

To test this assumption of blisters resulting from a combination of compressive stress and poor film adhesion to the substrate, 10nm and 50nm thick Au and Pt films were deposited at a higher sputtering gas pressure of 20 mTorr. Since a higher sputtering gas pressure is expected to reduce the initial compressive stress in the film and result in a transition to a tensile stress; an elimination or reduction in the blister formation of these films was anticipated. This did, indeed, occur. No blisters were found on the films deposited at high gas pressure, for both the annealed and the as-deposited samples. These films also had qualitatively better adhesion than the films deposited at 4mTorr.

Unexpectedly, these films all showed a capillary agglomeration process instead of the fractal agglomeration process observed for the Pt and the thicker Au films deposited at lower pressure. Figure 4.19 show SEM images of the capillary agglomeration process for the 50nm Au and Pt thin films deposited at high gas pressure. These films were observed to agglomerate following a process similar to that observed in the Cu and Ru thin films. The blister-free, 10nm thick Au film was also observed to follow a capillary agglomeration process. Significantly, these Au and Pt films that did not have a fractal agglomeration process also did not have the delamination blisters.

This coincidence of delamination blisters and fractal agglomeration is significant, and suggests that the fractal agglomeration may be a morphological instability that occurs from both
top and bottom surfaces of the film simultaneously, as if the film were free-standing, rather than adhered to the substrate and de-wetting from just the free surface downwards. This view is supported by the observation that the delamination blisters, when present, were also found to be a more probable region for void nucleation in the Au and Pt thin films.

Figure 4.20 shows SEM images of four examples of Au and Pt films that illustrate this tendency. In all of the images, voids are formed in the blister region. It should be pointed out that the film portion that is free-standing in the blister region is susceptible to grain boundary grooving on both top and bottom surfaces. Grain boundary triple points are expected to be coincident on the top and bottom surfaces of these films due to their equiaxed grain structure. For such a film microstructure, a void would be expected to nucleate more readily in the freestanding portions of the film than in an adhered region.
Figure 4.19. Surface morphologies of 50nm thick annealed Au and Pt films deposited at 20mTorr: 50nm Au films (a) as-deposited before annealing; (b) 300 °C; (c) 450 °C; (d) 600 °C; 50 nm Pt films (e) as-deposited before annealing; (f) 600 °C; (g) 750 °C; (h) 900 °C.
Figure 4.20. Void nucleation at blisters observed in Au and Pt films deposited at 4mTorr:

(a) 20nm thick Pt film annealed at 300 °C; (b) 20nm thick Au film annealed at 450 °C; (c) 50nm thick Au film annealed at 600 °C and (d) 50nm Pt film annealed at 600 °C.

A fractal appearance as the film breaks up is also consistent with the “nearly free-standing” view proposed here for the low pressure deposited Au and Pt films. An initial void can propagate more readily as a linear defect in the free standing film without the mass transport needed to move film atoms away from the voided region in an adhered film.

4.7 Effect of Cap Layer on Agglomeration Kinetics

The study of a free-standing film, with two free surfaces, is experimentally difficult. However, it is experimentally convenient to prepare samples with no free surfaces, by the sputter deposition of a SiO₂ encapsulation layer on top of the metal films. Samples having 3 nm and 10
nm thick encapsulation layers on 20 nm and 50 nm thick films of all four metals studied were prepared, and annealed as before to study the agglomeration process. Figure 4.21 shows SEM images of the Cu and Pt thin films as illustrative examples.

For all cases, the presence of an encapsulation layer reduced the tendency of the film to agglomerate, with the thicker encapsulation layer having a stronger effect. These tendencies are summarized in figure 4.22, which show the thickness at which the initial void formation and percolation threshold is reached for all four metals as a function of anneal temperature.

Figure 4.21. Effect of encapsulation layer on agglomeration behavior: SEM images of annealed 50nm thick Cu and Pt films deposited at 4mTorr: Cu films annealed at 500°C (a) without cap layer; (b) with 3nm cap layer; (c) with 10nm cap layer. Pt thin films annealed at 650°C (d) without cap layer; (e) with 3nm cap layer; (f) with 10nm cap layer.
Figure 4.22. Effect of encapsulation layer on agglomeration behavior. Graph showing thickness vs temperature, of films deposited at 4mTorr, at: (a), (c) and (e) void nucleation; (b), (d) and (e) island formation.
The greater effectiveness of the thicker encapsulation layers to prevent film agglomeration is consistent with the encapsulation layers having a primarily mechanical effect to reduce the grain boundary grooving (playing a role in the force balance), rather than a surface chemistry effect that modifies the mass transport on the film top surface. Thus encapsulation layer can find its application to promote grain growth in interconnects ensuring line stability.

The films used for the encapsulation series of experiments were all deposited at 4 mTorr and both fractal agglomeration for Pt and Au and capillary agglomeration for Cu and Ru were observed as before, indicating that while the kinetics of the agglomeration process were slowed by the encapsulation layer, the fundamental driving forces for the two agglomeration processes remained similar. Therefore it can plausibly be stated here that at higher annealing temperatures thicker encapsulation layers can be employed in order to obtain greater grain growth, ensuring stability of the thin film while reducing the resistivity of the thin film.
CHAPTER FIVE: CONCLUSION

The effect of annealing on the classical size effect in the Cu having thicknesses in the range of 10nm to 200nm thin films was studied and reported here. The films studied were observed to have weak or no fiber texture and a normal extent of grain growth, forming a typical, equiaxed, thin film metallic microstructure. The un-annealed Cu thin films were found to have higher resistivity than the annealed films.

The resistivities of un-annealed films were found to follow Mayadas and Shatzkes model and the annealed films were found to follow Fuchs size effect theory. When annealed the films undergoes grain growth resulting in lower resistivities thereby confirming the role of grain size on resistivity of the film. However, there is a limit to annealing, i.e. agglomeration phenomenon.

The agglomeration behavior of Cu, Ru, Au and Pt thin films of thicknesses in the range of 10 nm to 100 nm were investigated and the extent of and the qualitative appearance of the film agglomeration as a function of annealing temperature was reported.

It was found that Au and Pt films deposited at 4 mTorr have circular delamination, relatively poor adhesion, and have a “fractal” appearance during agglomeration. Cu and Ru thin films deposited at the same pressure have better adhesion, do not have delamination, and agglomerate with the more common appearance of an increasing density and size of voids.

Au and Pt films deposited at 20 mTorr have improved adhesion, an absence of delamination, and an agglomeration appearance similar to that of the Cu and Ru thin films. It was observed that the delaminated regions, when present, were preferred areas for initial void
formation. The fractal appearance of the agglomerating films is postulated due to the rapid propagation of a linear void defects in free-standing and weakly adhered films.

Samples prepared with a SiO$_2$ encapsulation layer on top of the metal films were observed to follow a similar agglomeration process as the un-encapsulated films of the same metal, but with significantly higher annealing temperatures required to develop the same extent of agglomeration. A 10 nm thick encapsulation layer was found to have a stronger effect than a 3 nm layer, and this was postulated as due to a mechanical hindrance of grain boundary grooving, and hence void initiation, at the film top surface.

The un-annealed samples with SiO$_2$ encapsulation layer were found to have higher resistivity than the samples without encapsulation layer. Moreover, the resistivity increases with the thickness of the cap layer. However, when annealed the samples with cap layer are found to have lower resistivity than their counterparts, mainly due to prolonged grain growth in the metallic thin film without breaking down.

Results in this work suggest that future studies should include grain growth mechanism in encapsulated films to understand the higher resistivity at room temperature. Future studies should also include a quantitative study of the relationship of film stress to the agglomeration morphology, and a cross-sectional TEM study of the “fractal” agglomeration samples, to test the hypothesis that grain boundary grooving is occurring on both top and bottom film surfaces.
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