Single Switch AC/DC Converter with Power Factor Correction (PFC)

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Issa Batarseh
University of Central Florida

Peter Kornetzky
University of Central Florida

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SINGLE-SWITCH AC/DC CONVERTER WITH POWER FACTOR CORRECTION (PFC)

Inventors: Issa Batarseh, Oviedo, Fla.; Peter Kornetzky, Ilmenau, Germany

Assignee: University of Central Florida, Orlando, Fla.

Filed: Jun. 22, 1998

Primary Examiner—Adolf Dencke Berhane
Attorney, Agent, or Firm—Brian S. Steinberger; Law Offices of Brian S. Steinberger

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4,533,986 8/1985 Jones ............................... 363/17
5,224,025 6/1993 Divan et al. ...................... 363/16
5,416,387 5/1995 Cuk et al. ......................... 363/200
5,442,534 8/1995 Cuk et al. ......................... 363/16
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5,461,301 10/1995 Truong ......................... 323/207

PSPICE simulation and experimental results, a measured power factor of 0.99 was obtained by this single switch converter.

One-stage power factor correction (PFC) with output electrical isolation. The converter has a configuration of combining a boost circuit and a forward circuit in one power stage. To relieve the voltage spike caused by the leakage inductance of the power transformer, two bulk storage capacitors are used. The same power switch is shared by the PFC circuit and the power conversion circuit. Due to its simplified power stage and control circuit, this converter presents a better efficiency (87%), lower cost and higher reliability. Detailed steady state analysis results show this novel converter has both good power factor correction and excellent regulation capabilities.
Fig. 3
Fig. 4 Storage capacitor voltage of the converter.

Fig. 5 Ac/dc conversion characteristics of the converter.
Fig. 6 Maximum duty cycle.

Fig. 7 Line regulation capability of the converter.
Fig. 8 Load regulation capability of the converter.
Fig. 9(a) Voltage (upper) and current (lower) at the switch.

Fig. 9 (b) Line voltage and filtered input current of the converter.
Fig. 10 (a) Voltage (upper, 200V/div.) and current (lower, 2A/div.) at the switch.

Fig. 10 (b) Line voltage (upper, 200V/div.) and filtered input current (lower, 1A/div.) of the converter.
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SINGLE-SWITCH AC/DC CONVERTER
WITH POWER FACTOR CORRECTION (PFC)

This invention relates to AC to DC converters. This invention is a Continuation-In-Part of U.S. Provisional Patent Application 60/050,476 titled “AC/DC Converters” filed Jun. 23, 1997.

BACKGROUND AND PRIOR ART


U.S. Patents have been proposed for AC/DC converters with power factor correction but fail to overcome the problems presented above. See for example, U.S. Pat. Nos. 5,224,025 to Divan et al.; 5,416,387 and 5,442,539 to Cuk et al.; 5,479,331 to Lenni; 5,510,974 to Gu et al.; 5,515,257 to Ishii; 5,559,688 to Pringle; 5,592,128 to Hwang; 5,594,629 to Steigerwald; 5,598,326 to Liu et al.; 5,600,546 to Ho et al.; and 5,619,404 to Zak.

SUMMARY OF THE INVENTION

The first objective of the present invention is to provide a switching power supply that operates from AC line voltage having a high power factor and output isolation.

The second object of this invention is to provide for a one-stage power factor correction in an AC to DC converter.

The third object of this invention is to provide an AC to DC converter having an output transformer that allows the converter to be used for single output and multi-output applications.

The fourth object of this invention is to provide an AC to DC converter where the leakage inductance of the forward mode power transformer will not cause an additional voltage stress at the power switch so that a power switch having a lower voltage rating and less power dissipation can be used.

The fifth object of this invention is to provide an AC to DC converter which uses the leakage inductance of its power transformer as part of the power supply design and
converter 1 includes voltage supply VAC, 10, which can be alternating voltage or current line, that provides sinusoidal voltage with rms value of approximately 120 Volts or another value with a line frequency of approximately 60 Hz, and the like. Output terminals of voltage supply 10, 10a and 10b are connected to input terminals 20a and 20b of any type of an electro magnetic interference (EMI) filter 20. EMI filter, 20 includes storage devices that attenuates high transients of current passing terminals 20c and 20d on the way to the terminals 10c and 10b of voltage supply VAC. Output terminals of EMI filter 20, 20e and 20d are connected to the input terminals 50a and 50b of a line rectifier 50 of a conventional type such as KBLO6 or any other type consisting of a bridge arrangement of unidirectional conducting devices such as semiconductor diodes in a way that positive voltage of output of line rectifier is delivered to terminal 50c and negative voltage is delivered to terminal 50d which is connected to ground level 53 of boost/forward (primary) stage 53. Terminal 50c is connected to terminal 102a of an inductive device 1, 102, having a value of approximately 420 µH, and the like.

Terminal 102b is connected to terminal 104a of a unidirectional conducting device D1, 104 such as a fast acting semiconductor diode such as MUR850, and the like. Output terminal of D1, 104b is connected to positive terminal 106a of a controllable switching device 106, such as a solid state switch such as power MOSFET Type IRF740 or another type of a switching device, and the like. Negative terminal of switching device 106b is connected to ground level 53.

Switching device 106 switches on and off with a frequency higher than line frequency and with a ratio of an on and off time that is processed from output voltage at terminal V0, 132 with respect to output ground, 130 is kept constant within small limits. While switching device S, 106 is on, Inductive device 1, 102 receives energy from voltage supply VAC, 10 via EMI filter 20 and line filter 50. While switching device S 106 is off, energy stored in inductive device 1, 102 is mainly transferred to the capacitive devices CS2, 116 and CS1, 114 via the chain D1, 104, and CS2, 116 and D2, 112 and CS1, 114 and terminal 50d and terminal 50c to terminal 102a of inductive device L, 102. The capacitances of capacitive devices CS1, 114 and CS2, 116 have a value of approximately 820 µF that is great enough to keep the voltages VCS1 and VCS2 across capacitive devices CS1, 114 and CS2, 116 constant within small limits at a value that is always greater than peak value of voltage supply VAC, 10 during normal operation. D2 is a unidirectional conducting device such as a fast acting semiconductor diode such as Z336X and the like. This mode of operation is alike a boost converter and shapes the average current drawn from the power supply VAC, 10 to be of the same shape like the voltage Vline across the power supply VAC, 10. Referring to FIG. 1, forward mode transformer TR, 100 consists of two primary windings 110a and 118m with equal turn numbers and secondary winding 122. The turn ratio of windings 110:118:122 is approximately 1:1:0.4. Furthermore leakage inductors L1, 108 and L2, 120, have a value of approximately 260 µH (each) and the like, in serial to primary windings 110m and 118m respectively.

Referring to FIG. 1, storage capacitors CS1, 114 and CS2,116 are connected to the primary part of forward mode transformer TR, 100 as follows: Terminal 114a of capacitive device CS1, 114 and terminal 118c of leakage inductance L2, 118 are connected to ground 53. Terminal 114b of capacitive device CS1, 114 and terminal 112b of unidirectional conducting device are connected together with terminal 110a of primary winding 110m. Terminal 114b of
capacitive device CS2, 116 and terminal 112a of unidirectional conducting device are connected together with terminal 118a of primary winding 118m. Terminal of 110b of leakage inductance L1, is connected to terminal 116b of capacitive device CS2, 116 and to terminal 106a of switching device D3. The terminals 110b, 118a and 112a of forward mode transformer are marked with a dot. They are marked as the beginning of the windings, this means that they always have the same polarity with respect to the terminals 118b, 118a and 122b. While switching device S, 106 is on, energy is transferred from the capacitive devices CS1, 114 and CS2, 116 to the secondary winding 122 of forward mode transformer TR, 100. While this happens part of the energy stored in the capacitive devices CS1, 114 and CS2, 116 is also stored in the leakage inductors L1, 110 and L2, 118. These two inductors act as a current limiter for energy transfer. If switching device S, 106 is off, energy stored in the leakage inductors L1, 110 and L2, 118 is fed back into the storage devices CS2, 116 and CS1, 114 as well as into the secondary winding 122 of forward mode transformer TR, 100. The secondary winding 122 can be completely isolated from the primary side. RL corresponds to the resistive part of a possible load between the output terminal VO, 132 of converter and output ground 130. Secondary winding 122 and unidirectional conducting device D3, 124 can be an unidirectional conducting device such as a fast acting semiconductor diode such as MUR850 and the like. Components 112a, 124 and capacitive device CL, 126 form a closed loop, where current flow is only allowed towards terminal 124b of semiconducting device D3. Terminals 122a of secondary winding 122 and negative terminal 126a of capacitive device CL are connected to output ground level. Capacitive device CL has a value of approximately 900 μF, that keeps output voltage VO constant within small limits while current ID3 of unidirectional device D3, 124 is not equal to load current IL.

The basic circuit schematic of the novel single switch converter is shown in FIG. 1A. It can be shown that in steady state the converter operates in four operation modes during one switching cycle. Table I shows the four modes of operation and conducting devices during their corresponding time intervals. The equivalent circuits of the four operation topologies are shown in FIG. 2 and converter key waveforms are shown in FIG. 3.

Notice that in one switching cycle, the line voltage can be considered as a constant voltage 10, represented by Vg in the equivalent circuits. Capacitors CS1, 114 and CS2, 116 are designed to be large and equal. Hence, in the steady state analysis, each capacitor voltage was approximated by a dc source VCS1=VCS2=VCs. The four modes of operation are discussed as follows:

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Time intervals</th>
<th>Conducting device</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0 ≤ t &lt; t1</td>
<td>S: 106, D1: 104, D2: 112, D3: 124</td>
</tr>
<tr>
<td>M2</td>
<td>1 ≤ t &lt; t2</td>
<td>S: 106, D1: 104, D2: 112, D3: 124</td>
</tr>
<tr>
<td>M3</td>
<td>2 ≤ t &lt; t3</td>
<td>S: 106, D1: 104, D2: 112, D3: 124</td>
</tr>
<tr>
<td>M4</td>
<td>3 ≤ t &lt; t4</td>
<td>S: 106, D1: 104, D2: 112, D3: 124</td>
</tr>
</tbody>
</table>

A. Mode 1 (0 ≤ t < t1)

Referring to FIG. 1A, mode 1 begins at t=0 when the power switch is turned ON 106. With diode D1 104 conducting, the source voltage is applied to the input choke inductor L1 102, causing the current through the inductor increasing linearly. During this mode, energy is transferring from the source to the choke inductor. On the other hand, diode D2 112 is blocked by the two-capacitor voltages since the positive end of CS2 is grounded by the power switch. Thus, the diode splits the primary sides of the forward transformer into two symmetrical branches with one storage capacitor in each. These capacitors (previously charged) feed the primary sides of the forward transformer individually, resulting in part of the energy stored in the two capacitors being transferred to load, represented by load register RL, 128 and to output storage capacitor CF during this mode.

This mode ends at t=t1 when the power switch is turned OFF as shown in FIG. 3. During this mode, we have

\[
\begin{align*}
&i_1(t) = i_{10}(t) = \frac{V_s}{L_1} t, \\
&i_2(t) = i_{21}(t) = \frac{nV_{CS} - V_s}{nL_2} t, \\
&i_{B1}(t) = \frac{2}{n} i_{B2}(t) = \frac{2nV_{CS} - V_s}{n^2 L_1} t, \\
&i_{B2}(t) = 0, V_0(t) = 0.
\end{align*}
\]

The duration of this stage is

\[
\Delta t = T_1 D,
\]

Where

\[
D = \frac{n - b}{T_1},
\]

is the duty cycle.

B. Mode 2 (t1 ≤ t < t2)

Referring to FIG. 2b, during this operation mode, the power switch is turned OFF and diode D2 is turned ON due to a current IL+2 IL1 flowing through it. The equivalent topology is shown in FIG. 2 (b). Under the constraint of KCL, both the storage capacitors, CS1 and CS2, are being charged by current IL+IL1 during this operation mode. With the linear decreasing of the inductor current IL, magnetic energy stored in the choke L1, 102 is being converted into electric energy and being stored into the storage capacitors. Thus the energy loss of the storage capacitors during Mode 2 is being recovered. At the same time, the leakage inductances L1, 110 and L2, 118 of the forward transformer is completely demagnetized, i.e. IL1 and IL2 become zero, the converter’s operation enters Mode 3. Using FIG. 2(b), the following expressions are obtained:

\[
\begin{align*}
&i_1(t) = i_{11}(t) = \frac{V_s}{L_1} DT_1, \\
&i_2(t) = i_{22}(t) = \frac{nV_{CS} - V_s}{nL_2} DT_1, \\
&i_{B1}(t) = \frac{2}{n} i_{B2}(t) = \frac{2nV_{CS} - V_s}{n^2 L_1} DT_1, \\
&i_{B2}(t) = 0, V_0(t) = 2V_{CS}.
\end{align*}
\]
The time intervals $\Delta t_2$ is given by:

$$\Delta t_2 = t_2 - t_1 = \frac{nV_{C}}{V} DT_s,$$

(2b)

C. Mode 3 ($2 \leq t < 3$)

Referring to FIG. 2c, the choke inductor current, $i_L$, continues to decrease linearly in this mode. Owing to the existence of diode $D_3$, the primaries of the transformer present very high impedance (FIG. 2 (c)) with the currents through the windings can be negligible for energy transfer to the output. This mode ends when the choke inductor current reaches zero. The key voltages and currents in this duration can be described as followed.

$$i_L(t) = i_{D1}(t) = i_{D2}(t) = 0;$$

$$V_{CS} = 2V_{CS} - V_{C}.$$  

(3a)

The time intervals are:

$$\Delta t_3 = \Delta t_1 = \Delta t_2,$$

(3b)

where $\Delta t_3 = \frac{V_L}{2V_{CS}} - DT_s.$

D. Mode 4 ($3 \leq t < 4$)

Referring to FIG. 2d, the operation mode between $t_3$ and $t_0+T_s$, when the cycle repeats, is known as a free wheeling stage, which is used for regulation purposes. When the power switch is turned ON again at $t = t_0$, the converter operation goes into the next cycle. During this mode, we have

$$i_L(t) = i_{D1}(t) = i_{D2}(t) = 0;$$

(3a) Using the rms value of the line voltage as the input of the converter, the voltage across the storage capacitor can be determined by,

$$M = \frac{V_{CS}}{V_{nom}} - \text{ac/dc conversion ratio},$$

$$m = \frac{V_{CS}}{V_o} - \text{dc/dc conversion ratio},$$

$$m_2 = \frac{V_{CS}}{V_o} - \text{inductor ratio},$$

$$m = \frac{V_{CS}}{V_o}.$$  

(4)

A. Ac/De Conversion Ratio

Using the rms value of the line voltage as the input of the converter, the voltage across the storage capacitor can be determined by,

$$V_{CS} = \frac{V^2}{R_m};$$

(5)

Based on the assumption of lossless converter, we have

$$P_{in,ave} = P_{out,ave},$$

resulting in the following ratio,
From FIG. 6, it can be seen that for a given conversion ratio M, the smaller the transformer turn ratio is, the larger the maximum duty ratio will be. In practical application, selection of n should be made based on the trade off between regulation capabilities and device stresses.

Referring to FIG. 7, we can investigate the line regulation capability of the proposed ac/dc converter. For example, the converter was designed with n=0.25, Vo=50V. At load m n=0.5, the Mac gain can change between 0.1 to 0.82, which means theoretically, the output can be kept at 50V while the input voltage is changing within the range of 61V–95V. The duty ratio range is between 0.08 to its maximum 0.8. In short, ±20% variation in the line voltage requires the duty ratio change by 58% to maintain constant output.

Similarly, the load regulation capability can be examined by using FIG. 8. For an ac/dc converter with n=0.25, fS=50x10^3 Hz, L=300 µH, Mac=0.455 (Vline,rms=110V, Vo=50V), theoretically, m can vary between 0.1 to 1.3 with the output voltage being kept at 50V. If the load changes ±50%, to maintain a constant output, a duty ratio change of 66% is required.

C. Power Factor Correction

The line current is determined by

\[
i_{lin}(t) = \frac{\sqrt{2} V_{line} \cos(\omega t)}{2L} = \frac{\sqrt{2} V_{line,ref} \sin(\omega t)}{2L}
\]

where: \(\omega L\) is the line angular frequency.

Since Ts and L are constant and Dac is nearly constant, iline(t) and vline(t) have the same wave-shape. Therefore, a good power factor can be obtained by the novel converter.

D. Voltage and Current Stresses

TABLE II
Voltage and current stresses on switch and diodes under nominal condition

<table>
<thead>
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<th>Device</th>
<th>Voltage Stress</th>
<th>Current Stress</th>
</tr>
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<tbody>
<tr>
<td>S 106</td>
<td>2Vcs (\left(\frac{\sqrt{2} V_{line,ref}}{L} + \frac{2V_{Cs} - V_o}{nI_d}\right)DT_s)</td>
<td></td>
</tr>
<tr>
<td>D1 104</td>
<td>2Vcs (\frac{\sqrt{2} V_{line,ref}}{L} DT_s)</td>
<td></td>
</tr>
<tr>
<td>D2 112</td>
<td>2Vcs (\frac{\sqrt{2} V_{line,ref}}{L} + \frac{2V_{Cs} - V_o}{nI_d})DT_s</td>
<td></td>
</tr>
<tr>
<td>D3 124</td>
<td>(\frac{V_o + nV_{Cs}}{n^2I_d} DT_s) Approximately (\frac{2nV_{Cs} - V_o}{n^2I_d})DT_s</td>
<td></td>
</tr>
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</table>

Through steady state analysis, the voltage and current stresses on each switch were found as listed in Table II.

E. Output Voltage Ripple

By integrating the current through the output capacitor Cf, the output voltage ripple is given by

\[
\Delta V_o = \frac{m}{2n I_d C_f f_s^2} \left(2TD_m - 2D - n^2 k_{t_o}\right) - \left(\frac{1}{2m^2} - 1\right).
\]

From FIG. 6, it can be seen that for a given conversion ratio M, the smaller the transformer turn ratio is, the larger the maximum duty ratio will be. In practical application, selection of n should be made based on the trade off between regulation capabilities and device stresses.

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<td></td>
</tr>
<tr>
<td>D1 104</td>
<td>2Vcs (\frac{\sqrt{2} V_{line,ref}}{L} DT_s)</td>
<td></td>
</tr>
<tr>
<td>D2 112</td>
<td>2Vcs (\frac{\sqrt{2} V_{line,ref}}{L} + \frac{2V_{Cs} - V_o}{nI_d})DT_s</td>
<td></td>
</tr>
<tr>
<td>D3 124</td>
<td>(\frac{V_o + nV_{Cs}}{n^2I_d} DT_s) Approximately (\frac{2nV_{Cs} - V_o}{n^2I_d})DT_s</td>
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\]
F. Critical Choke Inductance

The critical choke inductance was found as

$$L_{cr} = \frac{DB_f}{f_s M^2}.$$  \hspace{2cm} (12)

To ensure the converter operating in DCM, the choke inductor must be selected with a value smaller than the critical inductance.

**Guideline of the Single Switch Converter**

The novel ac/dc converter can be based on the following principles:

- **a)** Selection of Transformer Turn Ratio $n$

  Selection of transformer turn ratio should be based on the trade off between regulation capabilities and voltage stresses on the devices. According to Eq. (5), a low $n$ will result in high voltage across the storage capacitors. Since all the voltage stresses on the switches ($S_1$ and $D_1-D_3$) depend on $V_{Cs}$, we prefer a higher transformer turn ratio. On the other hand, from FIG. 6, a higher $n$ causes the maximum duty cycle to be lower, reducing both the line and load regulation capabilities. Hence, a lower transformer turn ratio is desired in this case. In practical design, a proper value of $n$ should be chosen so that it gives enough regulation capabilities and lower voltage stresses as well.

- **b)** Setting of Nominal Duty Ratio and Normalized Load

  When $n$ has been chosen, a group of curves as shown in FIG. 8 for $n=0.25$ can be generated. The nominal duty ratio can be approximated by

  $$D_{nom} = 0.1 + 0.5(D_{max} - 0.1) = 0.1 + 0.5(0.65 - 0.1) = 0.38.$$ \hspace{2cm} (13)

  From FIG. 8, corresponding to the nominal duty ratio, normalized load $m$ can be found.

- **c)** Selection of Choke Inductance

  The value of choke inductance is given by

  $$L = n \cdot RL \cdot TS = 0.5 \times 50 \times 2 \times 10^{-5} = 500 \mu H.$$ \hspace{2cm} (14)

- **d)** Selection of $L_1$ and $L_2$

  From Table II, it seems that to relieve high current stresses, we should increase the inductance $LI$. But the effect will be very weak because the storage capacitor voltage increases with the increasing of $k=L_1/L$ as shown in Eq. (6c). In practical design, we prefer a small value of $k$ so that the voltage stresses can be reduced. For a given $k$, $L_1=L_2$ can be selected according to

  $$L_1=L_2=k \cdot L.$$ \hspace{2cm} (15)

- **e)** Selection of the Storage Capacitance

  To select the storage capacitors, let's consider that due to the missing of one line cycle, an average voltage drop of $V_{Cs}$ on the storage capacitor is allowed, then by analysis we have

  $$C_S = \frac{T_L}{k_s (2-k_s) R_s m^2},$$ \hspace{2cm} (16)

  and the voltage stress on the storage capacitor can be calculated by

  $$V_{C Seam} = \frac{V_0}{m}.$$ \hspace{2cm} (17)

  where $m$ can be determined by Eq. (4).

- **f)** Selection of Output Capacitor

  From Eq. (11), we get

  $$C_f = \frac{m}{2n} \cdot \frac{(2D_{nom} - 2D - n^2 \cdot k_s)^2}{m^2 \cdot 2} = \frac{1}{\Delta V_{Cs}}.$$ \hspace{2cm} (18)

  For a given design with specified ripple factor, we can find an output capacitance. Together with the output voltage, an output capacitor can be chosen.

- **g)** Selection of Switches

  The selection of switches should be based on their voltage and current stresses which can be calculated according to the equations listed in Table II.

  Based on the above guidelines, we obtain the converter parameters as follows.

  a) Transformer turn ratio $n$

  From FIG. 6, let’s select $n=0.25$ which gives a maximum duty ratio of 0.65 at $M_{max}=0.455$.

  b) The average duty ratio at nominal input is:

  $$D_{nom} = 0.1 + 0.5(D_{max} - 0.1) = 0.1 + 0.5(0.65 - 0.1) = 0.38.$$ \hspace{2cm} (13)

  From FIG. 8, $n=0.5$ can be chosen.

  c) The choke inductance is hence determined by

  $$L = n \cdot RL \cdot TS = 0.5 \times 50 \times 2 \times 10^{-5} = 500 \mu H.$$ \hspace{2cm} (14)

  d) Let’s choose $k=0.16$. Then we can select $L_1$ and $L_2$ as

  $$L_1=L_2=k \cdot L = 0.16 \times 500 = 80 \mu H.$$ \hspace{2cm} (15)

  e) Suppose that due to one line cycle missing, an average voltage drop of $0.1 V_{Cs}$ on the storage capacitor is allowed, i.e. $k_s=0.1$. Then we have

  $$C_s = \frac{T_L}{k_s (2-k_s) R_s m^2},$$

  where

  $$m = \frac{1}{2} \left[ 1 + \frac{k_s r_s}{2 D^2} + \sqrt{\left( \frac{1}{n} + \frac{k_s r_s}{2 D^2} \right)^2 + \frac{2 k_s r_s}{D^2}} \right].$$

  So

  $$C_s \approx \frac{1.667 \times 10^{-2}}{0.1} = 102 \mu F,$$

  and $VC_s = m V_0 = 207 V$.

  Select $CS=110 \mu F@250 V$.

  f) From Eq. (18), the output capacitance can be determined by

  $$C_f = \frac{m}{2n} \cdot \frac{(2D_{nom} - 2D - n^2 \cdot k_s)^2}{m^2 \cdot 2} = \frac{1}{\Delta V_{Cs}}.$$ \hspace{2cm} (18)

  For a given design with specified ripple factor, we can find an output capacitance. Together with the output voltage, an output capacitor can be chosen.
The theoretical switch and diodes voltage and current stresses under nominal condition are listed in Table III.

<table>
<thead>
<tr>
<th>Device</th>
<th>Voltage Stress (V)</th>
<th>Current Stress (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>414</td>
<td>3.69</td>
</tr>
<tr>
<td>D1</td>
<td>414</td>
<td>2.36</td>
</tr>
<tr>
<td>D2</td>
<td>414</td>
<td>3.69</td>
</tr>
<tr>
<td>D3</td>
<td>Approximately 153.5</td>
<td>5.32</td>
</tr>
</tbody>
</table>

According to the above-calculated stresses and considering switching time, we choose:

S: IRF840; D1, D2 and D3: MUR850.

Simulation and Experimental Results

By using the above circuit parameters, a closed-loop schematic of the proposed single switch converter was simulated by PSPICE and the simulation results are shown in FIG. 9. An experimental prototype of the converter was built up in the laboratory with the same circuit parameters. To obtain the transformers ratio (n=0.25), the primary windings and secondary windings were built with exciting inductance. Pulse-width-modulation chip SG3525 was used for the closed-loop control. The experimental waveforms of voltage and current at the switch and filtered line current, shown in FIG. 10a and 10b, were recorded by using an hp54542A oscilloscope. Both the simulated and the experimental waveforms agree well and show that the waveforms of the line voltage and the input current are almost sinusoidal ones with no phase difference, proving that a good power factor can be achieved by this converter topology. The measured power factor is 0.99. In the experiment, and an efficiency of 87% was obtained. Measured power factor and efficiency shows that the novel AC to DC converter can maintain 99% PF with the line changing from 85V AC to 135V AC. At the nominal load, 87% efficiency was obtained.

While the invention has been described, disclosed, illustrated and shown in various terms of certain embodiments or modifications which it has presumed in practice, the scope of the invention is not intended to be, nor should it be deemed to be, limited thereby and such other modifications or embodiments as may be suggested by the teachings herein are particularly reserved especially as they fall within the breadth and scope of the claims here appended.

We claim:

1. A power supply that provides a DC(Direct Current) power to a load from an AC (Alternating Current) source comprising:
   a rectifying stage for transferring electrical energy from an AC source into pulsating unipolar voltage pulses at output terminals;
   a boost stage having a controllable conducting means and a first unidirectional conducting means for controlling

   current flow from the output terminals of the rectifying stage and blocking the current flow into the opposite direction and a single controllable switching device connected across the output terminals; and
   an inductively coupled forward stage for connecting to a load; and
   an inductive-capacitive stage connected between said boost stage and said forward stage providing an inductive energy storing circuit when said switching device is closed and a capacitive charging circuit when said switching device is open, whereby a conversion efficiency of over approximately 80% AC to DC is achieved.

2. The power supply of claim 1 whereby said inductive-capacitive stage includes:
   a parallel circuit with a first branch having a first leakage inductance series connected to first primary input winding and then to a first storage capacitor, and a second branch having a second storage capacitor series connected to second primary input winding and a second leakage inductance with a second unidirectional conducting means having input terminal connected between the second storage capacitor and the second primary winding and an output terminal connected between the first primary winding and the leakage inductances when the switching device is closed.

3. The power supply of claim 1 wherein the controllable conducting means operates with a switching frequency that is greater than approximately 10 times higher than the frequency of the said AC source.

4. The power supply of claim 3 wherein a ratio between on and off time of said controllable means is controlled by:
   means for sensing at least one of voltage and current of the power supply.

5. The power supply of claim 4 wherein the ratio between on and off time of said controllable conducting means is further controlled by:
   a sensed overload of the power supply.

6. The power supply of claim 4 wherein the ratio between on and off time of said controllable conducting means is further controlled by:
   an external source chosen from one of: a voltage and current.

7. The power supply of claim 1 wherein the second controllable conducting means includes a device chosen from one of:
   a power MOSFET, an IGBT, and a BJT.

8. The power supply of claim 1 wherein the second unidirectional conducting means includes:
   semiconductor diodes.

9. The power supply of claim 1 wherein the second unidirectional conducting means includes:
   a zener diode.

* * * * *