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**Active Transient Voltage Compensator for Fast Transient Response Improvement**

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A direct current to direct current (DC-to-DC) converter having an active transient voltage compensator (ATVC) coupled with the DC-to-DC converter output terminal to improve a fast transient response of the DC-to-DC converter. The active transient voltage compensator compensates the DC output only during transient operation. The ATVC includes a transformer for reducing the ATVC current stresses to improve the compensator efficiency and injecting, absorbing high slew rate current, and a controller circuit for controlling ATVC operation in steady state and normal operation in transients. During step-up load the ATVC operates as a buck converter and during step-down load, the ATVC operates as a boost converter while the main converter operates at low switching frequency for good efficiency.
FIG. 1 PRIOR ART

FIG. 2 PRIOR ART
FIG. 4B
FIG. 5
FIG. 6A

FIG. 6B
FIG. 14

Main Isolated DC-to-DC Converter

FIG. 15

Main Isolated DC-to-DC Converter

FIG. 16
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ACTIVE TRANSIENT VOLTAGE COMPENSATOR FOR IMPROVING CONVERTER FAST TRANSIENT RESPONSE

FIELD OF THE INVENTION

This invention relates to voltage converters and, in particular, to methods, systems, apparatus and devices for increasing the fast transient response, power density and efficiency of a DC-to-DC converter.

BACKGROUND AND PRIOR ART

Widely applied to various electronic products, a DC-to-DC converter provides the functions of regulating the voltage level from a DC input voltage, such as boost or buck voltage conversion, and of maintaining the regulated voltage at the desired level. Under the transient high slew rate load, the unbalanced current between the DC-to-DC converter and output load current is provided by filter capacitors. There are two voltage spikes under the transient load. The first output voltage spike relates to equivalent series resistance (ESR), equivalent series inductance (ESL) of filter capacitors and slew rate of the load; the second output voltage spike is determined by to the energy stored in filter inductance and filter capacitance. Commonly, a large number of bulk and ceramic capacitor mounted close to load is used to reduce the output impedance for voltage spikes suppression. But it is not a suitable solution for higher slew rate load; low output voltage high output current applications because of the cost and size limitation. Output voltage spikes are the products of the output impedance, or called load line, and the output current. High bandwidth of a converter and small output impedance helps to reduce its voltage spikes under high slew rate load and high bandwidth also helps to reduce its output impedance.

The bandwidth of a converter is mainly limited by three delay times: the filter inductor capacitance (LC) delay time, controller delay time, and propagation delay time. Examples of propagation delays in DC-to-DC converters include signal sensing delay, driver delay, control IC delay, and extra optocoupler delay in isolated DC-to-DC converter. The key limitation of the current slew rate of the converter is the equivalent filter inductance. A known solution for improving the output slew rate involves increasing the switching frequency to reduce the equivalent inductance. However, the increase in switching frequency results in deterioration of converter efficiency. An attractive solution is extra dynamic channel with high switching frequency operation because it only operates during transient periods.

Current injection topology, such as linear mode current injection topology and switching mode current injection topology, handles the transient current and the main converter handles the static current. It is an attractive extra dynamic channel for transient response improvement technique because this technique allows high slew rate current injection in step-up load and energy absorption in step-down load while the main converter maintaining an optimal converter design for improved efficiency.

FIG. 1 is a schematic diagram of a DC-to-DC converter including a main converter 12 and incorporating a linear mode current injection topology 14 according to the prior art. The linear mode current injection topology 14 solution injects high slew rate current I_{slew} to the DC-to-DC converter 10 during step-up operation and clamps the output voltage V_{o} using resistive dissipation. However, the efficiency of the DC-to-DC converter 10 is reduced due to the large conduct-
BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a schematic diagram of a prior art DC-to-DC linear mode current injection topology.

FIG. 2 is a schematic diagram of a prior art DC-to-DC switching mode current injection topology.

FIG. 3 is a schematic diagram of a DC-to-DC converter using the active transient voltage compensator of the present invention.

FIG. 4A is a schematic diagram of a DC-to-DC converter of FIG. 3 including the magnetizing inductance, the resistance of magnetizing inductance and leakage inductance L_{L,R} of the active transient voltage compensator transformer.

FIG. 4B is a schematic diagram of a DC-to-DC converter of FIG. 3 including the controller block diagram of the main converter and the controller block diagram of the active transient voltage compensator.

FIG. 5 is a graph illustrating graphical representations of the operational voltage and current waveforms of the DC-to-DC converter of FIG. 4A with respect to time during step-up load mode, steady-state and step-down load mode operations.

FIG. 6A is a schematic of the step-up load mode operation of the active transient voltage compensator corresponding to time t1 to t1' as shown on the graph of FIG. 5.

FIG. 6B is a schematic of the step-up load mode operation of the active transient voltage compensator corresponding to time t1' to t2 as shown on the graph of FIG. 5.

FIG. 6C is a schematic of the steady state operation of the active transient voltage compensator corresponding to time t3 to t4 as shown on the graph of FIG. 5.

FIG. 6D is a schematic of the step-down load mode operation of the active transient voltage compensator corresponding to time t4 to t4' as shown on the graph of FIG. 5.

FIG. 6E is a schematic of the step-down load mode operation of the active transient voltage compensator corresponding to time t4' to t5 as shown on the graph of FIG. 5.

FIG. 7 is a schematic diagram of an experimental DC-to-DC converter using the active transient voltage comparator according to the present invention.

FIG. 8 shows the operational currents of the ATVC circuit in the experimental DC-to-DC converter of FIG. 7 during step-up load mode.

FIG. 9 shows the operational currents of the ATVC circuit in the experimental DC-to-DC converter of FIG. 7 during step-down load mode.

FIG. 10 show a comparison between the ATVC operational current I_{ATVC} the main converter output current I_1 and the DC-to-DC converter output current I_O during step-up load mode.

FIG. 11 show a comparison between the ATVC operational current I_{ATVC}, the main converter output current I_1 and the DC-to-DC converter output current I_O during step-up load mode.

FIGS. 12A and 12B are graphs of the DC-to-DC converter output voltage V_O during step-up load mode with ATVC and without ATVC, respectively.

FIGS. 13A and 13B are graphs of the DC-to-DC converter output voltage V_O during step-down load mode with ATVC and without ATVC, respectively.

FIGS. 14, 15 and 16 are schematic diagrams of alternative DC-to-DC circuits utilizing the ATVC of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before explaining the disclosed embodiments of the present invention in detail it is to be understood that the invention is not limited in its application to the details of the particular arrangements shown since the invention is capable of other embodiments. Also, the terminology used herein is for the purpose of description and not of limitation.

The following is a list of the reference numbers used in the drawings and the detailed specification to identify components:

Reference No. Component
10 Prior art DC-to-DC converter
12 Main converter
14 Linear mode current injection topology
16 Switching mode current injection topology
100 DC-to-DC converter
110 Main converter
120 DC-to-DC converter with controller block diagram
150 Active transient voltage compensator (ATVC)
160 Main converter controller
161 Step up controller for ATVC
162 Step down controller for ATVC
163 Logic block for ATVC
164 ATVC controller
210 Operational current waveform
212 Minimum current I_{min}
213 Output current I_O ramp up
214 Main converter output current I_1 increase
215 Maximum output current I_{max}
217 Output current I_O decrease
218 Main converter output current I_1 ramp down
220 Reference voltage waveform
221 Reference voltage Vref1
222 Reference voltage Vref2
223 Reference voltage Vref2
230 ATVC current waveform I_{ATVC}
240 Transformer primary current I_{L1} waveform
250 Transformer magnetizing inductance current I_{LM} waveform
260 Q_{at} driver signal voltage waveform
270 Q_{at} driver signal voltage waveform

The method, system, apparatus and device of the present invention reduce output voltage spikes in transients and improve the transient response by providing an active transient voltage compensator (ATVC) for use with isolated or non-isolated DC/DC converters. FIG. 3 is a schematic diagram of a conventional DC-to-DC converter incorporating the active transient voltage compensator 150 of the present invention. The components of the ATVC differ from the prior art linear and switching mode current injection topologies by the inclusion of the transformer T_r in addition to the synchronous rectifiers Q_{at} and Q_{at}. FIG. 4A is a schematic according to FIG. 3 including the magnetizing inductance I_{LM}, resistance R_{LM} of magnetizing inductance, and leakage inductance I_{L,K} of the ATVC transformer T_r.

FIG. 4B is a schematic diagram of a DC-to-DC converter of FIG. 3 including the controller block diagram 160 of the main converter 110 and the controller block diagram 164 of the active transient voltage compensator 150. The main converter 110 regulates the output voltage level by the close loop controller 160 with reference voltage Vref2 222, which feedbacks output voltage V_0 and output current I_1 with the gain G_{m}. ATVC controller 164 has two controllers: step-up controller 161 with reference voltage Vref1 221 and step-
down controller 162 with reference voltage Vref2 223. The step-up controller generates the driver signal of Qa1 only in the step-up load mode and the step-down controller generates the driver signal of Qa2 only in the step-down load mode. The logic block 163 in ATVC controller 164 is used to keep no ATVC operation in steady state and generate complimentary driver signal for Qa2 in step-up load mode and complimentary driver signal for Qa1 in step-down load mode in transient periods.

As identified in FIGS. 3 and 4A, Vop is the input voltage applied to the main converter 110. The main converter 110 has an output voltage Vout1 and a corresponding output current I1. The main converter 110 includes a filter capacitor C1 connected across the output. The filter capacitor C1 and the equivalent series inductance L1 and equivalent series resistance R1 are connected in parallel across the output of the main converter 110. The parasitic parameters of trace, socket are illustrated as resister Rp and inductor Lp parallel connected with the active transient voltage compensator 150 of the present invention. A second filter capacitor C2 is connected across the DC-to-DC converter output as decoupling capacitors. The capacitor C1 and the equivalent series inductance L1 and equivalent series resistance R1 are illustrated as serially connected across the output. The output of the DC-to-DC converter 100 incorporating the transient voltage compensator 150 according to the present invention are identified as output voltage Vop and output current Io. Alternative configuration for coupling the ATVC of the present invention with a DC-to-DC converter will be obvious to those skilled in the art.

During transient periods, the equivalent inductance of the ATVC is approximately equal to the leakage inductance of the transformer, while maintaining normal inductance of winding N2 that is paralleled with the parasitic Rp and Lp during steady state operation. The same time the ATVC transformer Tr injects a serial positive voltage source to provide a high slew rate current with the input voltage. Conversely, in step-down load, the active transient voltage compensator transformer provides a serial negative voltage to absorb high slew rate current with the output voltage. Using the transformer Tr, current handled by the ATVC is reduced, which contributes to a reduced conduction loss and switching loss in the ATVC.

There are three main modes for operation of the ATVC, step-up load mode, steady-state mode, and step-down load mode. In step-up load mode, the imbalance between the main converter 110 output current I1 and the DC-to-DC converter output current Iout results in a drop in the output voltage Vop. The decrease in the output voltage may even fall out of the DC-to-DC converter specification output voltage requirement.

To overcome the problem, the ATVC 150 kicks in as a buck converter by controlling Qa1 with the driver signal 260 to compensate the output voltage Vop when the output voltage Vop falls below the ATVC voltage Vref 221. The driver signal of Qa2 270 is complimentary with the driver signal of Qa1 260 in step-up load mode.

The ATVC 150 of the present invention injects a high slew rate current, which is based on the transformer leakage inductance LLL and the difference between the ATVC 150 supply voltage V1 and the DC-to-DC converter output voltage Vop as shown in FIG. 6A. The primary current I1p of the ATVC 150 transformer Tr; freewheels through Qa1 when Qa1 is off as shown in FIG. 6B. The primary current I1p and secondary current I2p of transformer Tr, together quickly catch up with the DC-to-DC converter output current Iop because of the small value of the leakage inductance LLL of the transformer Tr. Stepped-up load mode ends with the transformer Tr, magnetizing current I1p, increasing to the maximum output current K*Imax, K is the current divider between Rp and RL in steady state mode.

FIG. 5 is a graphical representation of operational current and voltage waveforms of the DC-to-DC converter corresponding to the operational schematics of FIGS. 6A through 6D. The first waveform 210 in FIG. 5 is a graphical representation of the main converter 110 and DC-to-DC converter 100 output currents, I1 and Iop. Referring to waveform 210, during step-up load mode the output current (Iop) 213 of the DC-to-DC converter 100 increases from minimum current (Imin) 212 to the maximum current (Imax) 216 during the time period t1 to t3. Operation of the ATVC 150 corresponding to time period from t1 to t3 in step up mode is detailed only in one switching cycle operation, Qa1 is on and Qa2 is off from t1 to t3, Qa1 is off and Qa2 is on from t3 to t2, shown in the schematic of FIG. 6A and FIG. 6B.

The ATVC 150 functions to sharply increase the ATVC current (IATVC) 230 from minimum current (K*Imin) to the maximum current (K*Imax) during the time period t1 to t3 with the slowly increasing main converter output current (I1) 214. This is accomplished by biasing Qa1 “OFF” and Qa2 “ON” by the driver signal 260 and 270, providing an essentially low impedance path to allow current to flow from voltage source V1 through transformer Tr, primary N1. The transformer primary current I1p and secondary current I2p with magnetizing current I1M increase the ATVC output current IATVC to catch up with the output current Iop as shown on waveforms 230, 240 and 250, respectively.

The ATVC continues to supply the current IATVC as shown in waveform 230 to maintain an output current Iop at Imax 216 from time t2 to t3 as the main converters current I1 is identified on the graph of FIG. 5 by the ramped up dashed line 214. Stepped-up load mode ends with the transformer Tr, magnetizing current I1M increasing to the peak current K*Imax.

With the introduction of the transformer Tr, to the conventional DC-to-DC converter of the prior art shown in FIGS. 1 and 2, the active transient voltage compensator 150 of the present invention only handles a small current, resulting in a reduced conduction loss and switching loss in the active transient voltage compensation topology than that of the prior art current injection topology. The current handled by the active transient voltage compensator 150 is calculated according to (K*Imax/(1+N)) where N is the turn-ratio of the transformer (N=N1/N2). In step-up load mode, the active transient voltage compensator also provides a high slew rate current, (1+N)*|(V1-V0)|/LLL approximately (1+N) times higher than that of switching current injection topology if the equivalent filter inductance is same.

In a steady-state mode, the time period on the graph of FIG. 5 between t3 and t4 is schematically illustrated in FIG. 6C. As shown, during steady-state Qa1 and Qa2 are biased off by the logic block 163 in the ATVC controller 164. The current of I1p and I2p equals to zero and the current I1M equals to K*Imax, K is the current divider ratio between Rp and RL. Design of the circuit to satisfy the following equation ensures that the active transient voltage compensator does not operate during the steady-state mode N*V1-V0-YD

where V1 is the transformer secondary voltage and V0 is the on-state voltage drop of body diode of synchronous rectifier Qa2.
During the step-down load mode, the ATVC operates as a boost converter by controlling the operation of Qa1 from the step-down controller 162 in the ATVC controller 164 when the output voltage V0 is higher than the ATVC reference voltage VREF of FIG. 5. The ATVC 150 recycles energy to the ATVC input voltage V1 during time t4 to t6, one switching cycle operation from t4 to t5 is detailed as shown in the schematic diagrams of FIGS. 6E and 6F. Referring to FIG. 6D, during step-down load Qa2 is biased to draw current IN1 from transformer primary N1 shown as a negative current in waveform 240, to suppress the output voltage spikes and recycle energy to ATVC input voltage V1. As shown by the decreasing dashed line 218, the main converter output current I1 decreases at a slower rate from time t4 to t6.

The driver signal of Qa1 as shown in 260 is complimentary with the driver signal of Qa2 as shown in 270 in step-down load mode. Referring to the operational schematic of FIG. 6E in conjunction with the graph of FIG. 5, from time t4 to time t5, the operation of the active transient voltage compensator switches Qa1 “ON” and Qa2 “OFF”, proving a path for transformer primary current IN1 to recycle energy to ATVC input voltage V1 to maintain the DC-to-DC converter output current I1 at Imin until the main converter current I1 ramps down to Ioff at time t6, as shown by the dashed line 218 of waveform 210. Step down load mode terminates when with the transformer Tr magnetizing inductance current ILM shown in waveform 250 decreasing to zero. As shown in FIG. 5, the ATVC draws the excess current to maintain the DC-to-DC converter output current I1 approximately at Imin.

In step-down load mode, ATVC absorbs high slew rate current, 

\[ (1+N)I_{V2}/L_{K2} \]

approximately (1+N) times higher than that of switching mode current injection topology if the equivalent filter inductance is same. The handled current by ATVC is as \( I/(1+N) \) times as much as the current of prior arts 14 and 16.

As described in the previous paragraphs corresponding to FIGS. 5 and 6A-E, the active transient voltage compensator 150 operates in high frequency for small equivalent filter inductance, so it injecting higher slew rate current in step-up load mode and recovers energy to the ATVC input voltage V1, in the step-down load mode. The active transient voltage compensator only operates in transient. The conduction loss of the transformer secondary winding N2 can be minimized by reducing the resistance of the transformer design. The inclusion of the active transient voltage compensator transformer T reduces the conduction losses and switching losses of Qa1 and Qa2 during the transient periods compared with the higher power losses resulting from use of the prior art current injection methods. Moreover, the optimal design for improved efficiency is carried out in the main converter with improved transient response at lower high frequency operation.

In summary, the present invention provides a method, system apparatus and device for improving the fast transient response of a DC-to-DC converter using the active transient voltage compensator (ATVC) topology of the present invention. The ATVC injects high slew rate current in step-up load and recovers energy during step-down load. The introduction of a transformer in the ATVC circuit reduces the compensator channel’s conduction loss and switching loss. The ATVC operates during transient periods to eliminate the effects of parasitic inductance that is series with ATVC resulting from voltage injection. The ATVC also achieves a wide bandwidth instead of pushing the main converter into high frequency operation to improve the main converters efficiency and maintains the converters output impedance while reducing the bulk capacitors.

**EXPERIMENT**

An experiment according to the DC-to-DC converter shown in the schematic diagram of FIG. 7 was carried out in the laboratory with a power distribution model for the processor with voltage regulator (VR), which was provided in VR10.0 by Intel. The DC-to-DC converter includes a main converter, filter circuit and incorporates the ATVC of the present invention between the main converter and the load. A three-phase VR and active transient voltage compensator are provided in parallel between inductor L1 and inductor L2 in the power distribution model. VR operates at 250 kHz and the ATVC is operated at 2.5 MHz. The experimental circuit is provided with a supply voltage Vp=12VDC, an output voltage V0=1.1VDC, an output current I0 between Ioff=100 amps and Imin=10 amps which is supplied to the load.

VRM10.0 defines dc-dc converters to meet the power supply requirements of desktop computer systems, which output voltage is 0.8375V-1.6000V with VID control code, and its current is up to 120 A; the output current slew rate for CPU is up to 1-2 A/ns. The socket load lines contain dc load line and transient load line as well as minimum voltage levels, which are measured at the processor socket dedicated pins between the voltage regulator and processor cavity.

FIG. 8 illustrates the operational currents of the ATVC circuit including the transformer T, primary current IP, secondary current I0, the magnetizing inductance current ILM, and the ATVC output current IARVC during step-up load mode. As shown, the ATVC circuit provides a higher slew rate positive current I0 during step-up load mode. Conversely, the operational currents provided by the ATVC during step-down load mode are shown in FIG. 9. As shown, the ATVC circuit provides a high slew rate negative current to recycle energy into the input voltage V1 during step-down load mode operation.

FIGS. 10 and 11 show a comparison between the ATVC operational current IARVC, the main converter output current I1 and the DC-to-DC converter output load current I0 during step-up load mode and step-down load mode, respectively. As shown in FIG. 10, the ATVC provides a higher slew rate current IARVC than the output current I1 provided by the main converter. According to the graph plotted in FIG. 10, the ATVC current IARVC increases approximately five times faster than the main converter output current to increase the output current I0 from Ioff=10 amps to Imax=100 amps. Likewise, during step-down load mode, the slew rate of the current provided by the ATVC decreases approximately five times faster than the main converter output current I1 as the ATVC recycles energy into the input voltage source for improved efficiency.

FIGS. 12A and 12B are graphs of the DC-to-DC converter output voltage V0 during step-up load mode with ATVC and without ATVC, respectively. As shown in FIG. 12B, during step-up load mode without ATVC the output voltage V0 includes two spikes. The first spike is the result of performance of capacitors and layout, ESR and ESL while the second spike is mainly determined by the closed loop design of the circuit. When the DC-to-DC converter incorporates the ATVC of the present invention, an improvement in the second voltage spike is shown in FIG. 12A. Similarly, an
improvement in the second spike is observed when the graph of the output voltage $V_o$ during step-down load mode without ATVC (FIG. 13B) is compared to the output voltage $V_o$ with ATVC as shown in FIG. 13A.

While the method, system, apparatus and device of the present invention has been illustrated and discussed when utilized the DC-to-DC converter as shown in FIG. 4, the ATVC may be utilized in other DC-to-DC converters, including but not limited to, the DC-to-DC converters circuits shown in FIGS. 14, 15 and 16. FIGS. 15 and 16 are schematic diagram of an isolated DC-to-DC converter using the ATVC of the present invention to improve transient response without pushing high frequency operation for the main isolated converter where $R_p$ and $L_p$ represent the parasitic parameters.

While the invention has been described, disclosed, illustrated and shown in various terms of certain embodiments or modifications which it has presumed in practice, the scope of the invention is not intended to be, nor should it be deemed to be, limited thereby and such other modifications or embodiments as may be suggested by the teachings herein are particularly reserved especially as they fall within the breadth and scope of the claims here appended.

We claim:

1. A direct current to direct current (DC-to-DC) converter having an improved fast transient response, the converter comprising:
a DC-to-DC main converter having an input terminal and a DC output terminal with a first and second capacitor connected across the output terminal; and
an active transient voltage compensator (ATVC) connected in parallel with the output terminal between the first and second capacitor, the active transient voltage compensator comprising:
a transformer having a primary winding and a secondary winding, one end of the secondary winding connected to one end of the first capacitor to provide a stepped inductance during the transient operation to compensate the output voltage while maintaining normal inductance during the steady state operation;
a switching circuit having a step-up synchronous rectifier and a step-down synchronous rectifier connected with one end of the transformer primary for controlling a transformer current, the other end of the primary and secondary connected to one end of the second capacitor; and
an ATVC controller connected to the ATVC for monitoring the output voltage and producing a driver signal for activating one of the step-up and step-down synchronous rectifiers to inject a voltage source to compensate the output voltage when the output voltage falls below an ATVC reference voltage and increases above the reference voltage, respectively, to compensate the DC output terminal voltage during a transient operation without switching loss during a steady-state operation.

2. The converter of claim 1, wherein the ATVC controller comprises:
a step-up control with the reference voltage for step-up mode, and
a step-down control with the reference voltage for step-down mode, and
a logic block to control no ATVC operation in steady state and normal operation in transient, wherein the ATVC injects the voltage source to improve transient response of the DC-to-DC converter.

3. The converter of claim 1, wherein the ATVC operates as a buck converter to compensate the output voltage when the output voltage falls below an ATVC reference voltage.

4. The converter of claim 1, wherein the ATVC operates as a boost converter to recycle a DC output terminal energy when the output voltage exceeds and ATVC reference voltage.

5. The converter of claim 1, wherein the DC-to-DC converter is an isolated DC-to-DC converter, wherein the ATVC improves transient response without pushing high frequency operation for the main converter.

6. The improved converter of claim 1, wherein the DC-to-DC converter is a non-isolated DC-to-DC converter.

7. A method for improving transient response for direct current to direct current (DC-to-DC) converter, the method comprising the steps of:

- connecting a first and second capacitor and an active transient voltage compensator (ATVC) in parallel with the main converter, the ATVC connected between the first and second capacitor; and
- injecting a voltage source during step-up load mode and step-down load mode to improve transient response during transient operation to compensate an output voltage to maintain output voltage requirements, wherein the ATVC handles a small current in transient loads that results in a reduction of conduction and switching losses and improves the injected current slew rate.

8. The method of claim 7, wherein the voltage injection step comprises the steps of:

- comparing a DC converter output voltage to an ATVC reference voltage;
- when the DC converter output voltage is less than the ATVC reference voltage, operating the ATVC as the buck converter to increase the first converter output current to achieve the maximum current; and
- when the DC converter output voltage is greater than the ATVC reference voltage, operating the ATVC as the boost converter to decrease the first converter output current to achieve the minimum current, wherein the ATVC compensates the output voltage to maintain output voltage specification requirements.

9. The method of claim 8, wherein the buck converter operation step comprises the steps of:

- providing a current path for conducting a forward ATVC current through the ATVC; and
- providing a coupler with the ATVC for coupling the forward ATVC current with the first converter output current to achieve the maximum output current.

10. The method of claim 8, wherein the buck converter operation step comprises the steps of:

- providing a first path for routing a first ATVC current through the ATVC;
- coupling the first ATVC current with the first converter output current to produce a second converter output current;terminating the first path when the second converter output current reaches a maximum output current;
- providing a second path for routing a second ATVC current through the ATVC;
- coupling the second ATVC current with the converter output current to maintain the an output voltage within converter specifications; and
terminating the second path when the first converter output current is substantially equal to the maximum output current.

11. The method of claim 7, wherein the boost converter operation step comprises the steps of:

providing a first path for routing a first reverse current through the ATVC;

terminating the first path when the second converter output current reaches the minimum output current;

providing a second path for routing a second reverse current through the ATVC; and

terminating the second path when the first converter output current is substantially equal to the minimum output current.

* * * * *