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PREDICTIVE MODELING FOR ASSESSING THE RELIABILITY OF BYPASS DIODES IN PHOTOVOLTAIC MODULES

by

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ABSTRACT

Solar Photovoltaics (PV) is one of the most promising renewable energy technologies for mitigating the effect of climate change. Reliability of PV modules directly impacts the Levelized Cost of Energy (LCOE), which is a metric for cost competitiveness of any energy technology. Further reduction in LCOE of PV through assured long term reliability is necessary in order to facilitate widespread use of solar energy without the need for subsidies. This dissertation is focused on frameworks for assessing reliability of bypass diodes in PV modules. Bypass diodes are critical components in PV modules that provide protection against shading. Failure of bypass diode in short circuit results in reducing the PV module power by one third, while diode failure in open circuit leaves the module susceptible for extreme hotspot heating and potentially fire hazard. PV modules, along with the bypass diodes are expected to last at least 25 years in field. The various failure mechanisms in bypass diodes such as thermal runaway, high temperature forward bias operation and thermal cycling are discussed. Operation of bypass diode under shading is modeled and method for calculating the module I-V curve under any shading scenario is presented. Frameworks for estimating the diode temperature in field deployed modules based on Typical Meteorological Year (TMY) data are developed. Model for predicting the susceptibility of bypass diodes for thermal runaway is presented. Diode wear out due to High Temperature Forward Bias (HTFB) operation and Thermal Cycling (TC) is studied under custom designed accelerated tests. Overall, this dissertation is an effort towards estimating the lifetime of bypass diodes in field deployed modules, and therefore, reducing the uncertainty in long term reliability of PV modules.
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LIST OF ABBREVIATIONS

DHI: Diffuse Horizontal Irradiance
DNI: Direct Normal Irradiance
FF: Fill Factor of current-voltage curve of a photovoltaic module
HTFB: High Temperature Forward Bias
HTRB: High Temperature Reverse Bias
I-V: Current-voltage curve of photovoltaic module
IEC: International Electro-technical Commission
Iᵢ: Forward current through a diode
Iᵢₘₚ: Current at maximum power point of a photovoltaic module
Iᵢᵣ: Reverse current through a diode
Isc: Short circuit current of a photovoltaic module
JEDEC: Joint Electron Device Engineering Council
LCOE: Levelized Cost of Energy
Pᵢ: Power dissipation in forward bias in a diode
Pₘₚ: Maximum power of a photovoltaic module
PV: Photovoltaic
PVQAT: Photovoltaic Quality Assurance Task Force
STC: Standard Test Conditions (25 °C ambient temperature and 1000 W/m² irradiance)
TC: Thermal Cycling
Tᵣ: Thermal Runaway Critical Temperature
Tᵣₓₙ: Temperature at which forward power dissipation equals reverse power dissipation. Crossover point between forward power vs Tₜ and reverse power vs Tₜ curves.
Tᵣₓₙₑₜ: Estimated crossover temperature
TG4: Task Group 4 on diodes of PVQAT
ΔTₜ: Difference between maximum and minimum diode junction temperatures for certain duration
Tₜ: Diode junction temperature
TMY: Typical Meteorological Year
Tₒᵖ: Operating temperature of diode (usually at thermal equilibrium)
Tₒᵖₑₜ: Estimated Operating temperature of diode (usually at thermal equilibrium)
Vᵢ: Forward voltage of a diode
Vᵢ⁻Tₜ: Linear relation between forward voltage of diode and junction temperature
Vₘ: Voltage at maximum power point of a photovoltaic module
Vₒ𝑐: Open circuit voltage of a photovoltaic module
CHAPTER 1 INTRODUCTION

1.1 Background

The first chapter of this dissertation provides an introduction to the rest of the chapters and summarizes the key aspects addressed in each of the chapters.

1.2 Literature review and gap identification

Chapter 2 begins with an overview of the problem of climate change and the role renewable energy sector can play in mitigating the climate change. The concept of Levelized Cost of Energy (LCOE) is illustrated along with the impact of PV reliability on LCOE. Key failure modes in PV modules are described along with the contribution of the author in relation to the failure mode. Failure modes and mechanisms in bypass diodes are described and the gaps in the current understanding regarding them are identified.

Chapter 3 has detailed discussion on the types of accelerated tests used for assessing PV module reliability. The brief history and the role of PV module qualification tests (IEC 61215) in mitigating the infant mortality of PV modules is discussed. Bypass diode test is procedure is described. Several limitations of the qualification tests in order to predict the PV lifetime and wear out are discussed. Gaps in the current accelerated testing methodology as it regards to bypass diodes are discussed in detail. Motivation for the dissertation based on the identified gaps in the current understanding of reliability of bypass diodes is described.
1.3 **Operation of bypass diodes under shading**

Chapter 4 begins with the description of the structure and physics of Schottky bypass diodes. Electrical properties and characterization methods for the various types of commercially available bypass diodes are discussed. Methodology for extracting diode electrical properties from datasheets along with the associated errors is described in detail. Various types of shading experienced by the module are described along with a generalized framework for quantifying the impact of any random shading scenario on the I-V curve of the shaded PV module.

1.4 **Modeling operating temperature of bypass diodes**

Chapter 5 begins with a discussion on various types of junction boxes and their thermal properties. Methods for measuring diode junction temperature are outlined. Methods for measuring thermal resistance of various junction boxes are described in light of the one dimensional thermal model. Outdoor measurements of diode junction temperature and shaded cell temperature are discussed. A framework for estimating the diode operating temperature from the information about module mounting, location, and module properties is described.

1.5 **Thermal runaway in bypass diodes**

Chapter 6 discusses the dynamics of thermal runaway in bypass diodes and a model for predicting the vulnerability of diodes for thermal runaway. Suggestions for developing a new thermal runaway test are also provided.
1.6 Wear out in bypass diodes

Chapter 7 has a discussion of wear out mechanisms in bypass diodes namely High Temperature Forward Bias (HTFB) Operation and Thermal Cycling (TC). Suggestions for developing accelerated tests to simulate wear out in diodes are provided.

1.7 Conclusions

Chapter 8 concludes with the discussion on important contributions from this dissertation. The significance of frameworks for predicting diode field temperature, assessing susceptibility for thermal runaway and wear out is discussed. Outlook for future work in this area is also provided.
CHAPTER 2 PHOTOVOLTAIC RELIABILITY

2.1 Climate Change and PV

2.1.1 Climate Change
Climate change is defined as change in the state of climate that can be measured by changes in the mean or variability of physical parameters and lasts for longer duration of time which could be of the order of several decades. The causes for climate change could be natural processes (e.g. volcanic eruptions, changes in solar cycle) or human activities (e.g. greenhouse gas emissions). There is increasing evidence that anthropogenic activities such as greenhouse gas emissions are resulting in climate change at an accelerating pace.

2.1.2 Role of energy sector in climate change
The data presented in this subsection is adopted from the 2014 report published by the Intergovernmental Panel on Climate Change (IPCC) (Bruckner T. & E. Hertwich, 2014). The contribution of greenhouse gas emissions from energy production and supply sector is known to be highest. In 2010, this sector contributed 35% of the total greenhouse gas emissions. United Nations Framework Convention for Climate Change (UNFCCC) and Kyoto Protocol were created in order to limit the worldwide greenhouse gas emissions going into the future. However, worldwide increased energy demand and increased use of coal in energy mix to meet that demand resulted in escalating the annual greenhouse gas emission growth rate due to energy sector from 1.7% in 1990-2000 to 3.4% in 2000-2010. Despite of ever increasing use of fossil fuels and depletion of these non-renewable resources, limited availability of fossil fuels is deemed insufficient to limit the CO2 equivalent concentration to 450 ppm, 550 ppm or even 650 ppm. Various options exist to reduce the greenhouse gas emissions from energy sector such as:
improving the efficiency during production, transmission, distribution of energy, use of renewable technologies with very low or zero greenhouse gas emissions, carbon sequestration and storage etc. However, stabilization of the greenhouse gas concentrations at low levels would require a complete transformation of energy system to close to zero greenhouse gas emission system and mere energy efficiency improvements will not be sufficient in the long term. The share of renewable energy technologies and nuclear energy needs to increase to close to 80% by 2050 in order to mitigate the climate change.

2.1.3 Options for mitigating climate change: nuclear vs renewables
Even though nuclear energy has a potential to generate large amount of electricity with low-greenhouse gas emissions, large scale penetration of nuclear energy has been facing inhibitions due to public concerns about the safety of nuclear power plants and the issues regarding safe disposal of nuclear waste. An earthquake followed by Tsunami on March 11, 2011 caused the meltdown of the Fukushima nuclear reactor in Japan which had worldwide, long-lasting repercussions for the role of nuclear energy for mitigating the climate change (Batty, 2012). In light of the Fukushima incident, all 50 nuclear power plants within Japan were shut down for inspection and maintenance by May 5, 2012 (Gerhardt, 2012). Significant rise in the public opinion against nuclear energy is expected to shape the country’s nuclear policy in the decades to come. Similar reaction was observed in several other parts of the world. For example, within a couple of months of the disaster, Germany announced that it will phase out all of its nuclear reactors by 2022, which were contributing about 27% of the country’s energy production at that time (Jorant, 2011). It is therefore, expected that renewable energy technologies will play dominant and crucial role in the 21st century in the efforts to mitigate the climate change.
2.1.4 Potential of solar photovoltaics

Serious consideration to renewable energy technologies for terrestrial use was given only after the energy crisis of 1973. Since then, government policies in incentives have shaped the growth of several renewable energy technologies such as solar photovoltaics (PV), solar thermal, wind, biomass, hydro and geothermal energy. It has been shown that the technical potential for solar energy is greater than any other form of renewable energy (Moomaw W., 2011). Levelized Cost of Energy (LCOE) of crystalline Silicon (c-Si) solar PV has reduced by 57% since 2009, which is highest reduction among all renewable energy technologies (Angus McCrone, 2013).

2.2 Levelized cost of energy for photovoltaics

LCOE is often used as a metric for determining cost-competitiveness of energy generation projects for any energy technology. LCOE can be defined by Equation 1

\[
LCOE = \frac{\text{Lifecycle Cost of Project}}{\text{Lifetime Energy Production}}
\]

(1)

Therefore, LCOE can also be considered as the cost at which the energy should be sold in order to break even during the lifetime of the project. Usually, LCOE is expressed in units of cents per Kilo-Watt Hours (c/KWh). LCOE can act as a guideline for project developers to determine the most competitive energy generation technology, it can help investors determine return on investment, trends in LCOE can help the policymakers decide the important energy sources in future and technology developers can compare new technologies with the existing ones by using
LCOE (Tarn Yates, 2012). Sunpower Corporation has published a simplified Equation to calculate the LCOE from financial perspective (Cambell, 2008).

\[
LCOE = \frac{\text{Project Cost} + \sum_{n=1}^{N} \left\{ \frac{AO}{(1 + DR)^n} - \frac{RV}{(1 + DR)^n} \right\}}{\sum_{n=1}^{N} \left\{ \frac{\text{Initial KWh} \times (1 + SDR)^n}{(1 + DR)^n} \right\}}
\]  

(2)

Where AO is annual operations cost, RV is residual value of the project after end of life, DR is the discount rate, SDR is the system degradation rate, Initial KWh is the energy generated by the project in the beginning and N is the lifetime of the project or operational timespan in years. It is clear from Equation 2 that reduction in the discount rate, project cost, operations cost and system degradation rate reduce the LCOE, while increase in the residual value, project lifetime and initial KWh reduce the LCOE.

2.3 Role of PV reliability in LCOE

The cost, efficiency and reliability are considered as three pillars of any PV technology. Cost influences the parameter ‘project cost’ while the efficiency affects the parameter ‘Initial KWh’ in the Equation 2. Reliability determines the lifetime of the project ‘N’, system degradation rate ‘SDR’ and most importantly, it can greatly influence the discount rate ‘DR’ used in the LCOE calculation in Equation 2. Manufacturers often provide warranties of the order of 25-30 years for silicon wafer based PV modules. Therefore, 25-30 years can be considered as the useful life of a PV module. However, it should be noted that these warranties have been traditionally determined by the competition and market requirements and are generally not based on physics based
predictive lifetime models. Improvements in the PV module design over the years have resulted in robust products and the module degradation rate can be assumed to be order of 0.5% per year for most recent silicon based PV modules (D. C. Jordan, 2013). However, the degradation rates for specific failure modes are known to vary significantly according to the specific module technology, materials and climate experienced by the PV modules during lifetime. Therefore, using a constant number for SDR in the LCOE Equation could result in over-simplification or overly optimistic calculation. For example, in year 2008 in Spain, LCOE calculation considering best case scenarios resulted in several PV project failures (Seth B. Darling, 2011). Discount rate is determined by the financers in order to take into consideration the uncertainty associated with the project. Uncertainty in the energy output could come from various sources such as variation in solar irradiance at a particular location, unpredictable degradation of PV technologies and from the variations in the rates of borrowing money for building new PV projects. New and unproven technologies usually have high discount rate in order to protect the investors (K. Brankera, 2011).

A sensitivity analysis of LCOE using Monte Carlo simulations has revealed that financial uncertainty described by discount rate has highest correlation with the LCOE (Seth B. Darling, 2011). In other words, increase in the discount rate due to increase in uncertainty is most likely going to result in significant increase in LCOE. Uncertainty in system degradation rate also has considerable correlation with LCOE. The degradation rates specified in the module manufacturer’s datasheets need to be validated from field data in order to increase the confidence in the provided specifications. Therefore, it is imperative that large amount of field performance
data of various PV technologies should be available in public domain. However, currently, issues regarding the confidentiality and liabilities preclude the field data from being easily accessible. Interestingly, uncertainty in the weather did not have significant correlation with the LCOE, demonstrating that it is not as important as uncertainty in discount rate and system degradation rate.

Over past couple of decades, the cost of solar PV has undergone drastic reduction due to improvements in manufacturing materials and processes. The efficiencies of the cells and modules have been steadily increasing due to innovation in cell processing technology and architectures. In early days of PV, the capital requirements for PV projects were very high and investors used high discount rates as there was insufficient field data for substantiating the projected performance of various PV technologies. Therefore, even though the manufactures were giving out warranties for ~ 20 years, from financial perspective, the performance of the PV system in later years and its residual value after operational life were not significant. However, as the capital cost requirements for PV projects have gone down, this scenario has changed. Now the performance of PV systems even after 15+ years can affect the financial calculations (Previtali, 2015). Therefore, developing understanding about the modes and mechanisms for wear out of PV modules has become an urgent necessity. Development of physics based predictive models for specific failure modes and corresponding accelerated tests have the capability to significantly reduce the uncertainty in predicting the PV performance. Therefore, in recent years, government bodies like US Department of Energy have announced several programs to develop such models to better understand the reliability of PV modules during their
service life (Kinsey, 2015). Once lifetime prediction models for PV module and its components are available, it will help to reduce the uncertainty and lower the LCOE for PV so that the technology can flourish without the need for any subsidies. There is an emerging trend among the project developers and financers to favor technologies that are proven to be reliable by either field data, accelerated testing or modeling, instead of solely relying upon the manufacturer’s warranties. This is because it has been observed numerous times that the life of a company could be shorter than the life of the PV project. This also points towards the need to develop frameworks to accurately assess the long term reliability of PV modules.

First step in this process is to perform survey of the various degradation / failure modes and mechanisms in PV modules. Once failure modes and mechanisms are studied, physics based models can be developed to predict the onset of degradation and progression of degradation leading to failure. Enhanced mechanistic understanding about specific failure mechanisms can also be used to develop accelerated tests that accurately simulate the service life exposure. In order to understand various failure modes and mechanisms in PV modules, it is necessary to discuss the typical module design, materials and components involved.

2.4 PV technologies and module construction

2.4.1 PV technologies
Solar cells work on the principle of photovoltaic effect in which potential difference is created across the terminals of a device when light is incident on it. First solar cell was created in 1954 by Bell Labs (D. M. Chapin, 1954). Since then the silicon based solar cell technology has undergone significant improvements in terms of efficiency and cost reductions. Solar cells based
on single crystal silicon (c-Si) are known to be more efficient as well as more expensive. Multicrystalline silicon (mc-Si) technology was developed in order to reduce the cost associated with wafers at the same time maintaining moderate efficiencies. Silicon based PV (c-Si and mc-Si) forms the majority of market share for PV modules. Due to the mature processing technology, the majority of the costs associated with silicon wafer based solar cells are materials costs. Therefore, it was realized that reducing the material consumption drastically could be a promising approach for further cost reduction in PV. As a result, thin film technologies such as amorphous silicon (a-Si:H), copper-indium-galium-selenide (CIGS) and cadmium telluride (CdTe) were developed. These technologies suffered in terms of efficiency, however, offered a promise of lower costs at large scale manufacturing level. So far, except for CdTe technology, it has been proven difficult for thin film technologies to compete with the continuously falling prices of the silicon based PV modules. Concentrated Photovoltaics (CPV) technology employs optical components in order to increase the solar irradiance on a high efficiency solar cell such as a multi-junction cell. Several other novel concepts are being explored at the research level such as Intermediate Bandgap Solar Cells, Quantum Dots and Nanowire based solar cells, Perovskite solar cells etc. Provided their feasibility for large scale manufacturing and reliability is proven, some of these technologies could lead to even lower LCOE for the PV in future. For the purpose of discussion in this dissertation document, only silicon based PV technology will be considered, unless otherwise specified. Therefore, the world ‘PV Module’ would mean a c-Si or mc-Si PV module.
Figure 1 a shows the cross section of a silicon based solar cell. Whenever a photon with energy greater than the bandgap of silicon is incident on the cell, it gets absorbed and an electron-hole pair is created. The electron and hole are separated from each other due to the electric field in the PN junction and the voltage is generated across the cell. The typical industrial cell consists of P-type mc-Si wafer with N-type emitter on top. Figure 1 b shows the top view of the cell in which front contact metallization is shown. The thick conductors are called ribbons while the thin metallic conductors are called fingers. The rear side of such cells is typically completely covered with Aluminum to act as back contact.

![Solar cell diagram](image)

Figure 1: (a) Solar cell cross sectional view (b) top view

### 2.4.2 Construction of PV modules

Several cells are connected in series in order to form PV modules. These cells are connected by ribbons and busbars within the module. Typical industrial modules consist of either 60 or 72 cells connected in series. The series connected cells are passed through lamination process in order to form the protective packaging. Typically, the module construction involves front sheet
of low-iron Sodalime glass, encapsulant as Ethylene Vinyl Acetate (EVA) and a polymer based backsheet made of materials such as Polyethylene Terephthalate (PET) or Tedlar-Polyester-Tedlar (TPT) (Figure 2).

Frame sealant or tape is typically used around the edges of the laminate to provide protection against moisture ingress. Usually, frames are put on the laminates to provide additional protection against glass breakage under mechanical loads. A junction box is then attached to the back of the framed laminate where positive and negative terminals are taken out and bypass diodes are connected per sub-string of cells (Figure 3). Bypass diodes provide protection to the PV module against shading by providing an alternate current path in the event of shading or current mismatch among the cells. Usually one bypass diode is used for each set of 20 / 24 cells connected in series. Therefore, typical commercial 60/72 cell modules have three bypass diodes. Junction box may be filled with pottant in order to provide additional resistance towards moisture / liquid water induced corrosion and electrical shorting. Once the junction box is sealed,
the module undergoes final electrical characterization and inspection at the manufacturing facility before it is shipped out.

Figure 3 Junction box and bypass diodes

2.5 Defining PV module failure

Figure 4 shows the current-voltage and power-voltage curves of typical 60-cell PV module.
Figure 4 Current-voltage(Red) and power-voltage(Blue) curves of typical 60-cell PV module

The important PV performance parameters such as short circuit current ($I_{sc}$), open circuit voltage ($V_{oc}$), current and voltage at maximum power point ($I_{mp}$ and $V_{mp}$) are identified. Following equations are applicable to the PV module I-V curve:

$$P_{max} = V_m \times I_m$$  \hspace{1cm} (3)

$$Fill\ Factor = \frac{V_m \times I_m}{V_{oc} \times I_{sc}}$$  \hspace{1cm} (4)

The efficiency of the module under standard conditions (Spectrum AM 1.5g and 25 C) is calculated using equation 5
Defining PV module failure is a subjective issue. A typically agreed upon definition for failure of a PV module is when its maximum power at rated conditions (or efficiency) drops below 80% of the initial value. In addition to this, various manufacturers may have their own set of criteria specified in the warranty such as a linear power degradation of <1% per year etc. Moreover, a PV module may be considered ‘failed’ if it poses a safety hazard, even if its power is within specified limits. This may happen when the mechanical or electrical construction of the module is compromised which could lead to safety risks or fire hazard.

2.6 PV Module failure modes

The modes by which a PV module can undergo degradation and eventually failure can be roughly classified into two types: wear out failures and catastrophic failures (Figure 5).
Wear out failures correspond to failure modes in which the PV module undergoes gradual deterioration, and this could lead to increasing power loss over time, and PV module failure at certain point of time. Catastrophic failures cause immediate reduction in module power below acceptable limits or render the PV module susceptible to significant safety hazard. This distinction among failure modes should be considered as guideline, as in reality there could be significant interaction between various failure modes and a wear out failure mode could result in development of a catastrophic failure.

Figure 5 PV module failure modes: wear out and catastrophic
2.6.1 Wear out failure modes

2.6.1.1 Encapsulant Discoloration

The phenomenon in which earlier generation standard cure and slow cure EVA encapsulants turn brown when exposed to UV and heat is called encapsulant discoloration. This process reduces the amount of light reaching the solar cells, and therefore the power output of the PV module. Oxygen is known to have a bleaching action, therefore, when a backsheet that permits diffusion of air in and out of the laminate (breathable backsheet) is used, it was found that the discoloration occurred near the center of the cells while the discoloration in the areas near the edge of the cell was bleached out. PV arrays that used concentration systems resulted in accelerated discoloration of the EVA because of increased exposure to UV and heat (Howard J. Wenger, 1991). Since this failure mode could be easily identified by visual inspection of the PV modules or inspection under UV light, it is easy to identify modules that are suffering from encapsulant discoloration and replace them as necessary. It was found that the discoloration happened due to certain additives in the EVA. At that time, glass manufacturers introduced a UV absorber – Cerium Oxide in the low iron glass to reduce the UV exposure of the EVA and decelerate the EVA browning. Later on, the EVA formulations were modified so as to ensure that the EVA is not susceptible to accelerated discoloration in the presence of UV, and the glass manufacturers removed the Cerium Oxide from their glass (John Wohlgemuth, 2010). Therefore, now it is necessary to test the performance of encapsulants under accelerated conditions of UV and high temperature to ensure that the encapsulant will not undergo significant discoloration during the service life of PV modules (Miller, 2015).
2.6.1.2 Delamination

PV module package consists of several interfaces such as glass-encapsulant, encapsulant-cell and encapsulant-backsheet. Any of these interfaces can undergo delamination due to weakening of the adhesive properties between these interfaces. Delamination can be easily identified by visual inspection of field deployed modules. Degradation in adhesional strength is usually associated with UV exposure at high temperature and presence of certain impurities such as Sodium on the cell interface. Delamination on the front side of the cell can cause significant reduction in the Isc and loss of electrical insulation when it is near the edges of the PV module (Shioda, 2013). Delamination can also cause moisture to condense in the delaminated areas to form liquid water and accelerate the corrosion. In case, this liquid water freezes to form ice, the associated expansion could accelerate the process of delamination. Delamination of backsheet can cause loss of electrical insulation of the PV module. In order to prevent delamination in field, it is necessary to choose module packaging materials and adhesives that are stable to long term UV exposure and control the flow of impurities along the interfaces during manufacturing.

2.6.1.3 Corrosion

Corrosion of the front side metallic interconnects can cause increase in series resistance and in worst case electrical disconnection of the affected areas of the cell. Corrosion can be identified by visual inspection of the front side metallization. Onset of corrosion can be identified by increased series resistance as measured from the I-V curve. The properties of the module packaging to permit diffusion of water vapor and capacity of the encapsulant to absorb water determine the amount of humidity exposure of the cell metallization during module service life (Michael Koehl, 2012). However, exposure to water vapor is not the only factor accelerating
corrosion in PV modules. The hydrolysis of EVA in the presence of UV, heat and humidity produces acetic acid which is known to attack the front contact metallization to facilitate corrosion (Atsushi Masuda, 2015). Use of non-breathable module packaging schemes that employ Aluminum based backsheet or glass as backsheet could result in accumulation of acetic acid in the module package thus accelerating the process of corrosion. In order to prevent corrosion, one may use encapsulants that do not result in acetic acid formation upon hydrolysis when appropriate moisture barriers are used in PV module packaging. Damp heat testing (85% RH, 85 C) for 1000 hours is an accelerated test in IEC 61215 to assess the tolerance of PV module packaging towards corrosion by humidity.

2.6.1.4 Solder Bond and Interconnect Failures

PV modules undergo diurnal thermal cycling as well as thermal cycling due to variations in the seasons. They also undergo mechanical loading due to wind, snow etc. These factors along with the differences in the coefficient of thermal expansion (CTE) cause stresses on the solder bonds and interconnects. This can lead to increased series resistance associated with the solder bond or in worst case solder bond or interconnect failure. Issues with solder bond and interconnects can be identified by Infrared imaging, I-V curve and EL imaging of the PV modules. Thermal cycling test in IEC 61215 is a method for assessing the robustness of solder bonds and interconnects in PV modules. It has been recommended that the thermal cycling test should be extended from 200 thermal cycles to at least 500 thermal cycles in order to realistically simulate the field exposure to the PV modules (Wohlgemuth, 2015). It has been shown that the solder bond and interconnect issues observed in field or during thermal cycling test could be related to the inherent quality issues associated with the module manufacturing process (Tadanori
Therefore, development and implementation of the QMS system for PV manufacturing is expected to mitigate this issue. Use of low CTE materials, softer and thinner ribbons, implementation of pull test as a quality control measure for solder bonds in manufacturing and use of redundancy are some of the approaches currently used to address the issue of solder bond / interconnect failure in PV modules.

2.6.1.5 Cell Cracking

Solar cells can develop cracks during cell / module manufacturing, handling, transportation, installation and field exposure. Reducing the wafer thickness has great potential to reduce the materials costs associated with PV manufacturing. However, attempts to reduce the cell thickness below 160 um are thwarted due to increased wafer breakage and reduced yield (S. Pingel, 2009). Cell cracks can result in electrically disconnected areas and cause increasing power loss during the service life of PV modules. In worst case scenario, cell cracks can cause permanent activation of the bypass diode in a PV module, resulting in approximately one-third power loss of PV module. PV industry has adopted several techniques for detecting cracked cells. For example, Resonance Ultrasound Imaging (RUV) is used as an Incoming Quality Control technique in cell manufacturing to discard the wafers with pre-existing cracks. EL imaging is often used in PV cell and module manufacturing facilities to identify cracks in completed solar cells / modules. Manufacturers use custom criteria based on the number of cracks per cell and number of cracked cells per module in order to reject the defective samples due to cell cracking. Cell cracks in outdoor deployed modules can be detected by techniques such as outdoor PL, Infrared imaging, fluorescence imaging, and sometimes visual inspection when the crack is obviously visible or the crack is decorated by formation of ‘snail trails’. The
phenomenon of ‘snail trails’ results due to discoloration of silver nanoparticles in the front contacts in the presence of UV, heat and humidity (Peng Peng, 2012). The cracks in the solar cells allow moisture to diffuse to the front surface of the cells. Snow-load, wind load and dynamic mechanical loading are the tests that can be used to assess the impact of cell cracking on immediate power loss in PV modules. However, these tests do not provide an insight for the power loss due to cell cracking a PV module may experience in service life. It has been recently realized that all cell cracks in PV module are not equal, with some being more benign than the others (M. Kontges, 2014). Also, the module packaging materials such as residual compressive stress due to backsheet can play significant role in determining the eventual power degradation due to cell cracks in service life (F. Haase, 2014).

The author along with other collaborators are developing a novel framework to assess the criticality of cell cracks found in PV module manufacturing that would take into account the effects due to PV module packaging and weathering during service life of PV modules. This involves performing a classification and statistical analysis of cell cracks in the rejected cells from PV module manufacturing, developing procedures to reproduce similar cracks in the custom modules with different packaging schemes and performing accelerated tests to correlate the type of crack to the power loss (V. Gade, 2015).

2.6.1.6 Potential Induced Degradation

PV modules are connected in series in order to limit the balance of system costs. The maximum system voltage in most countries is now 1000 V and in future it is likely to be increased to 1500 V (E. Gkoutioudi, 2013). Therefore, some PV modules in the array experience high voltages
with respect to ground. This high voltage between the cell circuit and ground results in the flow of leakage current through the module packaging materials. PV modules are known to degrade in the presence of high voltages by a failure mode called potential induced degradation (PID). PID can manifest itself in different forms depending on the polarity of the voltage experienced by the cells. When cells are at negative voltage with respect to ground, PID is known to cause increased shunting of the cells due to deposition of sodium ions in the stacking faults in the solar cell (Volker Naumann, 2014). Modules susceptible to shunting type of PID (PID-s) could suffer significant power loss within few years of service life. PID-s is known to be more prevalent in hot-humid climates and it is also known to have some correlation with the applied bias voltages and the leakage current flowing through the module. PID-s is also reversible to some extent when the polarity of the applied voltage is reversed.

The author has contributed to several studies aimed at understanding the evolution of leakage currents in the outdoor deployed PV modules under high voltage bias (N.G. Dhere, 2014a). An Arrhenius model was used to calculate the activation energies associated with the leakage current as a function of module temperature (N.G. Dhere, 2014b). A finite element analysis based model was created to analyze the distribution of potential, electric field and leakage current in the PV module (N. S. Shiradkar, 2013). It was shown that the electric field distribution is significantly altered when the module surface is covered with a conductive medium such as water/dew/aluminum foil to cause increased leakage currents. Dependence of the leakage current on the electrical resistivity of the module packaging materials was also elucidated.
PID is also known to happen with the cell circuit is held at positive voltage with respect to ground. This type of PID has caused accelerated degradation of the front contact metallization etc.(Hacke, 2011). Measures can be taken at cell, module and system level in order to avoid PID. At cell level, use of high conductivity anti-reflection coatings is known to reduce PID (Ken Mishina, 2013). At module level, use of high resistivity encapsulant and front glass is known to reduce the leakage current and therefore, the PID. At system level, whenever possible, the negative end of the PV array should be grounded in order to prevent the PID-s. However, implementing cell level solutions is the most cost effective approach for preventing PID because use of high resistivity encapsulant and glass is significantly more expensive, and implementing system level solutions may not be always possible due to use of transformer-less inverters that do not require grounding. Therefore, most leading PV module manufacturers now use ‘PID resistant’ cells as a preferred approach to prevent PID-s.

2.6.1.7 Shading Induced Hotspots

Hotspots are areas of localized heating in the PV module where the temperature is significantly greater than the surrounding area. Hotspots can be generated in the PV modules due to various reasons. Usually they appear as symptoms of some active degradation mechanism. For example, interconnect or solder bond degradation can cause current crowding and hotspots. Also, PID-s induced shunted cells can be seen as hotspots in the IR image. However, in this dissertation such incidents of hotspots are considered as manifestations of the underlying failure mechanism, while only shading induced hotspots are considered as a separate wear out mechanism. In the presence of bypass diodes, the maximum voltage across a shaded cell is the open circuit voltage generated by the rest of the cells in the sub-string of cells. This voltage could be between 12 V-
14 V for mc-Si modules. Even though this voltage does not cause instantaneous reverse breakdown of the cells, there could be significant amount of reverse current passing through the cell at such reverse voltages (Otwin Breitenstein, 2009). Also, the shaded cell becomes reverse biased and the power generated by the unshaded cells in the sub-string gets dissipated in the shaded cell. This results in formation of hotspots at the locations of shaded cells. Figure 6 shows the hotspot effect in a module where cell is 50% shaded. The temperature at the partially shaded cell increases to approximately 120 °C. Hotspot endurance test in IEC 61215 is used to certify PV modules against catastrophic failures due to shading induced hotspots. However, even though the module does not undergo catastrophic failure due to hotspots, it is possible that continuous high temperature operation of the cells could lead to wear out over time. Due to increased popularity of PV in urban areas, increasing number of PV systems are expected to experience shading. Therefore, it is an important failure mechanisms that needs additional investigation.
2.6.2 Catastrophic failure modes

2.6.2.1 Structural Failure

PV modules are secured to the mounting structures using specially designed clips, while the mounting structures are secured to the roof or the ground using appropriate connectors. Failure of any of these connectors and compromised securement of the PV modules is be termed as structural failure. The structures are required to be certified to withstand minimum required wind loads and snow loads. Snow load and wind load tests in IEC 61215 ensure that the modules passing these tests will not have more than 5% power loss at the end of the tests. Any power loss that occurs in these tests is mainly due to cell cracking, and the module structure overall remains intact. The module breakage test in IEC 61215 ensures that in the event module undergoes structural failure, the particles generated after module breakage will not pose a significant safety hazard. The guidelines and building codes of securing the modules and the installation structures are open to the interpretation of the licensed structural engineer (Stephen Barkaszi, 2010). Therefore, this process can lead to different design loads for same design specification. Inadvertently, this has a potential for installation errors to occur and eventually PV system
structure to give way under heavy wind or snow loads (UNIRAC, 2012). For example, few PV systems suffered damaged during hurricane Sandy (Levitan, 2012). Fortunately the number of PV systems that experienced damage was significantly less than what was expected after the hurricane.

2.6.2.2 Glass Breakage

The tempered glass is recommended to be used in silicon based PV modules, however, in some cases annealed or heat strengthened glass is also used. Tempered glass is resistant to the usual impacts experienced by the module during production, transportation, installation and service life. However, under certain extreme conditions, glass may give way to the impacts and shatter. This results not only in the loss of transmission but also loss of electrical insulation, and the PV module must be removed from the installation. Glass breakage can result from impact from hail, rocks, extreme snow or wind loads, extreme hotspots and arcing (John Wohlgemuth, 2010). Figure 7 shows an example from the field where glass breakage probably resulted from a rock hitting the module. The circled area shows the point of impact. Sometimes, inclusions in the glass can lead to spontaneous glass breakage (Barry, 2010). It is recommended to use tempered or chemically strengthened glass and employ appropriate glass inspection systems at PV module manufacturing in order to reduce the incidents of glass breakage.
2.6.2.3 *Ground Faults*

PV arrays are either grounded at positive or negative terminal or they are not grounded at all. PV modules and circuitry in between the array terminals should be well insulated from the ground. If this insulation is damaged, parts of the PV array could get accidentally grounded and the current would begin to flow in the ground loops. This process would continue until some component gets hot enough to melt and break the circuit. Ground faults can cause fires and severe safety hazards. Ground faults typically result from installation errors where module mounting clips have penetrated the module insulation and begin to come in contact with the cell circuit. This can be easily avoided by following proper installation practices. An ungrounded array would reduce the risk of damage due to ground faults as it takes two ground faults to cause current flow while a grounded array takes just one ground fault (N. Dhere, 2012)
2.6.2.4 Junction Box / Connector Failure

Junction boxes used in PV modules need to be electrically insulated from surroundings as they contain components at high voltages. Moisture or water ingress in the junction box can cause electrical shorting and corrosion of the interconnects. Junction boxes are rated for their resistance against moisture or water ingress, and use of junction box pottant can significantly reduce the occurrence of this problem. Junction boxes without pottant are usually vulnerable for water ingress and care should be taken to prevent that during transportation, storage and installation of the PV modules. Some junction box designs contain electrical connections held in place by mechanical joints. These mechanical joints could get loose over time and poor electrical connections can cause arcing in the junction box which could lead to fires (Willi Vaasen, 2007). Poor electrical connections in junction box and use of flammable materials could be a significant safety hazard so much so that it has caused entire companies to go bankrupt (Alioettinger, 2013). Junction boxes with welded electrical connections provide highest reliability but at an additional cost. Only materials and adhesives with proven long term reliability should be used to ensure the proper adhesion of the junction box to the module throughout the lifetime. Some adhesives may have reasonable adhesion strength in the beginning, but it could deteriorate during field exposure due to heat, humidity and UV (David C. Miller, 2014). Quick connectors are used for connecting the PV modules in series and making the end connections for PV array. These connectors are expected to provide protection to the electrical joints against moisture induced corrosion and water ingress during module service life. Connectors that tend to get loose over time due to mechanical, vibrational and thermal stresses, increase the risk of overheating and formation of arcs. Increased series resistance at the site of connectors due to corrosion leads to loss of output...
power by the PV array (Juris Kalejs, 2013). Due to the current lack of an accepted test procedure for qualifying PV connectors, connectors with proven field record should be preferred.

2.6.3 Interaction between failure modes

Failure modes in PV modules seldom occur in isolated manner. Typically, one failure mode is seen to accelerate the development of another and considerable interaction is observed between various failure modes and mechanisms. This makes it difficult to decipher the root cause that initiated the degradation process. A couple of case studies are discussed below to illustrate the typical field failures/degradation observed in PV modules.

The first case study pertains to field degradation of an old PV module manufactured in early 1980s. Figure 8 shows the front and rear view of the degraded module. Most likely, a shading or interconnect failure induced hotspot caused excessive heating at the identified cell. This overheating lead to burning and delamination of the backsheet. Once the moisture barrier of the PV module was compromised, increased moisture ingress accelerated the corrosion of front contacts. One can also see the heat, humidity and UV induced discoloration of the encapsulant. The discoloration seems to have worsened near areas of the cell that experienced higher temperature.
The second case study concerns with a 10 year old c-Si PV module in Florida. Author has co-authored a publication in which this case study has been discussed in significantly more details (Neelkanth Dhere, 2013). Several characterization techniques such as indoor and outdoor IR imaging, EL imaging and visual inspection were used to perform the failure analysis. Figure 9 shows the images of the same module/degraded cells taken using various characterization techniques. Current crowding at an interconnect resulted in excessive heating, which lead to formation of a burn-hole in the backsheet as shown in Figure 9. Higher temperatures also exacerbated the encapsulant discoloration at that particular cell.
Figure 9 Failure analysis by (a) Outdoor IR imaging (b) Indoor IR imaging (c) EL imaging (d) Visual Imaging

Figure 10 Burn-hole in the backsheet
Whenever multiple failure modes are observed in a PV installation, it can be useful to classify the failure modes according to the severity, likelihood of occurrence and detectability. Risk Priority Number (RPN) can be used to address this issue. In a study of field inspection of modules in a desert, it was shown that solder bond failures had highest RPN value followed by other failure modes such as encapsulant discoloration, backsheet detachment etc (Joseph Kuitche, 2014). Unfortunately, diode failures were not assigned any RPN number in that study. Even though interaction between different failure modes can makes it difficult to separate out contributions from each failure mechanism, the failures/degradation within the PV laminate are usually easier to detect by visual inspection and other characterization techniques and corrective action can be taken. On the other hand, bypass diode failures, which are discussed in next section, occur within the junction box, generally do not trigger additional observable failure modes and therefore are much harder to detect.

2.6.4 Bypass diode failures
Bypass diodes are used in PV modules to prevent the application of high reverse voltage across the cells in the event of shading. Bypass diodes can fail in two modes: short circuit and open circuit. For a commercial silicon PV module with three bypass diodes, a short circuited diode causes module to lose $1/3^{rd}$ of the power per failed diode. This immediately results in the failure of the PV module as the power drops below 80%. Whenever a bypass diode fails in open circuit, it does not immediately affect the module power output. However, if the sub-string of cells with the open-failed diode is shaded, shaded cells could be forced into extreme reverse bias, causing cell breakdown, overheating and in worst case fire hazard. Considering the potential safety issues, modules with open-failed diodes are also regarded as failed modules.
Group 4 of the International PV Module Quality Assurance Task Force (PVQAT) was formed to address the issues associated with bypass diode reliability and shading. Since 2012, author has been an active member of the group and has shared the results with the experts from the field on a monthly basis. Despite of the dire consequences of diode failure, limited information is available in published literature about field reports of diode failures. This is because module level, detailed monitoring is necessary to identify power loss in a module with short circuited bypass diode and difficulty in detecting open circuited bypass diode without special procedures. Recently, some research groups have employed special detection tools such as diode checker in order to specifically look for field failures of bypass diodes. Some of the recently published studies involving field failures of bypass diodes are discussed below: Kato et. al. have pioneered the use of the diode checker tool for detecting failed bypass diodes in field deployed PV modules. They found during inspection of an 8 year old PV plant in Japan, that out of 1272 modules, 47% showed diode failures: 3% had burn marks while 44% had no burn marks (Kato, 2012). Additional information about the failure mechanisms of diodes was not available. However, this was the first study that highlighted the need to look for diode failures during field inspection of PV systems. Tamizmani et. al observed diode failures in 26 modules out of 2352 modules in a c-Si plant in Arizona (Tamizmani, 2014). Failure mode was open circuit with clear cracks in the epoxy packaging material. This section of power plant was believed to have experienced shading issues. Diodes were not available for further failure analysis.
2.7 Motivation

Significant motivation for the work presented in this document has come from the author’s interaction with the members of the Task Group 4 on diodes and shading of the PVQAT that included experts from the diode and module manufacturing companies and national labs (Vivek Gade, 2014). Diodes in PV modules are expected to endure much harsher conditions for significantly longer duration than their counterparts in the consumer electronics. It was realized that despite of the severe consequences of diode failure, the performance and reliability of bypass diodes in PV modules themselves has not been evaluated very well, possibly due to lack of clarity on methods for estimating field stressors during service life and insufficient published data on diode field failures. Several members of the Task Group 4 of PVQAT believe that the current lack of sufficient field data is mainly a detection issue and that it could be just a matter of time before significant numbers of diode field failures are discovered and this is recognized as a serious problem. Recently published studies of PV power plant inspections using a specially designed experimental instrument (diode checker) support this belief. Also, currently available accelerated tests for bypass diodes in PV modules do not address all the failure mechanisms and provide inadequate information about the long term reliability of bypass diodes. Considering the gaps in the literature and the potential impact of this work on the field of PV reliability, developing predictive models for assessing the reliability of bypass diodes in PV modules was decided as the focus of this dissertation. The scope of this dissertation as it regards to various diode failure mechanisms is discussed in the next section.
2.8 Failure mechanisms in bypass diodes

Even though a diode is a simple P-N junction device with just two failure modes (open/short circuit), it has many possible failure mechanisms. As previously done with the PV module failure modes, these failure mechanisms can be categorized into two categories: catastrophic and wear out (Figure 11). Catastrophic failures result from one-time events while wear out failures result from gradual degradation of diode characteristics over time. The failure mechanisms addressed in detail in this dissertation are highlighted in red in Figure 11. Note that these are PV specific failure mechanisms. Therefore, they do not contain failure mechanisms such as electrical overstress by passing more than rated current through the diode, as most of the diodes used in PV modules are rated for 15 A or more, and there is no way by which a field deployed PV module could pass that amount of current through the bypass diode.
2.8.1 Arcing
The leads of the bypass diodes are mounted in the junction box using various methods. The diode leads may be welded, soldered or connecting using screw / mechanical connectors. If for any reason the electrical connection of diode leads with the rest of the circuit becomes poor, it can lead to arcing when current passes through the diode in the event of partial shading. Such an arc would most likely destroy the bypass diode in short duration. However, since these failures are unrelated to the diode device as such and can be categorized mainly as electrical connector issues, they are not part of the failure mechanisms analyzed in this dissertation.

2.8.2 Electrostatic Discharge (ESD)
It is known that the Schottky diodes are more prone to failure by ESD. ESD is an important concern in manufacturing where activities such as handling, junction box attachment and flash testing often have a potential to trigger ESD events. Not so long ago, ESD was regarded as No.1...
failure mechanism for bypass diodes in PV modules (Loo, 2012). Since PV module/junction box manufacturing sites are not necessarily conforming to the guidelines such as ESD 20:20, it was natural that the Schottky bypass diodes installed at these locations had potential to suffer from ESD. Some flash testers are also known to produce current surges that have potential to damage the bypass diodes in PV modules. Sometimes ESD events cause latent failures in diodes in which case the diode as a whole does not fail but small areas on the diode die suffer degradation. If such bypass diodes end up getting installed in the PV modules, they are prone to premature failure in the field. Instruments such as a flash tester and insulation resistance testers could also generate current surges that can damage the diodes (Whitfield, 2012). The need to come up with guidelines for avoiding ESD in manufacturing was perceived by the Task Group 4 of PVQAT and a technical specification for assessing the vulnerability of bypass diodes for ESD was developed (Whitfield, 2013). Since the development and dissemination of this technical specification, there has been more awareness among the PV and junction box manufacturers regarding the ESD and the protective measures that can be implemented at the factory level in order to avoid ESD. Since ESD is a completely avoidable failure by following best practices, it is not included in the failure mechanisms modeled under this dissertation.

### 2.8.3 Thermal Runaway

When the PV module is partially shaded, the diode corresponding to the shaded sub-string gets forward biased. The power dissipation in the diode in forward bias begins to increase the temperature of the diode. If shading is held for sufficient time, the diode temperature stabilizes as it reaches thermal equilibrium. If the shading is suddenly removed, the diode returns to reverse bias. If the power dissipation in the reverse bias is greater than the heat dissipation capability of
the junction box, the diode temperature begins to increase. The reverse current (and power dissipation) increases exponentially with temperature. This leads to even more power dissipation and this process continues till the diode is completely destroyed by overheating. This phenomenon is called thermal runaway. It was recently realized from some experiments performed in the lab that the Schottky bypass diodes used in PV modules could be susceptible to thermal runaway (Fahrenbruch, 2010). Currently there are no accelerated tests in the IEC 61215 that can qualify a diode against thermal runaway. That means, there is nothing stopping a vulnerable diode from getting deployed in the field, other than the manufacturer’s voluntary initiatives. Also, it takes just one shading event under right environmental conditions for thermal runaway to take place. Considering the potential consequences, recently, a new “thermal runaway test” has been proposed and the test draft is under revision. Author has contributed towards development of the new thermal runaway test and has proposed a framework for predicting vulnerability of bypass diodes for thermal runaway. Figure 12 shows picture of a diode failed by thermal runaway in a lab experiment.
2.8.4 High Temperature Forward Bias (HTFB) operation

When the module is partially shaded, the diode becomes forward biased. The ambient temperature and the current passing through the diode determine the operating temperature of the diode. Some modules regularly experience shading during their lifetime. Therefore, the diodes spend significant amount of time in forward bias state. Depending on the module mounting configuration (roof/rack mount), location (hot/temperate), extent of shading, and the current passing through the diode, the diode may have to operate at high temperature for considerable time during service life. Long term, high temperature operation is known to reduce the lifetime of the Schottky diodes, just like any other semiconductor components. The bypass diode test in IEC 61215 does not provide adequate information about the long term reliability of diodes against HFTB mechanism. Several diodes/junction boxes were tested by the author using “Extended Bypass Diode Test”. One of the important limitations observed in the literature was models to estimate the temperature of the bypass diodes in field deployed modules under various conditions.
conditions. HFTB mechanism is discussed in details later in this dissertation along with the framework to estimate field stressors for this mechanisms and calculating the field equivalents of the accelerated tests.

2.8.5 **High Temperature Reverse Bias (HTRB) operation**

Bypass diodes operate in reverse bias in normal, unshaded state of the PV module. The voltage generated by the sub-string of cells (12-14 V) gets applied in the reverse direction. The temperature of the diodes in this state is typically equal to the module temperature as the reverse leakage currents are not sufficient to cause any significant self-heating. However, continuous operation of the diodes at reverse bias, and moderately high temperatures is known to cause localized breakdown at the die level which can eventually exacerbate to cause a complete failure of the device. Due to the large amount of environmental chamber time required for testing to failure and resource limitations, this mechanism has not been addressed in greater details in this document.

2.8.6 **Thermal Cycling (TC)**

Diodes experience stress not only from operating at elevated temperatures for long amount of time, but also from the thermal shock experienced by sudden or gradual changes in the temperatures experienced by them. A diode could experience temperature difference close to 200 °C just during a single day. The difference in the maximum and minimum temperatures (ΔT₁) experienced by the diode during a day is significantly more than that experienced by the module, because current passing through the diode in forward bias state significantly increases the diode operating temperature. Thermal cycling is known to cause die attach, solder bond and epoxy packaging failures. Current thermal cycling test in the IEC 61215 for the modules does not
involve passage of current through the diodes, therefore does not replicate the $\Delta T_J$ experienced by the diodes in field deployed modules. It has been proposed that thermal cycling should be performed for at least 50 cycles with current through the diodes. In this dissertation, framework for estimating the field stressors for thermal cycling along with the results from the thermal cycling test with current passing through the diode are discussed later in this dissertation.
CHAPTER 3 ACCELERATED TESTS FOR RELIABILITY ASSESSMENT

3.1 Introduction to Accelerated Tests

Ideally, all products should be tested in the field prior to large scale deployment in the market. However, this may not be practical due to many reasons. For example, the time period in which degradation in field conditions could be seen may be in several years for PV modules that are warranted to last for 25 years. Clearly, this timeframe is impractically longer than the product development cycles. Accelerated tests are used to accurately replicate the field failures in the laboratory conditions in much shorter amount of time. This is usually performed by using higher stress levels than those experienced by the products in the field. However, if the stress levels in accelerated tests are much higher than field conditions, extraneous failure mechanisms may trigger which are irrelevant as they will never be observed in field. Accelerated tests are not only useful to the manufacturers of the products, but also to the third parties interested in performing comparative reliability assessment of products from various manufacturers. Field failure data for PV modules and components is rarely available in adequate amounts in public domain because of the confidentiality and other concerns of the manufacturers. For some other products such as consumer electronics, the product useful life (~3 years) is much shorter than the time it would take for field failures to show up. Therefore, in all such cases, accelerated tests are only way out to assess the reliability of new products made using different designs, materials or processes. It is important to address the accelerated test methodology, types of accelerated tests and their capabilities and limitations in order to understand their role in understanding the long term reliability of PV modules and bypass diodes.
3.2 Types of Accelerated Tests

G. Hobbs devised the names of several types of accelerated tests shown in Figure 13 (Hobbs, 2007). Most of the discussion regarding the types of accelerated tests in this chapter is based on the book by H. McLean (McLean, 2009). Basically these accelerated tests can be divided into two categories depending on the type of information retrieved from them. In the qualitative approach, HALT, HASS, HASA, QT tests are used to arrive at robust design of the product, identify and reduce the defects related to manufacturing process. Since the stressors used in this approach are considerably high, the failure data is generally not very useful for quantitative estimation of product service life. Despite of this, the failure data can provide useful qualitative insight into modes and mechanisms of failure. The information about modes and mechanisms of failure obtained from qualitative tests can be used to design quantitative tests such as ALT/ADT and perform statistical analysis on the failure/degradation observed during testing to yield quantitative information about the service life of a product. Levels of stressors used in ALT/ADT are only moderately high as compared to stressor levels experienced by products in their service life. This ensures that the failure mechanisms in these accelerated tests would be accurately replicate those observed in field. Each type of accelerated test is briefly discussed below:
3.2.1 Highly Accelerated Lifetime Test (HALT)

HALT is a qualitative test used to detect and correct design faults and weak links during product design phase. When the cycle of HALT, identification of weak links and design improvement is iteratively performed, the result is typically a robust design of the product that will have long service life before wear out failures begin. During HALT, the product is subjected to conditions of stressors much severe than what it would experience in the operating conditions. Typical stressors used in HALT are high temperature, rapid temperature cycling, vibration, humidity and pressure. Depending on the amount of stressors used and product under test, HALT may not provide any quantitative estimate of the service life of the product.
3.2.2 Highly Accelerated Stress Screening (HASS)

HASS is a qualitative test used to identify and correct process flaws during the mass production of the product. HASS is used to identify and screen out the products with birth defects that may fail before the average service life of that product. Since HASS is typically carried out on 100% of the manufactured products, this makes it possible to weed out the defective products before they are shipped out to the customers and it helps to accelerate the process of identifying flaws in manufacturing process. The stressors used in HASS testing are milder than those used in HALT and are more representative of the use environment of the products. It should be noted that since HASS is aimed at identifying failures corresponding to defective products, it is not useful to estimate the service life of the products in field.

3.2.3 Highly Accelerated Stress Auditing (HASA)

Special chambers are required to perform HALT and HASS testing. Often, considering the physical size of the product, volume of the products manufactured and available resources, it is impractical to perform HASS testing on 100% of the manufactured products. HASA methodology is very similar to HASS, except that instead of testing 100% of the manufactured products, a small sample of products is subjected to testing. Samples representative of each process/batch of materials are usually selected and design of experiments is used to identify flaws in the manufacturing process. Considering the similarities between the HASS and HASA methodologies, most of the discussion for HASS can be applied for HASA.

3.2.4 Qualification Test (QT)

QT is an individual accelerated test or a test sequence used for qualifying the product designs under certain certification programs. The aim of QTs is to prevent the products with poor designs
from entering the market by identifying them before they are mass manufactured. The difference between QT and HALT is that the stress levels and their durations in QT are limited so as to make them reasonably fast and cost effective. Unlike HASS tests which are quality control tools aimed at identifying process flaws, and performed on 100% of the produced products, QTs quality the product design instead of individual products. QTs aim for reducing the infant mortality of the products at significantly less cost as compared to HALT or HASS testing.

3.2.5 Accelerated Lifetime Test (ALT)
Due to short product development cycles, it is essential to get the information about service life of products in a short period of time. Field failure data for the products is valuable, but it may not be possible to have sufficient field data to get failure distributions due to various reasons such as long time to failure (e.g. PV Modules) or service life being greater than useful life of the products (e.g. computer hard drives). Therefore, ALT is used to generate failure data and distributions for products using moderate levels of stressors once the key failure modes and mechanisms are identified. The assumption of ALT is that the failure distribution type remains unchanged as the stressor levels are varied and the distribution parameters are a function of accelerating variables. In order for this assumption to be valid, stressor levels only moderately higher than the operating conditions of the product are used. A parametric model is used to empirically fit the failure data and predict the service life under various operating conditions.

3.2.6 Accelerated Degradation Test (ADT)
In ALT, the products are tested till failure and the failure data is collected. On the other hand, in ADT, the physical process responsible for degradation leading to failure is monitored. The methodology for ADT is similar to ALT, the difference being the degradation rate, instead of
failure rate is monitored. In reliability testing, the failure can be defined as a hard failure when the product stops working or soft failure when a certain amount of degradation has reached. ADT is especially useful for items that have soft failures (e.g. PV modules). For highly reliable items the rate of degradation under normal operating conditions is extremely small. Therefore, these products are tested at elevated levels of stressors so that degradation rate can be measured. Once the distribution of degradation at elevated stress levels is known, the degradation rate under normal operating conditions can be predicted. Detailed knowledge of the degradation process is required to carry out ADT.

3.3 The Bathtub Curve

The bathtub curve has been historically used for understanding the reasons for failure during different phases of the product life cycle (Figure 14). In the early stages of the product life, the failure rate could be high due to birth defects in the products. This period of increased failure rate is identified as “infant mortality period”. Once Qualification Testing (QT) has been performed to arrive at a robust and mature product design, HASS testing is typically used to weed out the products with birth defects and it is successful in reducing the infant mortality of the products. The middle portion of the bathtub curve is identified by constant failure rate. In this phase the product undergoes random failures. HALT testing is used to make products more robust so that they would have a high service life before wear out begins. The last portion of the bathtub curve is again identified by increased failure rate due to wear out. Some products with relatively lower useful lives are discarded before they could reach the wear out phase. However, in case of products with very long service lives like PV modules, the wear out portion of the bathtub curve
is also important. For such products, mere HALT testing does not provide a guarantee that the product would last for expected service life. For such products, lifetime estimation by ALT / ADT has direct implication on the project finance. For example, in early years of PV, the energy produced by modules in years >20 had negligible impact on the project finance. However, since the cost of PV has undergone significant reductions, even the energy produced in years >20 has considerable financial implications. Physics based models or functions that provide accurate predictions of long term PV performance are needed in addition to the ALT/ADT tests for estimating degradation rates for various failure mechanisms to predict the wear out failures.

![Bathtub curve and applicability of various accelerated tests](image)

Figure 14 Bathtub curve and applicability of various accelerated tests

One possible way to understand the wear out mechanisms in PV module is to inspect >20 year old PV systems. However, the long term reliability of modules manufactured with different Bill
of Materials (BOM) would be significantly different. Therefore, inspection of modules that were manufactured 20 years ago may not provide adequate information to predict the long term reliability of recently manufactured modules using much lower BOM and latest technology. Depending on the failure mechanism under investigation, the duration of ALT/ADT could be significantly long as well. Therefore, in addition to the development of ALT/ADT, it is immensely important to develop frameworks and models to predict the long term reliability of PV modules.

3.4 Accelerated Tests for PV modules

3.4.1 Brief history of PV specific Accelerated Tests
Jet Propulsion Laboratory (JPL) performed the pioneering work in the development of accelerated tests for PV modules. In 1975-81, JPL purchased PV modules from manufacturers in five blocks of procurement dispersed over time for their Flat-Plate Solar Array (FSA) Project (C. R. Osterwald, 2009). The modules from the manufacturers were required to pass a certain series of accelerated (qualification) tests before procurement could be made. The qualification tests were revised for each block based on the field results and accelerated test results from the modules procured in earlier blocks. These tests were based on the reliability tests performed by NASA for space arrays. These tests included tests such as thermal cycling, humidity-freeze, hi-pot, mechanical load and hail impact tests. JPL was also in process of procuring block VI in 1985, with the inclusion of tests such as bypass diode test, damp heat, and UV exposure test. However, due to budget cuts, this procurement was terminated (Wohlgemuth, 2010). During similar time frame, the European Joint Research Commission (JRC) was also developing accelerated tests for PV modules. The European standards 501 and 502 had many similarities
with the JPL block V. The European standard 503, JPL block VI and culmination of best ideas from all around the world formed the basis of the first edition of IEC 61215 in 1993 (IEC, 1993). This became the standard that all major c-Si PV module manufacturers in the world used to qualify their modules before initiating the mass manufacturing for that particular module design. The bypass diode test was not included in the first draft of IEC 61215 because the international community felt that the test was not adequately developed at that time. The second edition of IEC 61215 in 2005 included the bypass diode thermal test along with some other modifications such as elimination of twist test, addition of wet leakage test and addition of requirement to pass peak power current through the module during 200 thermal cycles in order to test reliability of solder bonds (IEC, 2005). It should be noted that the process of incorporating new tests and changes in the IEC document is a significantly slow process and it can take years, if not decades for the changes to get accepted. Therefore, interim standards such as Qualification Plus were prepared that offered additional measures to ensure the long term reliability of PV modules (Sarah Kurtz, 2013). The accelerated tests specifically designed for bypass diodes are discussed below.

### 3.4.2 Bypass Diode Thermal Test: IEC 61215

The bypass diode thermal test or simply called as bypass diode test in IEC 61215 qualifies the diodes in the junction boxes for operation within acceptable temperature range. In this test, thermocouple is attached to the case of the center diode in a junction box along with wires to measure the forward voltage drop across the diode ($V_f$) and the junction box is sealed and attached to the back of the module (Figure 15). The test involves heating the module in an environmental chamber to $75 \, ^\circ C \pm 5 \, ^\circ C$ followed by passing forward current through the diodes
equal to the short circuit current \((I_f = I_{sc})\) of the module measured at STC, for 1 hour. The diode junction temperature is estimated from the measured diode case temperature \((T_{case})\) and the thermal resistance from junction to case \((R_{j,c})\) as given in the diode manufacturer’s datasheet using Equation 6.

\[
T_J = T_{case} + R_{j-c} \times V_f \times I_f
\]

The junction temperature should be less than the maximum rated junction temperature under forward bias, provided by the manufacturer, in order for the diode not to fail the test. Consequently, the diode forward current is increased to \(1.25 \times I_{sc}\) of the module and it is continuously passed through the diode for 1 hour. The diode should be functional in forward and reverse bias at the end of the test in order to pass the test.

![Figure 15 Setup for bypass diode test](image)

The one hour time used in bypass diode test is derived from the time it takes for the diode to attain thermal equilibrium and reach maximum junction temperature under given conditions of
forward current and ambient temperature. This test makes sure that the diodes/junction boxes with extremely poor thermal management (so much so that the diode temperature exceeds the rated maximum temperature) are identified. However, most of the commercially available diodes/junction boxes easily pass the test. Only 1 hour of exposure at high temperature is not sufficient to induce failures associated with continuous high temperature operation of the bypass diodes. In order to address this issue, NREL proposed an “Extended Bypass Diode Test” in the Qualification Plus standard (Sarah Kurtz, 2013). The only difference between the two bypass diodes tests is that the exposure time at current equal to Isc has been increased from 1 hour to 96 hours. Performance of various types of diodes and junction boxes under these tests is analyzed in this dissertation.

3.4.3 PV Module Qualification Tests: capabilities and limitations
PV module qualification tests are strict pass/fail tests that attempt to qualify the modules against a sequence of tests to ensure that the module design does not have obvious flaws which would result in premature failure of products in the field (Wohlgemuth, 2012). Modules that pass the qualification sequence are more likely to survive in the field and less likely to suffer from infant mortality. In many markets, passing the QTs in IEC 61215 is a minimum requirement to participate. Therefore, QTs need to be designed in such a way that most of the commercially available modules with ‘reasonably good’ design will pass and only those with obvious design flaws will fail. Today, most of the commercial modules pass the IEC 61215 qualification test sequence without suffering from any significant degradation. Approximately 10 modules are required for IEC 61215 test sequence for design qualification, before mass manufacturing of the modules with qualified design could be initiated. If any module fails any test in the IEC 61215,
the module design is revised and the module has to undergo entire certification sequence from beginning. PV module qualification tests in IEC 61215 have been very successful in reducing the infant mortality of PV modules over the years (Wohlgemuth, 2011). However, these tests were designed just for that purpose and it is important to understand their limitations.

Large (~1 GW) PV module manufacturing plants produce millions of PV modules per year. Clearly, the 10 or so modules that went through the IEC 61215 sequence is an insignificant number as compared to the volume of modules that are actually manufactured. Whether each produced module will have reliability similar to those modules that passed the QTs depends on the voluntary quality control asserted by the module manufacturer. Once the design of the PV modules has been qualified using IEC 61215, the manufacturer free to change the suppliers of the raw materials and make “reasonably small” changes to the design, without needing to go through additional certification process. Clearly, this can induce undesired changes in the module reliability. QTs do not address all the failure mechanisms that might occur in field. For example, there is no test in the IEC 61215 that addresses the potential induced degradation or thermal runaway in bypass diodes. Since most of the todays commercially available modules pass the IEC 61215 test sequence without undergoing any significant degradation, QTs are not useful for differentiating between the modules that will have long or short lifetimes. Clearly, these tests do not provide any information about the wear out in the PV modules. Therefore, QTs are not useful to predict the lifetime of PV modules in field.

3.4.4 Gaps in the accelerated tests for bypass diodes

Obviously, the general limitations of the qualification tests discussed in last section are also applicable to the qualification tests of bypass diodes. In this section, the gaps specifically in the
available accelerated tests for bypass diodes that were analyzed to determine the focus of this dissertation are discussed.

Firstly, the module temperature of 75 °C was selected as a best guess for the maximum module temperature attained by the PV modules in field. It has been shown that for roof mounted PV modules in hot-dry locations, the module temperature could get close to 100 °C. Therefore, the temperature of the bypass diodes in field could be more than the maximum temperature attained during the bypass diode test. In addition, it is not possible to come up with climate-specific rating of bypass diodes with the current test as the module temperature is fixed to 75 °C. The 1 hour exposure at high temperature was not aimed at simulating degradation by continuous operation at high temperature. Even the 96 hour exposure at high temperature in the extended bypass diode test seemed negligible as compared to the service life of the bypass diodes (25 years). Due to lack of frameworks for determining the diode temperatures in field as a function of module mounting, and environmental conditions, it was not possible to quantify the field stressors experienced by bypass diodes. This limitation had also made it impossible to determine the field equivalents of the accelerated tests for bypass diodes, which is an essential step for estimating service life.

There was no test in the IEC 61215 that could qualify the diodes against thermal runaway. Also, there were no models to predict the vulnerability of bypass diodes for thermal runaway as a function of the diode properties, module current and the junction box thermal properties. A draft for the thermal runaway test was proposed by the task group 4 of PVQAT, but it needed further improvements and substantiation based on the physics based models.
Thermal cycling as a part of IEC 61215 results in the temperature cycling of the module and its components from -40 °C to 85 °C. The temperature extremes were determined based on the estimated maximum temperatures experienced by the fielded PV modules. It was known that the bypass diodes, when forward biased, operate at much higher temperatures (~150 °C). Therefore, the ΔT\textsubscript{J} for PV modules used in the thermal cycling test was clearly inadequate to test the bypass diodes.

Overall, it was realized that there were two major bottlenecks in developing service life models for bypass diodes: (i) Lack of framework for estimating field stressors (ii) Lack of framework for predicting the vulnerability of bypass diodes for thermal runaway. Therefore, it was decided to address these two issues as a part of this dissertation. Once these issues are resolved, it would open up the possibility of developing lifetime prediction models for different failure mechanisms observed in bypass diodes.
CHAPTER 4  OPERATION OF BYPASS DIODES UNDER SHADING

4.1 Working principles of Schottky bypass diodes

4.1.1 Brief history of bypass diodes in PV modules
Bypass diodes were integral parts of the PV modules since early days of terrestrial PV module technology. In the beginning, silicon PN junction diodes were used as bypass diodes. These diodes had higher forward voltages as well as higher reverse breakdown voltages (~hundreds of volts). The reverse leakage currents in these silicon PN junction diodes were negligibly small for thermal runaway to be a serious concern. As the module currents increased over time, the power dissipation in the silicon PN junction bypass diode under shading became unacceptably high. Therefore, these diodes were eventually completely replaced by the silicon Schottky diodes that had lower forward voltages and therefore, low power dissipation in forward bias. Even though these diodes had lower forward voltages, they suffered from higher reverse leakage currents and lower reverse breakdown voltages (~40-50 V). This made them susceptible to undergo thermal runaway under certain conditions. Today, silicon Schottky diodes are ubiquitously found in the commercial PV modules. Therefore, most of the discussion in this dissertation relates to the silicon Schottky bypass diodes.

4.1.2 Structure of Schottky bypass diodes
Structure of a typical axial silicon based Schottky diode is shown in Figure 16. In this type of diode, the Schottky barrier is formed by the metal-silicon junction. The typical metals used for Schottky diode include platinum, molybdenum, chromium, tungsten etc. The semiconductor is usually n-type Silicon. The metal-semiconductor junction provides the rectification while the other silicon-aluminum junction is an Ohmic contact. Silicon die with metal contacts is then
encapsulated into an epoxy packaging to provide protection against environmental stressors. The Schottky diode could be incorporated in one of the many packaging schemes. The most commonly used packages for bypass diodes used in PV modules include axial and surface mount. Surface mount diodes have an option of mounting on a large metallic heat sink and therefore, due to better heat dissipation properties, they can be accommodated in smaller junction boxes.

![Figure 16 Structure of Schottky bypass diode](image)

**Figure 16 Structure of Schottky bypass diode**

### 4.1.3 Physics of Schottky bypass diodes

Schottky barrier diodes are majority carrier devices. Since N-silicon is commonly used semiconductor in the Schottky diodes, the majority carriers are electrons. When the cathode of the device is applied negative voltage with respect to anode, Schottky diode becomes forward biased. In silicon Schottky diodes, thermionic emission across the Schottky barrier is the dominant current transport mechanism. The current flowing through the Schottky diode in forward bias is given by Equation 7.
Where $I_f$ is the forward current, $A$ is the area of cross section of the device, $A^*$ is the Richardson constant, $T$ is the junction temperature in kelvin, $\phi$ is the Schottky barrier height, $k$ is Boltzman’s constant, and $V$ is the forward voltage across the device. The Schottky barrier height is determined by the material properties of the metal-semiconductor junction.

In the reverse bias, the leakage current through the Schottky diode ($I_r$) is given by following Equation 8.

$$I_r = A^*T^2 e\left(\frac{-q\phi}{kT}\right)$$

(7)

It is seen that the reverse leakage current increases exponentially with temperature.

### 4.2 Extracting data from diode manufacturer’s datasheets

The manufacturer’s datasheets for diodes provide detailed information about the forward and reverse I-V properties as a function of temperature, in addition to thermal and mechanical characteristics. For Schottky diodes, the forward I-V relationship is exponential, reverse current-voltage relationship at given temperature is approximately linear at lower reverse voltages, while the dependence of reverse current on junction temperature follows an exponential trend. These properties are usually provided in the datasheet in the graphical form. It is useful to digitize this information in order to be able to process the data using mathematical models. Graphical data
extraction software provide a semi-automatic and relatively accurate method of digitizing the data from graphs. Several freely available graphical data extraction software can be used for this purpose. Typically, this process involves following steps:

(i) Storing the graphical data in an image file

(ii) Loading the image file in the graphical data analysis software

(iii) Defining the start and end points on X and Y axes, defining axis type (linear or logarithmic) and entering the actual values of the physical parameters represented on the axes at the end points.

(iv) Clicking on the curve at selected locations to digitize the values.

(v) Storing the digitized points in csv or excel file format for further processing.

However, it is necessary to perform an error analysis to understand the effect of operator and software on the extracted data. The error analysis involves understanding the variation (in percentage) of the extracted parameter from the global mean for different types of software used and various operators participating in the study. For this purpose, two freely available graphical data extraction software and two operators were employed. The first software was a web-based tool to be operated using a web browser (Rohatgi, 2015), while the second software was a program that needed to be installed on the computer (Matthews, 2013). The software programs are referred as SW1 and SW2 respectively. The error analysis is separately performed for following three types of graphs typically analyzed in this dissertation: (i) Forward I-V (ii) Reverse I-V (iii) Reverse current as a function of temperature.
4.2.1 Forward I-V at 25 °C

For this case study, the forward I-V curve at 25 °C, given in the datasheet of a Schottky bypass diode 20SQ040 was used (Diotec, 2015). The Y-axis represents the current in logarithmic scale, while the X-axis represents the voltage. The operators were asked to click on the points where the I-V curve intersects the horizontal lines in the logarithmic plot. These intersection points correspond to a series of ‘nominal’ values of current such as: 0.02, 0.03, 1, 2, 3, 10, 20, 60 A. Whenever the operator clicks on a desired point, its X and Y coordinate are recorded in the software. However, only the values on X axis (voltage) are kept and the Y axis values (current) are replaced with the corresponding nominal values. Therefore, only the error analysis corresponding to the forward voltage values is performed. This process is repeated a total of four times (Number of operators=2, Number of software=2). Mean Vf for each value of current is calculated using following Equation 9:

\[
\mu_i = \frac{\sum_{sw=1}^{2} \sum_{op=1}^{2} \sum_{j=1}^{K} V_{f_i,op,sw}}{N}
\]

(9)

Where \( \mu_i \) is the mean \( V_f \) for current \( i \), \( op \) is operator and \( sw \) is software. The total number of replicates for a given combination of operator and software is \( K \), while \( j \) is the replicate number. In this case, since there were two replicates, the value of \( K \) was 2. \( N \) is the total number of measurements, which in this case was \( N = 2 \times 2 \times 2 = 8 \). The mean is assumed to be very close to the true value of the \( V_f \) at that current. The percentage error associated with each measurement of \( V_f \) (per operator, per software) for each current \( i \) is calculated using following Equation 10:
\[ e_{i,op,sw} = \frac{V_{f_{i,j,op,sw}} - \mu_i}{\mu_i} \times 100 \]  (10)

Figure 17 shows the percentage error (left Y axis) for each measurement of current, per operator and software as a function of the data point number. Increasing data point numbers correspond to the increasing values of current (right Y axis). It is seen that the deviation from the mean, for any value of current, operator and software is within \( \pm 2\% \). It is also seen that the error or the variation reduces at higher values of current. This effect makes it difficult to apply other statistical techniques such as ANOVA. Since power dissipation in the diode in forward bias is given by \( I \times V_f \), the error in the power dissipation can also be assumed to be \( \pm 2\% \). In fact for the values of current typically of interest for PV applications (1 A - 10 A), the error is within \( \pm 1\% \) of the global mean.
4.2.2 Reverse I-V at 25 °C

For this case study, the reverse I-V curve at 25 °C, given in the datasheet of a Schottky bypass diode 20SQ040 was used. The Y-axis represents the reverse current in logarithmic scale, while the X-axis represents the percentage of peak reverse voltage. The peak reverse voltage for this diode is 40 V. The operators were asked to click on the points where the voltages correspond to 8, 10, 12, 14 and 16 V. These voltage values were chosen because they correspond to the range of reverse voltages generated by sub-string of cells which are connected across the bypass diodes. Percentage error was calculated according to Equation 10 for these nominal values of voltages. Figure 18 shows the percentage error in reverse current for different values of voltages. It is seen
that in this case, the percentage error for different software and operators lies within ±3% of the global mean.

![Graph showing reverse IV error analysis](image)

**Figure 18 Reverse IV error analysis**

### 4.2.3 Reverse current vs Temperature at 12 V

For this case study, the reverse current values at different temperatures at a fixed reverse voltage of 12 V given in the datasheet of Schottky bypass diode 20SQ040 were used. The operators were asked to click on the points where the voltage was equal to 12 V, at temperatures of 25 °C, 75 °C, 125 °C and 150 °C. The value of 12 V was chosen because it is representative of the reverse voltage generated by sub-string of cells which are connected across the bypass diodes. Percentage error was calculated according to Equation 10 for these nominal values of voltages. Figure 19 shows the percentage error in reverse current for different values of temperatures. It is seen that in this case, the percentage error for different software and operators lies within ±2% of the global mean.
4.3 Electrical properties of bypass diodes

Seven commercially available diodes from three major manufacturers (A,B,C) were selected for comparison. These diodes were selected in such a way so that they would represent a wide spectrum of available bypass diodes differing in forward voltages and leakage currents. All of these diodes were at least rated for 12 A forward current and were rated for 40 V to 50 V in terms of reverse breakdown voltage. Note that this analysis does not reflect in any way on the overall quality of diodes produced by manufacturers but is limited to the selected types of diodes from those manufacturers. Figure 20 shows the forward I-V curves of these diodes measured at 25 °C. Forward voltage is plotted on the Y axis for various diodes and forward current is on the X axis. It is seen that there is significant difference in the forward voltages of the diodes for
given value of current. Table 1 shows the forward voltage drop and instantaneous power dissipation in each diode at forward current equal to 10 A, and temperature equal to 25 °C. The forward voltages in increasing order are given as A2<A1<B1<A3<C1<B2<C2.

Figure 20 Forward I-V curves of these diodes measured at 25 °C
Table 1: Forward voltage drop and instantaneous power dissipation at 10 A, and 25 °C

<table>
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<th></th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>B1</th>
<th>B2</th>
<th>C1</th>
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<td>0.552</td>
<td>0.481</td>
<td>0.553</td>
</tr>
<tr>
<td>$P_f = V_f \times 10$</td>
<td>4.52</td>
<td>4.16</td>
<td>4.68</td>
<td>4.63</td>
<td>5.52</td>
<td>4.81</td>
<td>5.53</td>
</tr>
</tbody>
</table>

Figure 21 shows the reverse leakage current ($I_r$) as a function of junction temperature for these diodes measured at 12 V. The $I_r$ for these diodes at 150 °C, 12 V is shown in the Table 2 along with the instantaneous power dissipation in reverse bias. It can be seen that there is more than two orders of magnitude difference in the maximum and minimum values of the reverse leakage currents of these diodes. This is a significant observation, as all of these diodes are designed for the same purpose of bypassing the module current under shading, and they all have passed the bypass diode test in IEC 61215. The diodes arranged in the order of increasing reverse leakage current are given as: C2<B2<C1<B1<A3<A1<A2. It can be seen that this order is almost completely reverse of the order in which their forward voltage drops increase. This can be explained from the current transport equations for Schottky diodes. Lower the forward voltage, higher is the reverse leakage current. Therefore, the diode choice is a compromise between the low forward voltage, low leakage current and cost.
Figure 21: Reverse leakage current ($I_r$) as a function of junction temperature at 12 V

Table 2: Reverse current for these diodes at 150 °C, 12 V

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>B1</th>
<th>B2</th>
<th>C1</th>
<th>C2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_r$</td>
<td>0.404</td>
<td>0.778</td>
<td>0.147</td>
<td>0.059</td>
<td>0.0106</td>
<td>0.0126</td>
<td>0.0075</td>
</tr>
<tr>
<td>$P_r = I_r \times 12$</td>
<td>4.85</td>
<td>9.34</td>
<td>1.76</td>
<td>0.71</td>
<td>0.13</td>
<td>0.15</td>
<td>0.09</td>
</tr>
</tbody>
</table>

4.4 Effect of shading on PV modules

Shading can cause hotspots and significantly reduce the instantaneous power output of the shaded PV module. This is because, the sub-string of cells corresponding to the shaded cell gets cut-off and the module current is bypassed through the bypass diode. In the absence of shading,
the bypass diodes would act as passive components in PV module. Regulatory bodies and PV installers use several techniques and software tools to identify preferable locations for solar deployment with reduced impact from shading. Nevertheless, most field deployed PV modules will invariably experience shading (full or partial) at some point of time due to shadowing from other parts of the PV array, trees, nearby structures, power lines, people, wildlife, leaves, bird droppings, uneven soiling, etc. With increasing penetration of PV into urban areas and rising popularity of micro-inverters that can limit the immediate effect of shading to the instantaneous power output of a single module, substantial number of PV systems are expected to be deployed in shaded conditions (Ha T. Nguyen, 2012). Various models have been proposed to predict the effect of shading on immediate power output of PV system (Deline, 2009) (Engin Karatepe, 2007). However, in this dissertation, the effect of shading is analyzed in order to understand the switching of bypass diodes. Therefore, the well investigated area of power loss due to shading is not the focus of this chapter. Instead, the less explored effects of shading on the bypass diodes themselves are studied.

4.5 Types of Shading

A field survey was carried out to determine the possible causes and types of shading experienced by field deployed PV modules. Depending on the temporal evolution of the shading experienced by the module, it can be classified into three categories: (i) Short term, random shading (ii) Intermediate term, periodic shading (iii) Long term, continuous shading
4.5.1 Short term, random shading

Short term, random shading events are triggered by events such as personnel walking nearby modules, bird sitting on the modules, leaf lying on the module flying off etc. These are usually caused by objects close to or on the module itself and may cover significant portion of the cell to trigger a significant mismatch. Figure 22 shows the examples of a short term, random shading events. The randomness is highlighted by the fact that same or similar shading event may or may not occur immediately. The bypass diode corresponding to the shaded sub-string gets activated as long as shading is there, and returns to reverse bias as soon as the shading is removed. Bypass diodes in modules experiencing this type of shading could undergo failure by thermal runaway.
4.5.2 Intermediate term, periodic shading
Intermediate term, periodic shading events are usually triggered by the objects surrounding the PV module that cause shading at some parts of the day or during certain times of the year. Figure 23 shows a PV system installed on the side of a highway in Florida. Since the modules are facing the trees, they receive daily shading during early morning and late afternoon hours. Figure 24 (a) and (c) are examples where the module experienced shading from mounting structures during peak afternoon hours. This shade will move along the module so that different sub-strings are shaded at different times. Figure 24 (b) is an example where module clips and even adjacent modules could contribute to shading during early morning or late afternoon hours. In this case, only certain cells in the PV modules would experience shading. Figure 24 (d) shows shading by
a nearby tree. Again, in this case, the shade would move along the module throughout the day so that different sub-strings of cells would be shaded.

Figure 23 PV system installed on the side of a highway in Florida

In periodic shading scenarios, each bypass diode would be activated for a certain number of hours during certain times of the day. In such cases, the removal of shading is also a gradual process and the diode current slowly reduces to zero as the shading is removed. Bypass diodes in modules receiving periodic shading are spend considerable time in activated, high temperature state during their service life. Therefore, they are susceptible to undergo failure by HTFB and TC mechanisms.
4.5.3 Long term, continuous shading

Long term shading usually results from objects stuck to the module surface. This may happen due to uneven soiling, bird droppings, pollens, leaves stuck under frame etc. Figure 25 (a) shows example of bird dropping, Figure 25 (b) shows uneven shading due to pollen grains stuck on the module front surface. In both of these cases, the objects stuck to the module surface would not be washed away in simple rain events. Therefore, the module will experience shading until it is manually cleaned. Figure 25 (c) shows a leaf stuck on the module surface shading small area of the cell while Figure 25 (d) shows shading due to uneven soiling. In case of uneven soiling, the shading could be removed if the module surface gets washed by during rain events. Since in this case, the shade remains continuously on the module, the bypass diode remains in activated state throughout the day. Depending on the current passing through the diode and the operating
temperature, the diodes in the modules experiencing this type of shading would be susceptible to HTFB and TC mechanisms.

**Figure 25 Examples of long term, continuous shading**

### 4.6 Effect of Shading on switching of bypass diodes

Notice: Significant amount of information in CHAPTER 4 (section 4.6 and 4.7) has been reprinted with permission from following publication by the author:


Most of the results in this section and section 4.7 are adopted from author’s publication in proceedings of SPIE (N.S. Shiradkar, 2014). Understanding the effect of shading on bypass
diodes on the modules is necessary for estimating the amount of time diode would be forward biased throughout the lifetime depending on the type and amount of shading received by the module. The switching of bypass diodes in a commercial 60-cell module with Schottky diodes as a function of shading is discussed using flasher I-V measurements as a diagnostic tool.

4.6.1 Experimental setup

Illuminated current-voltage (I-V) measurements were carried out on a commercial 60 cell c-Si module with Schottky bypass diodes in order to understand the switching of bypass diodes under the events of shading. The Figure 26 shows nomenclature for identifying various cells and bypass diodes in the module. As seen from the glass side of the module, the columns of cells are identified with alphabets from A to F while the rows are numbered from numbers 1 to 10. Each small square represents a cell. As seen from the junction box side, the bypass diodes are named as "Left", "Middle" and "Right" diode. Therefore, the diode "Left" is connected across the sub-string of cells from E1 to F1 (E1-->E10 and F10--> F1) while diode "Middle" is connected across a sub-string of cells from C1 to D1(C1-->C10 and D10--> D1) while diode "Right" is connected across a sub-string of cells from A1 to B1 (A1-->A10 and B10--> B1).
Shading a particular cell in a module results in reduced current output from that cell. This current mismatch generated by shading is responsible for switching of bypass diodes under appropriate conditions. Objects very near to the module cast dark shadows resulting in little or no production of photocurrent in shaded areas while the objects farther away cast diffuse shadows resulting in some photocurrent production in shaded areas. The current mismatch generated in the shaded cell is assumed to be directly proportional to the shaded area and the amount by which the irradiance received by the shaded cell has been reduced. In this section, the effect of dark shadows generated by shading a known amount of area of a particular cell at a time is analyzed. The cells were shaded by covering the required area of cell by sticking an opaque material (such as cardboard/rubber pieces) on the glass.
4.6.2 Illustration of switching of bypass diodes

Figure 27 shows the I-V curve of the module in unshaded state. This curve shows expected characteristics that should be present in a working PV module. Figure 27 shows the I-V curve when cell A1 was shaded 50%. A clear bump in the I-V curve is visible as a result of bypass diode switching. The regions of bypass diode On, Off and transitioning are identified. Table 3 shows the comparison of module performance parameters for the unshaded module I-V and A1_50% shaded I-V curves. It is seen that the open circuit voltage ($V_{oc}$) and short circuit current ($I_{sc}$) remain almost unchanged however there is significant reduction in the peak power ($P_{max}$) and Fill Factor (FF). The $I_{sc}$ remains unchanged because the bypass diode turns on near the low voltage region of the I-V curve and provides a bypass path for the current. A steep reduction in current near voltage equal to two-thirds of the $V_{oc}$ is formed due to switching of the bypass diode from On state to Off state. The bypass diode remains off as the voltage is increased to $V_{oc}$. 
Figure 27 (a) I-V curve of the module in unshaded state (b) I-V curve when cell A1 is 50% shaded

Table 3 Module performance parameters for unshaded and cell A1 50% shaded scenarios

<table>
<thead>
<tr>
<th>Shading</th>
<th>$P_{\text{max}}$ (W)</th>
<th>$V_{\text{oc}}$ (V)</th>
<th>$I_{\text{sc}}$ (A)</th>
<th>$V_{\text{m}}$ (V)</th>
<th>$I_{\text{m}}$ (A)</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unshaded</td>
<td>215.24</td>
<td>36.74</td>
<td>8.29</td>
<td>28.03</td>
<td>7.67</td>
<td>0.70</td>
</tr>
<tr>
<td>A1_50%</td>
<td>152.68</td>
<td>36.74</td>
<td>8.33</td>
<td>32.45</td>
<td>4.70</td>
<td>0.50</td>
</tr>
</tbody>
</table>

4.6.3 Various shading configurations
Table 4 shows the various ways by which the module was shaded before taking the flash I-V curve. At first, cell A1 was shaded from 0% shading to 100% shading. The resultant I-V curves are shown in Figure 28. It is seen from Table 4 that the major reason for power reduction is loss of Fill Factor as cell A1 was incrementally shaded. For shading levels below 10%, no measurable change was observed in the $P_{\text{max}}$. Due to presence of bypass diodes, the $P_{\text{max}}$ reduced in a non-linear way as the percentage of shading was increased. The bypass diode was found to turn on at approximately same voltage point for all shading levels however the duration for
which the diode remains on or is in transition from on->off increases as shading levels are increased. By symmetry, similar behavior would be observed when any single cell within the module is incrementally shaded assuming all cells have similar performance.

In order to understand the effect of shading two sub-strings of cells, cells C1 and F1 were incrementally shaded. It is seen in Figure 29 that this causes both bypass diodes ("Middle" and "Left") to turn On. The module power reduces significantly due to lower Fill Factor. Similar effects are expected when two cells in any two different sub-strings are shaded incrementally. It is important to note that the effect of shading two cells in the same sub-string would be similar to shading one cell in the same sub-string, however effect of shading two cells in two different sub-strings is much more severe.

To understand the effect of shading cells in all three sub-strings of the module, cells A1, C1 and F1 were shaded incrementally. In this case, unlike other cases, the fill factor remains the same, however the $I_{sc}$ shows considerable deterioration. This happens because when cells in all three sub-strings are shaded uniformly, the current output in all sub-strings of the module is reduced, no bypass diodes are turned On. It is interesting to note that the $P_{max}$ for shading two cells in different sub-strings (C1,F1) by 50% and $P_{max}$ for shading three cells in different sub-strings (A1,C1,F1) by 50% are very similar.

<table>
<thead>
<tr>
<th>Shading</th>
<th>Sub-</th>
<th>$P_{max}$ (W)</th>
<th>$V_{oc}$ (V)</th>
<th>$I_{sc}$ (A)</th>
<th>$V_{m}$ (V)</th>
<th>$I_{m}$(A)</th>
<th>FF</th>
</tr>
</thead>
</table>

Table 4 Effect of shading configurations on module performance parameters
<table>
<thead>
<tr>
<th></th>
<th>strings shaded</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Unshaded</td>
<td>None</td>
<td>215.24</td>
<td>36.74</td>
<td>8.29</td>
<td>28.03</td>
<td>7.67</td>
</tr>
<tr>
<td>A1_10%</td>
<td>1</td>
<td>214.6</td>
<td>36.74</td>
<td>8.32</td>
<td>27.98</td>
<td>7.66</td>
</tr>
<tr>
<td>A1_15%</td>
<td>1</td>
<td>212.42</td>
<td>36.73</td>
<td>8.32</td>
<td>28.64</td>
<td>7.41</td>
</tr>
<tr>
<td>A1_20%</td>
<td>1</td>
<td>207.87</td>
<td>36.73</td>
<td>8.33</td>
<td>29.52</td>
<td>7.03</td>
</tr>
<tr>
<td>A1_50%</td>
<td>1</td>
<td>152.68</td>
<td>36.74</td>
<td>8.33</td>
<td>32.45</td>
<td>4.70</td>
</tr>
<tr>
<td>A1_100%</td>
<td>1</td>
<td>140.61</td>
<td>36.66</td>
<td>8.30</td>
<td>18.26</td>
<td>7.70</td>
</tr>
<tr>
<td>C1F1_10%</td>
<td>2</td>
<td>213.82</td>
<td>36.73</td>
<td>8.26</td>
<td>28.01</td>
<td>7.63</td>
</tr>
<tr>
<td>C1F1_50%</td>
<td>2</td>
<td>147.76</td>
<td>36.74</td>
<td>8.20</td>
<td>32.49</td>
<td>4.54</td>
</tr>
<tr>
<td>C1F1_100%</td>
<td>2</td>
<td>64.25</td>
<td>36.55</td>
<td>8.19</td>
<td>8.47</td>
<td>7.58</td>
</tr>
<tr>
<td>A1C1F1_10%</td>
<td>3</td>
<td>213.27</td>
<td>36.75</td>
<td>8.10</td>
<td>28.027</td>
<td>7.60</td>
</tr>
<tr>
<td>A1C1F1_50%</td>
<td>3</td>
<td>145.46</td>
<td>36.70</td>
<td>4.96</td>
<td>32.45</td>
<td>4.48</td>
</tr>
</tbody>
</table>
Figure 28 I-V curve when cell A1 is shaded incrementally

Figure 29 I-V curve when cell combinations C1F1 and A1C1F1 are shaded incrementally


### 4.6.4 Effect of failed diodes on I-V curve

Whenever the bypass diodes in the PV module fail, its effect can be seen on the I-V curve under shading. In order to understand the effect of shorted bypass diodes on the I-V curve, "middle" diode in the module was shorted. Table 5 shows the measured module performance parameters under various shading scenarios. Figure 30 shows the I-V curves. Even when the module was not shaded, one third of the module power is lost as the shorted diode has taken out the sub-string of cells from circuit. The power reduction is mainly as a result of reduction in open circuit voltage. It can be seen that when cell C1 which is part of the sub-string corresponding to the shorted bypass diode is shaded, there is no measurable change in any of the performance parameters. However, when cell A1 is shaded, the bypass diode corresponding to that sub-string turns On, and expected bump in the I-V curve is seen. This also shows that it is possible to detect shorted bypass diodes in field by simply measuring the Voc of the module, and in case of shorted bypass diodes for commercial 60-cell c-Si modules, the Voc reduced by one-third per shorted diode.
Figure 30 I-V curves under sequential shading with middle diode shorted

Table 5 Module performance parameters under various shading scenarios

<table>
<thead>
<tr>
<th>Shading</th>
<th>Sub-strings shaded</th>
<th>$P_{\text{max}}$ (W)</th>
<th>$V_{\text{oc}}$ (V)</th>
<th>$I_{\text{sc}}$ (A)</th>
<th>$V_{\text{m}}$ (V)</th>
<th>$I_{\text{m}}$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unshaded_Middle_Shorted</td>
<td>None</td>
<td>142.80</td>
<td>24.57</td>
<td>8.36</td>
<td>18.53</td>
<td>7.70</td>
</tr>
<tr>
<td>C1_50%_Middle_Shorted</td>
<td>1 (sub-string corresponding to shorted diode)</td>
<td>142.70</td>
<td>24.56</td>
<td>8.34</td>
<td>18.55</td>
<td>7.69</td>
</tr>
<tr>
<td>A1_50%_Middle_Shorted</td>
<td>1</td>
<td>101.59</td>
<td>24.54</td>
<td>8.36</td>
<td>21.60</td>
<td>4.70</td>
</tr>
</tbody>
</table>

In order to understand the effect of open circuited diode on the I-V curve, the “Right” diode was open circuited and cells A1 and F1 were 50% shaded in separate experiments. Figure 31 shows the I-V curves for both cases. The diode corresponding to the sub-string of cells containing cell F1 was functional, and therefore, shading cell F1 resulted in the familiar bump in the I-V curve. However, when cell A1 was shaded, the current could not be bypassed through the diode as the bypass diode corresponding to this sub-string was open circuited. In this case, the cell A1 itself is
momentarily forced into extreme reverse bias as the entire voltage generated by the module gets applied across this cell. This has resulted in a peculiar bump in the I-V curve, which is seen to be less steep as compared to the bump associated with bypass diode switching. Table 6 shows the module performance parameters for this case. Note that the short circuit current of the module remained unchanged as the current was forced through the cell in reverse bias. This creates difficulty in the identification of open circuited diodes. Since this was a momentary I-V sweep, cell did not suffer permanent damage.

![I-V curves when right diode is open and single cells are shaded 50%](image)

Figure 31 I-V curves when right diode is open and single cells are shaded 50%

Table 6 Module performance parameters for open circuited bypass diode scenario

<table>
<thead>
<tr>
<th>Shading</th>
<th>Sub-strings shaded</th>
<th>$P_{\text{max}}$ (W)</th>
<th>$V_{\text{oc}}$ (V)</th>
<th>$I_{\text{sc}}$ (A)</th>
<th>$V_m$ (V)</th>
<th>$I_m$ (A)</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1_50%<em>Right</em></td>
<td>1 (sub-string corresponding to open)</td>
<td>150.93</td>
<td>36.73</td>
<td>8.17</td>
<td>32.61</td>
<td>4.62</td>
<td>0.50</td>
</tr>
</tbody>
</table>
### 4.7 Predicting I-V curve of a module under any shading scenario

It is clear from the discussion in section 4.6 that the current passing through the bypass diode under any shading scenario is dependent on the load across the PV module. Therefore, if I-V curve of the PV module under any random scenario could be constructed, the current passing through the diode in best case, worst case and any intermediate scenario, depending on the load could be predicted.

#### 4.7.1 Generalized framework for quantifying shading

It was shown from the field survey of shaded modules that shading could come in numerous forms, shapes and durations. Therefore, a need for a mechanism to quantify the effect of shading was underlined. Based on the results of experiments in section 4.6 and field results, a generalized framework for quantifying effect of any type of shading on the module was created. A parameter called cell mismatch factor (M) for cell i, which is similar to shade impact factor (SIF) described in the literature (Delin, 2009) is defined as follow:

$$M_i = \frac{A_{si}}{A_{celli}} \left(1 - \frac{L_{si}}{L_{ui}}\right)$$  \hspace{1cm} (11)

Where $A_{si}$ is the area of the shaded portion of the cell, $A_{celli}$ is the total area of the cell i, $L_{si}$ is the intensity of light received by shaded portion of the cell, $L_{ui}$ is the intensity of light received by...
the unshaded portion of the cell. Moreover, Area Factor \(A_{fi}\) and Intensity Factor \(L_{fi}\) of cell i are defined as follow:

\[
A_{fi} = \frac{A_{si}}{A_{cell i}} 
\]

\[
L_{fi} = \frac{L_{si}}{L_{ui}}
\]

Therefore, the simplified equation for the mismatch factor of the shaded cell would be:

\[
M_i = A_{fi} \left(1 - L_{fi}\right)
\]

The total current generated by the shaded cell i \(I_i\) is given by following equation:

\[
I_i = (1 - M_i) \times (I_{ui})
\]

Where \(I_{ui}\) is the current generated by the same cell under unshaded conditions. Since cells in the sub-strings are connected in series, the current is dominated by the cell carrying lowest current. Also, in the presence of bypass diodes, the reverse voltage applied across the cells is limited to 12 V – 14 V, which is not sufficient to cause large amount of reverse leakage current to flow.
Therefore, the current generated by the shaded cell can be calculated using equation 15. However, the actual current passing through the sub-string of cells is equal to the lowest current generated by any shaded cell. The current through the shaded sub-string of cells in the presence of bypass diodes is calculated using following equation:

\[ I_{sub-string} = (1 - M_{max}) \times (I_{u,sub-string}) \]

(16)

Where \( M_{max} \) is the maximum mismatch factor for any shaded cell in the same sub-string. \( I_{u,sub-string} \) is the current generated by the sub-string in the unshaded condition. It was observed that on a sunny afternoon, for most shading configurations and types, the current generated by the shaded portion of the cell was 4-8 times less than the current generated by unshaded portion. Therefore, under simplified assumption, the intensity factor can be assumed to be zero, and the mismatch factor in that case is dependent on the area factor alone. Area factors for various shaded cells can be calculated from the geometric configuration of the shading. Similar procedure can be used to calculate the current generated by any other shaded sub-string.

4.7.2 Linear superposition based model for predicting I-V curve

Several approaches have been discussed in the literature for calculating the maximum power output and the I-V curve of the module under shading. Many of these approaches rely on solving complex differential equations, and as the complexity of the system increases, so does the time required for accurate solution. Moreover, some approaches also require values such as shunt and series resistance of the shaded and unshaded cells, which could be tricky to compute or measure. The most reliable and easy to acquire characteristic of a PV module, cell or a bypass diode is the
I-V curve measured under conditions of interest. Therefore, a computationally fast and reliable approach based on linear superposition of the I-V curves was developed for predicting the I-V curve of the PV module under any shading scenario. The key inputs are I-V curve of the module measured under unshaded conditions, I-V curve of the diode and the mismatch factors associated with the shading scenario for each cell.

This approach is described using an example from the field. An outdoor deployed 36 cell module, with two sub-strings of 18 cells connected in series was used for this study. The module had one bypass diode per sub-string of 18 cells. One of the cells in a sub-string was shaded 50% and outdoor I-V curve was measured before and after shading. I-V curve of the bypass diode was obtained from the datasheet. The mismatch factor for 50% shading of one cell was calculated to be 0.5. “Nominal” I-V curve of an unshaded cell was obtained by dividing the voltage values from the I-V curve of the unshaded module by the number of cells (36).

\[ V_{cell,nominal} = \frac{1}{36} \times V_{module,unshaded} \]  

(17)

The I-V curve of the shaded cell was calculated from the current of unshaded cell and mismatch factor:

\[ I_{cell,shaded} = (1 - M) \times I_{cell,unshaded} \]  

(18)

The shaded cell limits the current through the sub-string of cells connected in series. I-V curve of the shaded sub-string of cells alone (without bypass diode) was calculated by using the current
values of shaded cell and the voltage values were obtained by liner addition of voltages for each cell for corresponding value of current. Similar procedure of linear superposition was used to calculate the effective I-V curve in the presence of bypass diodes. Figure 32 shows the comparison between the outdoor measured I-V curve and the predicted I-V curve under shading by the proposed model. It can be seen that the predicted curve is very close to the experimentally measured one. This model is being further developed to include effect of temperature dependence of reverse leakage current in cells.

![Measured I-V](image1)

![Calculated I-V](image2)

Figure 32 Comparison of measured and calculated IV under shading

### 4.7.3 Worst case shading scenario

Based on the discussion in the previous sections, it is clear that short circuiting the module has highest chances of passing largest amount of current through the bypass diode under partial shading. Also, as the percentage of cell shading increases, the current through the bypass diode also increases. Therefore, as far as the bypass diode is concerned, the worst-case shading scenario is the one in which at least one cell in a sub-string is completely shaded, therefore, the current generated by the other unshaded sub-strings within the module passes through the bypass
diode. This is also the case when highest power dissipation will take place in the diode, and has highest potential to increase the diode temperature. Therefore, onwards, in this dissertation, worst case shading scenario is considered, unless otherwise stated. This means that whenever a module is given with a particular short circuit current, it will be assumed that the entire short circuit current generated by the module passes through the bypass diode in worst case shading scenario. The definition of worst case shading changes depending on the context. For cells, the shading configuration that results in highest temperature rise will be termed as worst case shading, and it is occurs when approximately 50% of the cell is shaded. However, this is not the focus of this dissertation.
CHAPTER 5 CALCULATING DIODE TEMPERATURE IN FIELD

5.1 Methods for calculating junction temperature of diode

Under normal operation, bypass diodes in PV modules are reverse biased. Since reverse leakage current is not sufficient to cause any significant power dissipation, the diode experiences negligible self-heating. Therefore, the diode junction temperature is approximately equal to the module temperature, under thermal equilibrium. Whenever a PV module is partially shaded, the bypass diodes get forward biased. This increases the power dissipation in the diodes as the current generated by the module is now passing through the diode. It is important to ensure that under worst-case conditions, the diode temperature does not exceed the maximum rated junction temperature of the diode. Most commercially available bypass diode are rated for a maximum junction temperature of 200 °C in forward bias. Various methods for measuring/calculating diode junction temperature along with their advantages and limitations are discussed in this section.

5.1.1 Forward Voltage - Junction Temperature \( (V_f-T_J) \) method

For a given constant value of forward current, the forward voltage of the Schottky diodes reduces linearly as the temperature is increased. The slope of the \( V_f-T_J \) line is defined as the temperature coefficient of forward voltage at given value of current \( (\alpha_v) \). The \( V_f-T_J \) curves were generated from the datasheet values of the seven diodes discussed in section 4.3. A straight line was fitted through the data points using linear regression. The values of \( \alpha_v \) and \( R^2 \) of the linear fit for a forward current of 10 A are shown in the Table 7. For diode A1, values of forward voltage were available only at two temperatures, therefore, the \( R^2 \) is by default equal to 1. Figure 33 illustrates the linear fit along with the data points for diode C1.
Table 7 αv and R^2 of the linear fit between V_f and T_J for a forward current of 10 A

<table>
<thead>
<tr>
<th>Diode</th>
<th>Temperature Coefficient of V_f</th>
<th>Equation for V_f</th>
<th>R^2</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>0.0009557</td>
<td>0.4761072 - 0.0009557 x T_J(A1)</td>
<td>1*</td>
</tr>
<tr>
<td>A2</td>
<td>0.0009238</td>
<td>0.4387991 - 0.0009238 x T_J(A2)</td>
<td>1*</td>
</tr>
<tr>
<td>A3</td>
<td>0.0008776</td>
<td>0.4901903 - 0.0008776 x T_J(A3)</td>
<td>1*</td>
</tr>
<tr>
<td>B1</td>
<td>0.0007633</td>
<td>0.4844733 - 0.0007633 x T_J(B1)</td>
<td>0.98</td>
</tr>
<tr>
<td>B2</td>
<td>0.0009908</td>
<td>0.580839 - 0.0009908 x T_J(B2)</td>
<td>0.94</td>
</tr>
<tr>
<td>C1</td>
<td>0.0009382</td>
<td>0.5037273 - 0.0009382 x T_J(C1)</td>
<td>0.99</td>
</tr>
<tr>
<td>C2</td>
<td>0.0009538</td>
<td>0.5783652 - 0.0009538 x T_J(C2)</td>
<td>0.99</td>
</tr>
</tbody>
</table>

Figure 33 Linear fit along with the data points for diode C1

From the high values of R^2 it is clear that there is excellent empirical linear relationship between forward voltage and junction temperature of the diodes, in the temperature range of interest. Therefore, this method can be used to calculate the temperature when the forward voltage is known. The advantage of this method is that it can be applied for junction temperature measurement in real time, non-equilibrium conditions as well. This is because, for constant current, the forward voltage is only determined by junction temperature, and measurement of
voltage can provide real time information about the junction temperature. Also, in many applications, it’s more convenient, accurate and reproducible to solder wires at the diode for voltage measurement than it is to attach thermocouples to the case or to the lead. $V_f$-$T_J$ method is especially suitable for thermal characterization of diodes in the laboratory setting, and it has been shown to be more accurate and reliable than the other methods (Uchida & Konishi, 2012).

However, higher accuracy comes at significantly higher cost. For accurate characterization of $V_f$ over wide range of temperatures, it is necessary to have following equipment: (i) power electronics equipment capable of passing high currents (~10A) through the diode for extremely short duration (few milliseconds) in order to minimize errors caused by self-heating of the diode. (ii) fast oscilloscopes capable of measuring low forward voltages at high currents (iii) oven with considerable temperature uniformity. Since the oven needs to be heated and stabilized before measurements could be made, this process becomes very time consuming if measurement needs to be taken at large number of temperature values. Therefore, accurate $V_f$-$T_J$ characterization could only be performed for certain values of currents that are of interest. Also, it is impractical to use this method on large number of diodes in order to get statistically significant results. Another important drawback of this method is that is difficult to apply this method for measuring the temperature of diodes in field deployed modules, due to continuously changing current through the diode. The forward voltage in that case is determined by the current as well as temperature, and it is difficult to deconvolute the contributions from change in current and change in temperature. Often, it is not possible to make a direct measurement of current passing through the diode, and it could only be estimated based on the irradiance values. The errors
associated with this approach also reflect in errors in estimation of current through the diode, and therefore, the junction temperature.

Despite of these limitations, $V_{f}-T_J$ method is preferred method for performing characterization of selected diode samples in the lab, whenever resources are available. More importantly, this method can be used on the data from diode datasheets in order to calculate the $V_{f}-T_J$ coefficients as shown in Table 7.

5.1.2 Case/Lead temperature ($T_{case}$) method

In this method, a temperature measuring sensor, usually a thermocouple is attached to the diode case or lead. Temperature is recorded when the condition of thermal equilibrium is reached. Under thermal equilibrium, the temperatures of junction and the diode case/lead are stabilized, and following Equation 19 is used for calculating the junction temperature from the case temperature.

$$T_J = T_{case} + R_{j-c} \times P_f$$  \hspace{1cm} (19)

Where $R_{j-c}$ is the thermal resistance between diode junction and case, $T_{case}$ is the case temperature, and $P_f$ is the power dissipation in the diode under forward bias, at thermal equilibrium. Table 8 shows the thermal resistance values given in the diode datasheets. It can be seen that most manufacturers provide typical or maximum values, and they are not very different for different diodes. The advantages of this method are that it is quick, economical and negligible technical know-how is required on part of the operator. Therefore, it is preferred method for
diode junction temperature measurement in the industry/test labs. This method could also be very useful for monitoring the diode case temperature in the field deployed modules under sunny conditions. It has been proven later in this chapter that under sunny conditions, the current through the diode changes sufficiently slowly as the day progresses, therefore, maintaining a state of quasi-thermal equilibrium, and the $T_{\text{case}}$ method can be used for estimating the diode junction temperature.

Table 8 Thermal resistance from junction to lead/case for diodes under consideration

<table>
<thead>
<tr>
<th>Diode</th>
<th>Thermal Resistance Definition</th>
<th>Value of Thermal Resistance (K/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Junction-lead</td>
<td>&lt; 4</td>
</tr>
<tr>
<td>A2</td>
<td>Junction-lead</td>
<td>&lt; 2.5</td>
</tr>
<tr>
<td>A3</td>
<td>Junction-lead</td>
<td>&lt; 2.5</td>
</tr>
<tr>
<td>B1</td>
<td>Junction-case</td>
<td>&lt; 2.2</td>
</tr>
<tr>
<td>B2</td>
<td>Junction-case</td>
<td>&lt; 1.5</td>
</tr>
<tr>
<td>C1</td>
<td>Junction-lead</td>
<td>~ 2.5</td>
</tr>
<tr>
<td>C2</td>
<td>Junction-lead</td>
<td>~ 3.5</td>
</tr>
</tbody>
</table>

The downside of $T_{\text{case}}$ method is that is shown to be relatively inaccurate (Uchida, Konishi, & Okura, 2013). The values of thermal resistance given in the diode datasheet are only useful when the diode and the thermocouple are mounted in a very specific configuration, and large errors can be introduced if it is not performed properly. Also, this method can’t be used for real-time thermal characterization of the die as it takes considerable amount of time for changes in junction temperature to reflect in changes in case temperature. This means $T_{\text{case}}$ method can be used only in case of thermal equilibrium.
5.2 Analysis of thermal properties of the diode-junction box system

5.2.1 One-dimensional thermal model
Junction boxes provide the bypass diodes with protection against environmental parameters such as moisture and water, and they also provide electrical insulation from the bypass diodes the surroundings. Junction boxes also provide a thermal path from diode case/lead to the surroundings. Thermal properties of the junction box play a crucial role in determining the junction temperature of the bypass diodes installed in them. Figure 34 shows a one-dimensional conduction based thermal model of the bypass diode-junction box system. Different paths for the heat to flow from the diode junction to the ambient are identified.

Figure 34 One-dimensional conduction based thermal model of the bypass diode-junction box system

Usually, the diode thermal resistance from junction to case (Rth(j-case)) is provided in the manufacturer’s datasheets. Therefore, the path highlighted in Red in Figure 34 is of interest. The thermocouple is attached to the case of the diode to measure diode case temperature while another thermocouple measures the ambient temperature. Considering linearity of the system, we have following equations that describe the system:
Where $R_{th(j-amb)}$ is the thermal resistance from junction to ambient, while $R_{th(case-amb)}$ is thermal resistance from case to ambient. Characterization of the $R_{th(j-amb)}$ over wide junction temperature range is necessary to truly understand the thermal properties of the diode-junction box system.

Once values of $R_{th(j-amb)}$ are profiled, it becomes possible to look at the same system from different standpoint. Junction box can be considered as a heat dissipating component in the system. Therefore, the heat taken out by the junction box is given by following equation 21:

$$P_{cooling} = \frac{T_j - T_{amb}}{R_{th(j-amb)}}$$

(23)

Where $P_{cooling}$ is the amount of power dissipated by the junction box, or maximum amount of heat that can be taken out by the junction box at a given junction temperature.
5.2.2 Estimating diode operating point in forward bias

When a diode is forward biased with constant current, its temperature begins to increase as the power dissipated in the diode is more than the heat that could be taken out by the junction box. As the temperature increases, the forward voltage reduces linearly, and therefore, the power dissipation also reduces linearly. On the other hand, as the junction temperature increases, the cooling power of the junction box according to equation 23 also increases. The diode reaches thermal equilibrium when the power dissipated in the diode becomes equal to the cooling power, that is, the power taken out by the junction box. This is also called the operating point of the diode in the forward bias, for given forward current and ambient temperature.

The short circuit current of the state of the art silicon PV modules is presently between 9 A to 10 A. Therefore, in order to calculate the worst case scenario for each diode, it will be assumed that the diode is being considered for installation in the module with short circuit current equal to 10 A. This also means that whenever unspecified, the diode forward current will be assumed to be 10 A in the calculations. The ambient temperature will be assumed to be 75 °C, which is based on the ambient temperature during the bypass diode test in IEC 61215. Figure 35 illustrates the operating point estimation procedure for bypass diode A2. The Y axis shows the power dissipation (black line) as well as cooling capacity for three values of Rth(j-amb) as a function of junction temperature. The values of the Rth(j-amb) for cooling curves were chosen to represent the wide spectrum of junction boxes available. As per the definition, the operating point is obtained by the intersection of the forward power dissipation line and the cooling curves for each value of the thermal resistance.
Similar procedure was carried out to calculate the operating point for each diode, for three cooling curves. Figure 36 shows the distribution of operating temperature calculated at $I_f = 10$ A and $T_{amb} = 75$ °C for all diodes, for each cooling curve. In Figure 36, for a given diode, the points highest in temperature are for highest thermal resistance values (40 K/W), the lowest points are for lowest thermal resistance values (20 K/W), while the middle points are for thermal resistance equal to 30 K/W.

Figure 35 Operating point estimation procedure for bypass diode A2
It can be concluded that the thermal resistance has profound impact on determining the diode operating point under given conditions of forward current and ambient temperature. In addition to the thermal resistance, the diode forward voltage determines the operating point. Diodes with higher forward voltages tend to have higher operating points for the same thermal resistance. Therefore, such diodes would need to be installed in junction boxes with lower thermal resistance.

5.3 Measuring thermal resistance of junction boxes

5.3.1 Experimental setup
In this section, the attributes of the junction box, that determine the thermal resistance are discussed. From Equation 19, it is clear that in ideal linear scenario, the thermal resistance would be independent of the junction temperature, forward current, ambient temperature and power dissipation in the diode. Therefore, in ideal case, other than the $R_{th(j-case)}$, no other property of
the diode would influence the measurement of Rth(j-amb). In order to test this hypothesis, an experiment was conducted on nine different types of junction boxes in which Rth(j-amb) was measured at various forward currents and ambient temperatures. These junction boxes were chosen to represent a wide range of products available in the market and were named as JB1, JB2..JB9. These junction boxes were connected in series and attached to the back of a module. Since center diode is usually the hottest among three diodes, thermocouples were attached to the center diode in all junction boxes and wires were soldered to the center diodes for measurement of the forward voltage. The junction box lids were closed and the gaps through which the wires came out were sealed with a putty. The module, with junction boxes attached to it, was placed in the environmental chamber. Table 9 shows the number of diodes, their connection and unique properties of each junction box. Figure 37 shows the images of the junction boxes attached to the back of the module. This figure also gives a relative idea of the volumes of different junction boxes. Figure 38 shows the images of these junction boxes with the lid opened.
Figure 37 Junction boxes attached to the back of the module

Figure 38 Types of junction boxes used in the experiment
Table 9 Properties of each junction box under test

<table>
<thead>
<tr>
<th>Junction Box</th>
<th>Diodes</th>
<th>Current Rating</th>
<th>Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>JB1</td>
<td>3</td>
<td>9 A</td>
<td>High volume</td>
</tr>
<tr>
<td>JB2</td>
<td>3 pairs in series</td>
<td>16 A</td>
<td>High volume, metallic heat sink, diode redundancy</td>
</tr>
<tr>
<td>JB3</td>
<td>3</td>
<td>14 A</td>
<td>High volume, metallic heat sink</td>
</tr>
<tr>
<td>JB4</td>
<td>3</td>
<td>9 A</td>
<td>Low volume, large flat heat sink</td>
</tr>
<tr>
<td>JB5</td>
<td>3</td>
<td>8.5 A</td>
<td>Medium volume</td>
</tr>
<tr>
<td>JB6</td>
<td>3</td>
<td>-</td>
<td>Medium volume</td>
</tr>
<tr>
<td>JB7</td>
<td>3</td>
<td>13 A*</td>
<td>Low volume, surface mount diodes on heat sink, No pottant used</td>
</tr>
<tr>
<td>JB8</td>
<td>2</td>
<td>-</td>
<td>High volume, surface mount diodes on a PCB</td>
</tr>
<tr>
<td>JB9</td>
<td>3</td>
<td>13 A*</td>
<td>Low volume, surface mount diodes on heat sink, Pottant used</td>
</tr>
</tbody>
</table>

It should be noted that the current rating for junction boxes is not based on any well-defined test standard, and it is known to vary significantly from one manufacturer to the other. Therefore, current rating should be considered as a qualitative specification rather than quantitative. In this study, junction boxes with current rating close to at least 10 A were selected. Large volume junction boxes are generally air cooled, while small volume junction boxes rely on a larger heat sink and/or junction box pottant for heat dissipation. JB7 and JB9 were same type of box, except that junction box pottant was put in JB9 and not in JB7 for comparative study.

5.3.2 Full characterization of JB1
The experiment was carried out to measure the thermal resistance of the junction boxes at various values of forward currents (6, 8, 10, 12 A) and ambient temperatures 25 °C, 75 °C, 90 °C. The case temperature along with the forward voltage of the center diode was monitored as the module was placed in environmental chamber. The case study of the JB1 is discussed as an illustrative example. The thermal resistance of the diode in the JB1 between junction to case is 103
recorded from the datasheet (3.5 K/W). The diode junction temperature was calculated from $R_{th(j-case)}$ and the power dissipation in the diode. Then, using the junction temperature, ambient temperature and power dissipation values, the $R_{th(j-amb)}$ was calculated at thermal equilibrium for various values of forward currents and ambient temperatures. Figure 39 shows the $R_{th(j-amb)}$ for JB1.

![Figure 39 Experimental characterization of $R_{th(j-amb)}$ for JB1](image)

$R_{th(j-amb)}$ was found to be between 27 K/W to 35 K/W, and it was found to vary significantly with $T_J$ and $T_{amb}$ (Narendra Shiradkar, 2015). This indicates that assumption of constant $R_{th(j-amb)}$ of the one-dimensional thermal model is only approximately true and full thermal characterization of the junction box is necessary in order to determine thermal resistance as a function of temperature. One of the reasons for inaccuracies of the one-dimensional model is that it is only based on thermal conduction. At higher temperatures, heat dissipation by radiation becomes significant, and it is not accounted for, by the one-dimensional thermal model. One
possible solution to this issue is to perform complex Finite Element Method simulation involving distributed thermal model and accounting for conduction, convection and radiation. However, this approach seems to be of diminishing returns due to several reasons. The junction box interior designs are significantly complicated and continuously changing. The length of the module leads and backsheet also play a significant role in determining the thermal mass of the system. Also, time and resources required for this approach make it of little practical value to the PV industry. Instead, following simpler solutions are found to be more valuable considering their adaptation by the industry: (i) Standardize the measurement conditions for thermal resistance to eliminate the source of variation (ii) Consider the extreme values of thermal resistance in order to simulate worst-case and best-case scenarios.

5.3.3 Standardization of the thermal resistance measurement conditions
It was shown in previous section that the $R_{th(j\text{-amb})}$ was found to vary with forward current and ambient temperature. Standardization of the measurement conditions would provide a uniform foundation for comparison of thermal properties of various junction boxes. In line with the reasoning presented earlier in this dissertation, the standard forward current is proposed to be 10 A. There are two options for ambient temperature: 25 °C and 75 °C. The 25 °C option is near room temperature, and makes the measurement easier and more economical. The 75 °C option has ambient temperature same as the bypass diode test, and it is more representative of the module temperature in field. However, any of these ambient temperatures is capable of differentiating different thermal designs of the junction box. For example, Figure 40 shows the thermal resistance of JB1 and JB2 measured at 25 °C, and 10 A of forward current. Both of these junction boxes have high volume and are air cooled. The only difference being JB2 has a higher amount
of metal used as heat sink than JB1. This has resulted in much lower thermal resistance of JB2 (22 K/W) as compared to JB1 (33 K/W). Figure 41 shows comparison between thermal resistances of JB7 and JB9. These are same types of junction boxes, the only difference being JB9 was filled with pottant while JB7 was not. The addition of junction box pottant reduces the thermal resistance from 35 K/W to 25 K/W because pottant has better heat dissipation properties than the air. Since the thermal resistances of JB2 (large volume, with heat sink) and JB9 (small volume with pottant) are comparable, it can be concluded that it is possible to reduce the size of the junction box without compromising thermal properties if one uses junction box pottant.

![Figure 40 Comparison of thermal resistance of JB1 and JB2 (Better heat sink)](image-url)
5.4 Outdoor measurements of diode temperature and thermal resistance

The ultimate aim of any laboratory experiment or accelerated test is to predict what happens in the field. Field experiment was performed on a rooftop in Florida in order to verify the utility of the thermal resistance model discussed in earlier sections. A junction box of type JB1 was attached to the back of a field deployed module mounted on a rooftop installation. The electrical connections were made in such a way that the junction box was connected as a load across the module terminals. Since the junction box only had three bypass diodes in series, it offered negligible voltage drop and therefore, the current passing through the junction box could be assumed to be approximately equal to the short circuit current of the module. The module was first characterized on the flash I-V setup in the lab by measuring the short circuit current at various intensities. Figure 42 shows the graph between the module short circuit current on Y axis and irradiance on X axis. Since the relationship is almost perfectly linear, a regression fit was
calculated to predict the module short circuit current at STC based on the solar irradiance values.

Equation 22 is the relationship based on regression.

\[ \text{Short Circuit Current}_{STC}(A) = 0.0034035 + 0.0082831 \times \text{Irradiance} \left( \frac{W}{m^2} \right) \]  

(24)

However, this equation does not take into consideration the temperature dependence of the short circuit current. The typical value of thermal coefficient of short circuit current is +0.06%/°C. Following equation is used to calculate the Isc of the module at module temperature.
Following parameters were measured at every 5 second interval on a sunny day in Florida: Solar irradiance using a pyranometer, ambient temperature by putting the temperature sensor beneath the module, current passing through the diodes by putting a shunt resistor in series, case temperature of the diode by attached thermocouple and forward voltage drop across the diode.

Figure 43 shows the irradiance, ambient temperature below the module (T_{amb}) and the current passing through the diode on a sunny afternoon.

\[ Isc (A) = Isc_{STC} (1 + 0.0006 \times (T_{module} - 25)) \]

(25)

The diode junction temperature was calculated by considering the value of R_{th(j-case)} to be 3.5 K/W from the diode datasheet. Figure 44 shows the variation of the diode junction temperature.
and forward voltage over this time interval. The regions of non-equilibrium where the diode is heating up, and quasi-thermal equilibrium where the diode has reached a state of quasi-thermal equilibrium are identified.

Figure 44 Outdoor measured diode junction temperature (left) and forward voltage (right) indicating regions of non-equilibrium and quasi-thermal equilibrium.

The thermal resistance from junction to ambient (Rth(j-amb)) is plotted in Figure 45 with respect to time. It is seen that in the region of quasi-thermal equilibrium, the value of Rth(j-amb) remains approximately constant and it is within the range predicted by the experiments performed in environmental chamber during full characterization experiment.
Figure 45 Outdoor measured $R_{th(j-amb)}$ for JB, the value in quasi-thermal equilibrium is close to 35 K/W

Since the process of predicting diode junction temperature from known thermal resistance ($R_{th(j-amb)}$) is exactly opposite of this process, this shows that the information obtained during full thermal characterization of junction boxes along with the one-dimensional thermal model could be used to predict the diode temperature in field provided the certain assumptions are met and the environmental data is available.

5.5 Modeling of diode temperature in field

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Narendra Shiradkar, Vivek Gade, Eric Schneller and Kalpathy Sundaram, “Revising the Bypass Diode Thermal Test in IEC 61215 Standard to Accommodate Effects of Climatic Conditions and
In this section, in order to effectively illustrate the diode temperature calculations, 30 K/W was chosen to be typical value for $R_{th(j-amb)}$ for junction boxes in field. However, it should be noted that the relative nature of final results are independent of the absolute value of $R_{th(j-amb)}$ because the temperature of all diodes is similarly affected by the thermal resistance. The module package considered in this study is standard glass/cell/polymer backsheet. For fixed tilt systems, yearly energy production is typically maximized when the modules are mounted at latitude tilt. Therefore, large amount of PV modules in the field are mounted at latitude tilt. Hence in this study, the rack and roof mount modules are assumed to be mounted at latitude tilt. The Typical Meteorological Year (TMY) data of three locations in the US representing three distinct climatic zones: Denver to simulate temperate, Miami to simulate hot and humid and Phoenix to simulate hot and dry climates was used in this study. The TMY data contains hourly data for various meteorological parameters such as ambient temperature, irradiance, wind speed which are representative of certain time/day of the year at that location. TMY data file contains the Direct Normal Irradiance (DNI) and Diffuse Horizontal Irradiance (DHI) values. The total irradiance incident on a module at fixed tilt is given by sum of the direct and diffuse radiation incident on it. Equations 27 and 28 respectively are used to calculate diffuse and direct irradiance incident on the module from DNI and DHI values.
Total Irradiance = Direct Irradiance + Diffuse Irradiance

\[ \text{Total Irradiance} = \text{Direct Irradiance} + \text{Diffuse Irradiance} \] (26)

\[ \text{Diffuse Irradiance} = DHI \times \left( \frac{180 - \beta}{180} \right) \] (27)

Direct Irradiance
\[ = DNI \times (\sin \delta \sin \phi \sin \beta - \sin \delta \cos \phi \sin \beta \cos \gamma \]
\[ + \cos \delta \cos \phi \cos \beta \cos \text{HRA} + \cos \delta \sin \phi \sin \beta \cos \gamma \cos \text{HRA} \]
\[ + \cos \delta \sin \gamma \sin \text{HRA} \sin \beta) \] (28)

Where, \( \delta \) is the Declination Angle, \( \phi \) is the latitude of the location, \( \beta \) is module tilt, \( \gamma \) is module azimuth (orientation measured from South to West), and HRA is hour angle.

Using TMY data and the Sandia model, module temperatures for two mounting configurations and three climatic zones were calculated on hourly basis for a period of one typical meteorological year. For bypass diodes in the junction boxes of field deployed modules, the module temperature can be considered as ‘ambient temperature’ experienced by the diodes. The module temperature was calculated using Sandia model for rack mount (open rack) and roof mount (insulated back) configurations. The form of Sandia model is given in following equation (D.L. King, 2004):

\[ T_{\text{Module}} = T.I. \times \exp(a + b \times WS) + T_{\text{amb}} \] (29)

Where \( T_{\text{Module}} \) is the module temperature, T.I. is the total irradiance on the module, WS is wind speed, \( T_{\text{amb}} \) is the ambient temperature and \( a \) and \( b \) are constants.
The diode temperature not only depends on the module temperature but it is also a strong function of the current flowing through the diode, which is essentially the short circuit current of the module in worst case condition. In practical applications with power optimizers in place, the maximum current flowing through the diode is the current at maximum power point of the PV module. This occurs when one cell in that sub-string is completely shaded. In this study, a typical commercially available high efficiency PV module with a short circuit current of 9.29 A at STC and maximum power current of 8.85 A at STC is considered. Standard Test Condition (STC) for PV modules corresponds to module temperature of 25 °C and irradiance of 1000 W/m². For a diode in a junction box in a field deployed module, the diode temperature in thermal equilibrium is given by following equation:

\[ T_J = T_{\text{Module}} + R_{\text{th(j-amb)}} \times I_f \times V_f \]  

(30)

Where \( R_{\text{th(j-amb)}} = 30 \text{ K/W} \), \( I_f \) is current flowing through the diode and \( V_f \) is stabilized forward voltage under thermal equilibrium. For simplicity, in the following paragraphs of this section, following transformations are used: \( T \) for \( T_J \), \( I \) for \( I_f \), A for \( A_x A^* \), \( R_{J,A} \) for \( R_{\text{th(j-amb)}} \) and \( R_s \) for series resistance. Considering the effects of series resistance, \( V_f \) is given by following equation:

\[
V_f = \frac{kT}{q} \log \left( \frac{I}{A \times T^2 \times \exp \left( \frac{-q\varphi}{kT} \right)} \right) + I \times R_s
\]

(31)

Combining Equations 30 and 31, we have following equation:
For the diodes analyzed in this study, the diode constants and series resistance were determined from the electrical data given in the diode manufacturer’s datasheets. The Equation 32 was solved numerically using MATLAB solver to calculate the diode junction temperature in field.

\[
T - T_{Module} = \frac{kT \times I \cdot R_{j-A}}{q} \log \left( \frac{I}{A \times T^2 \times \exp \left( \frac{-q \phi}{kT} \right)} \right) + I^2 \times R_s \times R_{j-A} = 0
\]  

(32)

5.6 Results for diode temperature in field

Figure 46 shows the module temperature calculated using Equation 29 for three climatic zones and rackmount configuration. It is immediately obvious that the temperature distribution profiles vary significantly with the climatic zones. Denver has highest spread of temperatures; Phoenix has highest absolute module temperatures while Miami has somewhat lower temperatures as well as lower spread. Even though Miami is recognized for hot and humid climate, large number of hourly data points in TMY data with cloudy skies can result in overall lower module temperatures. Since module temperatures hardly reach 75 °C, the choice of 75 °C ambient temperature during bypass diode test has been a good choice.

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Figure 46 Distribution of module temperatures during TMY under rackmount configuration for (a) Denver (b) Miami (c) Phoenix

Figure 47 shows the module temperatures for three climatic zones and roofmount configuration. It is clear that the module spends significant amount of time at temperatures greater than 75 °C in hot and dry climate of Phoenix. Even in other two climatic zones, the maximum module temperature is greater than 75 °C. Therefore, it may be concluded that for modules to be installed in roofmount configurations, 75 °C ambient temperature during bypass diode test is not sufficient to simulate the typical maximum field temperature for the diode. A publication by the
The diode temperatures in field were calculated using Equation 32 and using the module temperature data for three climatic zones and two mounting configurations. Similar trends were observed in the diode temperatures of all bypass diodes, while the absolute values of the
temperatures being only different. In order to focus only on the values diode temperatures in forward bias, only daytime data where irradiance assumed non-zero values in the TMY data was considered.

Figure 48 Distribution of daytime diode temperatures for diode C1 during TMY under rackmount configuration for (a) Denver (b) Miami (c) Phoenix

Figure 48 shows the distribution of daytime diode temperature for diode C1 for rackmount configuration at the three locations of interest. All the temperature distributions have unique shapes, depending upon the climate of deployment. At Denver, there are two peaks in the
distribution, one at lower temperatures while one at higher. Miami only has a peak at lower temperature, while Phoenix has a large peak at higher temperature. This indicates that the diode spends significant time at high temperatures in Phoenix, while it spends significant time at medium as well as low temperatures in Denver. From the absolute values of temperatures, it can be seen that the diode can be the hottest component within a defect/hotspot-free PV module.

Figure 49 shows the daytime diode temperature distributions for roofmount configuration for diode C1 for three climatic zones. The general shapes of the distributions are similar to those found for the rackmount configuration, however, the absolute values of the temperatures are higher. In fact the maximum diode temperature at Phoenix reaches close to 200 ºC for short time, which is typically the maximum rated temperature for PV bypass diodes.
5.7 Significance of diode field temperatures

The diode field temperature data is useful to assess the field stressors experienced by the diodes in their service life as a function of mounting configuration and the environmental conditions. Whenever actual meteorological data with more resolution in terms of time is available, it should be used instead of TMY data for improved accuracy of predictions. Ability to calculate diode field temperatures opens up various possibilities such as assessing the amount of stress induced by accelerated tests such as bypass diode test, extended bypass diode test, predicting the diode
lifetime in field whenever failure mechanisms and their activation energies are known and designing diodes/junction boxes tailored for specific climates and mounting configurations.
CHAPTER 6   THERMAL RUNAWAY IN BYPASS DIODES

6.1 Introduction to thermal runaway

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Bypass diodes in PV modules can undergo thermal runaway in forward to reverse transition when the partial shading on the module is suddenly removed. As it was mentioned earlier, currently, there is no test in the IEC standard for determining vulnerability of bypass diodes for thermal runaway. Author has developed a framework for estimating the vulnerability of bypass diodes for thermal runaway from the measured electrical characteristics or from the data given in the diode manufacturer’s datasheets (Shiradkar, Schneller, Dhere, & Gade, 2014). This framework, its applications and limitations will be described in this section. Figure 50 illustrates the phenomenon of thermal runaway from experimentally measured diode case temperatures.
Figure 50 (a) Forward-reverse transition does not cause thermal runaway (b) phenomenon of thermal runaway is observed with ever increasing temperature of the diode

Figure 51 shows the X-ray image of a diode failed by thermal runaway in a laboratory experiment. Heavy metals appear darker in X-ray image while lighter elements like silicon from the die and carbon from the epoxy packaging appear transparent. It can be seen that high temperatures led to diffusion of metal into the silicon die, thus resulting in short-circuit failure.
6.2 Estimating the temperature dependence of reverse characteristics of bypass diodes
The data required for the framework is the temperature dependent forward and reverse characteristics of the diode. In chapter 5, temperature dependence of the forward characteristics was discussed. In this section, the process of estimating reverse power dissipation in the diode as a function of temperature is described. Unless otherwise specified, a representative reverse voltage is assumed to be 12 V in this chapter.

Diode manufacturer's datasheet has information about the reverse current ($I_r$) as a function of reverse voltage at various diode junction temperatures. The values of $I_r$ at various temperatures from the datasheet are extracted. Regression fit is obtained between the logarithm of $I_r$ and the junction temperature. The reverse current of a Schottky diode as a function of junction temperature, at fixed reverse voltage is given by following equation:
\[ I_r = AA^* T^2 e^{\left(-\frac{q\varphi}{kT}\right)} \]  

Where

\( AA^* = \text{constant}, \ K = \text{Boltzman constant}, \ q = \text{charge of electron}, \ \varphi = \text{Schottky barrier height}. \)

Taking logarithm on both sides, we have:

\[ \log \left( \frac{I_r(T)}{T^2} \right) = -\left(\frac{q\varphi}{K}\right) \times \left(\frac{1}{T}\right) + \log(AA^*) \]  

Coefficients of the above equation are obtained from the slope and the intercept of the regression fit. Slope is used to estimate the Schottky barrier height while the value of the constant \( AA^* \) is calculated from the intercept. Once these constants are estimated, the temperature dependence of the reverse current in the Schottky diode can be predicted at given reverse voltage. This process was performed for all 7 diodes discussed in chapter 4 and the power dissipation in reverse bias as a function of temperature was calculated.

### 6.3 Condition for thermal runaway

Figure 52 illustrates the conditions under which a bypass diode undergoes thermal runaway in forward to reverse transition.
Figure 52 Illustration of the phenomenon of thermal runaway

The Y axis has power dissipation in forward & reverse bias along with the cooling capacity of the junction box as a function of junction temperature. There are junction boxes with two thermal resistance under consideration. In both cases, as the diode is forward biased, the power dissipation in the diode is more than the heat that can be taken out by the junction box, and therefore, the diode temperature begins to increase. This happens till the heat taken out by the junction box equals to the power dissipation in the diode, and thermal equilibrium is reached. In first case, there is a junction box with low thermal resistance (blue line). In this case, the operating point \( T_{op} \) in forward bias is point A. When the diode returns to reverse bias, the power dissipation in reverse bias is less than the maximum heat that can be taken out by junction box. Therefore, the diode temperature begins to decrease, and there is no thermal runaway.
However, in case of junction box with high thermal resistance (black line), the operating point is B, and when the diode returns to reverse bias, the power dissipation in reverse bias is greater than the heat taken out by the junction box at that temperature. This cases the diode temperature to increase, and the diode reverse current exponentially increases with increased temperature. This cyclic process results in uncontrolled increase in diode temperature and thermal runaway results. Points A* and B* are the points where the cooling curves intersect the diode reverse power curve. Whenever the operating temperature during forward-reverse transition in each case goes past point A* and B* respectively, thermal runaway results. The temperature at which the cooling curve intersects the reverse power curve of the diode is termed as thermal runaway critical temperature ($T_c$). Therefore, whenever the diode junction temperature during forward to reverse transition exceeds the critical temperature ($T_{op} > T_c$), thermal runaway results. With this definition of critical temperature, we have a situation where the critical temperature depends on the thermal resistance of the junction box. The point of intersection between the forward power and reverse power curves is termed at crossover temperature ($T_{cross}$). It should be noted that in the Figure 52, we have either of the following relationship between these three temperatures:

Point A: $T_{op} < T_{cross} < T_c$

(35)

Or
Considering the mathematical nature of the curves (reverse power curve being exponential, and forward power and cooling curves being linear), it can be proved that either of the following relationships will always exist between \( T_{op} \), \( T_{cross} \) and \( T_c \):

\[
T_{op} \leq T_{cross} \leq T_c
\]  

(37)

Or

\[
T_{op} \geq T_{cross} \geq T_c
\]  

(38)

That means, \( T_{cross} \) will always lie between \( T_{op} \) and \( T_c \). In other words, just by comparing \( T_{op} \) and \( T_{cross} \), it is possible to determine the relationship between \( T_{op} \) and \( T_c \). The advantage of using \( T_{cross} \) is that it is only dependent on the diode, and is independent of the junction box being used. Therefore, when the PV engineer is designing an appropriate diode/junction box system for the PV module, he will be able to decouple the choice of diode from the thermal resistance of the junction box. Again, from the nature of the curves, if the thermal resistance is gradually increased (from blue line to black line), there will be a point where the points \( T_{op} \), \( T_{cross} \) and \( T_c \) will coincide. The thermal resistance measured at this point is the maximum thermal resistance that can be used under given conditions of ambient temperature and forward current, before the diode undergoes thermal runaway.
Figure 53 illustrates these scenarios with a real life example of diode A3. The assumption is that the forward current is 10 A, reverse voltage is 12 V and the ambient temperature is 75 °C. Along with the forward and reverse power dissipation curves, the cooling curves are plotted for three values of $R_{th(j-amb)}$: 20 K/W, 30 K/W and 40 K/W.

![Graph showing cooling curves for diode A3](image)

Figure 53 $T_{op}$, $T_{cross}$ and $T_c$ for diode A3 for thermal resistances of 20 K/W, 30 K/W and 40 K/W.

Table 10 shows the $T_{op}$, $T_{cross}$ and $T_c$ for diode A3 for thermal resistances of 20 K/W, 30 K/W and 40 K/W in a tabulated form.
Table 10 $T_{op}$, $T_{cross}$ and $T_c$ from Figure 53 in tabulated form

<table>
<thead>
<tr>
<th>$R_{th(j-amb)}$</th>
<th>$T_{op}$</th>
<th>$T_{cross}$</th>
<th>$T_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>143</td>
<td>171</td>
<td>188</td>
</tr>
<tr>
<td>30</td>
<td>170</td>
<td>171</td>
<td>172</td>
</tr>
<tr>
<td>40</td>
<td>193</td>
<td>171</td>
<td>161</td>
</tr>
</tbody>
</table>

It is seen that with $R_{th(j-amb)}$ of 20 K/W, the $T_{op}$ is significantly less than $T_{cross}$ and $T_c$, therefore, the diode does not undergo thermal runaway. The system maybe over-designed, and there could be scope for increasing the thermal resistance (hence cost reduction) without risking thermal runaway. For $R_{th(j-amb)}$ of 40 K/W, the $T_{op}$ is significantly greater than the $T_{cross}$ and $T_c$, therefore, the diode definitely undergoes thermal runaway and the system needs to be redesigned with lower thermal resistance to avoid thermal runaway. For $R_{th(j-amb)}$ of 30 K/W, we almost have a limiting situation where $T_{op}$, $T_{cross}$ and $T_c$ are very close to each other. Even this system needs to be re-designed so as to operate the diode sufficiently in the safe zone.

### 6.4 Comparative susceptibility of diodes for thermal runaway

Similar analysis was performed on all 7 diodes under this study. Table 11 has all the results complied. The cases in red text indicate the combinations in which the diode is susceptible for thermal runaway. It can be seen that whenever the $T_c$ is greater than 200 °C, for any value of thermal resistance under consideration, diodes are not susceptible for thermal runaway. Also, the diodes A1 and A2, with higher leakage currents are susceptible for thermal runaway for thermal resistances of 30 K/W and beyond.
Table 11 Comparative assessment of susceptibility to undergo thermal runaway

<table>
<thead>
<tr>
<th>Diode</th>
<th>Rth(j-amb) (K/W)</th>
<th>$T_{op}$ (C)</th>
<th>$T_{cross}$ (C)</th>
<th>$T_c$ (C)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A1</strong></td>
<td>20</td>
<td>148</td>
<td>157</td>
<td>162</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>176</td>
<td>157</td>
<td>149</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>201</td>
<td>157</td>
<td>140</td>
</tr>
<tr>
<td><strong>A2</strong></td>
<td>20</td>
<td>138</td>
<td>140</td>
<td>141</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>162</td>
<td>140</td>
<td>129</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>183</td>
<td>140</td>
<td>120</td>
</tr>
<tr>
<td><strong>A3</strong></td>
<td>20</td>
<td>143</td>
<td>171</td>
<td>188</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>170</td>
<td>171</td>
<td>172</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>193</td>
<td>171</td>
<td>161</td>
</tr>
<tr>
<td><strong>B1</strong></td>
<td>20</td>
<td>150</td>
<td>187</td>
<td>203</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>180</td>
<td>187</td>
<td>189</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>206</td>
<td>187</td>
<td>180</td>
</tr>
<tr>
<td><strong>B2</strong></td>
<td>20</td>
<td>160</td>
<td>225</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>193</td>
<td>225</td>
<td>236</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>221</td>
<td>225</td>
<td>226</td>
</tr>
<tr>
<td><strong>C1</strong></td>
<td>20</td>
<td>148</td>
<td>219</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>177</td>
<td>219</td>
<td>236</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>202</td>
<td>219</td>
<td>226</td>
</tr>
<tr>
<td><strong>C2</strong></td>
<td>20</td>
<td>161</td>
<td>230</td>
<td>$&gt;250$</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>194</td>
<td>230</td>
<td>241</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>222</td>
<td>230</td>
<td>232</td>
</tr>
</tbody>
</table>

6.5 Tests for assessing the vulnerability of diodes for thermal runaway

It should be noted that the analysis in previous section was based on ideal scenario where exact values of $T_c$ and $T_{op}$ could be known. In reality these values can only be estimated. Therefore, a more practical approach that considers the errors and tolerances associated with measurements is discussed in this section.

Recently, a thermal runaway test has been proposed as a pass/fail test to assess the vulnerability of bypass diodes for thermal runaway (Uchida, 2014). This test uses current $= 1.25 \times I_{sc}$, ambient temperature of 90 °C and the reverse voltage = open circuit voltage generated by sub-string of
cells. However, this test needs significant resources, time and expertise on behalf of the operator. Also, this test does not have any predictive capabilities. Therefore, in order to provide a suitable alternative, an approach to assess the vulnerability of bypass diodes from bypass diode thermal test and the framework to predict thermal runaway is presented.

Bypass diodes in PV modules can undergo thermal runaway in forward bias to reverse bias transition when partial shading on the PV module is suddenly removed. A combination of two tests described here can be used to determine and quantify the susceptibility of bypass diode(s) in a junction box towards thermal runaway. The Test A is used to identify samples where the diode is obviously susceptible or is clearly not susceptible to undergo thermal runaway. The Test A employs a theoretical framework provided the diode manufacturer's datasheet and the diode junction temperature data from bypass diode test as described in IEC 61215 are available. On the other hand, the Test B is used whenever Test A is inconclusive. The Test B uses an experimental setup as described in the thermal runaway test draft (Uchida, 2014). This document describes cases, where depending on the sample properties, Test A or both tests A and B need to be used to determine the susceptibility of bypass diodes to undergo thermal runaway.

Following terms are defined for this purpose:

**Sample:** Diode in a junction box

**DUT:** Diode/Device under test

**I_{sc}:** Short circuit current of the PV module in which the diode and junction box are installed.

**V_r:** Open circuit voltage of the sub-string of cells connected across the bypass diode under test.

**V_f:** Voltage drop across the diode in forward bias
**Iₐ:** Current passing through the diode in forward bias.

**Iᵣ:** Current passing through the diode in reverse bias.

**Tₗ:** Junction temperature of the diode, assumed in Kelvin unless otherwise specified.

**Forward-reverse crossover temperature (Tᵣoss):** For a fixed forward current and reverse voltage, the crossover temperature is a temperature at which power dissipation in a diode in forward bias with a given forward current equals power dissipation in reverse bias with given reverse voltage.

**Estimated crossover temperature (Tᵣossₐst):** It is the value of critical temperature calculated by following procedure described in Test A.

**Lower limit crossover temperature (Tᵣossₐ):** It is lower bound on the actual critical temperature of the diode. It has also been defined as Tᵣossₐ = Tᵣossₐst – 10 °C

**Higher limit crossover temperature (Tᵣossₜ):** It is higher bound on the actual critical temperature of the diode. It has also been defined as Tᵣossₜ = Tᵣossₐst + 10 °C.

**Operating junction temperature during forward bias to reverse bias transition (Tₒp):** Is defined as the junction temperature when the diode undergoes transition from forward bias to reverse bias.

**Tₗ (1.25Iₛₗₜ,75 °C):** It is maximum diode junction temperature observed during the bypass diode test carried out according to IEC 61215 (at Iᵢ= 1.25xIₛₗ, Tᵣₐ₅mb = 75 °C)

**Estimated operating temperature (Tₒpₐst):** It is the operating junction temperature (at If=1.25xIₛₗ, Tᵣₐmb= 90 °C), estimated from the maximum diode junction temperature Tₗ (1.25Iₛₗₜ,75 °C) observed in the bypass diode test carried out according to IEC 61215 at Iᵢ=1.25xIₛₗ and Tᵣₐmb=75 °C.
Following equation is used to calculate $T_{opEst}$:

$$T_{opEst} = T_f(1.25I_{sc}, 75 \, ^\circ C) + 15 \, ^\circ C$$

(39)

$T_{opH}$: This is the higher limit on the actual operating junction temperature for a diode in given junction box (at $I_i=1.25I_{sc}$, $T_{amb}=90 \, ^\circ C$).

By definition, $T_{opEst} = T_{opH}$

$T_{opL}$: This is the lower limit on the actual operating junction temperature for a diode in given junction box (at $I_i=1.25I_{sc}$, $T_{amb}=90 \, ^\circ C$).

By definition, $T_{opL} = T_{opEst} - 10 \, ^\circ C$

The procedure to determine susceptibility of a bypass diode in a junction box towards thermal runaway is described in the flowchart shown in Figure 54. The cases, depending on sample properties, that require utilization of Test A or Test B are elucidated in Figure 55. In the Figure 54, $T_{crossEst}$ is written as $T_{cEst}$ due to limited availability of space.
Figure 54 Process flowchart to determine susceptibility of diodes to thermal runaway $T_{cEst}$ in the figure is actually estimated crossover temperature ($T_{crossEst}$)
Figure 55 Elucidation of various cases depending on the sample properties and appropriate tests (A/B) to be used for each case. $T_{cH}/T_{cL}/T_{cEst}$ correspond to $T_{crossH}/T_{crossL}/T_{crossEst}$ respectively.

Test A

1. Estimate thermal runaway forward-reverse crossover temperature ($T_{cross}$) from diode manufacturer's datasheet using procedure described in Appendix 1 for a forward current equal to $1.25 \times I_{sc}$ and reverse voltage equal to the open circuit voltage generated by the sub-string of cells that will get applied across the bypass diode ($V_r$).
2. Carry out the bypass diode test as described in IEC 61215 with forward current equal to 1.25xI_{sc}, ambient temperature of 75 °C and for duration of one hour. Record the maximum diode junction temperature at the end of the test T_J(1.25I_{sc}, 75 °C).

3. Calculate the estimated operating temperature (T_{opEst}) at I_f=1.25xI_{sc} and T_{amb}=90 °C using Equation 30.

3. Compare the T_{opEst} and T_{cEst} to follow one of the three possible cases:

**Case: 1** T_{opEst} < T_{cEst} - 10 °C

--> Diode is NOT susceptible for thermal runaway.

**Case: 2** T_{cEst} - 10 °C < T_{opEst} < T_{cEst} + 20 °C

--> Test A is inconclusive. Carry out Test B to determine susceptibility of diode for thermal runaway.

**Case: 3** T_{opEst} > T_{cEst} + 20 °C

--> Diode is susceptible for thermal runaway.

**Test B**

Perform the thermal runaway test proposed by Uchida. This test involves passing forward current equal to 1.25xI_{sc} through the diodes for one hour and application of reverse voltage across the middle diode equal to the open circuit voltage of the corresponding sub-string of cells. The diode fails the test if it undergoes thermal runaway.
6.6 Justification for the tolerance values for crossover temperature

$T_{\text{cross}}$ for thermal runaway can be estimated from the manufacturer’s datasheets by procedure described earlier in this dissertation. However, the actual $T_{\text{cross}}$ could be slightly different than the estimated critical temperature due to following reasons:

1) Electrical properties of the DUT could be slightly different than those given in manufacturer’s datasheet.

2) The diode reverse current shows deviations from Schottky diode model.

An algorithm to calculate lower and higher bounds on actual $T_{\text{cross}}$ based on the above mentioned sources of error is described below:

1) Value for manufacturing tolerance is defined to be $\pm M\%$ for forward and reverse current for a given voltage. For this calculation, $M=5$ is assumed.

2) Worst case deviation in reverse current data from the Schottky model is obtained from datasheet and following procedure described earlier in this dissertation. It is termed as $S\%$. It was seen that reverse current given in datasheet was greater than the value predicted by the Schottky model for every diode, but to a variable degree. Therefore, the Schottky model error factor $S\geq0$.

3) A combination of lower reverse power and higher forward power as a function of temperature result in higher $T_{\text{cross}}$. While a combination of higher reverse power and lower forward power as a function of temperature result in lower $T_{\text{cross}}$. This information is used to appropriately select signs of $M$ and $S$ to obtain lower and higher bounds on $T_{\text{cross}}$. 

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4) Calculation of lower bound on critical temperature ($T_{\text{cross}L}$): The forward and reverse currents are transformed according to following equations and $T_{\text{cross}L}$ is calculated.

$$I_f \rightarrow I_f \times (100 - M)/100 \tag{40}$$

$$I_r = I_r \times (100 + M) \times (100 + S)/100 \tag{41}$$

5) Calculation of higher bound on crossover temperature ($T_{\text{cross}H}$): The forward and reverse currents are transformed according to following equations and $T_{\text{cross}H}$ is calculated.

$$I_f \rightarrow I_f \times (100 + M)/100 \tag{42}$$

$$I_r \rightarrow I_r \times (100 - M)/100 \tag{43}$$

This procedure was repeated on three representative bypass diodes- Diode L, Diode M and Diode H that had low, medium and high estimated crossover temperature ($T_{\text{cross}\text{Est}}$) respectively. These diodes were chosen in such a way that they would represent full spectrum of typical Schottky diodes available in market. They varied widely not only in their critical temperatures but also in the deviation displayed from the Schottky model. Table 12 shows the values of various tolerances and $T_{\text{cross}L}$, $T_{\text{cross}\text{Est}}$ and $T_{\text{cross}H}$ for these diodes.
Table 12 Lower and higher bounds on crossover temperatures of three representative bypass diodes along with tolerances used to obtain these limiting values on crossover temperature.

<table>
<thead>
<tr>
<th>Diode- Temperature</th>
<th>Temperature (°C)</th>
<th>Manufacturing Tolerance (M%)</th>
<th>Deviation from Schottky Model (S%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Forward Current</td>
<td>Reverse Current</td>
</tr>
<tr>
<td>Diode L - T(_{\text{crossL}})</td>
<td>134 °C</td>
<td>-5%</td>
<td>5%</td>
</tr>
<tr>
<td>Diode L - T(_{\text{crossEst}})</td>
<td>142 °C</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Diode L - T(_{\text{crossH}})</td>
<td>145 °C</td>
<td>5%</td>
<td>-5%</td>
</tr>
<tr>
<td>Diode M - T(_{\text{crossL}})</td>
<td>166 °C</td>
<td>-5%</td>
<td>5%</td>
</tr>
<tr>
<td>Diode M - T(_{\text{crossEst}})</td>
<td>173 °C</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Diode M - T(_{\text{crossH}})</td>
<td>176 °C</td>
<td>5%</td>
<td>-5%</td>
</tr>
<tr>
<td>Diode H - T(_{\text{crossL}})</td>
<td>223 °C</td>
<td>-5%</td>
<td>5%</td>
</tr>
<tr>
<td>Diode H - T(_{\text{crossEst}})</td>
<td>226 °C</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Diode H - T(_{\text{crossH}})</td>
<td>229 °C</td>
<td>5%</td>
<td>-5%</td>
</tr>
</tbody>
</table>

It is clear from Table 1 that for a 5% manufacturing tolerance, lower bound on crossover temperature (T\(_{\text{crossL}}\)) is within 10 °C of the estimated critical temperature (T\(_{\text{crossEst}}\)). The higher bound on critical temperature (T\(_{\text{crossH}}\)) is actually within 3 °C of the T\(_{\text{crossEst}}\). However, just to be on safer side, the T\(_{\text{crossH}}\) can be taken as T\(_{\text{crossEst}}\) + 10 °C.

6.7 Justification for tolerance values for operating temperature

In this section, justification is provided for the values and tolerances of the lower and upper bounds of operating temperature.

From a thermal conduction equation, we have:
\[ T_j = T_{amb} + I_f \times V_f \times Rth(j - amb) \]  \hspace{1cm} (44)

\[ T_j(1.25Is_c, 90 \text{ C}) = 90 + I_f \times V_{f90} \times Rth(j - amb) \]  \hspace{1cm} (45)

\[ T_j(1.25Is_c, 75 \text{ C}) = 75 + I_f \times V_{f75} \times Rth(j - amb) \]  \hspace{1cm} (46)

\[ T_j(1.25Is_c, 90 \text{ C}) - T_j(1.25Is_c, 75 \text{ C}) = (90 - 75) + I_f \times Rth(j - amb)(V_{f90} - V_{f75}) \]  \hspace{1cm} (47)

Since \( V_{f90} < V_{f75} \), we have

\[ T_j(1.25Is_c, 90 \text{ C}) < T_j(1.25Is_c, 75 \text{ C}) + 15 = T_{opH} = T_{opEst} \]  \hspace{1cm} (48)

For six different samples (bypass diodes in junction boxes), the following Table 13 was generated in order to get a lower bound on \( T_j(1.25Is_c, 90 \text{ C}) \) by surveying the values of quantity \( I_f \times Rth(j-amb) \times (V_{f90} - V_{f75}) \).

**Table 13 Limits of quantity \( I_f \times Rth(j-amb) \times (V_{f90} - V_{f75}) \).**

<table>
<thead>
<tr>
<th>Sample</th>
<th>( Rth(j-a) ) (°K/W)</th>
<th>( I_f \times Rth(j-amb) \times (V_{f90} - V_{f75}) ) (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>22.85</td>
<td>-5.93</td>
</tr>
<tr>
<td>Sample 2</td>
<td>30.25</td>
<td>-7.45</td>
</tr>
<tr>
<td>Sample 3</td>
<td>33.29</td>
<td>-8.68</td>
</tr>
<tr>
<td>Sample 4</td>
<td>22.71</td>
<td>-5.55</td>
</tr>
<tr>
<td>Sample 5</td>
<td>27.70</td>
<td>-6.39</td>
</tr>
<tr>
<td>Sample 6</td>
<td>34.15</td>
<td>-8.45</td>
</tr>
</tbody>
</table>

It is clear from table 13 that one can safely assume minimum value of the term \( I_f \times Rth(j-amb) \times (V_{f90} - V_{f75}) \) to be -10 °C.
CHAPTER 7    WEAR OUT MECHANISMS IN BYPASS DIODES

7.1 Introduction to wear out mechanisms

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In wear out, the properties of the device gradually degrade over time which may lead to hard failure eventually. As pointed out earlier, three possible wear out mechanisms for Silicon Schottky diodes are HTFB, HTRB and TC. Out of which only HTFB and TC are discussed in this dissertation. Failure by HTRB under typical reverse voltages and common operating temperatures would require significant resources in terms of environmental chamber testing time. Therefore, that mechanism was not studied. In principle, interaction between wear out and catastrophic failure mechanisms such as thermal runaway is also possible. For example, gradual deterioration of diode electrical properties by one of the wear out mechanisms may lead to increase in the leakage current, and therefore reduction of the thermal runaway critical temperature for the diode. This may make the diode more vulnerable to thermal runaway.

7.2 High temperature forward bias (HTFB) operation

When a PV module is shaded, bypass diode(s) become forward biased and pass the current generated by the module. Depending on the ambient temperature and current of the module, the
$T_j$ could reach very high values close to 200 °C. Diodes in PV systems that experience regular shading have to operate at elevated temperatures for significant duration. HTFB operation can cause diffusion of metals and degradation in PN junction which can lead to increased leakage current over time. In order to simulate the HTFB operation, extended bypass diode test was proposed in the Qualification Plus standard (Sarah Kurtz, 2013). This test involves passing current equal to $I_{sc}$ of the module through the diodes for 96 hours followed by passing current equal to 1.25 x $I_{sc}$ for one hour. The diode passes the test if it is operational at the end of the test. This test was selected to simulate the HTFB failure mode in bypass diodes installed in nine different types of junction boxes earlier described in section 5.3. The junction boxes were chosen to span a wide range of thermal resistances. The forward voltage of the diodes were measured using a multimeter diode test functionality. Figure 56 shows the diode case temperatures and the module temperature measured during the test. The irregularities in one measurement were caused by a broken thermocouple. Mainly due to differences in the thermal resistances of the junction boxes, the diode case temperatures varied from 130 °C to 150 °C. No failures were found after the test. Also, no change in the electrical properties of the diodes was observed. This indicates that the test did not result in measurable degradation of the diodes. One possibility is to make the test harsher by increasing the ambient temperature to 90 °C or increasing the forward current to 1.25 x $I_{sc}$ during the test. Once measurable degradation during such test is observed, Activation Energy data for HTFB mechanism could be used in the Arrhenius model to predict the extent of degradation at any other test conditions. Activation energy data could be available from certain diode manufacturers or it can be used from the relevant JEDEC publications (JEDEC, 2010) or it can be experimentally determined by extensive environmental chamber testing. The
Experimental determination of activation energies would require testing on a large amount of samples for long duration, at harsher conditions in order to obtain statistically relevant data.

![Diode case temperatures for center diodes in nine junction boxes and module temperature measured during HTFB test](image)

**Figure 56** Diode case temperatures for center diodes in nine junction boxes and module temperature measured during HTFB test. (Shiradkar et al., 2015)

With the framework to predict diode temperature in field, it would be in principle possible to determine field equivalent of any accelerated test for HTFB once the failure mechanisms is known. Currently there is no published data for the failure distribution of silicon Schottky diodes under HTFB. Traditionally, Arrhenius model with certain activation energy has been used to calculate the acceleration factor with respect to field conditions at each climatic zone when compared with the operating conditions of diode during the extended bypass diode test.
\[ Acceleration\ Factor = \exp \left( \frac{E_A}{k} \times \left( \frac{1}{T_{test}} - \frac{1}{T_{field}} \right) \right) \]  

(49)

Where, \( E_A \) is activation energy, \( k \) is Boltzman constant, \( T_{test} \) is the diode temperature during the extended bypass diode test and \( T_{field} \) is the temperature of the diode in field. Acceleration factors are used to estimate the field equivalent hours at extended bypass diode test operating conditions. However, the applicability of Arrhenius equation to the HTFB mechanism can only be proven after statistically relevant failure / degradation data of the Schottky diodes is made available.

7.3 Thermal cycling

Shading and fluctuations in irradiance can lead to regular current cycling through bypass diodes. Self-heating results in thermal cycling with difference between maximum and minimum junction temperatures defined as \( \Delta T_J \). Bypass diodes under TC could have \( \Delta T_J \) significantly greater than that experienced by the module. Die attach, bond wire contacts and epoxy packaging of the bypass diodes are typically degraded by TC. A revised TC test for the modules in which the current will be passed through the diodes for last 50 cycles is under consideration by PVQAT. Since no detectable degradation was observed in the diodes that underwent extended bypass diode test, it was decided to use the same samples for the revised TC test. The minimum temperature in this test was -40 °C and maximum temperature was the \( T_J \) of the diode at maximum power current (8 A) and 85 °C ambient temperature. Figure 57 shows the diode case temperatures and module temperature during thermal cycling. Depending on the diode, the \( \Delta T_J \) varied from 170 °C to 190 °C. Since the module experienced \( \Delta T_J \) of only 125 °C, it is seen that
the modified TC test indeed stresses the diodes much more than the TC test in IEC 61215 in which the diodes remain reverse biased. However, despite of this, no failures or any noticeable degradation in electrical properties was found at the end of 50 thermal cycles. It is recommended that this test be performed for additional thermal cycles until measurable degradation or failures are seen. Once that happens, it would be possible to use a modified Coffin-Manson equation along with the activation energies for the certain failure mechanisms that are triggered by thermal cycling to estimate the extent of degradation at any other test condition.
Figure 57 Diode case temperatures during thermal cycling vs time in seconds. (Shiradkar et al., 2015)
CHAPTER 8  CONCLUSIONS

PV module warranties need to be substantiated with physics based service life models in order to further reduce the LCOE. Detailed understanding of the catastrophic and wear out failure mechanisms along with their interactions is a first step in the process. Once failure mechanism is known, the module environmental conditions during service life need to be modeled in order to estimate the degradation experienced by PV modules due to that particular failure mechanism in their service life. The next step is to develop appropriate accelerated tests which would induce field-like failures in the laboratory during reasonable timeframe.

Bypass diodes are primary components in PV modules that provide protection against shading. Failure of bypass diodes results in immediate failure of PV module. Thanks to the development of new devices such as diode checker, studies are being published that illustrate the circumstances of field failures of bypass diodes. Various failure mechanisms in bypass diodes were discussed. Procedure to digitize the data from diode datasheets was illustrated with associated error analysis. Partial shading of PV modules was classified into different categories and its effects on diode switching and reliability were discussed. Generalized framework to capture the effect of any shading scenario on the I-V curve of the partially shaded module was discussed. It was shown that a faulty diode could be detected using I-V curves under partial shading and worst case shading scenario for the diodes occurs when one cell in a sub-string of cells is completely shaded.
It was pointed out that there is a lack of framework estimate the diode temperature in field deployed modules. The notion of thermal resistance was developed and various types of junction boxes were characterized in the environmental chamber to measure their thermal resistance. From the outdoor measurements it was shown that the diode remains in quasi-thermal equilibrium condition when operating in forward bias in a field deployed module because the change of module current due to change of irradiance is very slow. This condition is applicable unless rapidly changing cloud cover or dynamic partial shading is encountered. Based on this, a model for calculating diode temperature in field based on environmental data was developed. Histograms of module and diode temperatures at Denver, Miami and Phoenix were generated as representative climates for rack and roof mount configurations.

It was shown that even commercially available didoes could be susceptible for thermal runaway in appropriate environmental conditions and currently there was no test procedure to prevent such diodes from being used in PV modules. A framework to assess the vulnerability of diodes for thermal runaway was developed. New parameter called thermal runaway critical temperature was introduced to predict the susceptibility of diodes for thermal runaway. Using this framework, it is now possible to estimate how far the diode is operating from the thermal runway point and it can be used as a design guideline for choosing appropriate bypass diodes and junction boxes for the modules. An addendum to the bypass diode test was also proposed which could be used to assess the thermal runaway susceptibility of diodes from their performance in the bypass diode test.
Accelerated tests were performed to understand wear out failures by HTFB and TC mechanisms, however, no detectable degradation was found. Therefore, harsher test conditions were recommended to observed any measurable change.

In summary, frameworks for predicting the diode temperature in field and its vulnerability to various failure mechanisms were developed. This framework can be used to predict service life whenever data about diode electrical properties and activation energies for various failure mechanisms is available.

The future work in this area would comprise of following: (i) Performing extensive accelerated testing in environmental chamber to determine the failure distributions and activation energies for HTFB and TC failure mechanisms (ii) Model the service life of the diodes for various climatic zones and mounting configurations using appropriate models for HTFB and TC failure mechanisms. (iii) Perform extensive environmental chamber testing to understand nature of failures observed in HTRB mechanism. (iv) Deploy diodes/junction boxes outdoor with current passing through them and monitor periodically for field failures (v) Develop diode/junction box systems tailored for specific climatic zones and mounting configurations.
LIST OF REFERENCES


UNIRAC. (2012). PV Racking is structural engineering: UNIRAC.


