UHF Frequency Synthesizer

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UHF FREQUENCY SYNTHESIZER

BY

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B.S.E.E., Michigan Technological University, 1980

THESIS

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ABSTRACT

This thesis describes the design, implementation and testing of a UHF frequency synthesizer. The synthesizer is designed to provide a sine wave output programmable from 400 MHz to 500 MHz in 0.1 MHz increments. The synthesis technique utilized is Digital Coherent Indirect Synthesis. This technique uses phase locking to provide a range of stable output frequencies all derived from a single crystal reference. Component design and system level analysis are presented in detail.
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CHAPTER I
INTRODUCTION

Frequency synthesis has evolved over the years from the early direct synthesis techniques to the modern indirect methods. Direct frequency synthesizers are usually comprised of a crystal-controlled oscillator with a bank of crystals switched in. The process is slow and requires an additional crystal for each desired frequency. Indirect synthesis utilizes feedback in a phase-locked loop to provide a range of coherent frequencies from a single stable crystal reference. The phase-locked loop acts as an integral multiplier of the reference source.

A Digital Coherent Indirect Synthesis technique was chosen to design a UHF frequency synthesizer programmable to provide 400 MHz to 500 MHz in 0.1 MHz increments. This technique utilizes a programmable digital divider in the feedback path to adjust the output frequency. Recent advances in ECL and TTL integrated circuits allow the use of digital dividers operating at UHF frequencies. A block diagram of a Digital Coherent Indirect Synthesizer is shown in Figure 1.

The major component in a coherent indirect synthesizer is the voltage-controlled oscillator (VCO). Normally, at UHF frequencies, VCO design is a trial and error type procedure. The majority of the
Figure 1. Digital Coherent Indirect Synthesizer.

- 25 KHz Reference
- Phase Detector
- Programmable $\frac{\text{to}}{4000}$ $\frac{\text{to}}{5000}$
- Prescaler $\div 4$
- Low Pass Filter
- VCO
- $f_{\text{out}}$
design effort takes place in the lab, tuning the circuit to achieve the designed performance. In an attempt to minimize the debugging phase of the VCO design, S-parameter design techniques were used. The S-parameters are very useful in microwave circuit designs because of the measurement accuracy and transistor stability. Often a transistor will oscillate with a short or open circuit at one port, thereby making $\mathbb{V}_{11}$ and $Z_{11}$ meaningless.

This paper describes the component design as well as the system level analysis for the fully programmable coherent UHF frequency synthesizer.
CHAPTER II
PHASE-LOCK LOOP SYSTEM

**PLL Theory**

The heart of a direct, coherent, frequency synthesizer is a phase-locked loop. A block diagram of a PLL is shown in Figure 2.

![Block Diagram of PLL](image)

Figure 2. Phase-Locked Loop.

The phase detector produces a voltage proportional to the phase difference between the signals $\theta_1$ and $\theta_0/N$. This voltage is filtered and used as the control signal for the VCO. Any time variant signal
appearing at the input to the VCO will modulate the output signal. During phase lock, the output frequency is:

\[ f_0 = Nf_i \]  

(1)

The two major parameters in PLLs are the type and order. The type of a system refers to the number of poles of the loop transfer function \( G(s)H(s) \) located at the origin. The order of the system refers to the highest degree of the characteristic equation.

\[ 1 + G(s)H(s) = 0 \]  

(2)

The roots of the characteristic equation are the poles of the closed loop transfer function. For a PLL to track a reference frequency with zero steady-state error, a minimum of type 2 is required (Manassewitsch 1976).

**PLL Design**

A type 2, second order PLL system was chosen as the basis for this frequency synthesizer. The type 2 system allows phase coherence between the two input signals to the phase detector. The additional zero, added to make the system second order, increases stability. The requirements chosen for the PLL were:

- Output Frequency: 400 MHz to 500 MHz
- Frequency Steps: 100 KHz
- Lock-up Time: 10.0 msec
- Overshoot: < 20 %
The transfer functions for the known elements of the PLL are:

**VCO:**

\[
K_v = \frac{100 \text{ MHz}}{1.5 \text{ volt swing from P.D.}} \times 2\pi \text{ rad/s/V}
\]

\[
K_v = 4.19 \times 10^8 \text{ rad/s/V}
\]  \hspace{1cm} (3)

**Phase Detector (Motorola MC 4044):**

\[
K_p = 0.111 \text{ V/rad (Motorola Specifications)}
\]  \hspace{1cm} (4)

**Programmable Dividers:**

\[
N_{\text{min}} = \frac{f_{\text{min}}}{f_{\text{ref}}} = \frac{400 \text{ MHz}}{25 \text{ KHz}} = 16,000
\]  \hspace{1cm} (5)

\[
N_{\text{max}} = \frac{f_{\text{max}}}{f_{\text{ref}}} = \frac{500 \text{ MHz}}{25 \text{ KHz}} = 20,000
\]  \hspace{1cm} (6)

\(N_{\text{max}}\) will be used in loop equation calculations. The loop transfer function for a type 2 system is:

\[
G(s) H(s) = \frac{K_p K_v K_n}{s} \frac{K_f}{s^2} = \frac{K(s + a)}{s^2}
\]  \hspace{1cm} (7)

Therefore, \(K_f\) must be of the form:

\[
K_f = \frac{s + a}{s}
\]  \hspace{1cm} (8)

The circuit shown in Figure 3 gives the desired form for the filter transform function (Egan 1981). The transfer function for the first order active filter is:
Figure 3. Active Filter Design.

The overall loop characteristics can then be determined by proper selection of $R_1$, $R_2$ and $C$. Inserting the equation for $K_f$ into the loop equation yields:

$$G(s)\, H(s) = K_p \left( \frac{R_2}{R_1} \right) \frac{1}{s} \frac{1}{N} \left( \frac{1}{s} \right) \left( \frac{1}{N} \right)$$

and the characteristic equation becomes:

$$s^2 + \frac{K_p \, K_v \, R_2}{R_1 \, N} \, s + \frac{K_p \, K_v}{R_1 \, CN} = 0$$

The standard form of the C.E. is:
\[ s^2 + 2 \xi \omega_n s + \omega_n^2 = 0 \]  \hspace{1cm} (12)

where:

\( \xi = \text{damping coefficient} \)

\( \omega_n = \text{natural radian frequency} \)

Equating like coefficients in equations (11) and (12) gives:

\[ \frac{K_p K_v}{R_1 CN} = \omega_n^2 \]  \hspace{1cm} (13)

and

\[ \frac{K_p K_v R_2}{R_1 N} = 2 \xi \omega_n \]  \hspace{1cm} (14)

\( \omega_n \) can now be determined from percent overshoot and settling time. A damping coefficient of \( \xi = 0.8 \) will allow a peak overshoot of less than 20% and will settle within 5% at \( \omega_n t = 4.5 \) (Gardner 1967). Scaling this to the required lock-up time of 10 msec:

\[ \omega_n = \frac{4.5}{0.01} = 450 \text{ rad/sec} \]  \hspace{1cm} (15)

Solving equation (13) for the unknowns \( R_1 \) and \( C \):

\[ R_1 C = \frac{K_p K_v}{\omega_n^2 N} \]  \hspace{1cm} (16)

\[ R_1 C = \frac{(0.111) (4.19 \times 10^8)}{(450)^2 (20,000)} \]
Choose \( C = 470 \text{ nF} \), then \( R_1 = 24.4 \text{ k}\Omega \) (use standard value 24.9 k\( \Omega \)).

\( R_p \) is the parallel combination of \( R_1 \) and \( R_2 \):

\[
R_p = \frac{24.4 \text{ K} \cdot (7.5 \text{ K})}{(24.4 + 7.5) \text{ K}\Omega} = 5.74 \text{ K}\Omega
\]  

(18)

Use \( R_p = 5.62 \text{ K}\Omega \). A 741 op Amp was chosen for the high gain amplifier in the active filter.

With the loop filter design finished, the phase-lock loop is complete. One final parameter of interest in the PLL is the 3 dB bandwidth of the loop (Manassewitsch 1976).

\[
\text{BW}_{3\text{ dB}} = \frac{2\pi}{\omega_n} \left[ 2\xi^2 + 1 + \sqrt{(2\xi^2 + 1)^2 + 1} \right]^{\frac{1}{2}} \text{ Hz}
\]

(19)

\[
= \frac{450}{2} \left[ 2(0.8)^2 + 1 + \sqrt{(2(0.8)^2 + 1)} \right]^{\frac{1}{2}} \text{ Hz}
\]

\[
= 156.4 \text{ Hz}
\]

**PLL Operation**

The operation of the PLL is best described by an example. Starting from a steady-state condition, suppose the value of \( N \) is increased to achieve a higher output frequency. With \( N \) increased, the signal entering the phase detector is now a lower frequency than
the reference. According to the transfer function of the phase detector, this causes a higher output voltage. The increased voltage causes the VCO output frequency to increase until the two inputs to the phase detector are again the same frequency. While the loop filter blocks all high frequency signals from modulating through the VCO, it also slows the response time of the loop. Lock-up requires several sample intervals, with the divided VCO output getting closer to the reference frequency each time.
CHAPTER III
VOLTAGE CONTROL OSCILLATOR

VCO Design

The accepted method of UHF oscillator design uses a standard "cookbook" model with components scaled to the desired range, and the majority of the time spent in the lab "tweaking" the circuit to achieve the desired performance. This design process leads to unpredictable development time and no guarantee of performance. This paper describes the design of oscillators using much more reliable S-parameter design techniques.

There are three conditions that must be satisfied for oscillation to occur (Vendelin 1982):

1. \( K < 1 \) \hspace{2cm} (20)
2. \( \Gamma_0 S_{11}' = 1 \) \hspace{2cm} (21)
3. \( \Gamma_1 S_{22}' = 1 \) \hspace{2cm} (22)

where \( K \), the stability factor, is defined as:

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11} S_{22} + S_{12} S_{21}|^2}{2 |S_{12}| |S_{21}|} \hspace{2cm} (23)
\]
As seen in Figure 4, \( \Gamma_G \), the reflection coefficient looking back at the generator:

\[
\Gamma_G = \frac{Z_G - Z_0}{Z_G + Z_0}
\]  

(24)

\( \Gamma_L \), the reflection coefficient looking into the load:

\[
\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}
\]  

(25)

\( S_{11}' \), i.e. \( S_{11} \) with the load connected to the transistor:

\[
S_{11}' = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L}
\]  

(26)

and \( S_{22}' \), i.e. \( S_{22} \) with the generator connected to the transistor:

\[
S_{22}' = S_{22} + \frac{S_{12} S_{21} \Gamma_G}{1 - S_{11} \Gamma_G}
\]

It can be seen that the conditions of oscillation are only functions of the S-parameters of the transistor circuit and the impedance of the generator and load. The three oscillation conditions can actually be reduced to two independent conditions. It can be proven that if one port of the device is oscillating, the other port must also be oscillating. Therefore, criteria 2 and 3 are redundant.

Knowing the S-parameters of the transistor, the oscillator design process is reduced to three steps. First, select a transistor
configuration that gives $K < 1$ over the desired frequency range. This criterion can normally be met without additional feedback if the transistor is used in the common-base mode. The next step is to select an output load which gives $|S_{11}'| > 1$ over the frequency range of interest. Since $\Gamma_G \leq 1$, it follows that $|S_{11}'| > 1$ is required as a partial solution to criterion 2. Finally, the input port is resonated with a passive high-Q circuit at the desired frequency, solving criterion 2, $\Gamma_G S_{11}' = 1$. With these conditions met, the device is oscillating at both ports and since the input port is passive, the power is delivered to the output port. For a tunable frequency oscillator, the input resonator can be replaced with a varactor tuning network. As the impedance of the varactor is changed, the oscillation criteria are met at a different frequency.
The oscillation criteria can be met at a desired frequency with a wide range of input and output loads. A FORTRAN program was written as part of this paper to assist in the component selection. The program takes the S-parameters of the transistor and bias circuit, together with a selected realizable load, and determines the input network, if possible, that will solve for the oscillation criteria. For a tunable design, the program takes into account changes in S-parameters and impedances with varying frequency. A good tunable design is one that can meet the desired output frequency range with an input impedance range realizable by a single resonator network. The only factor that is not directly considered in this analysis is parasitic impedances that may show up in the lab. A complete listing of this program is given in Appendix B.

The VCO designed for this project was to have an operating range of 400 to 500 MHz. A Motorola BFW92A transistor was selected because of its high operating frequency and low input and output reactances. The common-base configuration was chosen to assure that oscillation criterion 1, \( K < 1 \), could be met without additional feedback. As is customary, the S-parameters given in the manufacturer specifications are for the common-emitter configuration. An operating point of \( V_{CE} = 10 \) volts and \( I_C = 15 \) mA was chosen because of the high gain-bandwidth product at that point. The CE S-parameters at this point for 500 MHz are (Motorola Data Sheet, BFW92A):
These CE S-parameters can be converted to the desired CB S-parameters using the method described in Appendix A. The resulting CB S-parameters are:

\[
S_{11} = 0.09 \quad @ \quad -137.0^\circ \\
S_{12} = 0.076 \quad @ \quad 71.0^\circ \\
S_{21} = 5.60 \quad @ \quad 87.0^\circ \\
S_{22} = 0.47 \quad @ \quad -21.0^\circ 
\]

These CB S-parameters result in a stability factor of \( K = -0.75 \), well below the required \( K < 1 \) to meet oscillation criterion 1. With condition one already satisfied, the transistor and necessary bias circuit was implemented on a copper board with OSM connectors at the input and output ports. The actual CB S-parameters were then measured, including the effects of the bias circuit and associated parasitics. The CB S-parameters measured on the HP-8507A Network Analyzer were:
These measured parameters agree fairly well with the parameters derived from the manufacturer's specifications. Since this is the transistor circuit in its final form, these parameters can be used with great confidence in designing the complete oscillator. Oscillation criterion 1 is still easily satisfied with a stability factor of $K = -0.35$ using the measured CBS-parameters. All that remains in the design phase is to find a combination of input and output loads to satisfy oscillation Criterion 2 over the 400 to 500 Hz range. After a few runs of the oscillation criteria program described in Appendix B, an easily realizable load combination is discovered. With a series inductance of 50 nH as the output load, the circuit will oscillate at 400 MHz with 15 pF input capacitance and at 500 MHz with 11.4 pF input capacitance. This range of input capacitance can be achieved with a Motorola 1N5441B varactor. According to Motorola specifications, the varactor has a capacitance of 15 pFs with 0.1 volts reverse bias and 11.4 pFs with 0.9 volts reverse bias. With increased reverse bias voltages, the varactor can have a capacitance as small as 5 pFs if required to counteract stray capacitance in the device implementation. The final VCO circuit is shown in Figure 5.
Blocking capacitors are 270pF mica.
RF chokes are 23nH air-core.

Figure 5. Complete VCO Circuit.
VCO Implementation

The VCO circuit designed in the last section using S-parameter techniques was built on two copper-clad boards. The first board, which was already built to measure the CB S-parameters, was modified only by adding the varactor across the input port in place of the OSM connector. The output load was put on a board by itself so the impedance at the desired frequencies could be measured directly on the network analyzer. Board two is a two-port device containing only the output load, a 50 nH inductance. The 50 nH inductance was achieved with the self-inductance of a one-half inch long strip of 22 gauge copper wire. The inductance was measured directly on the network analyzer. The RF was kept out of the dc power supply and the tuning voltage input by 23 nH air core RF chokes.

VCO Testing

Power was applied to the VCO with the output connected to the 50Ω input of the spectrum analyzer. With tuning voltages higher than predicted, the VCO gave the desired performance. The higher voltages are necessary due to the parasitic capacitance present in the boards and components. The parasitics add to the input capacitance requiring less capacitance than predicted from the varactor. Figure 6 shows the VCO output frequency as a function of tuning voltage. The power output of the VCO ranged from 7.2 mW to 12.8 mW over the frequency range.
The performance of the VCO was not completely repeatable from one measurement to the next. The performance seemed to be affected by the dc power supply lines and relative position of adjacent components. The dc supply lines were better isolated from the RF signals by replacing the RF chokes with ferrite beads. At RF frequencies, the ferrite beads provide a high series resistance with very little reactance. The VCO was then isolated from adjacent components by enclosing it in a grounded aluminum chassis. The performance of the modified VCO was then remeasured on the spectrum analyzer. Figure 7 shows the performance of the modified VCO. The power output of the modified VCO ranged from 9.0 mW to 13.4 mW over the frequency range.
The ferrite beads and the aluminum chassis reduced the parasitic capacitance such that a higher output frequency was generated with the same tuning voltage. The performance of the modified VCO was very stable and repeatable. Figures 8 and 9 show the spectrum of the VCO output at the ends of the tuning range. Figure 10 and 11 are time domain pictures of the same signals driving the 50Ω input to the oscilloscope.

Additional circuitry was needed to match the required tuning voltages of the VCO to the error voltage out of the phase detector. The phase detector output swings from 0.75 to 2.25 volts, while the VCO requires 3.5 to 15 volts. The match can be accomplished by an amplification of 8 with a level shift of -2.5 volts. Both the amplification and level shift can be accomplished by the single op amp circuit (Seidman 1983) shown in Figure 12.
Figure 8. VCO Spectrum V\textsubscript{tune} = 3.5 volts.
Figure 9. VCO Spectrum $V_{tune} = 15$ volts.
Figure 10. Time Domain Output, $V_{tune} = 3.5$ volts.
Figure 11. Time Domain Output, \( V_{\text{tune}} = 15 \) volts.
The desired amplification of 8 and level shift of -2.5 volts can be achieved with:

\[
V_0 = \frac{R_1 + R_2}{R_2 || R_3} V_{\text{in}} - \frac{R_1}{R_2 || R_3} \cdot \frac{V_{EE} R_2}{R_2 + R_3}
\]  

(27)

The desired amplification of 8 and level shift of -2.5 volts can be achieved with:

\[R_1 = 10 \, \text{K\Omega}\]
\[R_2 = 1.47 \, \text{K\Omega}\]
\[R_3 = 40 \, \text{K\Omega}\]
\[R_c = 1.27 \, \text{K\Omega}\]
\[V_{EE} = V^- = -10 \, \text{volts}\]
The required reference source was a very stable 25 KHz TTL compatible square wave. The logical choice for the reference is a crystal oscillator. The nearest, whole number multiple of 25 KHz, oscillator available was an 800 KHz source. The 800 KHz was divided down to 25 KHz using two cascaded BCD counters pre-set to divide by 32.

Figure 13. Reference Source Circuit.
CHAPTER V
PHASE DETECTOR

The phase detector of the phase-locked loop was chosen to be a Motorola MC4044 Phase-Frequency Detector. The phase-frequency detector acts as a phase detector during lock and aids acquisition when the loop is out of lock. The chip consists of logic circuitry plus a charge pump. The charge pump is illustrated in Figure 14. Logic circuitry closes $S_2$ to raise the value of $v_3$ or closes $S_1$ to lower it. This type of detector is ideal for a type-2 loop. Type-2 loops have no steady-state phase error; therefore, $S_1$ and $S_2$ never close and no transients are generated. The phase-frequency detector is also superior to other phase detectors because it has a full 720° phase range, compared to the standard 360°.

![Figure 14. Charge Pump.](image-url)
The transfer function of the phase frequency detector is shown in Figure 15. The output of the charge pump must be biased to +1.5 volts to ensure equal positive and negative swings of the output. Figure 16 shows the complete phase-frequency detector circuit layout.

Figure 15. Phase Detector Transfer Function (Motorola Data Sheet MC4044).

Figure 16. Phase Detector Circuit.
CHAPTER VI

FREQUENCY DIVIDER

Design

A frequency synthesizer requires programmable dividers to be placed in the feedback path of the phased-locked loop. As the divisor is changed, the output frequency of the synthesizer is changed. The synthesizer described in this paper requires a divider chain adjustable to divide between 16,000 and 20,000 in increments of 4. The first element in the chain must be an ECL fixed divide by 4 prescaler. This gets the VCO output down to the 125 MHz range where it can be followed by a divider programmable to divide from 4,000 to 5,000 in increments of 1. A programmable divider composed of four cascaded decade counters is difficult to implement at 125 MHz, even using ECL logic. However, a technique exists called "Pulse Swallowing" (Manassewitsch 1976) which allows direct high-frequency division without any sacrifice in resolution. This technique uses only one high-speed integrated circuit, followed by simple divider circuitry operating at one-tenth the speed. The high-speed logic consists of a Motorola MC12013 dual modulus prescaler. The prescaler can be programmed to divide by 10 or 11. The low speed division is performed by four Motorola MC-4016 TTL programmable decade counters. A counter control logic chip is utilized
to detect zero crossings of the MC-4016, control the modulus of the
MC12013, and provide an ECL-TTL interface. Figure 17 shows the circuit
diagram of the "Pulse Swallowing" logic.

The operation of the circuit is as follows. Initially, the three
most significant digits are programmed into counters, three, two and
one, respectively, to form:

\[ N_p = 100 N_{p3} + 10 N_{p2} + N_{p1} \]  \hspace{1cm} (28)

The least significant digit, A, is programmed into counter zero.

When operation begins, counters number three, two and one begin
counting down from \( N_p \). At the same time, counter zero begins counting
down from A. The modulus of the MC12013 is 11 until counter zero
counts down to zero, then the modulus switches to 10 where it remains
until \( N_p \) has reached zero. If the modulus was always 10, the operation
would be:

\[ f_{out} = 10 N_p \cdot f_{ref} \]  \hspace{1cm} (29)

But, by replacing A divide by 10s with A divide by 11s, the operation
is:

\[ f_{out} = [10 (N_p - A) + 11 (A)] \cdot f_{ref} \]
\[ = (10 N_p - 10A + 11A) \cdot f_{ref} \]
\[ = (10 N_p + A) \cdot f_{ref} \]  \hspace{1cm} (30)
Figure 17. Pulse Swallowing Programmable Divider.
Substituting in for $N_p$:

$$f_{out} = (1000 N_p^3 + 100 N_p^2 + 10 N_p + A) \cdot f_{ref} \quad (31)$$

This "pulse swallowing" circuit can provide divisors programmable up to 9999 operating on a 125 MHz signal with the maximum clock rate of the programmable dividers being 12.5 MHz.

**Implementation**

The two ECL prescalers were soldered onto copper boards with OSM input and output connectors. The divide by 4 prescaler board was enclosed in a grounded aluminum chassis due to its high speed and close proximity to the VCO and the other prescaler. All of the TTL circuitry was wired on a single bread board.

The prescalers were tested independently using a sine-wave generator with the outputs driving the 50Ω input to the oscilloscope. The prescalers performed as predicted with only slightly degraded pulse waveforms. The TTL dividers and control logic were then connected to the prescalers and the entire system performed as expected with a well defined pulse output.

The programmable inputs to the dividers were provided by a four-digit, BCD output, thumbwheel switch.
CHAPTER VII
RESULTS AND CONCLUSIONS

The elements that comprise the frequency synthesizer were all tested individually and performed as expected. When the subsystems were initially interconnected, somewhat degraded results were obtained. The lock range was smaller and the VCO noise was greater than was predicted by the operation of the individual components. Good phase lock was achieved over the 515 MHz to 565 MHz range. Figure 18 shows the unfiltered phase detector output while the loop is locked at 540 MHz. The phase detector will only put out a periodic rectangular waveform when the system is in phase lock. The duty cycle of this waveform determines the error voltage.

The spectrum of the output at 515 MHz and 565 MHz are shown in figures 19 and 20, respectively. The frequencies are correct, but the noise has increased over that of the independent VCO. The lock range is also limited by the output noise. As the VCO tunes farther from the center frequency, the noise increases to a point where phase lock is no longer possible.

Upon isolation of the individual components, it was determined that the increased noise was due, at least in part, to interference between the VCO and the dual modulous prescaler. The noise was reduced by shielding the prescaler.
Figure 18. Phase Detector Output While in Lock.
Figure 20. Spectrum of 565 MHz Output.
Future work along these lines could be beneficial to the better understanding of the frequency synthesizer system. Particular emphasis should be placed on packaging and phase noise analysis. Packaging was a major contributor to degraded performance, and phase noise can be critical in a Digital Coherent Indirect Synthesizer.
APPENDICES
APPENDIX A

COMMON-EMITTER TO COMMON-BASE S-PARAMETER CONVERSION
The conversion from common-emitter S-parameters to common-base S-parameters is a three-step process. The first step converts the CE S-parameters to CE h-parameters (Vendelin 1982).

\[ h_{11} = \frac{(1 + S_{11})(1 + S_{22}) - S_{12} S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}} \]

\[ h_{12} = \frac{2 S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}} \]

\[ h_{21} = \frac{-2 S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}} \]

\[ h_{22} = \frac{(1 - S_{22})(1 - S_{11}) - S_{12} S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12} S_{21}} \]

The second step converts the CE h-parameters to CB h-parameters (Casasent 1973).

\[ h_{11} \text{ CB} = \frac{h_{11} \text{ CE}}{(h_{21} \text{ CE} + 1)} \]

\[ h_{12} \text{ CB} = h_{11} \text{ CB} h_{22} \text{ CB} (h_{21} \text{ CE} + 1) - h_{12} \text{ CE} \]
The third and final step converts the CB $h$-parameters to CB $S$-parameters (Vendelin 1982).

\[
S_{11} = \frac{(h_{11} - 1)(h_{22} + 1) - h_{12} h_{21}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}}
\]

\[
S_{12} = \frac{2 h_{12}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}}
\]

\[
S_{21} = \frac{-2 h_{21}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}}
\]

\[
S_{22} = \frac{(1 + h_{11})(1 - h_{22}) + h_{12} h_{21}}{(h_{11} + 1)(h_{22} + 1) - h_{12} h_{21}}
\]

A FORTRAN program was developed, using these equations, to perform the conversion. The program greatly reduces the probability of error which can be quite high due to the fact that all the $S$ and $h$ parameters are complex numbers. The FORTRAN source code is listed on the following pages.
THIS PROGRAM CONVERTS COMMON EMMITTER S-PARAMETERS TO COMMON
BASE S-PARAMETERS.

1) CONVERT CE S-PARAMETERS TO CE H-PARAMETERS
   PAGE 12 "S-PARAMETER BOOK" BY VENDELIN

2) CONVERT CE H-PARAMETERS TO CB H-PARAMETERS
   PAGE 83 "ELECTRONIC CIRCUITS"

3) CONVERT CB H-PARAMETERS TO CB S-PARAMETERS
   PAGE 12 "S-PARAMETER BOOK" BY VENDELIN

COMPLEX S11_CB, S12_CB, S21_CB, S22_CB
COMPLEX S11_CE, S12_CE, S21_CE, S22_CE
COMPLEX H11_CB, H12_CB, H21_CB, H22_CB
COMPLEX H11_CE, H12_CE, H21_CE, H22_CE
COMPLEX Z11_CB, Z12_CB, Z21_CB, Z22_CB
COMPLEX Z11_CE, Z12_CE, Z21_CE, Z22_CE
COMPLEX DENOMINATOR

CHARACTER*20 TRANS
REAL IC
PI = 3.1415926
WRITE(6,*)'ENTER TRANSISTOR NUMBER(NAME).'
READ(5,9) TRANS

9 FORMAT(A20)
WRITE(6,*)'ENTER Vce (volts) and Ic (ma).'
READ (5,*) VCE, IC
WRITE(6,*)'ENTER FREQ IN MHZ.'
READ(5,*) F MHZ
WRITE(6,*)'ENTER MAG(NON-DB) AND PHASE(DEC) OF CE S-PARMS'
WRITE(6,*)'INPUT S11 MAG AND PHASE'
READ(5,*) S11_CE_MAG, S11_CE_PHASE_DEG
WRITE(6,*)'INPUT S12 MAG AND PHASE'
READ(5,*) S12_CE_MAG, S12_CE_PHASE_DEG
WRITE(6,*)'INPUT S21 MAG AND PHASE'
READ(5,*) S21_CE_MAG, S21_CE_PHASE_DEG
WRITE(6,*)'INPUT S22 MAG AND PHASE'
READ(5,*) S22_CE_MAG, S22_CE_PHASE_DEG

OPEN(UNIT=1,NAME='SPARAM',TYPE='NEW')
WRITE(1,*)
WRITE(1,2) TRANSISTOR 'TRANS', VCE = 'VCE', volts'
WRITE(1,2) Ic = 'Ic', ma'
WRITE(1,2) Freq = 'F_MHZ', 'MHz'
WRITE(1,2) CE MAGNITUDE PHASE'
WRITE(1,11) S11_CE_MAG, S11_CE_PHASE_DEG
WRITE(1,12) S12_CE_MAG, S12_CE_PHASE_DEG
WRITE(1,13) S21_CE_MAG, S21_CE_PHASE_DEG
WRITE(1,14) S22_CE_MAG, S22_CE_PHASE_DEG
WRITE(1,2)

11 FORMAT(2X,F8.5,3X,F8.2)
12 FORMAT(2X,F8.5,3X,F8.2)
13 FORMAT(2X,F8.5,3X,F8.2)
14 FORMAT(2X,F8.5,3X,F8.2)
$\text{S11}\_\text{CE\_PHASE} = \text{S11}\_\text{CE\_PHASE\_DEG} \times \pi/180$

$\text{S12}\_\text{CE\_PHASE} = \text{S12}\_\text{CE\_PHASE\_DEG} \times \pi/180$

$\text{S21}\_\text{CE\_PHASE} = \text{S21}\_\text{CE\_PHASE\_DEG} \times \pi/180$

$\text{S22}\_\text{CE\_PHASE} = \text{S22}\_\text{CE\_PHASE\_DEG} \times \pi/180$

$\text{S11\_CE} = \text{S11\_CE\_MAG} \times \text{CMPLX} (\cos (\text{S11\_CE\_PHASE}), \sin (\text{S11\_CE\_PHASE}))$

$\text{S12\_CE} = \text{S12\_CE\_MAG} \times \text{CMPLX} (\cos (\text{S12\_CE\_PHASE}), \sin (\text{S12\_CE\_PHASE}))$

$\text{S21\_CE} = \text{S21\_CE\_MAG} \times \text{CMPLX} (\cos (\text{S21\_CE\_PHASE}), \sin (\text{S21\_CE\_PHASE}))$

$\text{S22\_CE} = \text{S22\_CE\_MAG} \times \text{CMPLX} (\cos (\text{S22\_CE\_PHASE}), \sin (\text{S22\_CE\_PHASE}))$

CALL STABILITY FACTOR ($\text{S11\_CE}$, $\text{S12\_CE}$, $\text{S21\_CE}$, $\text{S22\_CE}$, $\text{CE\_STABILITY}$)

$\text{DENOMINATOR} = (1.0 - \text{S11\_CE}) \times (1.0 - \text{S22\_CE}) - (\text{S12\_CE} \times \text{S21\_CE})$

$\text{H11\_CE} = ((1.0 + \text{S11\_CE}) \times (1.0 + \text{S22\_CE}) - (\text{S12\_CE} \times \text{S21\_CE})) / \text{DENOMINATOR}$

$\text{H21\_CE} = 2.0 \times \text{S21\_CE} / \text{DENOMINATOR}$

$\text{H22\_CE} = ((1.0 - \text{S11\_CE}) \times (1.0 - \text{S22\_CE}) - (\text{S12\_CE} \times \text{S21\_CE})) / \text{DENOMINATOR}$

$\text{H11\_CB} = \text{H11\_CE} / (\text{H21\_CE} + 1.0)$

$\text{H22\_CB} = \text{H22\_CE} / (\text{H21\_CE} + 1.0)$

$\text{H12\_CB} = \text{H11\_CB} \times \text{H22\_CB} \times (\text{H21\_CE} + 1.0) - \text{H12\_CE}$

$\text{H21\_CB} = -\text{H21\_CE} / (1.0 + \text{H21\_CE})$

$\text{DENOMINATOR} = (\text{H11\_CB} + 1.0) \times (\text{H22\_CB} + 1.0) - (\text{H12\_CB} \times \text{H21\_CB})$

$\text{S11\_CB} = ((\text{H11\_CB} - 1.0) \times (\text{H22\_CB} + 1.0) - (\text{H12\_CB} \times \text{H21\_CB})) / \text{DENOMINATOR}$

$\text{S12\_CB} = 2.0 \times \text{H12\_CB} / \text{DENOMINATOR}$

$\text{S21\_CB} = -2.0 \times \text{H21\_CB} / \text{DENOMINATOR}$

$\text{S22\_CB} = ((1.0 + \text{H11\_CB}) \times (1.0 - \text{H22\_CB}) + (\text{H12\_CB} \times \text{H21\_CB})) / \text{DENOMINATOR}$

CALL STABILITY FACTOR ($\text{S11\_CB}$, $\text{S12\_CB}$, $\text{S21\_CB}$, $\text{S22\_CB}$, $\text{CB\_STABILITY}$)

CALL CMPLX TO MAG AND PHASE ($\text{S11\_CB}$, $\text{S11\_CB\_MAG}$, $\text{S11\_CB\_PHASE\_DEG}$)

CALL CMPLX TO MAG AND PHASE ($\text{S12\_CB}$, $\text{S12\_CB\_MAG}$, $\text{S12\_CB\_PHASE\_DEG}$)

CALL CMPLX TO MAG AND PHASE ($\text{S21\_CB}$, $\text{S21\_CB\_MAG}$, $\text{S21\_CB\_PHASE\_DEG}$)

CALL CMPLX TO MAG AND PHASE ($\text{S22\_CB}$, $\text{S22\_CB\_MAG}$, $\text{S22\_CB\_PHASE\_DEG}$)

WRITE(1,*) ' CB MAGNITUDE PHASE'

WRITE(1,11) $\text{S11\_CB\_MAG}$, $\text{S11\_CB\_PHASE\_DEG}$

WRITE(1,12) $\text{S12\_CB\_MAG}$, $\text{S12\_CB\_PHASE\_DEG}$

WRITE(1,13) $\text{S21\_CB\_MAG}$, $\text{S21\_CB\_PHASE\_DEG}$

WRITE(1,14) $\text{S22\_CB\_MAG}$, $\text{S22\_CB\_PHASE\_DEG}$

$\text{DENOMINATOR} = (1.0 - \text{S11\_CB}) \times (1.0 - \text{S22\_CB}) - (\text{S12\_CB} \times \text{S21\_CB})$
\[
Z_{11}\text{\_CB} = \frac{(1.0+S_{11}\text{\_CB})*(1.0-S_{22}\text{\_CB})+(S_{12}\text{\_CB}*S_{21}\text{\_CB})}{\text{DENOMINATOR}}
\]
\[
Z_{12}\text{\_CB} = \frac{2.0*S_{12}\text{\_CB}}{\text{DENOMINATOR}}
\]
\[
Z_{21}\text{\_CB} = \frac{2.0*S_{21}\text{\_CB}}{\text{DENOMINATOR}}
\]
\[
Z_{22}\text{\_CB} = \frac{(1.0-S_{11}\text{\_CB})*(1.0+S_{22}\text{\_CB})+(S_{12}\text{\_CB}*S_{21}\text{\_CB})}{\text{DENOMINATOR}}
\]

WRITE(1,*) ' CB INPUT IMPEDANCE = ',Z_{11}\text{\_CB}
WRITE(1,*) ' CB OUTPUT IMPEDANCE = ',Z_{22}\text{\_CB}
WRITE(1,7)CB STABILITY
7 FORMAT(' CB STABILITY FACTOR = ',F6.4)

STOP
END

SUBROUTINE COMPLEX_TO_MAG_AND_PHASE(COMP,AMP,PHASE_DEG)

COMPLEX COMP
PI = 3.1415926

AMP = SQRT(REAL(COMP)**2 + AIMAG(COMP)**2)

PHASE_DEG = ATAN2(AIMAG(COMP), REAL(COMP)) * 180.0/PI

RETURN
END

SUBROUTINE STABILITY_FACTOR (S_{11}, S_{12}, S_{21}, S_{22}, STABILITY)

C 2-PORT STABILITY FACTOR FROM PAGE 22 "S-PARAMETER BOOK" BY VENDELIN

COMPLEX S_{11}, S_{12}, S_{21}, S_{22}

D = CABS(S_{11}*S_{22} - S_{12}*S_{21})
STABILITY = \frac{(1.0 - CABS(S_{11})**2 - CABS(S_{22})**2 + D**2)/(2.0*CABS(S_{12}) * CABS(S_{21}))}{\text{DENOMINATOR}}

RETURN
END
APPENDIX B

OSCILLATOR CRITERIA DESIGN PROGRAM
THIS PROGRAM CALCULATES THE REQUIRED INPUT RESONATOR TO
MAKE AN OSCILLATOR OSCILATE. INPUTS FROM FILE OSC.DAT
ARE:
LINE 1: TRANSISTOR NAME (CHARACTER)
LINE 2: COLLECTOR TO EMITTER VOLTAGE, COLLECTOR CURRENT
LINE 3: FREQUENCY IN HZ.
LINE 4: S11, S12 (MAG AND PHASE)
LINE 5: S21, S22 (MAG AND PHASE)
LINE 6: LOAD RESISTANCE, LOAD CAP(pFS), LOAD INDUCT(nH'S)

\[
S11p = \frac{S11 + S21 \cdot \Gamma_{L}}{1 - (S22 \cdot \Gamma_{L})}
\]

CONDITIONS FOR OSCILLATION:
STABILITY FACTOR K<1
\[
\Gamma_{G} \cdot S11p = 1
\]

\[
\Gamma_{G} \cdot S12 \cdot S21 \cdot \frac{1}{1 - (S22 \cdot \Gamma_{L})}
\]

COMPLEX S11, S12, S21, S22, S11p, ZL, ZG
COMPLEX \Gamma_{L}, \Gamma_{G}
CHARACTER*20 TRANS
REAL IC, IND, IND_NH
PI = 3.1415926
Z0 = 50.0 !CHARACTERISTIC IMPEDANCE

OPEN(UNIT=1, NAME='OSC', TYPE='OLD')
READ(1,9) TRANS
FORMAT(A20)
READ (1,* ) VCE, IC
READ(1,*) FREQ1, FREQ2
READ(1,*) S11_MAG, S11_PHASE_DEG, S12_MAG, S12_PHASE_DEG
READ(1,*) S21_MAG, S21_PHASE_DEG, S22_MAG, S22_PHASE_DEG
READ (1,*) RL, CAP_PF, IND_NH

OPEN(UNIT=2, NAME='OSCOUT', TYPE='NEW')
WRITE(2,9) ' '
WRITE(2,9) ' TRANSISTOR ', TRANS
WRITE(2,9) ' Vce = ', VCE, ' volts'
WRITE(2,9) ' Ic = ', IC, ' ma'
WRITE(2,9) ' MAGNITUDE PHASE'
WRITE(2,11) S11_MAG, S11_PHASE_DEG
WRITE(2,12) S12_MAG, S12_PHASE_DEG
WRITE(2,13) S21_MAG, S21_PHASE_DEG
WRITE(2,14) S22_MAG, S22_PHASE_DEG
WRITE(2,*),' LOAD'
WRITE(2,*),' RESISTOR = ',RL,' OHMS'
WRITE(2,*),' CAPACITOR = ',CAP,' pF,' ' pFs'
WRITE(2,*),' INDUCTOR = ',IND,' nH,' ' nHs'
WRITE(2,*),' 11 FORMAT(' S11 ,4X,F8.5,3X,F8.2)
12 FORMAT(' S12 ,4X,F8.5,3X,F8.2)
13 FORMAT(' S21 ,4X,F8.5,3X,F8.2)
14 FORMAT(' S22 ,4X,F8.5,3X,F8.2)

S11_PHASE = S11_PHASE_DEG * PI/180.
S12_PHASE = S12_PHASE_DEG * PI/180.
S21_PHASE = S21_PHASE_DEG * PI/180.
S22_PHASE = S22_PHASE_DEG * PI/180.

S11 = S11_MAG * CMPLX(COS(S11_PHASE),SIN(S11_PHASE))
S12 = S12_MAG * CMPLX(COS(S12_PHASE),SIN(S12_PHASE))
S21 = S21_MAG * CMPLX(COS(S21_PHASE),SIN(S21_PHASE))
S22 = S22_MAG * CMPLX(COS(S22_PHASE),SIN(S22_PHASE))

CALL STABILITY_FACTOR (S11, S12, S21, S22, STABILITY)

WRITE(2,8) STABILITY
WRITE(2,*), ' 8 FORMAT(' STABILITY FACTOR = ',F6.4)
CAP = CAP_PF * 1.E-12
IND = IND_nh * 1.E-9

DO 100 I=1,2
IF (I .EQ. 1) FREQ = FREQ1
IF (I .EQ. 2) FREQ = FREQ2
WRITE(2,*), ' Freq = ',FREQ*1.E-6,' MHz'
WRITE(2,*), ' W = 2.0 * PI * FREQ
IF ( CAP .EQ. 0.0 .AND. IND .NE. 0.0 ) THEN ! INDUCTIVE LOAD
   XL = W * IND
ELSE IF ( CAP .NE. 0.0 .AND. IND .EQ. 0.0 ) THEN ! CAP LOAD
   XL = -1.0/(W * CAP)
ELSE
   WRITE(6,*),' EITHER CAP OR INDUCTANCE MUST BE ZERO.'
STOP
END IF

ZL = CMPLX( RL, XL)
WRITE(2,*)' LOAD IMPEDANCE = ',ZL
GAMMA_L = (ZL - Z0)/(ZL + Z0)
WRITE(2,*)' LOAD REFLECT COEF = ',GAMMA_L
S11P = S11 + (S12*S21*GAMMA_L)/(1.0-(S22*GAMMA_L))
WRITE(2,*), ' S11 PRIME = ',S11P
S11P_MAG = CABS(S11P)
WRITE(2,*), ' S11 PRIME MAGNITUDE = ',S11P_MAG
IF (S11P_MAG .LT. 1) THEN
    WRITE(2,*)'SORRY CANNOT MEET OSCILLATION CRITERIA.'
    GO TO 100
END IF
GAMMA_G = 1.0/S11P
WRITE(2,*)' GENERATOR REFL COEF =',GAMMA_G
ZG = 20 *(1.0+GAMMA_G)/(1.0-GAMMA_G)
WRITE(2,*)' GENERATOR IMPEDANCE =',ZG
XG = AIMAG(ZG)
IF (XG .GT. 0) THEN
    !INDUCTIVE RESONATOR AT GENERATOR
    RESONATOR = XG/W * 1.0E9
    WRITE(2,*)' INPUT RESONATOR =',RESONATOR,' nH INDUCTOR'
ELSE
    ! CAPACITIVE RESONATOR
    RESONATOR = -1.0/(W*XG) * 1.0E12
    WRITE(2,*)' INPUT RESONATOR =',RESONATOR,' pF CAPACITOR'
END IF
100 CONTINUE
CLOSE(2)
CLOSE(1)
STOP
END

SUBROUTINE CMPLX_TO_MAG_AND_PHASE(COMP,AMP,PHASE_DEG)
COMPLEX COMP
PI = 3.1415926
AMP = SQRT(REAL(COMP)**2 + AIMAG(COMP)**2)
PHASE_DEG = ATAN2(AIMAG(COMP), REAL(COMP)) * 180.0/PI
RETURN
END

SUBROUTINE STABILITY_FACTOR (S11, S12, S21, S22, STABILITY)
C
C 2-PORT STABILITY FACTOR FROM
C PAGE 22 "S-PARAMETER BOOK" BY VENDELIN

COMPLEX S11, S12, S21, S22
D = CABS(S11*S22 - S12*S21)
STABILITY = (1.0 - CABS(S11)**2 - CABS(S22)**2 + D**2)/
           (2.0*CABS(S12) * CABS(S21))
RETURN
END
REFERENCES


Motorola Semiconductor Products, Inc. Technical Data Specifications. Phoenix, AZ.

MC4044 "Phase-Frequency Detector"
BFW92A "Microwave Transistor"
1N5441B "Varactor"
MC12013 "Dual Modulous Prescaler"
MC12014 "Counter Control Logic"
MC4016 "Decade Counter"


