Energy-Aware Reconfigurable Logic Device Using Spin-based Storage and Carbon Nanotube Switching

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ENERGY-AWARE RECONFIGURABLE LOGIC DEVICES USING SPIN-BASED STORAGE AND CARBON NANOTUBE SWITCHING

by

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B.Tech. B.S.Abdur Rahuman University 2013

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in the Department of Electrical Engineering & Computer Science in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

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Major Professor: Ronald F. DeMara
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ABSTRACT

Scaling of semiconductors to the 14-nanometer range and below nanometer range introduces serious design challenges that include high static power in memories and high leakage power, hindering further integration of CMOS devices. Thus, emerging devices are under intense analysis to overcome these drawbacks caused by transistor size scaling. Spintronics technology provides excellent features such as Non-Volatility, low read power, low read delay, higher scalability as well as easy integration with CMOS in comparison with SRAM memories. In addition, Carbon-Nanotube Field-Effect Transistors (CNFETs) provide superior electrical conductivity, low delay and low power consumption in comparison with conventional CMOS technology. Thus in this thesis, a unique approach to amalgamate spintronics memory technology with CNFET for logic drive in a reconfigurable computing architecture, realizing ultimate circuit performance has been discussed.

A Carbon Magnetic Look-Up Table (CM-LUT) is proposed, using a Magnetic Tunnel Junction (MTJ) spintronic device as memory element and CNFET to perform the logical operations to read the data stored in the aforementioned devices. The proposed circuit is radiation resilient, ultra-low power and high speed operation and the ability to withstand high temperature gradient, Ideal for low power high performance battery operated mobile applications. In addition, the performance of hybrid drive for LUT to leverage fabrication feasibility of CMOS and performance of CNFET to realize fabrication cost effective design. The proposed 4-input 1-output CM-LUT utilizes 41 CNFETs and 16 MTJs for read operation and 35 CNFETs to perform write operation. The results for CM-LUT show 38 times energy reduction and 5.8 times faster circuit operation in comparison with CMOS-based spin-LUT.
I dedicate this work to my family who constantly encouraged and believed in me, which made this thesis possible. I also dedicate this thesis to my advisor Dr. Ronald F. DeMara for providing me with the opportunity to prove myself and also dedicating his precious time during his busy schedule and also for his excellent advising skills, guiding me to reach prominence. I also dedicate this work to my best friends, Gangadhar Madhavan who have picked me up, so many late nights and to Tajreen P. Khan for her constant support and enthusiasm during these active months.
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CHAPTER ONE: INTRODUCTION

Since the invention of the semiconductor in 1965, life has changed dramatically and it is hard to find an application that does not utilize a semiconductor in the present day scenario. Gordon E. Moore, the co-founder of Intel and Fairchild Semiconductor, has described in his paper [1] that the number of transistors roughly increases by a factor of two every 18 months. Moore’s Law is used as a guideline to set R&D and upcoming targets in semiconductor industry.

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

![Figure 1: Moore’s Law transistor history over the period of 4 decades [2].](image)
The number of transistor increase is evident in transistor size scaling, as shown in Figure 1. Scaling allows a larger number of transistors to be integrated on the same die area. Scaling also provides several advantages such as increase in switching speed, lower capacitance because of smaller size and decrease in power consumption at transistor level. Although semiconductor scaling provides several advantages, they cause numerous new design challenges due to transistor downsizing. As the transistor size decreases so does the width of the gate oxide insulator. At nanometer range, the gate oxide insulator is extremely thin. Due to the electric field, the current in the channel tunnels through the gate oxide, causing current leakage. This highly increases the leakage power consumption in the device and consequently, reduces the lifetime and reliability of the device. Figure 2 shows an increase in power consumption in different parts of various System on Chips (SoC), given by International Technology Roadmap for Semiconductors (ITRS) 2010.

Reducing the supply voltage is a great way to reduce the power consumption in the device. However, reducing supply voltage increases switching delay due to the decrease in drive currents. An efficient way to reduce the degradation in circuit speed is to decrease the threshold voltage for a fixed supply voltage as it increases gate overdrive of the transistors. Transistor size scaling reduces the range of threshold voltage scaling, as the device already operates in Near-threshold Voltage. Hence, it curtails the control to reduce power consumption in the device. Other challenges due to transistor scaling include subthreshold conduction, Drain-Induced Barrier Lowering (DIBL), manufacturing Process Variation and efficient lithography techniques to fabricate the device.
Beyond CMOS Computing

The drawback caused by transistor size scaling makes it arduous for the semiconductor industry to follow the Moore’s Law. International Technology Roadmap for Semiconductors (ITRS) 2010 has predicted that the growth of the semiconductor will slow down after 2013. This has led professionals and researchers in the semiconductor industry to look for alternative solutions to counteract this problem.

Reconfigurable fabric in storage of configuration memory data is the benefit provided by the application of post-CMOS devices. From [4], it is determined that SRAM based memory elements are one of the major cause of power consumption in FPGA. In case of power failure when using SRAM based memory cells, all the data stored in them is lost, but when we take advantage of non-volatility provided by spintronic devices, it greatly reduces the static power consumption in the application. Therefore, spintronic device pose as suitable candidate to replace SRAM [5].

Figure 2: ITRS SoC power consumption roadmap. (Red line indicating requirement of dynamic and static power) [3].
There are several different resistive memory technologies; popular devices include Phase Change Memory (PCM) [6] or Memristor [7] that can be used as a memory element, but that is out of the scope of this thesis. The simplest form of Magnetic Tunnel Junction (MTJ) shown in Figure 3 (a), has two ferromagnetic (FM) layers which are separated by a Non-Magnetic (NM) layer. When the magnetic orientation of both layers are similar, the electron suffers relatively less scattering and low resistance, referred to as the Parallel (P) state. On the other hand, if the magnetic orientation of the two layers are not similar, then the electron suffers a large amount of scattering, leading to high resistance, described as Anti-Parallel (AP) state. Parallel and Anti-Parallel states can reach up to a 600% difference in resistance, called Giant Magneto Resistance (GMR). This difference between the states can easily be distinguished using CMOS Sense Amplifier (SA) [8]. One of the two ferromagnetic layers is fixed to one spin direction and is called the fixed layer, while the orientation of the other layer, called the free layer, can be changed based on the direction of the applied current across the device, thus, storing binary information in the form of resistance. Magnetic Tunnel Junction (MTJ) provides various advantages such as non-volatility, lower read power and it is resilient to radiation [9]. Also, MTJ can be easily implemented at the backend of a pre-existing CMOS fabrication process. Figure 3 (b) shows the implantation of 1T1M MRAM using a CMOS backend fabrication process. It is noteworthy that spintronic devices utilized should be in memory, as opposed to implementing logic, the reason that spintronic devices have high switching delay and power.
Carbon Nanotubes (CNTs) are thin and ultra-long, cylindrical carbon molecules with unique electrical and thermal properties, potentially useful for range of nano-electronic and optics. CNTs are essentially a single sheet of graphene rolled into a cylinder, with diameters ranging from 0.6 to 5 nm. Their highest room-temperature mobility and scattering velocity make them suitable candidates for nano-electronics. Carbon Nanotube Field-Effect Transistors (CNFET) are promising candidates for replacing CMOS as they avoid fundamental limitations of traditional CMOS MOSFET. However, they have the same structure of MOSFET as shown in Figure 4, in a way that drain and source contacts control the flow of electrons in the CNTs by the application of electric field through the gate terminal, which means they can be replaced in already existing architectures without much design effort. Due to the excellent ballistic electronic conduction, resilience to electron migration, having the capability to withstand current densities in the order of $10^9$ A/cm$^2$ (which is 1000 times better compared to any noble metals) and operating in low voltage range [11], CNFET can be used to design circuits with supreme performance.
In recent years, Field Programmable Gate Array (FPGA) has undergone intense development due to their flexibility and Research and Development (R&D) as compared to Application Specific Integrated Circuits (ASIC). The transistor density of FPGA is much higher compared to ASIC, the number of transistors in ASIC is 5 billion and on the other hand FPGA has 20 billion [13] [14]. The sections below discuss the advantages of FPGA.

**Reconfigurability**

Since FPGA can offer hardware reconfigurability, the ability to transform hardware is a favorable feature mainly in the embedded systems where it is difficult to physically replace or refurbish hardware. This an especially useful feature when using in aerospace or mission critical applications. To repair a Single Event Upset (SEU) such as a stuck at fault on the configuration memory, we would have to flush the configuration memory and reload the fault free configuration.
data. On the other, hand if there is a hard fault where an interconnect is permanently fused to either high or low, then Genetic Algorithm (GA) can be imitated to evaluate which part of the hardware is healthy, and intrinsically find a way around the fault. This is mainly possible because of Partial Reconfiguration (PR), which is available in modern FPGAs, where a healthy part of the FPGA stays online while it is being refurbished. Likewise, if the mission time of the FPGAs is completed, it can be effortlessly loaded with new designs after evaluating the hardware, thus, improving the life expectancy of the application and not necessarily retiring a perfectly good hardware. This could be especially good when using long range satellites.

Whereas MTJ’s are less sensitive to radiation [15] and when used in conjunction with radiation hardened MOSFETs like the ones in IBM SOI series MOSFETs [16], the circuit is robust to radiation induced faults. Additionally, it also retires the need for employing techniques such as scrubbing. On the other hand, refurbishment techniques like GA are still essential because very large amount of radiation can still cause hard faults.

ASIC Prototyping

Verification of ASIC designs can be done on an FPGA to ensure that it is working functionally correct. Most of the verification is done on software simulations, so one of the verification steps is done on FPGA, as verifying the design functionality on a physical hardware is prudent. Also this form of verification dramatically reduces the development cost, as the fabrication of a complex industrial size ASIC is really expensive, just the mask alone would cost millions of dollars. Additionally FPGAs are programmed with Hardware Description Language (HDL), so the ASIC design engineers can easily port their designs into the device.
Leveraging emerging devices, used in conjunction with reconfigurable fabric, can help prototyping of ASIC designs, which also has emerging devices in them, and additionally can monitor how they interact with each other on a physical hardware. Furthermore, the number of circuits that can be implemented in a specific area increased.

**Hardware Acceleration**

Utilizing the advantages of partial reconfiguration, FPGA can be configured based on application demand during runtime. In a situation where the application is using varying amount of parallelization, the hardware can be reconfigured as a serial processing CPU, and similarly reconfigured into parallel computing engine to process a set of parallel instructions. When the segments of instructions are sequential, the FPGA can be configured into a single core CPU with appropriate cache sizes to efficiently process serial instructions. The soft core can be the master, sensing the instruction flow, and the remainder of the FPGA can be reconfigured as adder cores, similar to GPU which is efficient in throughput. Program analyzed reconfiguration could be an efficient tradeoff between high performance and can also implement energy efficiency using partial reconfiguration.

Compared to CMOS, CNFET has reduced delay and can efficiently read the states of the MTJ, providing much higher acceleration and lower power consumption. Since reading the information stored in MTJ is fast and denser compared to SRAM, larger cache can be implemented, hence further improving the performance of the circuit.
Components inside a Configurable Logic Block (CLB)

Look Up Table (LUT)

An LUT is a basic storage element, which can realize any Boolean function. The size of the Boolean function is limited by the amount of available input and output to the LUT. In 7 series Xilinx FGPAs, LUTs consist of 6 inputs and 2 outputs. These LUTs can implement any six-input Boolean function or two five-input Boolean function with two shared inputs. They can split further down, but the functions with 2 outputs or less can only be implemented. Larger Boolean functions can be implemented using a series of MUXs or combining multiple slices. [17].
SRAM, which is the memory element used to store the information in an LUT, can be replaced by MTJ memory cells. They provide reduced read delay, non-volatility, low read power and higher integration density compared to SRAM.

Multiplexer (MUX)

MUXs, used as signal selectors, are found in different parts of the CLB of the FPGA. Larger Boolean functions can be implemented when MUXs are used in combination with an LUT. When combining a MUX with the LUT in 7 series FPGA, it can be used to realize a 7 input function or 8 input function (when combining all the LUT together in a slice of a CLB). Similarly, function generators, in association with a MUX in 7 series FPGA, can be configured to implement larger MUXs. [17].

CNFET possess the same structure as MOSFET, and provide much better electrical conductivity and lower power consumption. Thus, CNFET can be easily integrated with the already existing circuit design of MUX, providing excellent circuit performance.

Storage Elements

CLB of an FPGA consists of different storage elements such as edge trigger D Flip-Flop or Level-Sensitive latches. A D Flip-Flop can be driven directly from the output of the LUT by using MUX. Shift Registers can also be implemented using the available flip-flops and LUTs, but are only available on SLICEM of CLB. [17]. Similar to the design of MUX, registers can be implemented easily using CNFET.
RAM & ROM

Large number of LUTs can be combined together to form RAM & ROM elements. This feature is only available on the SLICEM part of the CLB. These RAM elements can be implemented using different configurations ranging from Single to Quad-Ported RAM. ROM can be implemented using SLICEM and SLICEL slices, similar to RAM configurations. [17].

If MTJ is used as memory cells in RAM, since by itself provides non-volatility, it would eliminate the need for ROM elements. Also, using MTJ provides higher performance compared to DRAM and SRAM cells.

Carry Logic

CLB in FPGA has fast lookahead carry logic, which can perform fast arithmetic addition and subtraction. This carry logic is provided in addition to the LUT’s function generators in each slice. The carry logic is cascaded upwards to perform wider arithmetic operations. The carry chains, with a maximum height of 4 bits, can be utilized per slice, and each bit has a carry MUX and a dedicated XOR for adding the operands with selected carry bits.

NOTE: CLB is split into two slices, the top is SLICEM (has additional features) and the bottom one is SLICEL. [17].

When the carry logic is designed using CNFET, the delay and power is much lower compared to CMOS design. As a result, it provides more acceleration compared to CMOS design.
### Architectural Improvements in FPGA

Table 1: Architectural Improvements leading to post CMOS utilization in FPGA by commercial manufacturers.

<table>
<thead>
<tr>
<th>Company</th>
<th>Product Details</th>
<th>Architecture improvement</th>
<th>Power</th>
<th>Scalability</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Altera Corp</td>
<td>From Stratix II FPGA</td>
<td><strong>Adaptive Logic Modules (ALM)</strong> – LUT Improvement, Can apply variable size of input to a standard 6-LUT. For instance, a standard 6-LUT can be used as a 6-LUT or two 5-LUT with shared input but separate output combinations[18, 19].</td>
<td>Reduces power as more logic functions are implemented compared to other architectures. Implementing LUT designs from this thesis using MLUT and CMLUT, in conjunction with MUX can tremendously increase power savings.</td>
<td>Better than BLE4 (Basic Logic Element) as it reduces the area of logic. MTJ have better scalability compared to SRAM.</td>
<td>Faster compared to BLE4. MTJ and CNFET are faster in memory and, drive and logic respectively, compared to CMOS.</td>
</tr>
<tr>
<td>Stratix Series 40nm</td>
<td>Programmable Power Technology – Power reduction by select critical and non-critical path and apply appropriate power sizing based on the available slack (Using Threshold voltage Sizing Vth)[20].</td>
<td>37% reduction of power with this Improvement, As compared to the same FPGA without this. (For 700K Logic Elements)</td>
<td>As Devices Operating at NVT, Vth cannot be scaled with size. But Transistor count is directly proportional to the amount of power saving. So Little reduction can provide large Power saving.</td>
<td>Good as timing critical circuits are not affected.</td>
<td></td>
</tr>
<tr>
<td><strong>Altera Corp</strong></td>
<td><strong>Stratix Series 40nm</strong></td>
<td><strong>MultiTrack Interconnect:</strong> connects one LAB to another with hops. Hops intern increase capacitance. Hence fewer the hops, the less high-speed logic[20]. This provides 1-Hop interconnectivity.</td>
<td>Reduces power by using less high speed logic.</td>
<td>Increase in number of LAB’s could make the architecture much more difficult to use fewer ‘hops’ hence high speed interconnect might be required.</td>
<td>Since Multitrack Interconnect uses 1-Hop, The power to delay ratio is low.</td>
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<td></td>
<td><strong>Hierarchical Clocking:</strong> Groups LAB’s using the same clock [20]. Automated optimization by Quartus II software.</td>
<td>If the clock is not used by any logic, That clock is shut down to reduce power consumption.</td>
<td>NA</td>
<td>NA</td>
<td>Improved as the capacitive load on the clock is lowered.</td>
</tr>
<tr>
<td></td>
<td><strong>Dynamic On-Chip Termination (DOCT):</strong> The ability to turn on and off serial and parallel termination dynamically during data transfer [20].</td>
<td>65% power saving of static power in 1067 Mbps</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td><strong>Built-In Hard IP:</strong> Hard IP provides more power saving than soft IP [20].</td>
<td>Operates in a wide range of modes with different power consumption</td>
<td>NA</td>
<td>NA</td>
<td>Inversely proportional to power. Different modes varying power and speeds.</td>
</tr>
<tr>
<td><strong>Xilinx</strong> 7 Series Devices</td>
<td><strong>Optimized Transistor Mix:</strong></td>
<td>Power saving from 40-80% compared to previous generations.</td>
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<td>-----------------------------</td>
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<tr>
<td>28 nm</td>
<td>Threshold voltage optimized transistors to operate between high speed and low power [21].</td>
<td>Poor, As devices are further scaled, voltage scaling options becomes narrower.</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>They use the available slack to optimize the transistors from 0.9-1V.</td>
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<table>
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<tr>
<th><strong>7 Series Devices</strong></th>
<th><strong>Stacked Silicon Interconnect</strong></th>
<th><strong>Static power savings of 40% compared to monolithic device with same density.</strong></th>
</tr>
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<tbody>
<tr>
<td></td>
<td><strong>Technology:</strong> One of the two dies stacked on top of each other, might provides worst case leakage and the other operating on normal leakage specification. Stacked Silicon Interconnect provides lower worst case leakage in comparison with a die consisting of same density. [21, 22].</td>
<td>NA</td>
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<td></td>
<td>Improves I/O performance as it reduces the bottlenecks (Problem faced in monolithic FPGA) and improves speed and reduces power.</td>
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<table>
<thead>
<tr>
<th><strong>7 Series Devices</strong></th>
<th><strong>Integrated Blocks:</strong></th>
<th><strong>Static power saving of 90% compared to soft-IP. Obtained by reduction in number of transistors.</strong></th>
</tr>
</thead>
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<tr>
<td></td>
<td><strong>Integrated block eliminate the need for programmable interconnects, and reduces trace length and logic levels. Thus reducing dynamic power and area footprint. 10x reducing in power can be achieved, if soft-IP are replaced with an integrated block [21].</strong></td>
<td>Good, The number of transistors required to realize a particular logic is reduced.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Excellent, Since capacitive load on the circuit is reduced the circuit might switch faster</td>
</tr>
</tbody>
</table>
### Xilinx 7 Series Devices

**Power Gating of Unused Blocks**: Shut off unused blocks of transistor devices to reduce leakage power.

- Improvement compared to earlier generations of FPGA: The ability to control unused RAM blocks to save power [21].
- Complete emendation of RAM leakage based on usage.
- Good, more devices in the block equals more power saving.
- On contrary the ability to power gate reduces as the transistors get smaller.
- Speed of the device can be affected when the power Gated Block are accessed (Requires some time to turn on).

**Partial Reconfiguration**: The user has the ability to control and run parts of their design to either operate in high performance or low power consumption [21].

- Power savings of 80% when the logic which are timing critical are used in high performance and non-critical logic in low-power consumption.
- Works on available slack in the circuit.
- As the device gets smaller very poor voltage optimization, hence ability to switch from high performance and low power will be slim.
- No significance on speed, as the device can both in high speed or low speed.

**28nm HPL**: The FPGA fabric was built with 28nm transistors which have reduced leakage power [21].

- Static power saving of 50% and 65% operation in 1V and 0.9V respectively.
- Also eliminates the need of static power management strategies.

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</table>
Xilinx  7 series and Zynq 7000

**Intelligent Clock Gating:** Clock Gating is applied to circuit, after analyzing their logic equations and identifying source registers that are idle, which do not contribute to the result at every clock cycle. The software uses clock enables (CEs) in logic, available in abundance to realize fine-grain clock gating. This capability is extendable to logic level gating to reduce switching activity [21].

Up to 30% reduction in dynamic power. Good, more unused block can be turned off. Better, as the unused block are turned off, hence lower capacitance and delay.

---

**Actel Corp Microsemi**

IGLOO, IGLOO PLUS, ProASIC3 L

**Clock Gating at Chip Level:** The entire functionality of the FPGA is suspended, disabling all the switching activity at logic level and beyond. [23].

---

**Scope Of Post CMOS Devices Considered In This Thesis**

Whereas FPGAs are very large, complex devices, there are many potential targets to the application on post CMOS devices between contemporary chips. The scope of uses targeted in this thesis has been restricted to logic function storage and reprogrammability function, which are central to FPGA operation. They are typically encapsulated as LUT’s in this thesis. We designed these ubiquitous elements using CNFET & MTJ. These existing elements add features such as non-volatility, fast read speeds, higher integration density and lower power consumption discussed
in chapter 3 and 4. Other secondary functions with FPGA chip interconnect and routing mechanisms are out of the scope of this thesis.

Overview of MTJ-based LUT

From previous sections, the usage of SRAM cells is the major source of power consumption in FPGA, and scaling only makes it worse. The introduction of emerging devices like MTJ can replace SRAM cells, with additional advantages including non-volatility, high read speeds and being resilient to radiation. Non-volatility and high read speeds give LUT superior performance compared to SRAM based designs. Considering the fact that FPGA needs to be configured only once, Spin-LUT [24] can be used to realize an instant ON feature. Also the power consumption of Spin-LUT is low compared to SRAM based LUT.

The detailed design of MLUT is described in chapter three. To read the state of the MTJ, we use the design of Pre-Charge Sense Amplifier (PCSA) from [25], with comparison of the difference in resistance between the two states. There are other sense amplifiers described in this paper but since it pre-charges to supply voltage at every clock low and senses at clock high, it is quite advantageous when connected with a register. A select tree structure using pass transistor is used to accommodate 16 MTJ, to store 16 bits of a function to the end of the PCSA. Since the resistance of MTJ varies with respect to apply voltage, it has advantages to use 4 MTJ in reference part of the MTJ, which is equivalent to \((R_P + R_{AP})/2\). Since the write time is much larger in comparison with read time, designing a write circuit with five times the size of the normalized transistor size reduces the write time due to the increase in inward current flow. The remaining of the write circuit is described in chapter two. This gives a much better differentiation between the
states as the resistance is in the middle. To give the readers better comparison of the results, 45nm CMOS technology node is used from Arizona State University [26, 27], CNFET model from Stanford University [28] and MTJ compact model from Perdu University [29], and the circuit is simulated using HSPICE.

**Contribution of this Thesis**

1. Design of Magnetic Look-Up Table (MLUT), using MTJ in place of SRAM cells which intern reduces power consumption and delay in the LUT.

2. Design of CNT based Pre-Charge Sense Amplifier (PCSA) to read the state of the MTJ.

3. Design of Carbon Magnetic Look-Up table (CMLUT), using CNFET in place of CMOS and utilizing the excellent ballistic and electrical characteristics of Carbon Nano Tubes (CNTs) and use in place of CMOS to realize ultimate performance.
Figure 6: Contribution of this thesis provides (a) MTJ structure using CoFeB magnetic layers and MgO as tunneling layer [30], (b) MTJ Top Transmission Electron Microscope (TEM) image at 40 nm diameter from [30], (c) cross-sectional TEM image showing different structures of the MTJ at nanometer range, (d) Schematic of a normal SRAM cell, (e) TEM image of CMOS on silicon-on-insulator [31] and (f) showing TEM image of CNFET [32].
Organization of Thesis

This thesis is organized into six chapters and, Figure 7 gives the outline of these chapters. Chapter One deals with background and motivation behind work with Field Programmable Gate Arrays architectures, trends and issues. This chapter also gives a basic outline of the design of MLUT. Chapter Two discusses the related works and different resistive memory based devices. These include Memristor, Phase-Change Memory (PCM), Domain Wall, Racetrack and MTJ based LUT. Chapter Three portrays the complete design of the MLUT. It formulates the structure and characteristics of the Magnetic Tunnel Junction (MTJ) device, Perpendicular Magnetic Anisotropy (PMA), Tunneling Magneto Resistance (TMR) and Giant Magneto Resistance (GMR). This chapter also describes the basic introduction to operation of Pre-Charge Sense Amplifier (PCSA), Reference Circuit, Select Tree and high speed write circuit. Chapter Four discusses the design of the Carbon Magnetic Look-Up Table (CM-LUT). Characterization, design and formulation of the CNT and CNFET and the fabrication method are examined in this chapter. It also has a detailed description of CNFET based PCSA, Select Tree and high speed write circuit. Chapter Five deals with functional verification of the MLUT and CM-LUT, Energy delay analysis and area analysis based on the number of transistor used to implement the LUT design. Chapter Six conveys the conclusion. Technical summery of the LUT design proposed herein, circuit reliability analysis and fabrication feasibility. This chapter conveys the future works and circuit simulation at CLB level and further.
Figure 7: Organization of Thesis
CHAPTER TWO: RESISTIVE MEMORY BASED LOOK-UP TABLE

Resistive memory technology are the devices where the state of the device is changed in the application of some form of energy (like voltage, current, magnetic field or thermal excitement). The difference between the two states is the change in electrical resistance. This change in resistance is usually quite large in magnitude so that the MOSFET based Sense Amplifier (SA) can easily differentiate the change in resistance. Most of the technologies developed, such as spintronics, Memristor and Phase-Change Memory, retain their state even after voltage is removed, hence the data stored in the devices are non-volatile, retainable for several years and the state change is quite fast in comparison with the traditional memory technologies.

This is especially useful because of the transistor scaling disadvantages discussed in Chapter one. MOSFET faces challenges in leakage and standby-power, and SRAM is volatile, meaning that it requires constant application of power to retain the stored data. While using Non-Volatile resistive memory technologies, we could completely turn off the power, thus gaining huge power savings. Additional features of instant ON/OFF can be realized. Having eliminated the need for data transfer between slow external flash memories, resulting in a device which can go into power saving mode with almost no power consumption, and instantly waking up from it without any noticeable delay and continue its operation from its power off.
Memristor Based Look-Up Table (mr-LUT)

Memristor is an electronically switchable semiconductor thin film sandwiched between two metal contacts, within which the resistance of the device can be changed with application of electrical voltage. The memristor described in [30, 31], is designed in such a way that the titanium dioxide layer is sandwiched between two platinum electrodes. The semiconducting thin film contains two layers of titanium oxide, one layer containing pure intrinsic titanium dioxide, which is highly resistive (undoped layer) in nature, and the other layer, also containing titanium dioxide, is filled with oxygen vacancies (doped layer), highly conductive in nature. The structure of memristor is shown in Figure 8 from [32]. When a voltage is applied across the device, the positive charge will repel the oxygen vacancies in the doped region onto the undoped region containing pure titanium oxide, thus reducing the overall resistance in the device. Similarly, when a negative voltage is applied across the device, the entire process is reversed, resulting in an increase in resistance of the device. With a small read current, the state of the memristor can be easily determined. The state of the memristor is preserved, even after the applied bias is removed, providing a non-volatile memory element.

![Figure 8: Memristor Cell Structure][1]

[1]: https://example.com/memristor.png
Memristor based Look-Up table, designated herein as mr-LUT is designed in [33] without using a nano-crossbar. This design provides significantly faster data access and lower power consumption compared to traditional SRAM based LUT. One terminal of the memristor is connected to the word line of the controller, while the other terminal is connected to the bit line and grounded though a transistor as shown in Figure 9. The number of memristors connected to each bit line determines the dimension of the LUT. Read is performed by making read enable $R_{EN}$ high and selecting the inputs A or B in the controller as shown in Figure 10. Inputs A and B are used for selecting which memristor to read. For instance, to read the state of the M11 memristor, inputs A and B are held low, turning on transistor T1. The remaining memristors on the bit lines are connected to high resistance as transmission gate TG2, TG3, TG4 in the controller is turned off. Thus the output can be read by applying a read voltage through WL1 and propagating across T1 NMOS and selecting the appropriate signal sel(0) through the output MUX Out.

The write operation is performed when the write enable $W_{EN}$ is high. From the controller diagram in Figure 10, C is used to select which part of the memristor to select, for instance when C is 0, M11 and M21 are selected. From the design, it can be determined that the BL is connected to the ground through the MOS transistor, thus other branches in the circuit are unaffected. Therefore, by turning ON T1 transistor and using a bidirectional voltage applied through D0, the state of the memristor can be changed.
Figure 9: Memristor LUT [33].

Figure 10: Controller for Memristor LUT [33].
Phase-Change Memory Cell Based Look-Up Table (PCM LUT)

Similar to other emerging resistive memory technologies, PCM also provides advantages such as non-volatility, small size, high endurance and high resistance transformation ratio ($R_{\text{RESET}}/R_{\text{SET}}$). Phase-Change Random Access Memory (PCRAM) consists of a Germanium Antimony Tellurium ($\text{Ge}_2\text{Sb}_2\text{Te}_5$) GST Phase-Change Layer and an NMOS to allow the data access as shown in Figure 12. The state of the GST layer can be altered setting the bit-line (BL) to a fixed potential and applying differential voltage pulse at word-line (WL). In [34], 2.5V with 200 ns pulse width with 100 and 1000ns raise and fall time respectively, is applied at WL to write it as ‘crystallization’ (SET). Similarly, 3V with 20 ns pulse width with 19 and 1 ns raise and fall time pulse, is applied at WL to change the state of the PCM to ‘amorphization’ (RESET). It is to be noted that according to [34] that PCRAM cell can be reversibly transformed over $10^7$ cycles. The resistance of the PCRAM depends on the applied current, as it varies with different level of applied current.

PCM LUT described in [34], is designed in such a way that the PCM is integrated with CMOS using an unfolded CMOS MUX, which takes 3 inputs as shown in Figure 11. The top and bottom voltages, $V_{\text{top}}$ and $V_{\text{bottom}}$, are connected to 2.5V at transformation stage and 1V and 0V, respectively, during normal operation. The state stored in the PCM is read by applying inputs to select a particular branch of the select tree. PCM cells are programmed independently for complementary logic such that the output be easily distinguished between high/low without conflict. For instance, to configure the LUT to represent a NAND gate, we program PCM cells $\text{PC}_{N1}$ and $\text{PC}_{P2}$~$\text{PC}_{P8}$ to high and similarly, set $\text{PC}_{P1}$ and $\text{PC}_{N2}$~$\text{PC}_{N8}$ to low. Thus, when an input $(A, B, C)$ is set to $(1, 1, 1)$ is supplied, the first branch is selected, and the output is pulled to zero.
Figure 11: Schematic of 3 input PCRAM LUT [34].

Figure 12: PCM RAM cell [34].
Spintronics based Resistive Memory Look-Up Table

Domain Wall Shift Register-Based Magnetic Look-Up Table (DW-LUT)

Current-Induced Domain Wall (DW) motion is a new switching mechanism, quite similar to racetrack memories technologies, which has the potential for higher integration density, lower power, high speed and the ability to realize instant ON/OFF feature. These devices, similar to MTJ, can be easily integrated at the back end of CMOS fabrication process with a few additional masks [35]. MTJs are used as read and write heads, to sense and change the state of the DW cell respectively.

The design of DW-LUT consists of a MUX select tree to accommodate the $2^n$ number of bits of $n$ inputs and a high speed sense amplifier to detect the resistive state of the spintronics device with respect to the reference resistance [25, 36]. DW-LUT design uses complementary data storage to ensure high computing speed and resilience to process variation, essential requirements of logic application. The design of DW-LUT is shown in Figure 13. The DW-LUT shift register is designed as two magnetic tracks are connected together with a couple of MTJ write heads, which nucleate opposing magnetization through the same current $I_{\text{write}}$ by spin-Torque Transfer (STT) switching approach. To realize an $n$ input design, it requires $2^n$ constrictions and $2^{n+1}$ MTJ, so for a 3 input LUT, it requires $2^3$ constrictions and $2^4$ MTJs. The current $I_{\text{shift}}$ propagates both the tracks simultaneously to ensure the data stored at the same position of the dual of the magnetic tracks, but with opposing configurations. Thus allowing a sense amplifier to be able to compare the state between the two tracks and produce a necessary digital output.
It is to be noted that the $I_{\text{write}}$ and $I_{\text{shift}}$ should not be overlapped to avoid moving or writing errors. Additionally, for best switching or sensing, the size of the MTJ write head should be larger than read head, as lower resistance can reduce the rate of oxide barrier breakdown. On the contrary, high resistance with small size can improve sensing performance [36]. According to [36], the DW nucleation and STT switching approach consumes considerable amount of power due to the high current flow. Although this is the case only when there is a need to change data, for example if there is already ‘0’ then there is no need to write ‘0’ the same cell. The reconfigurable speed of DW-LUT is high (in the range of 1ns), but we could further improve by increasing $I_{\text{shift}}$ current, reducing the distance between two constrictions (as the distance to propagate is small because of the size) or using some pinning techniques [36].

Figure 13: Domain Wall motion Look-Up Table (DW-LUT) [36].
Racetrack Memory based LUT (RM-LUT)

Similar to how the data stored in MTJ, Racetrack Memories also stores the information in the form of magnetic orientation. This data is stored in multiple magnetic domains, separated by constrictions called Domains Walls, which can be propagated through a nano-wire using application of current [5]. From the invention of 3D racetrack memories and storing multiple bits in one single magnetic strip, Racetrack Memories are expected to have ultra-high area efficiency [5] and holds to one of the promising memory technologies in the future. It is to be noted that for a relatively low current, the speed of domain walls can reach up to 100 m/s for a Ta/CoFeB/MgO structure [5]. Due to the recent advances in high TMR ratio in PMA MTJ, the logic density can be increased as it avoids the need for complementary structure for distinguishing data. The read and write operations for the racetrack memories can be performed simultaneously, as the read and write current are on different paths. As you can see in Figure 14, the structure of Racetrack Memories LUT includes MTJ0 which acts as write head and MTJ1-8 which acts as read heads for the Pre-Charge Sense Amplifier (PCSA), reading the magnetization data in the form of resistance in comparison with the reference resistance. PCSA is really important as it gives ultra-fast data access in ~ 100ps, low power operation and is resilient to radiation induced faults. Usage of PCSA retires the need to use Flip Flops in LUT, thus simplifying the whole structure and allowing faster data access. MUX based select tree is used for accommodating the 8 bits of memory element for a 3 input Look-Up Table. Bidirectional current is supplied through the write head to change the state of the domain wall cell.
The design of MLUT described in [24] is quite similar to the spin based designs discussed in this chapter. The state of the MTJ is read by using a local Sense Amplifier designed by [37] proposed using SRAM-based sense amplifier rather than using a Pre-Charge Sense Amplifier (PCSA). Since this design uses complementary sensing design, it requires $2^{n+1}$ numbers of MTJ to realize an $n$ input look up table. The write circuit is also designed in such a way, that to change 1 bit of information, the state of 2 MTJs need to be changed. This design also uses localized sense amplifier for each bit, as shown in the Figure 15, and uses NMOS switching structures to select the appropriate memory element based on the input. Figure 15 shows the implementation of 2
input look-up Table, where C0 and C1 are the inputs to which bit to select, I0, I1, I2, I3 are the discharge path to the ground terminal and Out produces the output of the LUT.

Figure 15: MTJ based LUT, Spin LUT [24].

Table 2 lists several important matrices for non-volatile LUT designs using emerging technologies. For instance, mrLUT excels at speed of operation by exhibiting a phenomenally low sub-pico second delay. Meanwhile CNFET-LUT and CMLUT proposed herein excel for power and energy metrics. The CM LUT dissipates the least power of the designs listed which is less than 1 micro watt.
Table 2: Related Works Table

<table>
<thead>
<tr>
<th>Research Work</th>
<th>Technology</th>
<th>Power (µW)</th>
<th>Delay (pS)</th>
<th>No of Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memristor LUT [33] (mrLUT)</td>
<td>CMOS + Memristor</td>
<td>9.42 (Value calculated from J operating at 1 GHz)</td>
<td>0.0353 (value reported in Table 4 of [33])</td>
<td>4</td>
</tr>
<tr>
<td>PCM LUT [34]</td>
<td>CMOS + PCM</td>
<td>N/A (only standby reported)</td>
<td>470.3</td>
<td>3</td>
</tr>
<tr>
<td>DW-LUT [36]</td>
<td>CMOS + DW</td>
<td>28 (Value calculated from J operating at 2 GHz)</td>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>CNFET-LUT [38]</td>
<td>CNFET + SRAM</td>
<td>4.236</td>
<td>78.5</td>
<td>4</td>
</tr>
<tr>
<td>STT-MRAM based LUT</td>
<td>CMOS + MTJ</td>
<td>27.2</td>
<td>189.55</td>
<td>4</td>
</tr>
<tr>
<td>Proposed Work</td>
<td>CNFET + MTJ</td>
<td>0.7</td>
<td>35</td>
<td>4</td>
</tr>
<tr>
<td>(values provided in Chapter 5)</td>
<td></td>
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</table>
CHAPTER THREE: MTJ BASED LUT

Magnetic Tunnel Junction (MTJ)

MTJ Structure

![MTJ Structure](image)

Figure 16: MTJ Structure [3].

The simplest form of MTJ consists of two ferromagnetic layers separated by an anti-ferromagnetic layer or an insulator layer. MTJ devices usually consist of, one of the two ferromagnetic layers pinned to a particular spin direction, called pinned layer, whereas the orientation of the other layer called free, layer can be altered as shown in Figure 16. Thus, when electrons flowing through these ferromagnetic layers consisting of spin orientation in Parallel (P) to each other, suffer relatively low scattering when flowing through the anti-ferromagnetic layer, the overall resistance of the device is low. On the contrary, when electrons flow through the ferromagnetic layer, with its electron spin being Anti-Parallel (AP) with each other, the electrons flowing through the anti-ferromagnetic layer suffer greater scattering. This effect is called Giant MagnetoResistance (GMR), observed by Albert Fert in France and Peter Grünberg in Germany.
[39, 40], which led to the birth of spintronics. Tunneling MagnetoResistance (TMR) observed by Julliere in 1975 [41], is the resulting effect when using an insulator layer instead of an antiferromagnetic layer, which is sandwiched between two ferromagnetic layer, and is used in modern spintronics devices.

Figure 17 illustrates the tunneling effect in the MTJ, in which (a) shows the parallel state where the electron can pass without any scattering. Similarly, (b) shows the Anti-Parallel state where the electron suffers higher scattering causing fewer electrons pass through the insulator layer realizing higher resistance. In this thesis, the convention is to depict the hole current on diagrams depicting charge flow. In other cases where electron behavior is essential to the discussion, the electron current will be identified per se.

Comparing the GMR effect to MTJ is called the TMR effect, where the electrons are tunneled through the insulator layer. The tunneling conductance summarized can be given in a tunneling magnetoresistance ratio that is defined as

$$TMR = \frac{\Delta R}{R_p} = \frac{R_{AP} - R_P}{R_P} = \frac{G_P - G_{AP}}{G_{AP}}$$
R_{AP} and R_{P} are the resistance of Anti-Parallel and Parallel states of the MTJ, and G_{AP} and G_{P} is the relationships between conductance of Anti-Parallel and Parallel states. The mathematical equation for conduction and spin polarization is defined as,

\[ G_P = N_{M1}N_{M2} + N_{m1}N_{m2} \]
\[ G_{AP} = N_{M1}N_{m2} + N_{m1}N_{M2} \]
\[ P_t = \frac{N_{Mi} - N_{mi}}{N_{Mi} + N_{mi}} \]

N_{Mi} and N_{mi} are the effective densities of state of majority and minority electrons at Fermi energy at both layers respectively. Thus, the TMR ratio based on effective density of states can be expressed in terms of spin polarization by the equations,

\[ TMR = \frac{2P_1P_2}{1 - P_1P_2} \]

In recent years, the structure of nanopillers used in [8] consists mainly of Cobalt Ferric and Boron structure (CoFeB), ferromagnetic thin films and a Magnesium Oxide (MgO) based insulator layer. This structure can realize a Tunneling MagnetoResistance effect (TMR) of up to 600% resistance at room temperature due to the use of single-crystal MgO tunnel barrier, sometimes also called Giant TMR [42, 43]. This difference in resistance can be easily differentiated by using a CMOS sense amplifier (SA) as in [25]. This is also an essential feature to avoid the CMOS process mismatch and parameter variation. It is the basic building block of non-volatile memories, called Magnetic Random Access Memories (MRAM), which would be discussed in detail in upcoming sections. Despite many favorable properties current and future challenges with MTJs such as oxide thinness which can accelerate Time Dependent Dielectric Breakdown (TDDB) and read disturbance risks whereby sensing P/AP state, may inadvertently modify the stored value.
MTJ Switching Approaches

To change the state of the MTJ, some form of magnetization energy is supplied to the device. There are numerous ways to switch the state of the MTJ device such as Spin Transfer Torque (STT), Field-Induced Magnetic Switching (FIMS), Thermally Assisted Switching (TAS), Thermally Assisted Spin Transfer Torque (TAS+STT) and Giant Spin Hall Effect switching (SHE).

Field Induced Magnetic Switching (FIMS) is a form of switching approach where two orthogonal current lines are used to induce magnetic field, thus switching the magnetization direction of the free layer of the device [44]. The advantage of using this structure is sensing, which is entirely independent of write line. This was used in the first generation of MRAM. Due to the requirement of high current to generate the required magnetic fields and drawbacks caused by speed and density, its commercial usage is limited in future generations [3].

Thermally Assisted Switching (TAS) is an addition to FIMS approach. This switching approach uses the current flowing through the MTJ device to increase the temperature of the device above ordering temperature, hence reducing the required switching magnetic field [45, 46]. Thus, in addition to the bit line which allows write selectivity, another line is added to the structure which acts as a heating element. This method promises lower power, higher density and better thermal stability compared to the previous FIMS approach. Due to the time required to heat and cool the device, it greatly increases the speed of operation of the device [3].

Giant Spin Hall Effect (GSHE) is one of the new switching methods, which uses a structure similar to MTJ device. A high-Z electrode (made up of Pt, Ta or W) is added to the free layer structure of the already existing MTJ stack, which produces high spin currents with respect to the
direction of the applied current through the electrode [47], as shown in Figure 18. The ends of the high-Z electrode are connected with a highly conductive metal (Cu) to minimize write resistance. Thus, the spin direction of the free layer can be changed by applying a bi-directional current through the copper terminals. The state of the device is read by applying a read current vertically through the device, similar to the normal read operation of the MTJ, using a sense amplifier. This form of switching approach promises to provide low write energy and switching delay compared to other switching approaches.

![Diagram of GSHE MTJ stack](image)

Figure 18: GSHE MTJ stack [47].

Thermally Assisted Spin Transfer Torque is a method of combining TAS and STT (discussed in the next section) switching together proposed by [48, 49]. Similar to STT approach, bi-directional current flows through the device. This current heats up the device above blocking temperature of the AFM layer that is associated with the free layer. When the current exceeds the threshold value of the STT, the magnetic direction of the free layer is changed. This method provides advantages such as increase in density, switching power and good thermal stability, however this method of switching requires some cooling time and power for heating the device, which hinders the use in low power, high speed applications.
Spin Transfer Torque (STT)

Similar to the effect observed in TMR and GMR structures, the current passing through the structure is polarized according to the magnetization orientation of the two ferromagnetic layers. Based on the Momentum Conservation principle, the angular momentum caused by current passing through the device, influences the magnetic direction of the free layer. This MTJ switching approach is called Spin Transfer Torque (STT). This method of switching was proposed by Berger and Slonczewski in 1996 [50, 51]. When the number of polarized electrons exceeds a particular value, usually termed as critical current $I_C$, the torque with is exerted on the free layer results in changing its magnetization orientation. STT switching approach requires a bidirectional current to change the MTJ state from antiparallel to parallel and vice versa. Since STT switching requires significantly lower current compared to the amount of current required to generate magnetic field necessary for switching in FIMS, it is widely used in the MTJ implementation. STT switching is used through the course of this thesis, as shown in Figure 19.

Figure 19: STT switching approach [3].
Types of Spin Orientation

Perpendicular Magnetic Anisotropy (PMA)

For the design of high performance MTJ, there are four main criteria to be satisfied, namely, high thermal stability, low switching power, low switching delay as well as the ability to withstand semiconductor fabrication process. In recent years, it has been found that shrinking of MTJ with in-pane magnetic orientation makes it arduous to fulfill the criteria. Perpendicular Magnetic Anisotropy (PMA) MTJ requires less switching current compared to In-pane Magnetic Anisotropy (IMA). In addition, PMA also provides better TMR ratio compared to IMA structures. The threshold current $I_{C0}$ for current induced magnetization switching is given by

$$I_{C0} = 2\alpha \frac{\gamma e}{\mu_B g} E$$

Where $E$ is the energy barrier which separates the two magnetization layers, $\alpha$ is the magnetic damping constant, $\mu_B$ is Bohr magneton, $g$ is the function of spin polarization, $\gamma$ is the gyromagnetic ratio, and $e$ is the electron charge. For in-pane anisotropy, the energy barrier $E$ is replaced by the demagnetization energy $E_{\text{demag}}$, resulting in a larger $E$, thus requiring larger current compared to PMA MTJ [52]. Consequently, CoFeB-MgO MTJ structure provides superior performance because small area, small critical current and high TMR ratio.
The design of 4 input 1 output LUT uses several components as illustrated in the Figure 20. The components are required for different purposes such as PCSA for reading the state of the MTJ based on the resistance of the reference MTJ, Select Tree to accommodate $2^n$ number of memory element for an $n$ input LUT, Write Circuit to produce the bi-directional current required to change the state of the MTJ, Reference Stack to compensate the increase in transistor resistance for proper sensing of PCSA and finally MTJ arrangement in the reference circuit which eliminates the need for complementary writing circuit (which increases the write power consumption). The detailed explanation and use is described in the respective upcoming sections.
Magnetic Random Access Memory (MRAM)

MRAM is the basic memory element implementation in conjunction with CMOS design. Rudimentary MRAM consists of an MTJ and an access transistor. This design is called 1T1M design. This is one of the primitive approaches which makes use of STT switching and an access NMOS to change the state of the MTJ. The gate of the NMOS is connected to Word Line (WL), source of the NMOS is connected to Select Line (SL), the drain terminal is connected to the pinned layer of the MTJ, and Bit Line (BL) is connected to the free layer of the MTJ, as shown in Figure 21. The data stored in MTJ can be accessed by turning ON access NMOS and when the current flowing from BL to SL increases above the critical threshold current, then the state of the MTJ is switched from AP to P as shown in the Figure 21. Switching the state from P to AP is similar to the aforementioned method, with an exception that BL is connected to the fixed layer and the drain of the access NMOS is connected to the free layer, as illustrated by the figure below. The density of the MRAM chip is limited by the use of crossbar architecture, as there increase in sneak currents [53, 54].

Figure 21: MRAM design.
Write Circuit

4-Transistor Design

As the MTJ requires a bi-directional current to change its state, the primitive design uses 4 transistors to generate the bi-directional current for the state change. This design of the write circuit is presented in [24], which uses a complementary switching structure, where one PMOS and one NMOS will be turned ON, one on both sides of the circuit, thus, changing the state of two MTJs simultaneously. MOSFETs on either side of the circuit are turned ON by the use of logic gates which are controlled by input and write enable. If the write circuit is not complementary then, one PMOS and one NMOS are connected to the free layer. Similarly, one PMOS and one NMOS are connected to the pinned layer of one MTJ. Thus, the write is tailored to one MTJ to write 1 bit of data.

Figure 22: (a) Showing 1 bit switching structure and (b) showing complementary switching structure [24].
Inverter and Transmission Gate Design

![Transmission Gate write design](image)

Through the course of this thesis, the entire write circuit used is based on transmission gate design. Transmission Gate (TG) acts as a switch, passing either of the logic inputs to the output when it is turned ON. On the contrary, TG completely isolates the write inputs when it is turned OFF, as it goes into high resistance state. The outputs of the TG are connected to the free and pinned layer of the MTJ as shown in Figure 23. The transmission gate connected to the free layer acts as word line, which is used to select $n$ bit MTJs in the LUT. The transmission gate connected to the pinned layer acts as write enable. Thus, a bi-directional current is generated based on the input to the bit line. Compared to the previous design of 4 transistors to generate the bi-directional current, this design is considerably simpler to implement.

The width of the transistors in the transmission gate are increased, as increasing the width of the transistor will in turn increase the current flowing through the device. This reduces the switching delay of the MTJ. In this design, the transistor width is increased by twice the normalized size, so as to keep the switching delay within two clock cycles.
Read Circuit

CMOS-based Approaches

In conventional CMOS based FPGAs, there are two design strategies amenable for efficient read operations of stored logic functions. First, an approach using pass transistors has been popular [55], in this approach SRAM cell is connected through a tree of pass transistors to allow decoding of the logic function, which is encoded as an address within the bit cell stack. Recently, tradeoff studies for deeply scaled SRAM based FPGAs have indicated that transmission gate based mux tree can offer advantages to mitigate increasing effects of process variation [56]. Rather than adopting a transmission gate based design in this thesis, two factors have been taken into consideration to use pass transistors as the baseline control structure. The first factor in favor of pass transistors is the area requirement being roughly half of corresponding design using TG. Second, TG require complemented and un-complemented inputs which increase interconnection requirements. Thus, pass transistors have been chosen for comparison with emerging device technologies using the novel design proposed.

Pre-Charge Sense Amplifier (PCSA)

The design of Pre-Charge Sense Amplifier designed by Zhao [25] is used to read the state of the resistive memory based devices. PCSA proposed in the above design provides high read speeds (usually in a few hundredth of a Pico seconds), ergo ubiquitously used to read the state of the resistive memory based devices. Figure 24 demonstrates the transistor level design of PCSA. A clock disable NMOS (MWR1) is used in addition to PCSA design, to block the write current
discharge through the ground, when the clock is high. Making the write circuit to operate independent to the clock. The output to the PCSA is determined based on the rate of discharge of the current flowing through the MTJ on sensing and reference side (MTJ1 and MTJ2 respectively), as a result the node Q and Q’ is pulled to high or low voltage based on the resistance of the MTJ. Detailed working of CNFET based PCSA design is explained in the next chapter.

Figure 24: PCSA to read the state of the MTJ
It can be obtained from previous section, that PCSA by itself can only accommodate only 1 bit of data. A 4-input 1-output LUT need 16 bits of storage elements, hence a 1:16 MUX select tree is added to the PCSA. The sensing side of the read circuit is illustrated in Figure 25. Based on the input to the select tree, a section of a tree of NMOS is selected, which is thus read PCSA. Due to the increase in transistor resistance on the sensing side, 4 NMOS’s are added to the reference side which are always ON to compensate the increase in resistance, as shown in Figure 26. Thus at any time during the operation of the LUT, 1 MTJ is selected and compared with the reference side to produce a necessary binary output. In addition, using the reference MTJ as configured in the next section eliminates the need for complementary write circuit. The detailed working of the CNFET-based select tree is described in the next chapter.
Using this reference in the reference circuit retires the need for complementary sensing MTJs. In complementary style of MTJ read or write circuit, to store 1 bit of information, we would require the change the state of two MTJs. Hence, this form of circuitry uses additional memory footprint per bit and the write power per bit is significantly high as well. This form of reference circuit is scaling friendly, as only 4 MTJ are required to implement an LUT of any size as long as there is only one output.

The design of the reference circuit is illustrated in Figure 27. After compensating the transistor resistance by using a reference tree, the reference resistance consists of 2 MTJ with parallel and 2 MTJs with anti-parallel configuration, connected together in parallel and series, as shown in the Figure 27. Equivalent resistance of the MTJ in series configuration:

\[ R_{series} = (R_{AP} + R_P) \]
And equivalent resistance of MTJs connected in parallel:

\[
\frac{1}{R_{\text{parallel}}} = \frac{1}{R_{\text{series}}} + \frac{1}{R_{\text{series}}} = \frac{1}{(R_{\text{AP}} + R_P)} + \frac{1}{(R_{\text{AP}} + R_P)}
\]

\[
R_{\text{parallel}} = \frac{(R_{\text{AP}} + R_P)}{2} = R_{\text{ref}}
\]

Where \(R_{\text{AP}}\) and \(R_P\) are the equivalent resistance of MTJ in Anti-Parallel and Parallel states respectively, and \(R_{\text{ref}}\) is the equivalent resistance of the entire reference circuit with respect to MTJ.

For instance, if the resistance of MTJ in parallel configuration is 3k\(\Omega\) and MTJ in Anti-Parallel configuration is 7k\(\Omega\), according to the above equation, \(R_{\text{ref}}\) will be 5k\(\Omega\). Thus, if the MTJ in the sensing side is in parallel configuration, the resistance in the reference side will be higher and vice versa for the other state. Hence, a complementary structure is sensed using the aforementioned PCSA without changing the state of the MTJ.
CHAPTER FOUR: DESIGN OF CARBON MAGNETIC LOOK-UP TABLE (CM-LUT)

Carbon Nanotubes Field Effect Transistor

Carbon Nanotube (CNT)

Carbon Nanotubes comprise of a sheet of graphene containing carbon atoms arranged in a honeycomb lattice as shown in Figure 28. CNTs can be visualized as a sheet of graphene rolled up to form a cylindrical, tube-like, hollow structure. These tubes are used to transport electrons or holes in ballistic or near ballistic medium, first demonstrated by Bethune and Iijima in the year 1993, in paper [57] and [58] respectively. The band structure of a single walled carbon nanotube can be given by the chiral vector $C_h$ [59],

$$C_h = na_1 + ma_2$$

Where, $n$ and $m$ are the chirality of the tube, and $a_1$ and $a_2$ represent the unit vectors of the graphene lattice. Based on the chiral vector, there can be three configurations of CNT from [59-61],

1. If $n=m$, then the CNT act as metallic properties.
2. If $n-m=3i$, where $i$ is an integer, CNT acts as a semiconductor with small band gap.
3. If $n-m\neq3i$, then CNT will act as a semiconductor with large band gap.

The length of $C_h$ is thus the circumference of the tube,

$$C_h = a\sqrt{n^2 + m^2 + nm}$$

$$D_{CNT} = \frac{C_h}{\pi}$$
where $D_{CNT}$ represents the diameter of the CNT, which usually ranges within a few nanometers. CNTs have quasi 1D structure, the flow of electrons is restricted through the axis of the tube. Thus, there is no scattering except for forward and backward scattering due to electronphonon interactions in the tube [62]. Achieving ballistic or near ballistic, as the electron can travel without scattering. The Mean Free Path (MFP) obtained was around $1000nm$ for CNT [63], much longer than 40 nm obtained by copper interconnects at room temperature[59]. The electron mobility of CNT is in the range of $10^3$ to $10^4$ cm$^2$/Vs, observed in experiments in transistors reported by [62-64]. The current carrying capacities of Multi Walled CNT are in the order of $10^9$ A/cm$^3$, which are three times higher in comparison with copper, mainly limited by the electron migration effect in copper [65]. Since CNTs provide excellent electrical conductivity with low electron scattering, they are of main interest in nanoscale low power, high speed electrical devices.

Figure 28: Graphene CNT operating as metallic or semiconducting based on chiral vector [59].

Recent implemented computing systems using CNT include:

- Carbon nanotube computer designed in [66], consisting of instruction fetch, data fetch, a two-bit ALU and write back stages.
FPGA designed using CNFET [38], which illustrates the design of a CLB with carry-chain, LUTs, MUX, Latch, Register, RAM, shift register LUT and ROM.

**CNFET Design**

CNFETs are typically classified into two types, namely Schottky Barrier (SB) controlled FET and MOSFET-like CNFET. SB-FET consists of an intrinsic CNT connecting source and drain contacts, where the gate terminal electrostatically controls the conductivity of the device. The conduction of the device is governed by the tunneling of majority carriers through the SBs at the end contacts. SB-FET devices possess ambipolar conduction, where a single device can control the conduction of both electron and holes. Due to the problems faced by SB-FET, such as high subthreshold slope and ambipolar conduction, these drawbacks significantly decrease the ON current and increase the OFF current. This limits the usage of SBFET in high performance and low power applications.

CNFET based on MOSFET-like CNFET consists of a structure similar to the conventional MOSFET. The channel of this type of CNFET is made up of intrinsic multiple CNTs, and its conduction is controlled electrostatically by applied potential on the gate terminal, as illustrated in Figure 29. The CNTs, which act as channel, are placed on a silicon substrate, such as SiO$_2$. The gate terminal and the CNTs are separated by high K dielectric material, such as HfO$_2$ to insulate the channel and the gate. The source and drain terminals are doped with impurities at the contacts to improve electron and hole transportation, thus, resulting in a unipolar conduction device. Since a MOSFET-like CNFET possess low subthreshold slope and low OFF current, this makes it an
ideal candidate for low power high performance circuit design [59]. Throughout this thesis, CNFET is referred to as a MOSFET-like CNFET for simplicity.

Figure 29: Different CNFET Device Structures [59].

**CNFET Device Characteristics**

The electrical characteristics are important to evaluate the performance of CNFETs, thus different mathematical expressions are used for modeling these CNFETs by [67]. The device operation is composed of these behaviors, which include ON current, energy and delay calculation. The expression for ON current for a single CNT channel is given by,

\[ I_{CNFET,1} = g_{CNT}(V_{suply} - V_{SS'} - V_{th,CNT}) \]

where \( g_{CNT} \) is the transconductance per CNT and \( V_{th,CNT} \) is the threshold of semiconducting CNT with diameter of 1.51nm from [68]. \( V_{SS'} \) is the voltage across the source doped CNT regions and is expressed as

\[ V_{SS'} = I_{CNFET,n} \times \frac{L_{S,CNT} \rho_{S,CNT}}{n} \]

where \( L_{S,CNT} \) is the length of the doped source region of the CNT and \( \rho_{S,CNT} \) is the resistance per unit length of the doped source CNT region. Thus, the drive current for CNFET is given by,
\[ I_{CNFET} = \frac{ng_{CNT}(V_{supply} - V_{th,CNT})}{1 + g_{CNT}L_{S,CNT}\rho_{S,CNT}} \]

To increase the drive current for a CNFET with fixed \( V_{supply} \), increasing the number of tubes in the channel significantly increases the drive current. This is especially important to implement fast write circuit for MTJ, which is discussed in the upcoming sections.

The switching delay is directly proportional to the capacitance \( C_{CNFET,n} \) and the supply voltage \( V_{supply} \), and inversely proportional to the drive current of the CNT \( I_{CNFET,n} \). Thus the expression for switching delay \( \tau_{CNFET,n} \),

\[
\tau_{CNFET,n} = \eta_{CNT,C}\eta_{CNT,R} \frac{C_{g-CNT,1}L_{g,CNT}V_{supply}}{g_{CNT}(V_{supply} - V_{th,CNT})}
\]

where \( C_{g-CNT,1} \) is the capacitance per unit gate length \( (L_g) \), \( L_{g,CNT} \) is the lithographically defined gate length, \( \eta_{CNT,C} \) is the parasitic capacitance of the gate terminal and \( \eta_{CNT,R} \) is the series resistance caused by doping in the CNT at source region.

The energy required for switching CNFET is directly proportional to the total capacitance, \( C_{CNFET,n} \), and supply voltage. According to [62], the total capacitance in CNFET is equal to the gate capacitance, \( C_{g-total(CNT),n} \), of the device due to small capacitance in S to D and D to S regions, which is given by,

\[
C_{g-total(CNT),n} = C_{g-CNT,n}L_{g,CNT} + C_{g-parasitic}W_{g,CNT}
\]

where \( L_{g,CNT} \) and \( W_{g,CNT} \) are the length and width of the lithography defined gate. The expression for energy consumption in CNFET is given by \( Energy_{CNFET,n} \) such that,

\[
Energy_{CNFET,n} \propto C_{CNFET,n}V_{supply}^2
\]
Figure 30: Performance comparison of 4 inverter chain designed using CMOS and CNFET [67].

The Fan out delay and energy consumption of a four inverter chain (FO4) designed using CNFET and CMOS transistor is shown in Figure 30. This graph also shows the effect of increase in number of tubes per CNFET transistor. The normalized number of tubes used to design CM-LUT is ‘5’, as it provides good tradeoffs between delay and energy consumption. The above graph also shows the impact of process variation in CNFET manufacturing process, as the existing fabrication process is in its infant stages and causes a huge amount of process variation. One can observe from the above graph that CNFET provides a superior circuit over CMOS for a given gate length and supply voltage. When compared with CMOS designs, an ideal CNFET, with the number of tubes ranging from 4-8 can improve by 5 times in FO4 delay and 2.6 times in energy consumption. It is noteworthy to mention, fabricating an ideal CNFET is impracticable, as the current CNT synthesis can cause 10-70% of CNT to be metallic in property [67, 69]. These metallic CNTs conduction cannot be controlled by the gate, causing a resistive short between source and drain in the circuit [67].
Figure 31: CNFET Fabrication Process [59].
The fabrication of MOSFET-like CNFET is shown in Figure 31. The silicon substrate is thermally grown on a silicon wafer as show in Figure 31 (a). Then, alignment markers are placed using lithography techniques to decide where each element of CNFET will be placed, as shown in Figure 31 (b). After the markers are placed, photo resist window is placed to deposit the catalyst for the growth of CNTs, seen in Figure 31 (c). Drops of catalyst, or a metallic sheet of catalyst, is placed in between the photo resist, displayed in Figure 31 (d). After the catalyst is deposited, the photoresist is etched away, leaving behind only the deposited catalyst, as shown in Figure 31 (e). The deposited catalyst is used to develop into CNTs using, chemical vapor deposit (CVD), resulting in the formation of CNTs for the channel, shown in Figure 31 (f). After the CNTs are formed in the channel, using lithography techniques, source and drain terminals are patterned, which is shown in Figure 31 (g). Then, palladium (Pd) is deposited on the terminal forming the source and drain contacts. The high-K dielectric, HfO₂, and gate terminal are placed by using an atomic layer deposition (ALD) and a lift-off technique without overlapping the source or drain regions, shown in Figure 31 (h). After the gate terminals, the exposed CNT where the dopant impurities are added for a unipolar mode of conduction, which is displayed in Figure 31 (i). For N-channel CNFET, the exposed source and drain regions are exposed to potassium (K) in vacuum [70], and for P-channel CNFET, the exposed regions are exposed to tri-ethylxonium hexachloroantimonate (C2H5)3O+SbCl6 (OA) [71].
Figure 32: I-V curve for CNT semiconductor switching behavior [72].

The typical I-V curve for semiconducting CNT is shown in Figure 32. From [72], it can be observed that with the application of potential across CNT increases current flow to a particular level and saturates after. Also, the application of negative potential across the device, allows current flow but the increase is gradual and several magnitudes lower in comparison with forward bias, and thus aiding in ambipolar device conduction.

CM-LUT

The transistor level design of a CNFET based LUT is shown in Figure 33. Several different components are combined together to realize a 4-input, 1-output LUT. In upcoming sections, different components, which are implemented using CNFET, are demonstrated. The significance of each component is discussed in its respective section. Thus, a 4:1 LUT, with 41 CNFETs to read 16 MTJs storing 1 bit each and 4 MTJ-based reference circuits, eliminates the need for complimentary switching structure. The write circuit consists of 34 CNFETs to change the state of 16 MTJs. The write circuit has enhanced the number of tubes in the transmission gate in order
to realize a faster MTJ switching approach. Since CNFET has faster drive capacity compared to CMOS, the entire sensing operation of the LUT is in the range of a few pico seconds.

Figure 33: CNFET based LUT (CM-LUT) transistor level design

Write Circuit

CNFET-based Transmission and Inverter Gate Design

Figure 34: CNFET based MTJ write circuit
As discussed in the previous chapter, MTJ requires a bi-directional current for state change. This bi-directional current is supplied by 2 transmission gates, each connected to the either end of the MTJ. Thus, for an $n$ bit LUT, we require a $2^{(n+1)} + 2$ number of FETs to change the state of $2^n$ MTJs. As SB CNFET provides ambipolar conduction, it can replace TG, henceforth reducing area. Ambipolar conduction is defined as the ability of a device to conduct both electrons and holes, with the application of appropriate potential at the gate terminal. SBFET is not used in this design due to low ON current, which tremendously increases the switching time of MTJ. In addition, SBFET has high OFF current [59]. For example, when the write is disabled, the read circuit is no longer isolated from the write input signals, thus, the read operation can be disrupted.

From the device characteristics section mentioned above, it can be obtained that the drive current is directly dependent on the number of tubes present in the channel for a given supply voltage. Thus, an increase in number of tubes increases the drive current, aiding in faster switching of the MTJ state. In this design, 60 tubes are used in the write TG, so that the MTJ can switch within 2 clock cycles similar to the CMOS write circuit. The number of tubes can be increased by tuning the “tubes” parameter while defining the CNFET transistor to increase the drive capability of CNFET.
Pre-charge sense amplifier can provide significantly higher reliability, low power and high speed sensing operation, making it an ideal candidate for sensing operation for resistive memory devices. Since the sensing speed of PCSA is in the order of a few hundred pico seconds, it has the ability to realize the instant ON feature from [25]. The design of PCSA, proposed by Zhao, is illustrated in Figure 35, and is extensively used for sensing in resistive memory based devices to read the state of the devices.

The operation of PCSA is as follows. The design of PCSA consists of a 4 P-Channel and 3 N-Channel CNFET. In this design, P-channel MP1 and MP4 are used for Pre-Charging the outputs Q and Q’ to supply voltage VDD at every clock low, however there is no current flow...
through the MTJ as the N-channel CNFET MN1 and MN2 are still in OFF condition. At clock high, pre-charged voltage starts discharging through the N-channel CNFET MN1 and MN2, which are now turned ON, as the gate of the N-channel is connected to Q and Q’. Also at clock high, the discharge N-channel CNFET MN3 is turned ON, and the voltage at Q and Q’ starts discharging through MTJ1 and MTJ2 respectively. From the fact that current discharges faster when the resistance is low, the branch of the circuit consisting of MTJ in parallel state will discharge its current faster in comparison with the other side. According to the above Figure, MTJ1 is in parallel and MTJ2 is in anti-parallel state. Thus, Q’ discharges to the ground faster compared to Q, turning ON P-channel CNFET MP3 and pulling the output of Q to high. Also to be noted, since Q controls the P-channel CNFET MP2 and N-channel CNFET MN1, when Q is high, this keeps the N-channel MN1 to always discharge Q’ to the ground and blocking MP2 from charging back to supply voltage. The operation is reversed when the states of the MTJs are reversed, producing Q as low and Q’ as high. This state is held until the next clock low, where it is charged back to supply voltage. [25].

Include a clock disable N-channel CNFET, which is placed in series with the clock controlled N-channel CNFET, to disable discharge. The purpose of this N-channel CNFET is to stop the clock controlled discharge to the ground when the data is written to the MTJ. This is performed to change the state of the MTJ from P to AP, in which current is flowing through the pinned layer to the free layer. However, when the clock is high, the clock controlled N-channel CNFET MN3 is turned ON, hence the write current is discharged through the ground. This N-channel CNFET is controlled by Write Enable (WE). When the write enable is high, the transistors are turned OFF, as shown in Figure 35.
Since the design of PCSA from Zhao [25] can accommodate only 1 bit of data, to accommodate 16 bits of data, a 16:1 MUX select tree is used. A tree of transistors, consisting of $2^{(n+1)} - 2$ number of transistors to accommodate $2^n$ number of bits, is implemented to realize an $n$ input and 1 output LUT. Figure 36 shows the implementation of a 4 input and 1 output LUT, where MTJ1 to MTJ16 are used to store 16 bits of data, and a select tree consisting of 30 N-channel CNFET are used to accommodate the 16 bits of data. For any instance of reading, the select tree requires 4 transistors to read the state of any MTJ in the sensing side, hence there is an increase in resistance between the sensing side and the reference side, resulting in erroneous output. As shown in Figure 37, the reference MTJ has resistance between the two states, eliminating the need for
complementary write structure, which has comparatively high power consumption as two bits need to be changed to write 1 bit of data. Thus, 4 transistors connected in series will help balance the resistance between the two sides and eliminating sensing errors. A, B, C, D are the inputs to the select tree, which help in selecting which MTJ will be read. If the input to the LUT is (0, 0, 0, 0), the right most MTJ is selected, representing bit 0.

The design is quite similar to TG design used by [55], where the use of the full swing feature of the TG produces comparatively lower power consumption in comparison. This design is much simpler and has comparatively lower power consumption and much smaller area in comparison with the TG design, due to the fact that they require greater number of transistors to realize a design having identical functionality.
Summary

This chapter deals with the physical and device characteristic of the CM-LUT. This includes the conducting properties of CNTs, which can either be metallic or semiconducting based on the chiral vectors. Furthermore, this Chapter deals with different CNT based MOSFETs, which also discusses favorability and the reason behind using MOSFT-like CNFET. Important mathematical parameters which characterize the device operation is discussed in this Chapter, in addition to the fabrication methods. The performance of CNFET in comparison with CMOS is analyzed. Finally, the design of CM-LUT is presented, followed by its read and write components, comprising of device optimizations to implement fast and power aware design.
CHAPTER FIVE: EXPERIMENTAL RESULTS

Functional Verification

In this section the operational behavior of the proposed CM-LUT is verified using various sensing circuits developed in the preceding chapters.

Write Circuit Verification

![Write Circuit Diagram]

Figure 38: CNFET Write Circuit

The write circuit implemented in CM-LUT is illustrated in Figure 38. The transient analysis verifying the write circuit is show in Figure 39 and Figure 40, displaying the change in state of the MTJ from Anti-Parallel (AP) to Parallel (P), respectively. The simulation result shown in the graph below, consists of three signals namely, spin orientation \( (\text{Spin}) \), Voltage across Free Layer and Fixed Layer \( (v(\text{FreeL,FixL})) \) and input voltage \( (v(\text{BL})) \). Signal \text{Spin} indicates the orientation of the electron in Free Layer in \( \text{rad} \), which can be either \( \pi \) or \( 0 \text{ rad} \), indicating AP or P respectively. It can be observed that when a positive voltage is applied to the input BL (BLbar signal is derived...
by adding an inverter in-between these two terminals) and the configuration of the MTJ is in AP, Spin signal drops to $0 \text{ rad}$ from $\pi \text{ rad}$, indicating a change in state (Figure 39) at approximately 3ns. It can also be observed that there is a drop in voltage between the Free Layer and Fixed Layer ($v(\text{FreeL},\text{FixL})$), indicating a change in resistance across the device. Similarly, when applying a negative voltage through BL, the state of the MTJ can be changed from P ($0 \text{ rad}$) to AP ($\pi \text{ rad}$). The worst delay observed when implementing this write circuit is approximately 3ns, hence for a read circuit operating at $1 \text{ GHz}$, it uses two clock cycles to write one bit of data. This is due to the fact that the circuit is operating a voltage of $1.2 \text{ V}$, enhanced width in CMOS and increased number of tubes in CNFET. The power consumption to change one bit of data using CMOS design is $57\mu\text{W}$ and $49\mu\text{W}$ when using CNFET based write circuit.

Figure 39: MTJ state change from AP to P
Read Verification

Read circuit is verified extensively by implementing different Boolean expressions. Figure 41 shows the transistor level implementation of the MLUT. The outputs and input can be visualized in Figure 42, where $v(Q)$ is the output of the MLUT, which is a binary voltage, $v(CLK)$ is the input clock to the circuit, which is operating in $1 \text{ GHz}$, and $v(A)$, $v(B)$, $v(C)$, $v(D)$ are the inputs to the select tree to decide which of the 16 MTJs to read.

For the simplicity of verification in this thesis, the MTJs are loaded with configuration $<0101\ldots01>$, which is shown in the truth table represented in Table 3, where binary 0 represents AP and 1 represents P configuration of an MTJ. Initially the input select signals A, B, C, D are set to $(0, 0, 0, 0)$, selecting MTJ1 as seen from the Figure 41. From the table below it can
be concluded that MTJ1 is in AP configuration. Thus, the output is verified by the voltage discharging to the ground, and the output Q is pulled to binary 0 as seen in Figure 42, (from 500ps to 1ns) sensing at clock high. Then, the input is changed to \((1, 1, 1, 1)\), selecting MTJ16, which will be in P configuration. The output can be corroborated by observing Q pulled to high, representing binary 1, observed in the second clock cycle from Figure 42 (from 1.5ns to 2 ns). The delay of the LUT is measured by the amount of time it takes to discharge to 10% of VDD. Other logic functions such as AND, NAND and NOR are verified, but not discussed in this thesis. It is always a good practice not to read while writing and vice versa, so the write does not affect the read, thus preventing sensing errors. Hence, while reading, the WR signal is low, enabling MWR1 NMOS to allow clock controlled discharge for proper sensing operation.

Table 3: Truth Table Loaded as initial configuration to extensively verify LUT.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>X</th>
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<tbody>
<tr>
<td>0</td>
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</table>
Figure 41: Transistor level design of MLUT read circuit

Figure 42: Transient Analysis of MLUT to verify the circuit design.
Figure 43 shows the transistor level design of CM-LUT discussed in this thesis. The functionality of CM-LUT is verified similar to the verification method. The input to CM-LUT is similar to MLUT, as shown in Figure 44. As the worst case delay is measured during sensing a binary zero, it can be clearly observed that CM-LUT has much steeper curve discharging to ground, indicating increase in switching speed. Like previous verification methods, configuration as shown in Table 3 is loaded, and then applying a binary voltage of \((0, 0, 0, 0)\), to the input of the select tree, MTJ1 read. This can be observed by discharge of Q to the ground in Figure 44. On the contrary, when applying a binary voltage of \((1, 1, 1, 1)\), across the input of the select tree, MTJ16 is selected. This can be seen as Q is pulled to high during clock high.
Figure 44: Transient Analysis of CM-LUT to verify the circuit design
### Energy and Delay analysis

Table 4: Energy and Delay Table for a 4:1 LUT using different voltages ranging from Nominal to low power.

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Drive Technology</th>
<th>Power (µW)</th>
<th>Delay (ps)</th>
<th>EDP (nWps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2 (Nominal)</td>
<td>CNFET</td>
<td>1.89</td>
<td>36.89</td>
<td>0.0697</td>
</tr>
<tr>
<td></td>
<td>CMOS</td>
<td>25.6</td>
<td>201.56</td>
<td>5.1599</td>
</tr>
<tr>
<td>1.1</td>
<td>CNFET</td>
<td>1.57</td>
<td>36.25</td>
<td>0.0569</td>
</tr>
<tr>
<td></td>
<td>CMOS</td>
<td>21.21</td>
<td>210.9</td>
<td>4.4731</td>
</tr>
<tr>
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<tr>
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<td>1.02</td>
<td>38.86</td>
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<tr>
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<td>0.79</td>
<td>39.6</td>
<td>0.0312</td>
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<tr>
<td></td>
<td>CMOS</td>
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<td>278.94</td>
<td>2.9009</td>
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<tr>
<td>0.7 (Low power)</td>
<td>CNFET</td>
<td>0.58</td>
<td>41.96</td>
<td>0.0243</td>
</tr>
<tr>
<td></td>
<td>CMOS</td>
<td>7.55</td>
<td>340.6</td>
<td>2.5715</td>
</tr>
</tbody>
</table>
MLUT consists of 4 PMOS and 3 NMOS to implement the PCSA, 30 transistors to implement a 4 input select tree accommodating 16 MTJs, 4 NMOS to compensate the increase in transistor resistance and finally 17 PMOS and 17 NMOS to implement the write circuit and a clock disable NMOS. Thus, to implement the entire LUT, it takes 3.21 pm$^2$.

Implementing a CM-LUT requires a 4 P-Channel CNFET and 3 N-Channel CNFET to implement PCSA, 30 N-Channel CNFET to implement a select tree, 4 N-Channel CNFET to match the resistance between the sensing and the reference side and lastly 17 N-Channel CNFET and 17 P-Channel CNFET to implement the write circuit and a clock disable N-Channel CNFET. The area required to implement the entire CNFET is given by 0.108 pm$^2$. Thus CM-LUT requires less area compared to MLUT, with the same size of the LUT (calculated based on the number of transistors required to implement the LUT and multiplying by its individual area, the actual layout may vary).

The area of the MTJ remains the same in both the designs as we made no changes to the MTJ. There are 16 MTJs to store 16 bits of data and 4 MTJs, acting as reference circuit. Thus the entire area occupied by MTJ is 0.393 pm$^2$, which will be implemented in the back end of the CMOS fabrication process and will be connected using a series of “vias”. However, this does not include the total area of the LUT.
Summary

This Chapter dealt with verifying the proposed LUTs functionality using various simulation. These simulations results were verified by the potential difference at respective nodes, using spin orientation defining the state of the MTJ or current flowing each node. Finally, the Energy Delay Product (EDP) was presented at different voltages ranging from nominal to low voltage. Also, a transistor count estimation is calculated to access the area requirements of the proposed CM-LUT relative to traditional CMOS-based designs.
CHAPTER SIX: CONCLUSION

The circuit simulation of MLUT and CM-LUT is carried out in HSpice from Synopsis. The CMOS model is obtained from ASU 45nm PTM model, the MTJ model is obtained from Perdue and the CNFET model is obtained from Stanford. The transient analysis of the netlist consisting of respective components to realize a 4:1 LUT is performed. Promise of improvement by judicious corporation of CMOS logic and emerging devices was indicated by the results of functional feasibility, energy delay and area.

Technical Summary

In this thesis, the design of CM-LUT has been discussed, which uses MTJ as a storage element and CNFET to perform the logic drive to read the data stored in the Non-Volatile resistive memory based devices. A high performance sense amplifier, implemented using CNFET, is used to read the state of the MTJ, and a high speed MUX Select Tree is used to accommodate $2^n$ number of bits for an $n$ input LUT. The reference MTJ configuration described in this thesis, retires the need for complementary write circuit, which adds huge amount of power overheads as the write energy is the largest power consuming component in an MTJ based circuit. The write circuit implemented in this thesis, has an enhanced number of tubes to increase the drive current, thus obtaining an MTJ switching within 2 clock cycles (at 1 GHz operation). The obtained write circuit provides ultimate performance in terms of write delay and the area required to implement it. However, a CM-LUT is realized with 7 CNFETs to implement read circuit, 30 CNFETs to implement select tree, 4 CNFETs to compensate the resistance mismatch, 16 MTJs to store bit
information, 4 MTJs for reference, 34 CNFETs with enhanced number of tubes to implement the write circuit and finally a CNFET to disable clock controlled discharge. This results in an LUT with 38x energy improvement and 5x speed improvement, realizing ultimate circuit performance.

Circuit Reliability

While detailed reliability analysis was not the primary focus of the thesis, there are several contributions of the proposed CM-LUT which can advance reliable operation. The need for reliable operation is well established with respect to manufacturing defects [73], runtime hard faults occurrences, and transient soft errors [74-77]. The proposed CM-LUT can ameliorate the latter due to its use of NV MTJ storage devices within each LUT [78]. This can provide immunity to high energy particle strikes, which can cause SEU in conventional CMOS-based SRAM LUT design. As MTJ has the same write and read path and the fact that read current is 5-10 times lower than the critical current required to change the state of the MTJ, every so often this low current may cause a magnetic disturbance changing the magnetic state of the memory cell, contributing to undesirable behavior referred to as read disturbance [79]. One of the way is to use a synthetic ferromagnetic free layer, as proposed in [80], providing higher immunity to read disturbances at device level. Additional circuit level techniques have also been proposed in the literature [79, 81, 82]. These techniques employ either temporal redundancy, special redundancy or voltage margin to mitigate the likelihood of read disturbances. On the other hand there is a greater analysis to assess the impact on read disturbances and endurance considerations, which are new concerns introduced by use of MTJ in reconfigurable fabrics.
Technical Insights Gained

LUT designed based on SRAM as memory and CMOS as drive technology faces a pile of design challenges at nanometer ranges. The design of CM-LUT designed in this thesis, provides great advantages such as lower power consumption and faster device operation in comparison with conventional CMOS based LUT and spin-based LUT designs. As MTJ is spin based instead of charge based (as in SRAM) they are resilient to radiation induced high energy particle strikes, CM-LUT is less susceptible to radiation induced soft errors. The proposed circuit can achieve zero standby power, when utilized the advantage of non-volatility provided by MTJ memory element. Since, the CNFET has the ability to sense the state of the MTJ in a few pico seconds, LUT can be turned on instantly without any noticeable delay.

When developing a faster write circuit with CMOS, the design is quite straightforward to increase the width of the transistor, which in turn increases the drain current, aiding in faster switching. On the other hand, it is quite challenging to design the same with CNFET to determine with parameter to alter for a given voltage. Another challenging aspect while designing CM-LUT wire circuit is to cease the write current discharge to the ground when the clock is high, thus implementing a write circuit independent of clock. Other challenges faced were integrating two different technology files together, to enforce them in a single circuit. As GSHE memory provide better advantages in comparison with MTJ, the circuit designed in this thesis can provide better performance in terms of energy and switching delay when GSHE is used as memory element. The Implementation of GSHE in place of MTJ is fairly simple, as they both require bi-directional current to change their state. Also, in case of implementing large LUTs, using 3D racetrack memories could be area efficient.
Due to manufacturing imperfections caused by process variation and immature CNFET fabrication process, the cost to manufacture CNFET, in comparison with conventional large scale CMOS, can be high. Thus, experimenting with different configurations of logic drive technology can provide advantages of good circuit performance in addition to the cost effective fabrication process. Figure 45 shows the implementation of CMOS based PCSA and CNFET based Select Tree. The converse of the same consisting of CNFET based PCSA and CMOS based Select tree is also simulated and analyzed in this section, as shown in Figure 46. The transistor technology, containing either CMOS or CNFET, should be in correlation with the select tree while designing reference stack which eliminates the discrepancy in resistance between the sensing and the reference side. The write circuit implemented in both the designs uses CMOS technology, as large numbers for a single channel CNT synthesis is difficult.
Figure 46: CNFET based PCSA and CMOS based Select Tree

The analysis of these designs indicate that first, the design consisting of CMOS based PCSA and CNFET based select tree, has comparable performance tradeoffs in comparison with the other design. Select Tree consists of a pool of transistors provided that most of them are idle in OFF condition. Huge amounts of energy consumption, in comparison with the remainder of the circuit, is a result of the increase in OFF current at nanometer ranges. Since CNFET has low leakage and low OFF current it is logical to implement in Select Tree in comparison with CMOS. The circuit realized constitutes to an average power consumption of 2.69µW and a delay of 242ps, while the latter produces 19.24µW of power consumption and a delay of 410ps. Hence, the design consisting of CMOS based PCSA and CNFET based Select Tree provides a cost effective design with acceptable depreciation in performance.
Future Works

The MTJ, CMOS and CNFET models obtained from Perdue, ASU and Stanford are the latest at the time of writing this thesis. The simulation of the new predicative technology model will be carried out when they become available. To have an overview of circuit performance at architecture level, VPR, developed by University of Toronto [83], can be utilized readily by inputting the architectural parameters in the architecture description file as an input to VPR. Since VPR is entirely time driven program, the timing analysis obtained from this thesis at LUT level can be imported, with additional components to realize a CLB level. Also VPR can utilize the place and route that can include simulation of switch box in the simulation.

It is of significance, that CNTs provide superior electrical conductivity as they provide ballistic or near ballistic transport of electrons or holes. In addition, CNTs can withstand high current densities and are resilient to electron migration. These features make metallic CNTs, which are conductive in nature, in the design of interconnects, achieving a slower aging process with relatively lower losses, in comparison with copper based interconnects.
APPENDIX A: MLUT HSPICE CODE
41LUT.sp

** Author: Mohan Krishna Gopi Krishna
** Email: mohankrishna.gopikrishna@knights.ucf.edu

** This SPICE file demonstrates the operation of a 4:1 Look Up Table (LUT)

*** Libraries ***

.hd1 './mtj_libs_encoded/needsmtj_1_0_0b.va'
.lib './CMOS_lib/45nm_nominal_bulkCMOS.pm' CMOS_MODELS
.inc './CMOS_lib/NangateOpenCellLibrary_supply.sp'

*** Options ***

.option post=1
.option probe=0
.option runlvl=6
.option ingold=2
.option accurate=1
.option method=bdf
.option bdfrtol=1e-8
.option bdfatol=1e-9
.option numdgt=10
.option brief
.option measfile=1
.option lis_new=1
.option vaopts=str('-G')
.save

*** MTJ Parameters/Definitions ***

.param pi='4*atan(1)'
.param kB='1.3806503e-23'
.param Temperature='25'
.param Ms='700'
.param alpha='0.028'
.param W='25e-9'
.param L='pi*25e-9'
.param Tm='1.4e-9'
.param Ea='56*kB*(300)*1e7'
.param Volume='W*L*Tm*1e6'
.param K='(Ea/Volume)'
.param P_L='0.8'
.param P_R='0.3'
.param Lambda_L = '2'
.param Lambda_R = '2'

.param P = '0.1*pi/180'
.param AP = '179.9*pi/180'
.param PinL = '0.0*pi/180'
.param vdd = 1.2

vdd vdd 0 'vdd'

**********************************************************************
***                     Initial Conditions                         ***
**********************************************************************
.ic V(th11) AP
.ic V(ph11) PinL
.ic V(th12) P
.ic V(ph12) PinL
.ic V(th13) AP
.ic V(ph13) PinL
.ic V(th14) P
.ic V(ph14) PinL
.ic V(th15) AP
.ic V(ph15) PinL
.ic V(th16) P
.ic V(ph16) PinL
.ic V(th17) AP
.ic V(ph17) PinL
.ic V(th18) P
.ic V(ph18) PinL
.ic V(th19) AP
.ic V(ph19) PinL
.ic V(th110) P
.ic V(ph110) PinL
.ic V(th111) AP
.ic V(ph111) PinL
.ic V(th112) P
.ic V(ph112) PinL
.ic V(th113) AP
.ic V(ph113) PinL
.ic V(th114) P
.ic V(ph114) PinL
.ic V(th115) AP
.ic V(ph115) PinL
.ic V(th116) P
.ic V(ph116) PinL
.ic V(th120) AP
.ic V(ph120) PinL
.ic V(th117) P
.ic V(ph117) PinL
.ic V(th118) AP
.ic V(ph118) PinL
.ic V(th119) P
.ic V(ph119) PinL

*Reference
```
*** Netlist ***
V_HAX hax 0 '0.0'
V_HAY hay 0 '0.0'
V_HAZ haz 0 '0.0'

* Input Voltages
* Clock Input

Vclk CLK 0 pulse (0 vdd 0.5ns 1ps 1ps 0.5ns 1ns)

* Select tree Input

Va A 0 pulse (0 vdd 1ns 1ps 5ns 10ns)
Vb B 0 pulse (0 vdd 1ns 1ps 5ns 10ns)
Vc C 0 pulse (0 vdd 1ns 1ps 5ns 10ns)
Vd D 0 pulse (0 vdd 1ns 1ps 5ns 10ns)

* Write Inputs
* Bit Line

Vbl BL 0 0

* Word Line to Select MTJ

Vwl1 WL1 0 0
Vwl2 WL2 0 0
Vwl3 WL3 0 0
Vwl4 WL4 0 0
Vwl5 WL5 0 0
Vwl6 WL6 0 0
Vwl7 WL7 0 0
Vwl8 WL8 0 0
Vwl9 WL9 0 0
Vwl10 WL10 0 0
Vwl11 WL11 0 0
Vwl12 WL12 0 0
Vwl13 WL13 0 0
Vwl14 WL14 0 0
Vwl15 WL15 0 0
Vwl16 WL16 0 0

* Write Enable Input

VWe WE 0 0

* Inverter and Transmission Gate subckt

.SUBCKT TR_INV WL IN OP VSS VDD
  M_i_0 WLbar WL VSS VSS NMOS_VTL W=0.415000U L=0.050000U
  M_i_1 WLbar WL VDD VDD PMOS_VTL W=0.630000U L=0.050000U
```
M_i_2 OP WL IN VSS NMOS_VTL W=0.900000U L=0.050000U
M_i_3 OP WLbar IN VDD PMOS_VTL W=1.800000U L=0.050000U
.ENDS

*Select tree Inverters
Xinv1 A Abar 0 vdd INV_X1
Xinv2 B Bbar 0 vdd INV_X1
Xinv3 C Cbar 0 vdd INV_X1
Xinv4 D Dbar 0 vdd INV_X1
Xinv6 WE WEbar 0 vdd INV_X1

* Read Circuit
*Pre-Charge Sense Amplifier
*NMOS
MN1 Qbar Q SL1 0 NMOS_VTL W=0.415000U L=0.050000U
MN2 Qbar SLref 0 NMOS_VTL W=0.415000U L=0.050000U
MNwr MTret WEbar MTret1 0 NMOS_VTL W=0.415000U L=0.050000U
MN3 MTret1 CLK 0 0 NMOS_VTL W=0.415000U L=0.050000U

*PMOS
MP1 Qbar CLK vdd vdd PMOS_VTL W=0.630000U L=0.050000U
MP2 Qbar vdd vdd PMOS_VTL W=0.630000U L=0.050000U
MP3 Qbar vdd vdd PMOS_VTL W=0.630000U L=0.050000U
MP4 Q CLK vdd vdd PMOS_VTL W=0.630000U L=0.050000U

*Select Tree
MN4 SL1 Abar SL2 0 NMOS_VTL W=0.415000U L=0.050000U
MN5 SL1 A SL3 0 NMOS_VTL W=0.415000U L=0.050000U
MN6 SL2 Bbar SL4 0 NMOS_VTL W=0.415000U L=0.050000U
MN7 SL2 B SL5 0 NMOS_VTL W=0.415000U L=0.050000U
MN8 SL3 Bbar SL6 0 NMOS_VTL W=0.415000U L=0.050000U
MN9 SL3 B SL7 0 NMOS_VTL W=0.415000U L=0.050000U
MN10 SL4 Cbar SL8 0 NMOS_VTL W=0.415000U L=0.050000U
MN11 SL4 C SL9 0 NMOS_VTL W=0.415000U L=0.050000U
MN12 SL5 Cbar SL10 0 NMOS_VTL W=0.415000U L=0.050000U
MN13 SL5 C SL11 0 NMOS_VTL W=0.415000U L=0.050000U
MN14 SL6 Cbar SL12 0 NMOS_VTL W=0.415000U L=0.050000U
MN15 SL6 C SL13 0 NMOS_VTL W=0.415000U L=0.050000U
MN16 SL7 Cbar SL14 0 NMOS_VTL W=0.415000U L=0.050000U
MN17 SL7 C SL15 0 NMOS_VTL W=0.415000U L=0.050000U
MN18 SL8 Dbar MT1 0 NMOS_VTL W=0.415000U L=0.050000U
MN19 SL8 D MT2 0 NMOS_VTL W=0.415000U L=0.050000U
MN20 SL9 Dbar MT3 0 NMOS_VTL W=0.415000U L=0.050000U
MN21 SL9 D MT4 0 NMOS_VTL W=0.415000U L=0.050000U
MN22 SL10 Dbar MT5 0 NMOS_VTL W=0.415000U L=0.050000U
MN23 SL10 D MT6 0 NMOS_VTL W=0.415000U L=0.050000U
MN24 SL11 Dbar MT7 0 NMOS_VTL W=0.415000U L=0.050000U
MN25 SL11 D MT8 0 NMOS_VTL W=0.415000U L=0.050000U
MN26 SL12 Dbar MT9 0 NMOS_VTL W=0.415000U L=0.050000U
MN27 SL12 D MT10 0 NMOS_VTL W=0.415000U L=0.050000U
MN28 SL13 Dbar MT11 0 NMOS_VTL W=0.415000U L=0.050000U

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MN29 SL13 D MT12 0 NMOS_VTL W=0.415000U L=0.050000U
MN30 SL14 Dbar MT13 0 NMOS_VTL W=0.415000U L=0.050000U
MN31 SL14 D MT14 0 NMOS_VTL W=0.415000U L=0.050000U
MN32 SL15 Dbar MT15 0 NMOS_VTL W=0.415000U L=0.050000U
MN33 SL15 D MT16 0 NMOS_VTL W=0.415000U L=0.050000U

*Reference Stack

MN34 SLref vdd SLref1 0 NMOS_VTL W=0.415000U L=0.050000U
MN35 SLref1 vdd SLref2 0 NMOS_VTL W=0.415000U L=0.050000U
MN36 SLref2 vdd SLref3 0 NMOS_VTL W=0.415000U L=0.050000U
MN37 SLref3 vdd MTref 0 NMOS_VTL W=0.415000U L=0.050000U

* Write Circuit

Xinv5 BL BLbar 0 vdda INV_X1
Xwl1 WL1 BL MT1 0 vdda TR_INV
Xwl2 WL2 BL MT2 0 vdda TR_INV
Xwl3 WL3 BL MT3 0 vdda TR_INV
Xwl4 WL4 BL MT4 0 vdda TR_INV
Xwl5 WL5 BL MT5 0 vdda TR_INV
Xwl6 WL6 BL MT6 0 vdda TR_INV
Xwl7 WL7 BL MT7 0 vdda TR_INV
Xwl8 WL8 BL MT8 0 vdda TR_INV
Xwl9 WL9 BL MT9 0 vdda TR_INV
Xwl10 WL10 BL MT10 0 vdda TR_INV
Xwl11 WL11 BL MT11 0 vdda TR_INV
Xwl12 WL12 BL MT12 0 vdda TR_INV
Xwl13 WL13 BL MT13 0 vdda TR_INV
Xwl14 WL14 BL MT14 0 vdda TR_INV
Xwl15 WL15 BL MT15 0 vdda TR_INV
Xwl16 WL16 BL MT16 0 vdda TR_INV
Xwe WE BLbar MTret 0 vdda TR_INV

* MTJ Memory Elements

XMTJ1 MT1 MTret hax hay th11 ph11 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
L='L'
Tm='Tm'
Ms='Ms'
Lambda=0 alpha='alpha'
Lambda_L='Lambda_L'
Lambda_R='Lambda_R'
LLG_Temp='0.0'
thermScale='0.0'

XMTJ2 MT2 MTret hax hay th12 ph12 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
L='L'
Tm='Tm'
Ms='Ms'
Lambda=0 alpha='alpha'
Lambda_L='Lambda_L'
Lambda_R='Lambda_R'
LLG_Temp='0.0'
thermScale='0.0'

XMTJ3 MT3 MTret hax hay th13 ph13 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
L='L'
Tm='Tm'
Ms='Ms'
Lambda=0 alpha='alpha'
Lambda_L='Lambda_L'
Lambda_R='Lambda_R'
LLG_Temp='0.0'
thermScale='0.0'
XMTJ4 MT4 MTret hax hay haz th14 ph14 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ5 MT5 MTret hax hay haz th15 ph15 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ6 MT6 MTret hax hay haz th16 ph16 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ7 MT7 MTret hax hay haz th17 ph17 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ8 MT8 MTret hax hay haz th18 ph18 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ9 MT9 MTret hax hay haz th19 ph19 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ10 MT10 MTret hax hay haz th110 ph110 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ11 MT11 MTret hax hay haz th111 ph111 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ12 MT12 MTret hax hay haz th112 ph112 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ13 MT13 MTret hax hay haz th113 ph113 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'

XMTJ14 MT14 MTret hax hay haz th114 ph114 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG.Temp='0.0' thermScale='0.0'
MTJ15 MTret hax hay haz th115 ph115 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

MTJ16 MT16 MTret hax hay haz th116 ph116 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

*Reference MTJ

MTJ20 MTref MTref1 hax hay haz th120 ph120 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

MTJ17 MTref1 MTret hax hay haz th117 ph117 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

MTJ18 MTref2 MTref hax hay haz th118 ph118 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

MTJ19 MTref2 MTret hax hay haz th119 ph119 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

******************************************************************************
***                           Analysis                                      
******************************************************************************
.tran 1p 2.5n
.option runlvl=6
.MEASURE TRAN pow AVG POWER FROM=0.5n TO=1.5n
.end
APPENDIX B: CM-LUT HSPICE CODE
This SPICE file demonstrates the operation of a Look Up Table (LUT) with CNFET as Drive and MTJ as Memory Element.

*For optimal accuracy, convergence, and runtime*

*Parameters/Definitions*

```
.param TEMP=27
```
* CNFET parameters:

```
.param Cc=0      CoupleRatio=0
.param m_cnt=1    Efo=0.6
.param Wg=0       Cb=40e-12
.param Lg=32e-9   Lgef=100e-9
.param Vfn=0      Vfp=0
.param m=19       n=0
.param Hox=4e-9   Kox=16
```

* MTJ parameters

```
.param pi='4*atan(1)'
.param kB='1.3806503e-23'
.param Temperature='25'
.param Ms='700'
.param alpha='0.028'
.param W='25e-9'
.param L='pi*25e-9'
.param Tm='1.4e-9'
.param Ea='56*kB*(300)*1e7'
.param Volume='W*L*Tm*le6'
.param Ka='(Ea/Volume)'
.param P_L=0.8'
.param P_R=0.3'
.param Lambda_L='2'
.param Lambda_R='2'
```

```
.param P='0.1*pi/180'
.param AP='179.9*pi/180'
.param PinL='0.0*pi/180'
```

*** Initial Conditions ***

```
.ic V(th11) AP
.ic V(ph11) PinL
.ic V(th12) P
.ic V(ph12) PinL
.ic V(th13) AP
.ic V(ph13) PinL
.ic V(th14) P
.ic V(ph14) PinL
.ic V(th15) AP
.ic V(ph15) PinL
.ic V(th16) P
.ic V(ph16) PinL
.ic V(th17) AP
.ic V(ph17) PinL
.ic V(th18) P
.ic V(ph18) PinL
.ic V(th19) AP
.ic V(ph19) PinL
.ic V(th110) P
.ic V(ph110) PinL
.ic V(th111) AP
```
.ic V(ph111) PinL
.ic V(th112) P
.ic V(ph112) PinL
.ic V(th113) AP
.ic V(ph113) PinL
.ic V(th114) P
.ic V(ph114) PinL
.ic V(th115) AP
.ic V(ph115) PinL
.ic V(th116) P
.ic V(ph116) PinL
.ic V(th120) AP
.ic V(ph120) PinL
.ic V(th117) P
.ic V(ph117) PinL
.ic V(th118) AP
.ic V(ph118) PinL
.ic V(th119) P
.ic V(ph119) PinL

*Reference

*Supplies voltage param:
.param vdd=1.2

vdd vdd 0 'vdd'

**********************************************************************
***                           Netlist                              ***
**************************
****************************
V_HAX
hax 0 0 '0.0'
V_HAY
hay 0 0 '0.0'
V_HAZ
haz 0 0 '0.0'

*Input Voltages
*Clock Input

Vclk clk 0 pulse (0 vdd 0.5ns 1ps 1ps 500ps 1ns)

*Select Tree Input

Va A 0 pulse (0 vdd 1ns 1ps 1ps 5ns 10ns)
Vb B 0 pulse (0 vdd 1ns 1ps 1ps 5ns 10ns)
Vc C 0 pulse (0 vdd 1ns 1ps 1ps 5ns 10ns)
Vd D 0 pulse (0 vdd 1ns 1ps 1ps 5ns 10ns)

*Write Inputs
*Bit Line

Vbl BL 0 0

*Word Line to select MTJ

Vw1 WL1 0 0
Vw12 WL2 0 0
Vw13 WL3 0 0
*Write Enable Input*

Vwe WE 0 0

*Inverter Sub CKT*

```
.SUBCKT INV_X1_CNPFET A ZN VSS VDD

.*PININFO A:I ZN:O VDD:P VSS:G
.*EQN ZN=!A

XM_i_0 ZN A VSS VSS NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
 n1=19 n2=0 tubes=5

XM_i_1 ZN A VDD VDD PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
 n1=19 n2=0 tubes=5

.ENDS
```

*Inverter and Transmission gate sub CKT*

```
.SUBCKT TR_INV_CNPFET WL IN OP VSS VDD

XM_i_0 Wbar WL VSS VSS NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
 n1=19 n2=0 tubes=5

XM_i_1 Wbar WL VDD VDD PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
 n1=19 n2=0 tubes=5

XM_i_2 OP WL IN VSS NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
 n1=19 n2=0 tubes=5

XM_i_3 OP Wbar IN VDD PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
 n1=19 n2=0 tubes=5

.ENDS
```
*Select Tree Inverters

Xinv1 A Abar 0 vdd INV_X1_CNFET
Xinv2 B Bbar 0 vdd INV_X1_CNFET
Xinv3 C Cbar 0 vdd INV_X1_CNFET
Xinv4 D Dbar 0 vdd INV_X1_CNFET

*Write inverters

Xinv6 WE WEbar 0 vdd INV_X1_CNFET
Xinv7 BL BLbar 0 vdd INV_X1_CNFET

*Read Circuit
*Pre-Charge Sense Amplifier
*NCNFET

XCNTn1 Qbar Q SL1 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

XCNTn2 Qbar SLref 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

XCNTn3 MTret1 clk 0 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

XCNTnwr MTret WEbar MTret1 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
* Clock Disable
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

*PCNFET

XCNTp1 Qbar clk vdd vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

XCNTp2 Qbar Q vdd vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

XCNTp3 Q vdd vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

XCNTp4 Q clk vdd vdd PCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

*Select Tree
XCNTn4 SL1 Abar SL2 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn5 SL1 A SL3 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn6 SL2 Bbar SL4 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn7 SL2 B SL5 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn8 SL3 Bbar SL6 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn9 SL3 B SL7 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn10 SL4 Cbar SL8 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn11 SL4 C SL9 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn12 SL5 Cbar SL10 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn13 SL5 C SL11 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn14 SL6 Cbar SL12 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn15 SL6 C SL13 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn16 SL7 Cbar SL14 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9
  n1=19  n2=0  tubes=5

XCNTn17 SL7 C SL15 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn18 SL8 Dbar MT1 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn19 SL8 D MT2 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn20 SL9 Dbar MT3 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn21 SL9 D MT4 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn22 SL10 Dbar MT5 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn23 SL10 D MT6 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn24 SL11 Dbar MT7 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn25 SL11 D MT8 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn26 SL12 Dbar MT9 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn27 SL12 D MT10 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn28 SL13 Dbar MT11 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn29 SL13 D MT12 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5

XCNTn30 SL14 Dbar MT13 0 NCNFET Lch=Lg  Lgeff='Lgef'  Lss=32e-9  Ldd=32e-9  
  + Kgate='Kox'  Tox='Hox'  Csub='Cb'  Vfbn='Vfn'  Dout=0  Sout=0  Pitch=20e-9  
n1=19  n2=0  tubes=5
**Reference Stack**

*XCNTn31* SL14 D MT14 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

*XCNTn32* SL15 Dbar MT15 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

*XCNTn33* SL15 D MT16 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9 Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0 Sout=0 Pitch=20e-9
n1=19 n2=0 tubes=5

*Write Circuit*

*Xw11* WL1 BL MT1 0 vdd TR_INV_CNFET
*Xw12* WL2 BL MT2 0 vdd TR_INV_CNFET
*Xw13* WL3 BL MT3 0 vdd TR_INV_CNFET
*Xw14* WL4 BL MT4 0 vdd TR_INV_CNFET
*Xw15* WL5 BL MT5 0 vdd TR_INV_CNFET
*Xw16* WL6 BL MT6 0 vdd TR_INV_CNFET
*Xw17* WL7 BL MT7 0 vdd TR_INV_CNFET
*Xw18* WL8 BL MT8 0 vdd TR_INV_CNFET
*Xw19* WL9 BL MT9 0 vdd TR_INV_CNFET
*Xw110* WL10 BL MT10 0 vdd TR_INV_CNFET
*Xw111* WL11 BL MT11 0 vdd TR_INV_CNFET
*Xw112* WL12 BL MT12 0 vdd TR_INV_CNFET
*Xw113* WL13 BL MT13 0 vdd TR_INV_CNFET
*Xw114* WL14 BL MT14 0 vdd TR_INV_CNFET
*Xw115* WL15 BL MT15 0 vdd TR_INV_CNFET
*Xw116* WL16 BL MT16 0 vdd TR_INV_CNFET
*Xwe* WE BLbar MTret 0 vdd TR_INV_CNFET

*MTJ Memory Elements*
XMTJ1 MT1 MTr et hax hay haz th11 ph11 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ2 MT2 MTr et hax hay haz th12 ph12 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ3 MT3 MTr et hax hay haz th13 ph13 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ4 MT4 MTr et hax hay haz th14 ph14 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ5 MT5 MTr et hax hay haz th15 ph15 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ6 MT6 MTr et hax hay haz th16 ph16 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ7 MT7 MTr et hax hay haz th17 ph17 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ8 MT8 MTr et hax hay haz th18 ph18 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ9 MT9 MTr et hax hay haz th19 ph19 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ10 MT10 MTr et hax hay haz th110 ph110 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ11 MT11 MTr et hax hay haz th111 ph111 PMAMTJ Ku2='K' W='W' P_L='P_L' P_R='P_R' + L='L' Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L' + Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'
XMTJ12  MT12  MTret hax hay haz th112 ph112 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ13  MT13  MTret hax hay haz th113 ph113 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ14  MT14  MTret hax hay haz th114 ph114 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ15  MT15  MTret hax hay haz th115 ph115 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ16  MT16  MTret hax hay haz th116 ph116 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

*Reference MTJ

XMTJ20  MTref MTref1 hax hay haz th120 ph120 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ17  MTref1 MTret hax hay haz th117 ph117 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ18  MTref1 MTret hax hay haz th118 ph118 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

XMTJ19  MTref2 MTret hax hay haz th119 ph119 PMAMTJ Ku2='K' W='W' P_L='P_L'
P_R='P_R'
+ L='L'  Tm='Tm' Ms='Ms' Lambda=0 alpha='alpha' Lambda_L='Lambda_L'
+ Lambda_R='Lambda_R' LLG_Temp='0.0' thermScale='0.0'

**********************************************************************
***                           Analysis                             ***
**********************************************************************
.tran 1p 2.5n
.option runlvl=6

.print tran v(MT1,MTret)

.MEASURE TRAN pow AVG POWER FROM=0.5n TO=1.5n

.end
REFERENCES


